



PCN Number: SM122117 Chgnot.doc rev 13 1/14

Product/Process Change Notification (PCN)							
Customer: Newark	Date: 12/21/2017						
Customer Part # and/or Lot# affected: A4987SESTR-T and A4987SLPTR-T							
Originator: Scott Mitti	Phone: 508-854-5627						
Duration of Change:	Permanent X Temporary (explain)						
Summary description of change: Part	Change: X Other:						
Semiconductor LLC (PSL), Bloomington	7SESTR-T and A4987SLPTR at wafer fab, Polar, MN, USA, utilizing 8" ABCD5 technology. Allegro will he 8" ABCD5 technology wafer line at United inshu, Taiwan.						
What is the part or process changing	from (provide details)?						
•	7SESTR-T and A4987SLPTR at wafer fab, Polar , MN, USA, utilizing 8" ABCD5 technology.						
What is the part or process changing form, fit and/or function)?	to (describe the anticipated impact of this change on						
	facturing for A4987SESTR-T and A4987SLPTR to the 8" Microelectronics Corporation (UMC), Hsinshu, Taiwan.						

Note: Validation of equivalence within a specific application is at the discretion of the Customer





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Is a PPAP update required?	Yes	No X
Is reliability testing required? (If Yes. refer to attached plan)	Yes X	No (explain)



Reliability Qualification Results

 Device:
 4987 (949871)
 Package:
 ES (4x4 MLP)

 Assy Lot #:
 1732122HAAA
 Assembly Location:
 UTAC

 Number of Leads:
 24
 Lead Finish:
 100% Sn

 Fab Location:
 UMC
 Tracking Number:
 4103

Reason for Qualification: 4987 - (949871) - DMOS Dual Full-Bridge PWM Motor Driver With Overcurrent

Protection

Reliability Qualification Results								
4987, STR#4103					Requirements			
Stress Test	Abv.	Test #	Test Method	Test Conditions	s.s.	Results		
HAST	HAST	A2	JESD22-A110	130°C, 2 ATM, 60% RH, 0, 96 hrs	77	0 Rejects		
High Temperature Operating Life	HTOL	B1	JESD22-A108	125°C, 0, 168 hrs	77	0 Rejects		
Electrostatic Discharge Human Body Model (STR#4047)	НВМ	E2	JESD22-A114	Test Conditions, Sampling Size are defined in the Test Method		Classification 2, HBM = 2.5kV		
Electrostatic Discharge Charged Device Model	CDM	E3	JESD22-C101	Test Conditions, Sampling Size are defined in the Test Method		Classification = C3, >1kV		
Latch-Up (STR#4047)	LU	E4	JESD78	Test Conditions, Sampling Size are defined in the Test Method		Class II, Level A		
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions - 30 pcs.		0 Rejects; Cpk>1.67		

This device qualification is considered to be passing all environmental stress evaluations per the Allegro MicroSystems qualification specifications.

Approved by:

Robert Demers

Robert Demers Sr. Product Safety and Reliability Allegro MicroSystems, LLC

Allegro MicroSystems, LLC

Proprietary



cc: Allegro Sales/Marketing/Quality



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Expected completion date for internal qualification: Complete **Expected PPAP availability date:** N/A Target implementation date: June 2018 Estimated date of first shipment: July 2018 **Expected sample availability date:** Available Upon Request Yes **Date Required: Customer Approval Required:** No **Notification Only Please note:** It is our intention to inform our customer of changes as early as possible. Under Allegro's procedure for product/process change notification, Allegro strives, based on its technical judgment, to provide notification of significant changes that may affect form, fit or function. However, as Allegro cannot ensure evaluation of product/process changes for each and every application; the customer retains responsibility to validate the impact of a change on its application suitability. If samples are needed for validation of a change, requests may be made via the contact information provided herein. Please contact your Account Manager or local Sales contact for any questions. We would kindly request your consideration so we can meet our target date for implementation. Unless both parties agree to extend the implementation date, this change will be implemented as scheduled. Customer comments/Conditions of Acceptance: Title: Approved by: Date: