Freescale Semiconductor
Quick Start

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QorIQ T2080 Development System Quick Start Guide

1 Introduction

This document describes the T2080QDS board and its related hardware kit. It also explains and verifies, the basic board operations in a step-by-step format.

The document lists the settings required to connect switches, connectors, jumpers, push buttons, and LEDs to the peripheral devices.

The T2080QDS board functions with an integrated development environment (IDE), such as Freescale CodeWarrior. However, the instructions for working with the IDE are beyond the scope of this document.

Contents

2 Related documentation

Table 1 lists the additional documents that you can refer to, for more information on T2080QDS.

Some of these documents may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1. Related documentation

Document	Description
T2080 QorIQ Integrated Multicore Communication Processor Family Reference Manual	This document provides a detail description on T2080 QorIQ multicore processor, and on some of its features like memory map, serial interfaces, power supply, chip features, and clock information.
T2080 QorIQ Advanced Multicore Processor Data Sheet	This document contains T2080 information on pin assignments, electrical characteristics, hardware design, considerations, package information, and ordering information.
IR36021 Datasheet	This document details the Digital POL buck controller with I2C and PMBus interface. IR36021 is used as dual power supply (VDD & GVDD) for T2080 devices.
RTL8211EG-VB-CG Integrated 10/100/1000M Ethernet Transceiver Datasheet	This document explains the use of RTL8211 as T2080 dual channel GigaEthernet PHY.
T2080QDS Reference Manual	This document details about the individual implementation of T2080 Development System platform that supports T2080 Power Architecture processor.

NOTE

Freescale Semiconductor, Inc. does not own *IR36021 Datasheet* and *RTL8211EG-VB-CG Integrated 10/100/1000M Ethernet Transceiver Datasheet* and are mentioned solely for the reference purpose.

3 T2080 chassis images

This section demonstrates the manner in which the chassis are arranged on the T2080QDS board.

NOTE

The Hardware kit contents can be found in attached packing list provided with the board support package.

Figure 1 and Figure 2 shows the T2080 QDS external view, that includes front and back enclosure of chassis.

Figure 1. T2080QDS chassis front view

Figure 2. T2080QDS chassis back view

Figure 3 shows the open state of T2080QDS chassis:

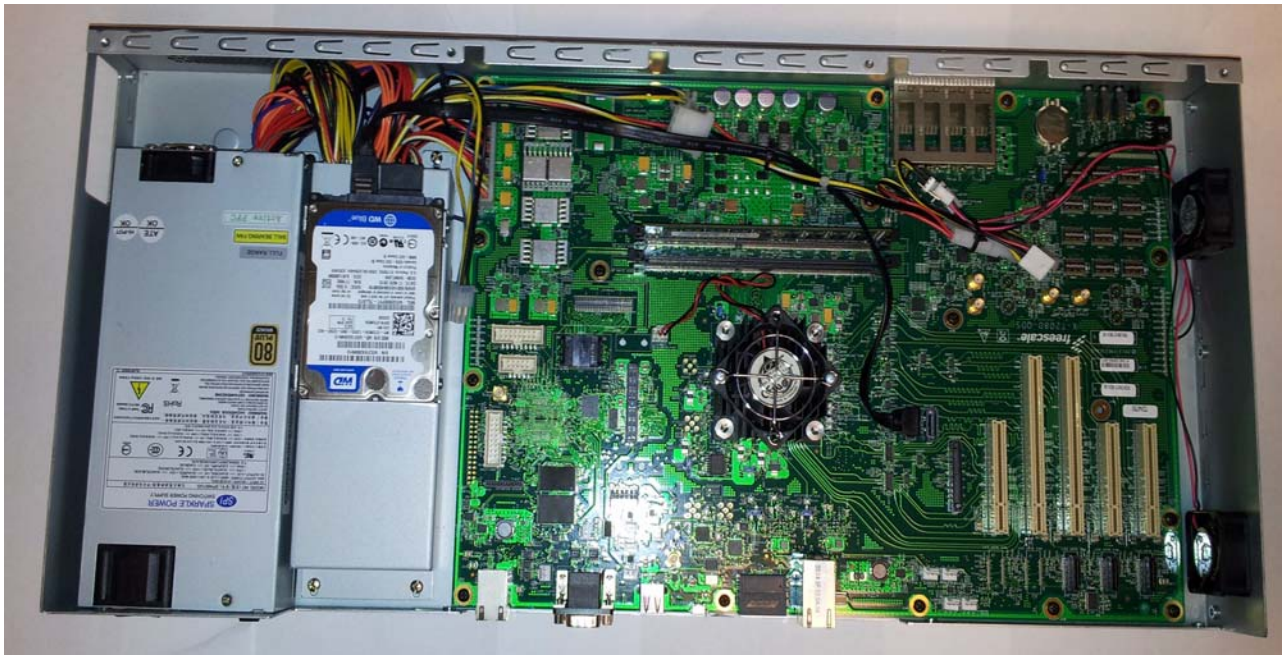


Figure 3. T2080QDS open state of chassis

4 T2080QDS board drawings

In this section:

4.1 T2080QDS Component Side View

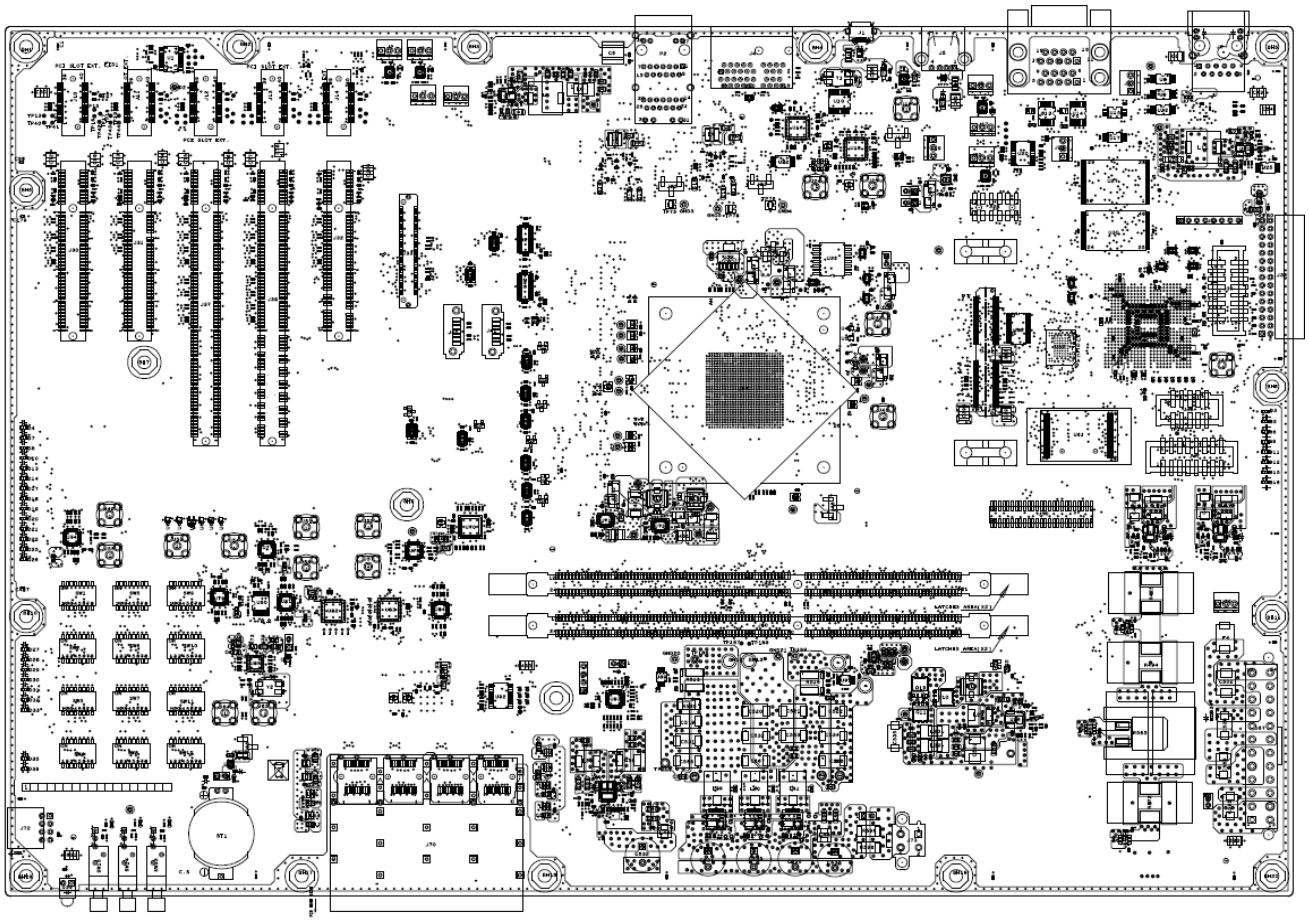


Figure 4. T2080QDS Component Side View

4.2 T2080QDS Print Side View

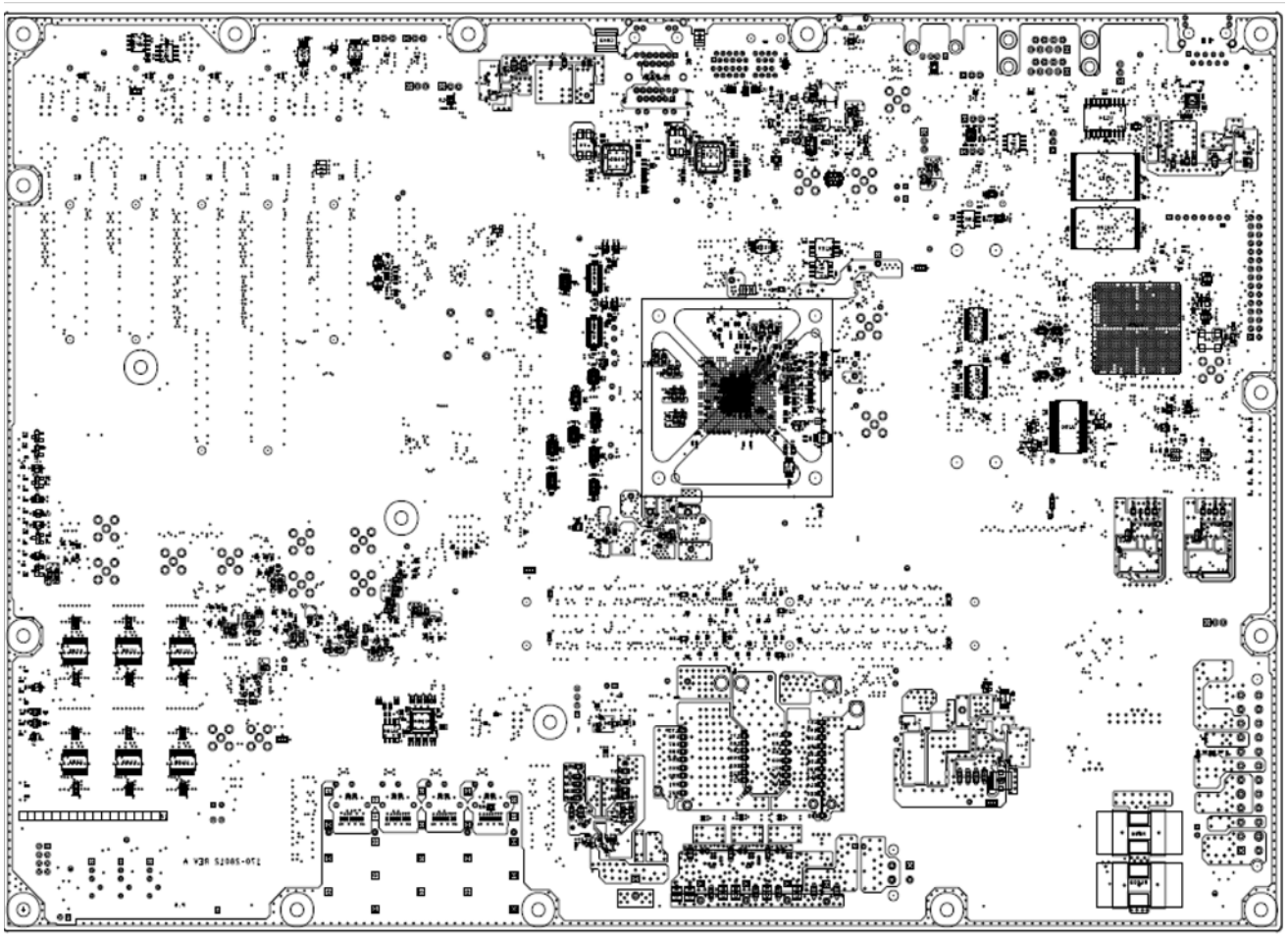


Figure 5. T2080QDS Print Side View

5 Switch default settings

Table 2 shows the default DIP-switch positions to establish the T2080QDS mode.

NOTE

Ensure the DIP-switches are set according to the default values.

Table 2. T2080QDS default configurations

Mode	Term	Default Value	Unit
AVDD_CGA1, AVDD_CGA2, AVDD_PLAT, AVDD_D1	PLL Supply Voltages (Core, Platform, DDR, and SRDS)	1.8	V
AVDD_SRDS1, AVDD_SRDS2,	SERDES PLL 1 & 2 Supply Voltages (Filtered from XVDD)	1.35	V
G1VDD Voltage	DDR DRAM I/O Supply Voltage	1.5[Default]/1.35	V
S1VDD, S2VDD Voltage	Core power supply for SerDes transceiver	1.0	V
X1VDD, X2VDD Voltage	Pad power supply for SerDes transceiver	1.35	V
OVDD Voltage	General I/O Supply: MPIC, GPIO, eSDHC, DDRCLK and IFC system control and power management, clocking, debug, and JTAG I/O voltage	1.8	V
DVDD Voltage	DUART, I²C, DMA,	1.8[Default]/2.5/(3.3-Optional)	V
CVDD Voltage	eSPI & SDHC Blocks Supply	1.8[Default]/(2.5/3.3-Optional)	V
LVDD Voltage	Ethernet, EMI1, 1588, XFI	2.5	V
FA_VL Voltage	Reserved for internal use	0/(1.025-Optional)	V
PROG_MTR	Reserved for internal use	0/(1.89-Optional)	V
PROG_SFP	Security fuse programming override supply	0/(1.89-Optional)	V
TH_VDD	Thermal monitor unit supply	1.8	V
VDD_LP Voltage	Low Power Security Monitor Supply	1.0	V
VDD	Cores & platform supply	1.025	V
USB_SVDD1 & 2	USB PHY Analog 1.0V Supply	1.025	V
USB_OVDD1 & 2	USB PHY Transceiver 1.8V Supply	1.8	V
USB_HVDD1 & 2	USB PHY Transceiver 3.3V Supply	3.3	V
SYSCLK (Synthesizer REF CLK)	System Clock	100	MHz
Platform Clock	Depends on RCW	600	MHz
DDR CLK (Synthesizer REF CLK)	Depends on RCW	133.33	MHz

Table 2. T2080QDS default configurations

Mode	Term	Default Value	Unit
D1_DDR_CLK	Memory Bus Clock	933.333	MHz
Fman CLK	Depends on RCW	700	MHz
Core Clock	Depends on RCW	1800	MHz
SD1_REF1 CLK	SerDes1 Reference Clock 1	156.250	MHz
SD1_REF2 CLK	SerDes1 Reference Clock 2	100	MHz
SD2_REF1 CLK	SerDes2 Reference Clock 1	100	MHz
SD2_REF2 CLK	SerDes2 Reference Clock 2	100	MHz
EC1_GTXCLK_125	Eth1 MAC reference clock	125	MHz
EC2_GTXCLK_125	Eth2 MAC reference clock	125	MHz
USBCLK	USB Block reference clock	24	MHz
TSEC_1588_CLK_IN	PTP block input clock	125	MHz
RTC CLK	Real-time Clock	3.125	MHz

5.1 Switch configurations

Table 3 explains T2080QDS switch settings.

Table 3. Switch configurations

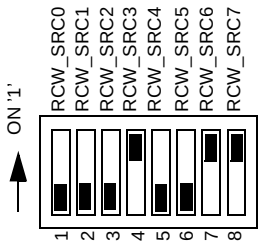
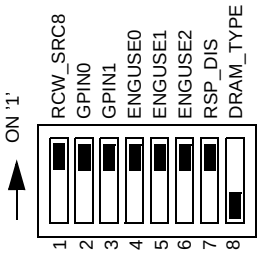
Configuration	Details
SW1 Configuration 	**SW1.1 – SW1.8: RCW_SRC[0:7]** (RCW Configuration Source) Defines RCW configuration sources [0:8] as per T2080 RM • 0_0001_0111 - 8bit NOR Flash (async 32b) • 0_0010_0111 - 16b NOR Flash (Default) • 0_0100_0000 - SDHC/eMMC • 0_0100_0101 - SPI (24b addr.) • 0_0100_1001 - I2C (ext. addr.) • 0_100x_xxxx - Hard-coded RCW • 1_0000_0100 - 8bit NAND Flash, 2kB page, 64pages/block **Note:** Last configuration bit is defined by SW2.1
SW2 Configuration 	**SW2.1 – RCW_SRC[8]** (RCW Configuration Source) Defines RCW configuration sources [0:8] as per T2080 RM **SW2.[2:3] - GPIN [0:1]** 11 - Application defined **SW2.[4:6] - ENGUSE [0:2]** 111 - Reserved **SW2.7: RSP_DIS** • 1 - Reset Seq. normal [Default] • 0 - Reset Seq. Pause **SW2.8: DRAM_TYPE** • 0 - DDR3 (1.5V) [Default] • 1 - DDR3L (1.35V)

Table 3. Switch configurations

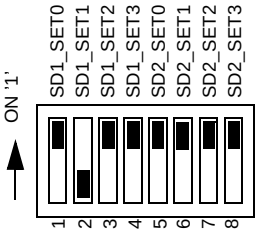
Configuration	Details
SW3 Configuration 	**SW3.[1:4]: SYSCLK Rate** • 0000 - 66.667 MHz • 0001 - 83.333 MHz • 0010 - 100.000 MHz (Default) • 0011 - 125.000 MHz • 0100 - 133.333 MHz • 0101 - 150.000MHz • 0110 - 160.000 MHz • 0111 - 166.667MHz • 1000 - 64.000 MHz **SW3.[5:6]: DDR Clock Rate** • 00 - 66.667 MHz • 01 - 100.00 MHz • 10 - 125.000 MHz • 11 - 133.333 MHz [Default] **SW3.7: Spare** • 1 - [Default] **SW3.8: SERDES Spread Spectrum** • 0 - Disable CLK1, and CLK2 [Default] • 1 - Enable CLK1, and CLK2 **Note:** For valid combinations of SYSCLK and DDRCLK, see Section 13, “Appendix A: Combinations of SYSCLK and DDRCLK”.
SW4 Configuration 	**SW4.[1:2]: SERDES1 Clock1** • 00 - 100.00 MHz (from 8T49N222A) • 01 - 125.000 MHz • 10 - 156.250 MHz [Default] • 11 - 100.00MHz **SW4.[3:4]: SERDES1 Clock2** • 00 - 100.00 MHz (from 8T49N222A) • 01 - 125.000 MHz • 10 - 156.250 MHz • 11 - 100.00MHz [Default] (fixed from 871S1022EKLFT) **SW4.[5:6] SERDES2 Clock1** • 00 - 100.00 MHz (from 8T49N222A) • 01 - 125.000 MHz • 10 - 156.250 MHz • 11 - 100.00MHz [Default] (fixed from 871S1022EKLFT) **SW4.[7:8] SERDES2 Clock2** • 00 - 100.00 MHz (from 8T49N222A) • 01 - 125.000 MHz • 10 - 156.250 MHz • 11 - 100.00MHz [Default] (fixed from 871S1022EKLFT)

Table 3. Switch configurations

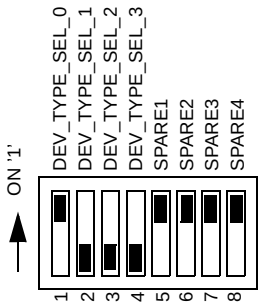
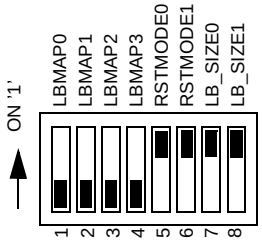
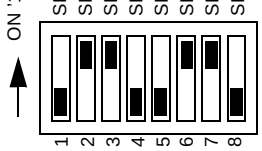
Configuration	Details
SW5 Configuration 	**SW5.[1:4] Device Type Selection [1000=T2080/T2080E]** **SW5.[1] TESTSEL_B** • 1 - [Default] **SW5.[2:3] SVR[0:1]** • 00 - [Default] **SW5.[4] ALT_CPU** • 0 - [Default] **SW5.[5] Spare1** **SW5.[6] Spare2** **SW5.[7] Spare3** **SW5.[8] Spare4**
SW6 Configuration 	**SW6.[1:4] IFC Device Mapping** • 0000 - CS0 -> NOR; CS1 -> PJET; CS2 -> NAND [Default] • 1000 - CS0 -> PJET; CS1 -> NOR; CS2 -> NAND • 1001 - CS0 -> NAND; CS1 -> NOR; CS2 -> PJET **SW6.[5:6] RESET_REQ Mode** • 00 - Do nothing - ignore • 10 - Assert HRESET (feedback) • 11 - Restart System [Default] **SW6.[7:8] IFC Size** • 00 - 8 bit • 01 - 16 bit • 10 - 28 bit • 11 - 32 bit [Default]
SW7 Configuration 	**SW7.[1:8] SERDES1 Protocol (0x66)** • 01100110 **Note:** The DIP-SWITCH positions reflect the SerDes Protocol for T2080 SD1. For more details, see Table 19-2, “SerDes Lanes Assignments and Multiplexing” of *T2080QDS Reference Manual* .

Table 3. Switch configurations

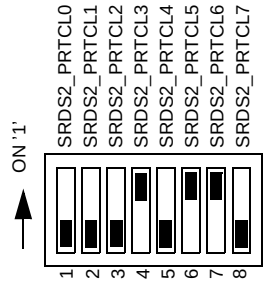
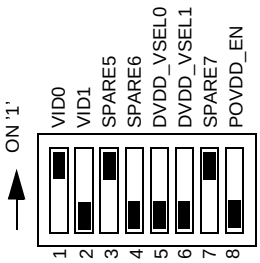
Configuration	Details
SW8 Configuration  	**SW8.[1:8] SERDES2 Protocol (0x16)** • 00010110 **Note:** The DIP-SWITCH positions reflect the SerDes Protocol for T2080 SD2. For more details, see Table 19-2, “SerDes Lanes Assignments and Multiplexing” of *T2080QDS Reference Manual.*
SW9 Configuration  	**SW9.[1:2] VID Preset** • 00 - 0.975V • 01 - 1.000V • 10 - 1.025V [Default] • 11 - 1.050V **Note:** To change the default voltage value of SW9[1:2], set SW10.5=1, and turn power OFF/ON the cycle. **SW9.[3:4] SPARE 5,6 (CVDD Preset)** • 10 - [Default] • 11 - Reserved **Note:** CVDD value is set by J34 connector. **SW9.[5:6] DVDD Preset** • 00 - 1.8V [Default] • 01 - 2.5V • 10 - 3.3V • 11 - Reserved **SW9.7: SPARE7 (LVDD Preset)** • Not used [Default] **SW9.8: POVDD Enable** • 0 - Remains OFF [Default] • 1 - Can be Powered up

Table 3. Switch configurations

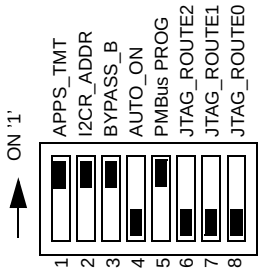
Configuration	Details
SW10 Configuration  	**SW10.1: APPS/TMT Mode** • 1 - APPS; Runs Normally [Default] • 0 - TMT; Pause reset for remote control **SW10.2: I2C Remote Address** • 0 - 0x64(Data) + 0x65(Ctrl); • 1 - 0x66(Data) + 0x67(Ctrl) [Default] **SW10.3: Bypass** • 0 - Disable Alarm Handling • 1 - Normal Mode [Default] **SW10.4: Auto ON** • 0 - Normal Mode [Default] • 1 - Power up, if ATX powered **SW10.5: PMBus Programmer** • 1 - PMBus programmer set [Default] • 0 - PMBus programmer off **SW10.[6:8]: JTAG Routing** • 000 - CCS to DUT Only [Default] • 001 - CCS to QIXIS Only (Use for I2C EEPROM's programming) • 010 - CCS to QIXIS, then DUT • 011 - Aurora to QIXIS, then DUT • 100 - CCS to QIXIS to DUT to Board 2

Table 3. Switch configurations

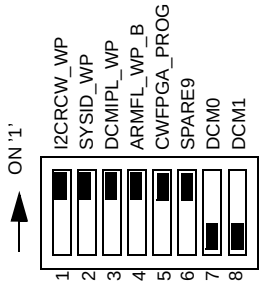
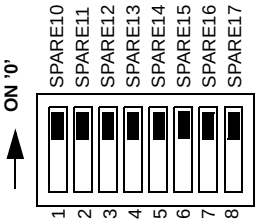
Configuration	Details
SW11 Configuration 	**SW11.1: Protect BootSeq** • 1 - BootSeq protected; [Default] • 0 - BootSeq unprotected **SW11.2: Protect System ID** • 1 - System ID protected; [Default] • 0 - System ID unprotected **SW11.3: Protect DCM Software** • 1 - OCM Software protected; [Default] • 0 - OCM Software unprotected **SW11.4: Protect ARM Boot Code** • 1 - ARM Boot Code protected; [Default] • 0 - ARM Boot Code unprotected **SW11.5: CWTAP FPGA Programming** • 1 - Normal Mode [Default] • 0 - Connect CWTAP Header to FPGA for programming **SW11.6: SPARE 9** **SW11.[7:8] DCM Control** • 00 - Reserved; [Default]
SW12 Configuration 	**SW12.[1:8]: SPARE**

Figure 6 shows the T2080QDS DIP-switch locations.

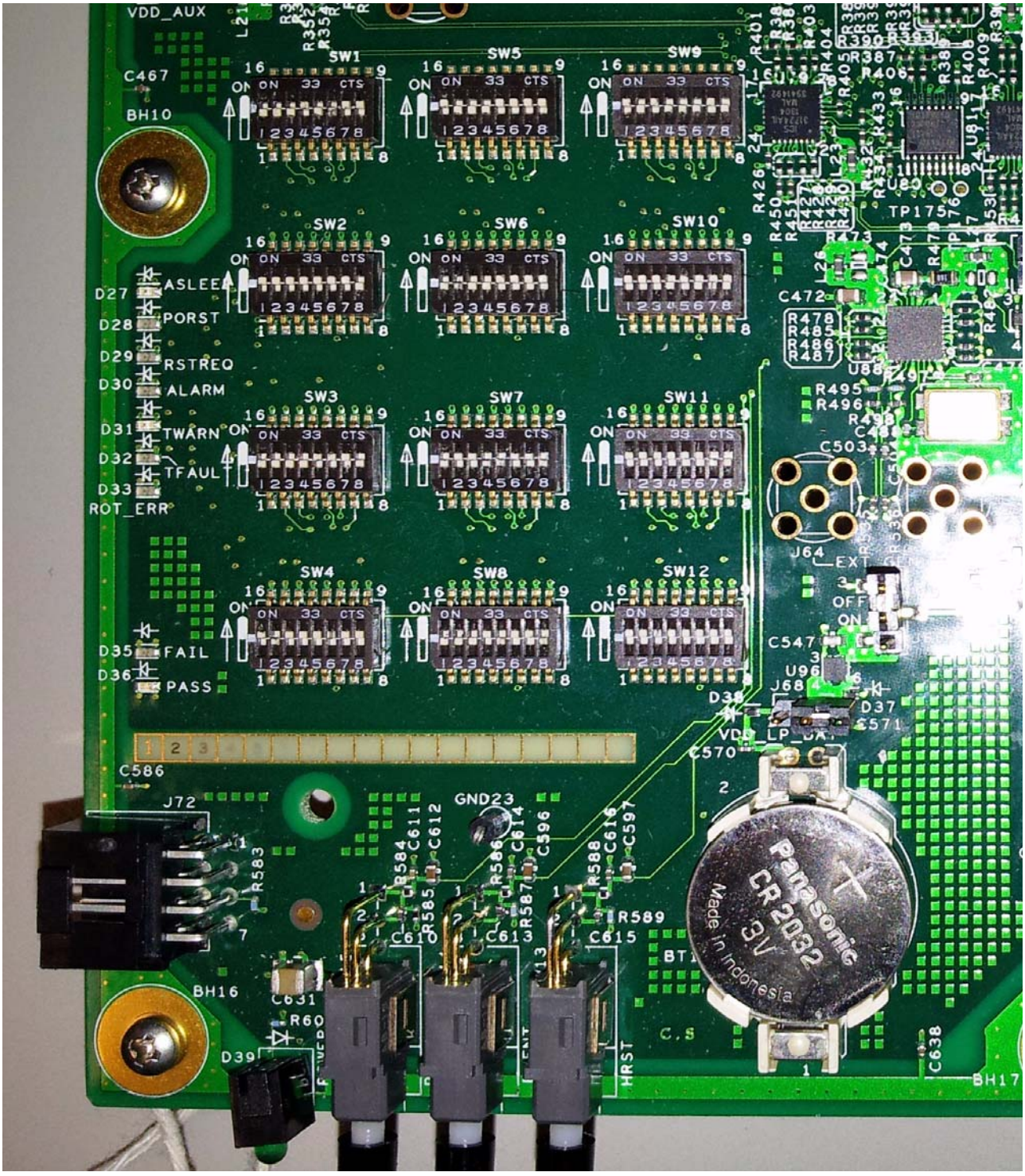


Figure 6. T2080QDS DIP-switch locations

6 Connector default settings

Table 4 lists the factory default connector settings for T2080QDS board.

Table 4. T2080QDS connector default settings

Connector	Name/Function	Type	Features	Description
J1	USB2 OTG	Micro-AB USB	5-pin	OPEN
J2	I2C2 REMOTE	Header	1x3-pin	External I^2C2 remote connection (3V3)
J3	I2C3 REMOTE	Header	1x3-pin	External I^2C3 remote connection (3V3)
J4	SD/SDHC/eMMC Card Adapter Slot	Socket	36-pin	No inserted SD/SDHC/eMMC adapter card
J5	USB1 Host	USB Type-A	4-pin	OPEN
J6	QIXIS Remote Control Ethernet Port	RJ45	8-pin	OPEN
J7	I2C3 Processor	Header	1x3-pin	T2080 I^2C3 connection (DVDD)
J8	I2C1 Host Unbuffered	Header	1x3-pin	KOMODO External I^2C1 connection (3V3)
J9	I2C1 CH3	Header	1x3-pin	External I^2C remote connection (3V3)
J10	SLOT-1 Sideband	Socket	2x20-pin	For SGMII riser card
J11	SLOT-2 Sideband	Socket	2x20-pin	For SGMII riser card
J12	SLOT-3 Sideband	Socket	2x20-pin	For SGMII/XAUI riser card
J13	SLOT-4 Sideband	Socket	2x20-pin	Not assembled
J14	SLOT-5 Sideband	Socket	2x20-pin	Not assembled
J15	I2C4 Processor	Header	1x3-pin	T2080 I^2C4 remote connection (DVDD)
J16	External System Clock Source	SMA COAX	—	OPEN
J17	I2C1 Host Buffered	Header	1x3-pin	External I^2C1 connection (3V3)
J19	I2C1 CH1	Header	1x3-pin	External I^2C remote connection (3V3)
J20	I2C1 REMOTE	Header	1x3-pin	External I^2C1 remote connection (3V3)
J21	I2C1 CH2	Header	1x3-pin	External I^2C remote connection (3V3)
J24	USBCLK	SMA COAX	—	Not assembled
J25	1588_EXTCLK	SMA COAX	—	Not assembled
J28	1588 TEST	Header	2x6-pin	TSEC_1588 PTP test OPEN
J29	QIXIS DISPLAY	Header	1x8	FPGA optional service display connection OPEN
J30	PEX SLOT-1	PEX Socket	98-pin	OPEN
J31	PEX SLOT-2	PEX Socket	98-pin	OPEN
J32	PEX SLOT-5	PEX Socket	98-pin	OPEN

Table 4. T2080QDS connector default settings

Connector	Name/Function	Type	Features	Description
J33	AURORA	AURORA Socket	2x35-pin	External AURORA cable connection
J36	CWTAP	Header	2x15-pin	External CWTAP module header
J37	PEX SLOT-3	PEX Socket	164-pin	OPEN
J38	PEX SLOT-4	PEX Socket	164-pin	OPEN
J39	COP/JTAG	Header	2x8-pin	External USB-TAP connection
J40	SATA1	SATA	7-pin	External SATA cable connection
J41	SATA2	SATA	7-pin	External SATA cable connection
J42	SYSCLK	SMA COAX	—	Not assembled
J43	IFC TEST PORT	SOCKET	120-pin	IFC Add-in card slot
J44	XTRIG	SMA COAX	—	Internal testing use
J45	DDRCLK	SMA COAX	—	Not assembled
J46	FPGA PROG	Header	2x5-pin	OPEN
J47	CASCADE	Header	2x8-pin	Cabled to 2nd board COP connector OPEN
J49, J55	EXTGEN_SLOT1,2	SMA COAX	—	Not assembled
J50	PROMJET	Header	2x25-pin	External PROMJet Flash emulator connection
J51, J56	EXTGEN_SLOT3-5	SMA COAX	—	Not assembled
J52, J57	SD1_REFCLK	SMA COAX	—	OPEN
J53, J54	SD2_REFCLK	SMA COAX	—	OPEN
J58	DDR3 DIMM2	DDR3 uDIMM Socket	240-pin	uDIMM 72bit (with ECC) Single/Dual Rank - optional
J59	HEATSINK FAN	Header	1x3-pin	12V FAN
J60	DDR3 DIMM1	DDR3 uDIMM Socket	240-pin	uDIMM 72bit (with ECC) Single/Dual Rank inserted
J63	U93 optional programming	Header	1x4-pin	Not assembled
J64, J65	EXTGEN	SMA COAX	—	Not assembled
J67	ATX-PS	Connector	2x12-pin	External ATX-PS connection
J70	XFI[1:4]	Cage/Connector	4x20-pin	SFP Modules connection
J72	CHASSIS	Header	2x4-pin	Chassis LED and software's connection
J73	ATX-PS 12V2	Connector	2x2-pin	External ATX-PS 12V connection
P1	Dual RS-232: • UART1/3-Bottom • UART2/4-Top	DB-9 RS-232	2x9-pins	External RS-232 adapter cable connection OPEN

Table 4. T2080QDS connector default settings

Connector	Name/Function	Type	Features	Description
P2	Dual RJ45: • EC1-Bottom • EC2-Top	RJ-45	Dual 2x8-ports	Dual GETH Port connection OPEN
U61	SUBASSEMBLY IC MEM FLASH 1GB 130NS 2.7-3.6V 1.8V IO TSOP56 + SKT 56 TSOP SMT 0.5MM 210H AU	Socket +NOR flash	56-pin	1GB NOR Flash inserted
BT1	Battery Holder	Socket	—	Standby battery CR2032 inserted

Figure 7 shows the connectors locations.

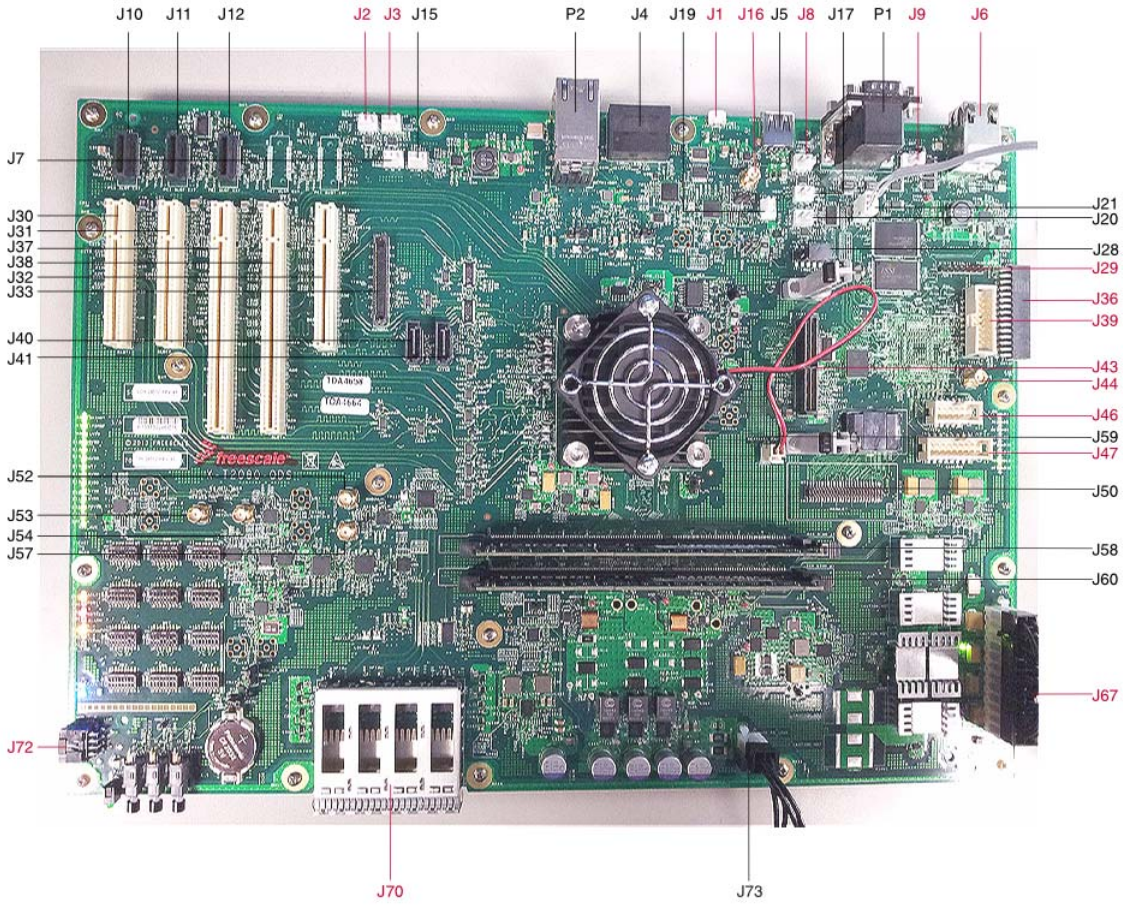


Figure 7. T2080QDS connectors

7 Jumper default settings

Table 5 lists the factory default jumper settings for T2080QDS.

Table 5. T2080QDS Jumper default settings

Jumper	Type	Features	Name/Function	Description
J18	Header	1x3-pin	SYSCLK_SEL	• 1-2 pins shorted - On-board clock source selected [Default] • 2-3 pins shorted - external clock generator selected
J22	Header	1x3-pin	EC2 GTXCLK	• 2-3 pins shorted - T2080 GTXCLK 125 is driven from on-board clock generator [Default] • 1-2 pins shorted - T2080 GTXCLK 125 is driven from Eth PHY Realtek RTL8211EG-VB-CG CLK125 output
J23	Header	1x3-pin	EC1 GTXCLK	• 2-3 pins shorted - T2080 GTXCLK 125 is driven from on-board clock generator [Default] • 1-2 pins shorted - T2080 GTXCLK 125 is driven from Eth PHY Realtek RTL8211EG-VB-CG CLK125 output
J26	Header	1x2-pin	PROG_MTR	• Shorted: Connect POVDD (1.89V) to T2080 PROG_MTR pin • Open [Default]: T2080 PROG_MTR pin PD'd
J27	Header	1x2-pin	PROG_SFP	• Shorted: Connect POVDD (1.89V) to T2080 PROG_SFP pin • Open [Default]: T2080 PROG_SFP pin PD'd
J34	Header	1x3-pin	CVDD_SEL	• 1-2: 1.8V [Default] • 2-3: 2.5V
J35	Header	1x2-pin	USB1 MODE	• Shorted: [Default] - Host Mode • Open: Device Mode
J48	Header	1x3-pin	FA_VL	• FA_VL voltage selector • 1-2 pins shorted FA_VL=VDD_CPU • 2-3 pins shorted (GND) [Default]
J61	Header	1x2-pin	U88 buffer mode selector	• Shorted: Bypass U88 SS PLL, and force it to operate as simple buffer • Open[Default]: U88 operate as PLL buffer
J62	Header	1x2-pin	PROG_VPG	• Shorted: Force U93 be 1st time programmed • Open[Default]: Normal mode
J66	Header	1x3-pin	VDD_LP_DET	• 1-2: ON; • 2-3: OFF [Default]
J68	Header	1x2-pin	VDD_LP_BAT	• Connected: Enabled VDD_LP_BAT • Disconnected [Default]: Disabled VDD_LP_BAT
J69	Header	1x2-pin	FORCE ATX-ON	• Connected: Force ATX-PS ON • Disconnected [Default]: Normal operation
J71	Header	1x2-pin	12V current sense resistors bypass	Not assembled

Figure 8 shows the T2080QDS jumper locations.

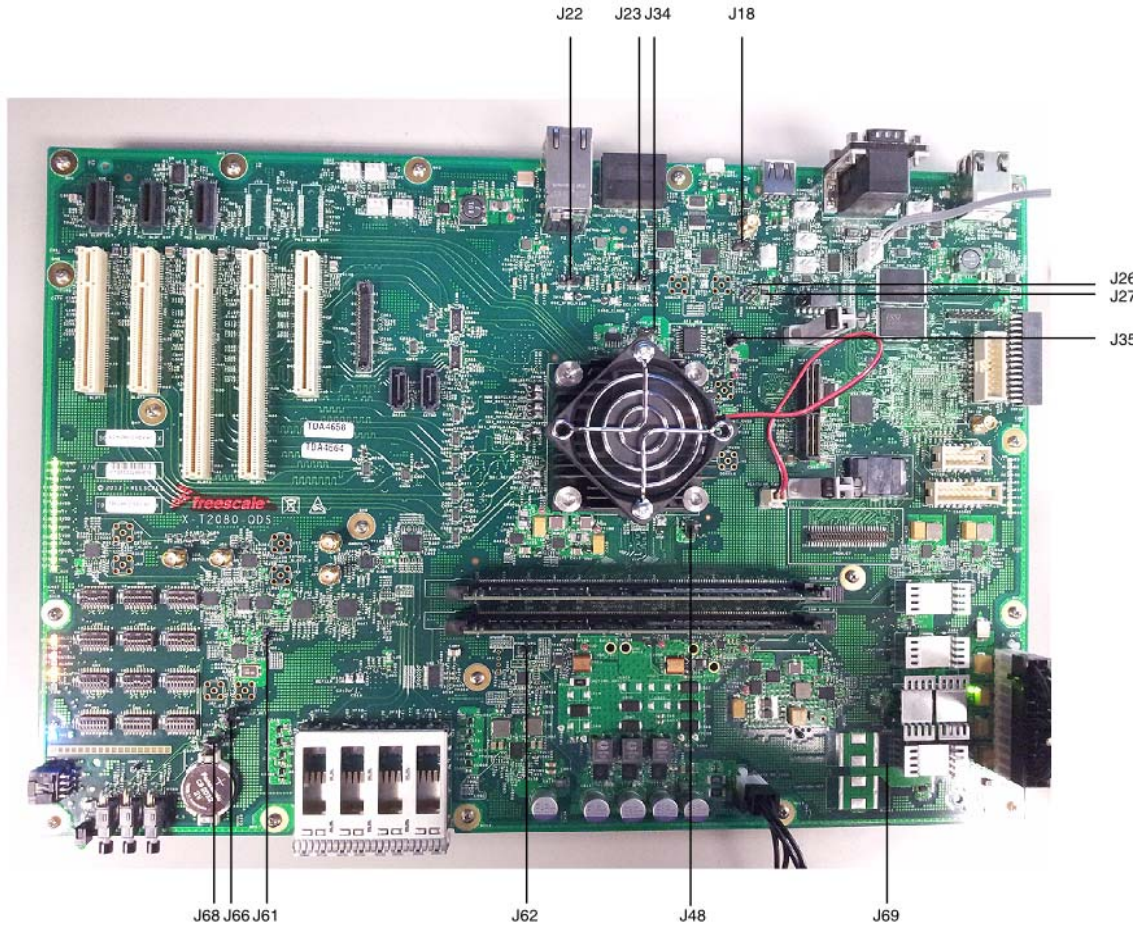


Figure 8. T2080QDS jumper locations

8 Push buttons

Table 6 lists the functioning of push buttons of theT2080QDS board.

Table 6. T2080QDS push buttons

Push Button	Function	Description
SW15	POWER (ON/OFF)	• Press SW15 to assert Power-ON/OFF • Powered by an external ATX power supply by J67 and J73 power connectors • System automatically powers-on after asserting ATX power supply if SW10.4=1
SW14	EVENT	Press SW14 to issue processor IRQ (TBD)
SW13	Hard Reset (HRST)	Press SW13 for Hard Reset

Figure 9 shows the push button locations.

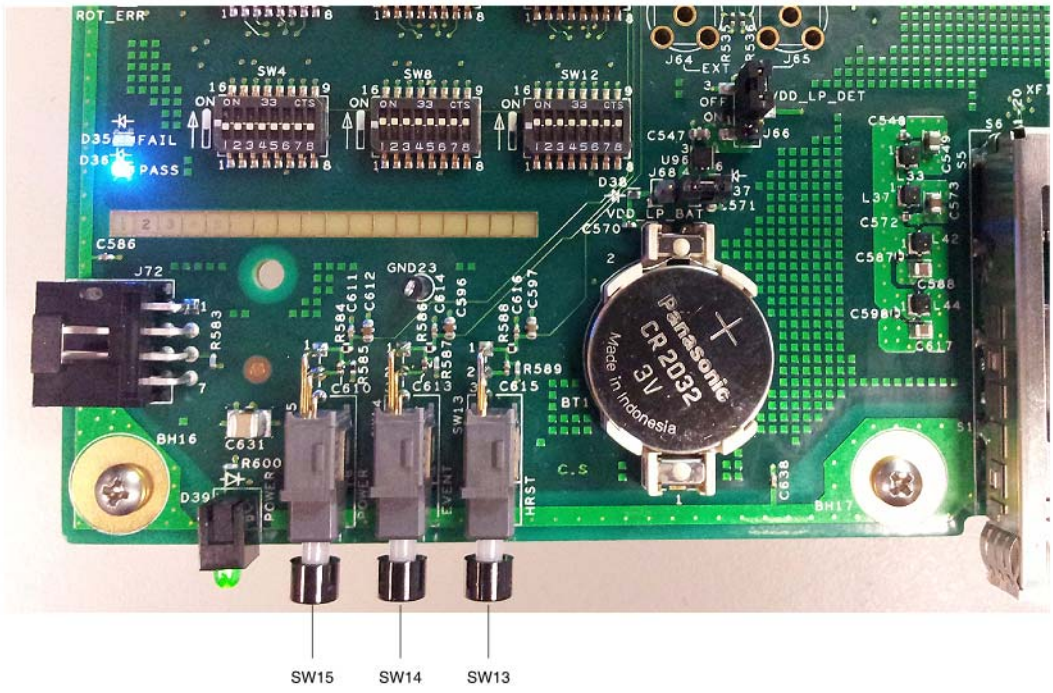


Figure 9. T2080QDS push button locations

9 LED lights

Table 7 explains the LED locations and Figure 10 lists the functioning of T2080QDS LED lights.

Table 7. T2080QDS LEDs

LED	Color	Name	LED ON	LED OFF
D3	Green	M0	FPGA IFC Master is active	FPGA IFC Master is not active
D5	Green	M1	FPGA ARM CPU is active	FPGA ARM CPU is not active
D6	Green	M2	Remote I2C_Host is active	Remote I2C_Host is not active
D9	Green	M3	FPGA I2C Master is active	FPGA I2C Master is not active
D11	Green	M4	FPGA JTAG Tap is active	FPGA JTAG Tap is not active
D12	Green	M5	FPGA OCM transaction is active	FPGA OCM transaction is not active
D15	Green	M6	FPGA OCM is enabled (OCM heartbeat)	FPGA OCM is disabled
D16	Green	M7	FPGA is active (FPGA heartbeat)	FPGA is not active
D4	Green	3V3HOT	Power Good: 3V3HOT	Failed: 3V3HOT Power
D7	Green	1V5HOT	Power Good: 1V5HOT	Failed: 1V5HOT Power
D8	Green	LVDD	ON: LVDD voltage supply	OFF: LVDD voltage supply
D10	Green	OVDD	ON: OVDD voltage supply	OFF: OVDD voltage supply
D13	Green	1V8	ON: 1V8 voltage supply	OFF: 1V8 voltage supply
D14	Green	GVDD	ON: GVDD voltage supply	OFF: GVDD voltage supply
D17	Green	VTT	ON: VTT voltage supply	OFF: VTT voltage supply
D18	Green	DVDD	ON: DVDD voltage supply	OFF: DVDD voltage supply
D19	Green	SVDD	ON: SVDD voltage supply	OFF: SVDD voltage supply
D20	Green	CVDD	ON: CVDD voltage supply	OFF: CVDD voltage supply
D21	Green	XVDD	ON: XVDD voltage supply	OFF: XVDD voltage supply
D22	Green	POVDD	ON: POVDD voltage supply	OFF: POVDD voltage supply
D25	Green	VDD	ON: VDD voltage supply	OFF: VDD voltage supply
D26	Green	VDD_AUX	ON: VDD_AUX voltage supply	OFF: VDD_AUX voltage supply
D27	Yellow	ASLEEP	Asserted: T2080 HRESET	T2080 HRESET unasserted
D28	Red	PORESET	Asserted: T2080 PORESET	T2080 PORESET unasserted
D29	Red	RSTREQ	Asserted: T2080 RESET REQUEST	T2080 RESET REQUEST unasserted

Table 7. T2080QDS LEDs

LED	Color	Name	LED ON	LED OFF
D30	Red	ALARM	One of the following: • GEN - A fault for which no specific additional data is available • PSQF - The QIXIS power sequencer failed to bring up all power supplies, as requested • PDOWN - One or more power supplies unexpectedly failed to supply stable power • ORIENT - A processor is incorrectly installed • VDDT - The VDD power supply temperature has exceeded the warning limits • TWARN - The temperature has exceeded the warning limits • TALERT - The temperature has exceeded the fault limits	Does not happen, any listed in LED ON column situations
D31	Yellow	TWARN	T2080 temperature is near to the maximum allowable	T2080 temperature is within the normal range
D32	Red	TFAULT	T2080 Exceed the permissible temperature	T2080 temperature is within the normal range
D33	Red	ROT_ERR	Incorrect processor orientation in the socket	Correct processor orientation in the socket
D34	Green	HOT_5V	ON: 5VSB ATX PS voltage supply	OFF: 5VSB ATX PS voltage supply
D35	Red	FAIL	One of the following: • Unsuccessful FPGA initialization • Incorrect processor orientation • Some/all of on-board voltage is in poor condition • Some/all of on-board reset configuration devices fail	One of the following: • Power Off • Successful FPGA initialization; correct processor orientation; and all on-board voltage is in good condition • All reset configuration and sequencer passed
D36	Blue	PASS	One of the following: • Successful FPGA initialization; correct processor orientation; and all on-board voltage is in good condition • All reset configuration and sequencer passed	One of the following: • Power Off • Unsuccessful FPGA initialization • Incorrect processor orientation • Some/all of on-board voltage is in poor condition • Some/all of on-board reset configuration devices fail
D39	Green	3V3	ON: 3.3V voltage supply	OFF: 3.3V voltage supply

Figure 10. T2080QDS LED (D) locations

10 Working environment

Table 8 lists the working environment required for T2080QDS.

Table 8. T2080QDS working environment

Mode	Component	Optional Expansion
Standalone	ATX12V	• Plug SGMII riser card into PEX slots 1, 2, or 3 • Plug XAUI riser card into PEX slot 3 • Insert SFP modules into XFI connector J70 • Insert SD/SDHC/eMMC adapter cards into J4 slot

NOTE

ATX12V powers the T2080QDS through J67 and J73 connectors. The power supply is 1U and is mounted inside the chassis.

11 Getting started with T2080QDS

The following section outlines the standalone activation of T2080QDS board.

The additional hardware options that are not contained in the T2080QDS kit includes:

- SD/SDHC/eMMC cards (additional)
- XFI modules
- Aurora, and PROMJet devices
- CodeWarrior USB TAP
- SGMII/XAUI riser cards

CAUTION

The board is marked with several **Caution Hot** locations (R425, R494, R563, R572, R996, and R1003); they are a consideration when the chip is in ASLEEP mode and no processor is attached on the board.

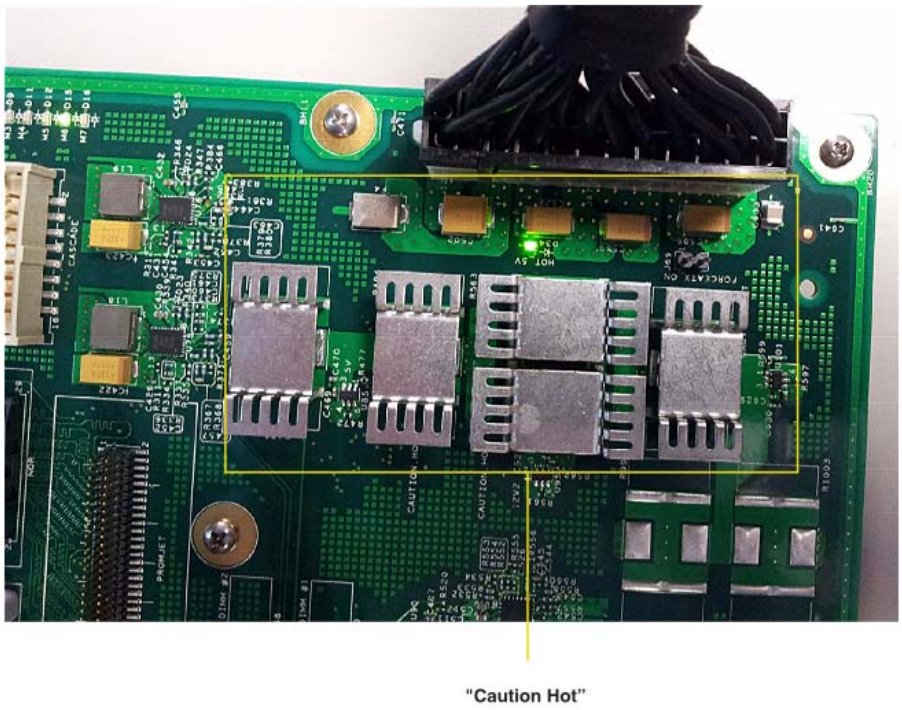


Figure 11. Caution hot locations for the T2080QDS Board

Use the following steps to ensure correct initial board power-up:

1. Verify that all hardware kit contents are present.
2. Check and verify the T2080QDS default switch settings. See Section 5, “Switch default settings”.
3. Check and verify the T2080QDS default connector settings. See Section 6, “Connector default settings”.
4. Check and verify the T2080QDS default jumper settings. See Section 7, “Jumper default settings”.
5. Establish the working environment for T2080QDS. See Section 10, “Working environment”.
6. Perform the initial board power-up and check LEDs for correct function.
   a) Power the board using the external ATX12V power supply. The LED D34 (HOT_5V) will glow green.
   b) Move the power switch (SW15) to ON.
   c) Verify the LEDs D3:D39 complete the Power-ON reset sequence.
   d) Move the power switch (SW15) to OFF.

Figure 12. LED connections

7. Follow the instructions to connect to the CodeWarrior USB TAP.

CAUTION

Make sure to follow the instructions in the given sequence to avoid any damage.

a) Align the red stripe of the USB-UTAP connector cable with Pin 1 of the JTAG/COP 16-pin connector (at J39).
b) Connect the connector cable to J39.
c) Move the power switch (SW15) to ON.
d) Verify the LEDs D3:D39 complete the Power-ON reset sequence.

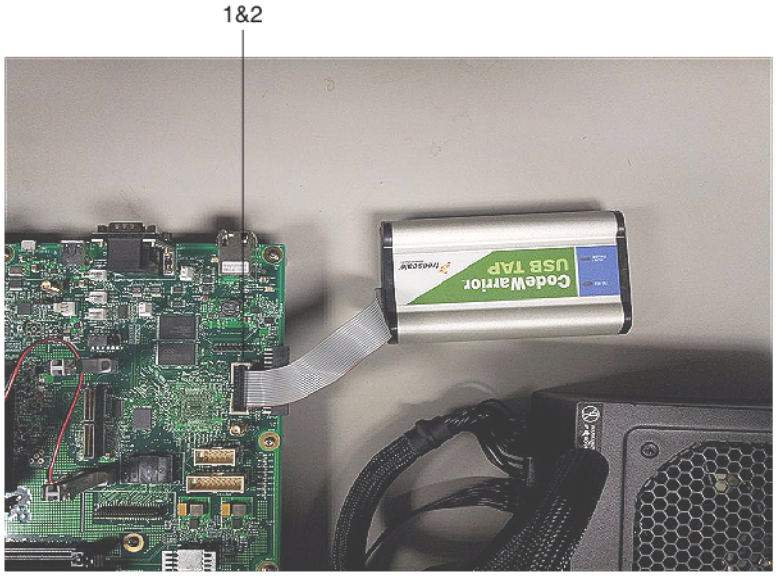


Figure 13. Connection with CodeWarrior USB TAP

NOTE

Freescale CodeWarrior USB TAP enables CodeWarrior IDE software to work with T2080QDS.

CodeWarrior USB TAP is not included in hardware kit.

8. Attach the cables as per user development needs and planned board use.
   a) Use a RS-232 standard serial cable to connect between DB9 (P1B-Bottom: UART 1/3) and the power cable.
   b) Select and connect the appropriate Ethernet RJ45 cable.
   c) Connect the shielded cable at P2-Bottom–GETH1,or P2–Top-GETH2.

NOTE

Only one shielded Ethernet RJ45 cable is included in the T2080QDS kit.

   d) Connect a USB*A-to-MicroUSB*B cable to J1 -USB2(OTG).

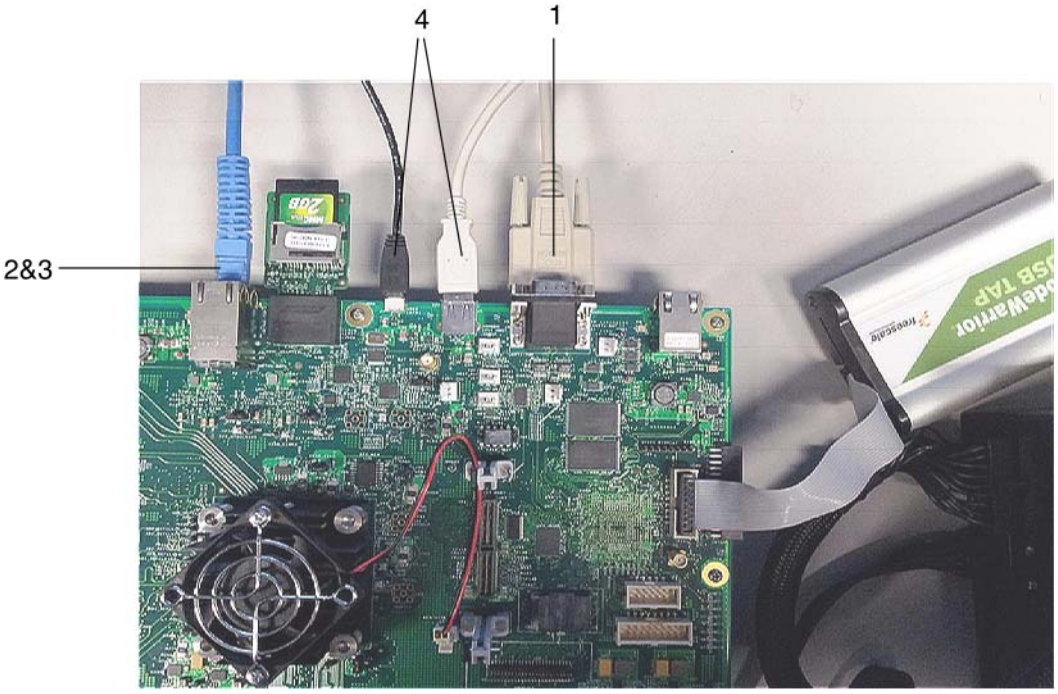


Figure 14. T2080QDS board connections

12 SerDes options

The following sections explains the four SerDes module setup options:

- Section 12.1, “SGMII riser card”
- Section 12.2, “XAUI riser card”
- Section 12.3, “PEX loopback card”
- Section 12.4, “SFP modules”

Table 9 shows the interfaces are distributed in different slots.

Table 9. SerDes options

PEX Slot #	Interfaces to be tested
1 (J30)	PEX4: Gen2 x1x2x4, Gen3 x1x2x4; SGMII x1x4
2 (J31)	PEX1,PEX2: Gen2 x1; SGMII x2x3
3 (J37)	PEX3: Gen2 x1x4x8; SGMII x2x4; XAUI-HiGig
4 (J38)	PEX1: Gen2 x4 x8, Gen3 x4; SRIO2
5 (J32)	PEX2 Gen2 x2x4; SRIO1

12.1 SGMII riser card

Follow the instructions to setup the SGMII riser card:

1. Select the configuration scenario, for example, the switch settings to be used.
2. Connect the supplied cables as per the instructions. See Section 11, “Getting started with T2080QDS”.
3. Insert the SGMII riser card into the J30, J31, and J37 slots.
4. Connect a cross cable to SGMII riser card connectors or a cable to an external destination.
5. Move the power switch (SW15) to ON.

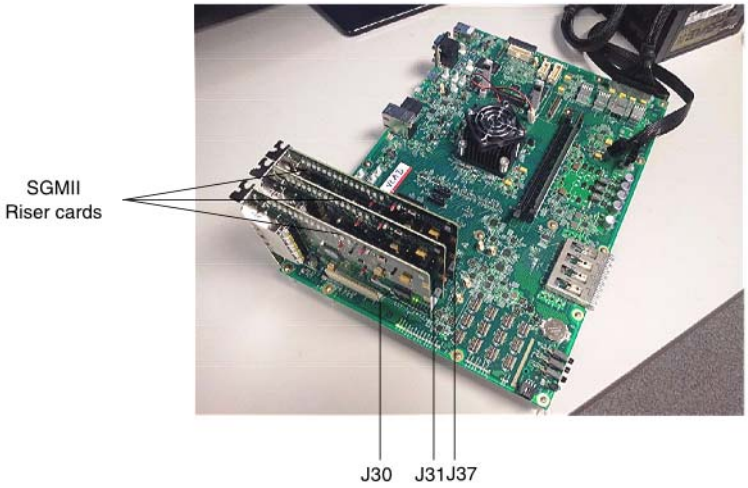


Figure 15. SGMII riser card connections

12.2 XAUI riser card

Follow the instructions to setup the XAUI riser card:

1. Select the configuration scenario, for example, the switch settings to be used.
2. Connect the supplied cables as per the instructions. See Section 11, “Getting started with T2080QDS”.
3. Insert the XAUI riser card into J37 slot.
4. Connect the cable to an external destination.
5. Move the power switch (SW15) to ON.

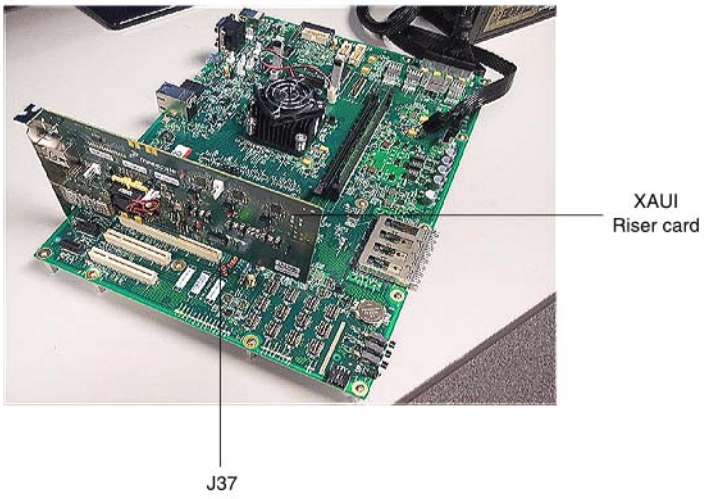


Figure 16. XAUI riser card connections

12.3 PEX loopback card

Follow the instructions to setup the PEX loopback card:

1. Select the configuration scenario, for example, the switch settings to be used.
2. Connect the supplied cables as per the instructions. See Section 11, “Getting started with T2080QDS”.
3. Insert the PEX loopback card into J30, J31, J32, J37, and J38 slots depending on the selected mode.
4. Move the power switch (SW15) to ON.

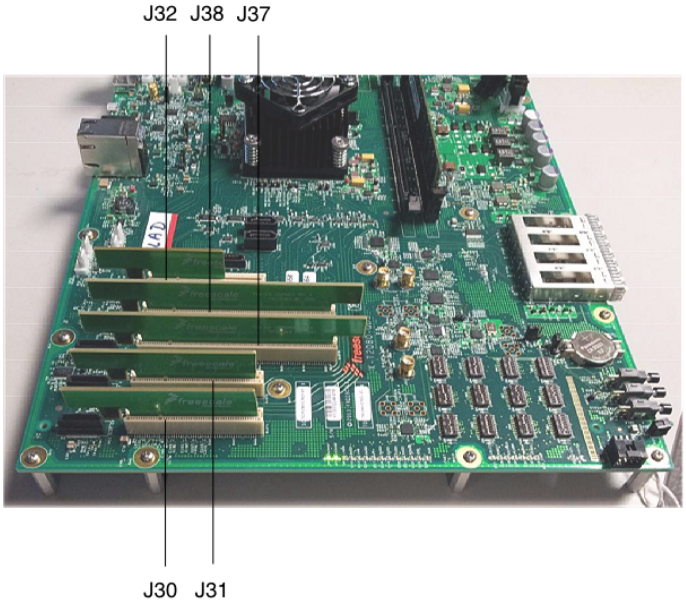


Figure 17. PEX loopback card connections

12.4 SFP modules

Follow the instructions to setup a SFP module:

1. Select the configuration scenario, for example, the switch settings to be used.
2. Insert SFP Modules or XFI Cable into cage or connector J70, depending on the selected mode.
3. Connect optical cable/cables between SFP modules or to external test system (alternatively connect XFI cable to the external test system).
4. Move the power switch (SW15) to ON.

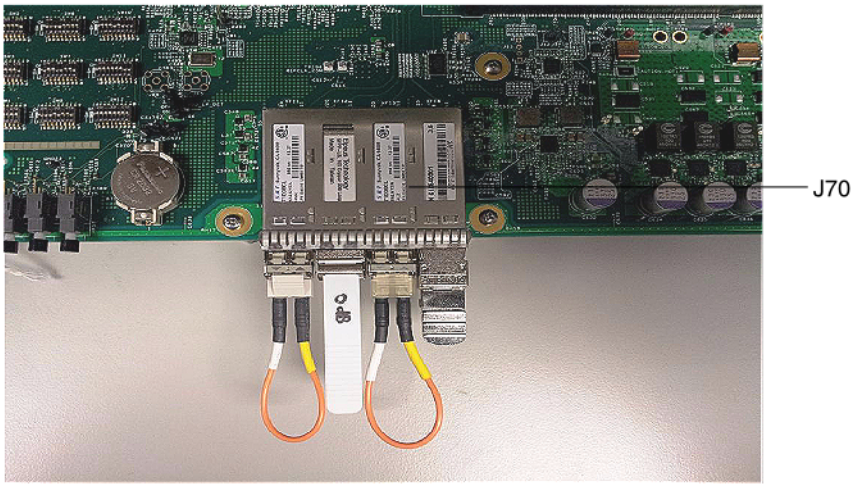


Figure 18. SFP module connections

13 Appendix A: Combinations of SYSCLK and DDRCLK

Figure 19 lists the correct combinations of SYSCLK and DDRCLK. The yellow and red markings are measured values different from expected values.

SYS	DDR	SYSCLK Expected	DDRCLK Expected	SYSCLK Actual	DDRCLK Actual
0000	00	66.666	66.666	66.667	66.667
0001	00	83.333	66.666	83.333	66.667
0010	00	100.000	66.666	100.000	66.667
0011	00	125.000	66.666	125.000	66.667
0100	00	133.333	66.666	133.333	66.667
0101	00	150.000	66.666	150.000	66.667
0110	00	160.000	66.666	160.045	65.901
0111	00	166.666	66.666	166.667	66.667
1000	00	64.000	66.666	63.976	63.976
0000	01	66.666	100.000	66.667	100.000
0001	01	83.333	100.000	83.333	100.000
0010	01	100.000	100.000	100.000	100.000
0011	01	125.000	100.000	125.000	100.000
0100	01	133.333	100.000	133.333	100.000
0101	01	150.000	100.000	150.000	100.000
0110	01	160.000	100.000	159.821	101.705
0111	01	166.666	100.000	166.666	100.000
1000	01	64.000	100.000	63.970	95.960
0000	10	66.666	125.000	66.666	125.000
0001	10	83.333	125.000	83.333	125.000
0010	10	100.000	125.000	100.000	125.000
0011	10	125.000	125.000	125.000	125.000
0100	10	133.333	125.000	133.333	120.000
0101	10	150.000	125.000	150.000	120.000
0110	10	160.000	125.000	160.040	124.479
0111	10	166.666	125.000	166.666	125.000
1000	10	64.000	125.000	63.973	127.000
0000	11	66.666	133.333	66.667	133.333
0001	11	83.333	133.333	82.091	133.398
0010	11	100.000	133.333	100.000	133.333
0011	11	125.000	133.333	120.000	133.333
0100	11	133.333	133.333	133.333	133.333
0101	11	150.000	133.333	150.000	133.333
0110	11	160.000	133.333	159.821	139.844
0111	11	166.666	133.333	166.741	129.688
1000	11	64.000	133.333	63.975	127.951

Figure 19. Combinations of SYSCLK and DDRCLK

14 Appendix B: Revision history

Table 10 summarizes revisions to this document.

Table 10. Revision history

Revision	Date	Description
Rev. 0	10/2015	Initial Public release.

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