MAX77752 Multi-Channel Integrated Power Management IC

General Description

The MAX77752 is a highly-integrated power management solution including three step-down converters, a low-dropout linear regulator, two external regulator enable outputs, two dedicated load switch controllers, and an inrush-current limiter which can be configured as a third load switch controller using OTP. The MAX77752 provides a combination of high-performance power management components, high-accuracy monitoring, and a customized top level controller that results in an efficient, size optimized solution.

The 40-pin, 5mm x 5mm x 0.8mm, 0.4mm pitch TQFN package is ideal for space constrained applications.

Numerous factory programmable options allow the device to be tailored for many variations of the end application.

Applications

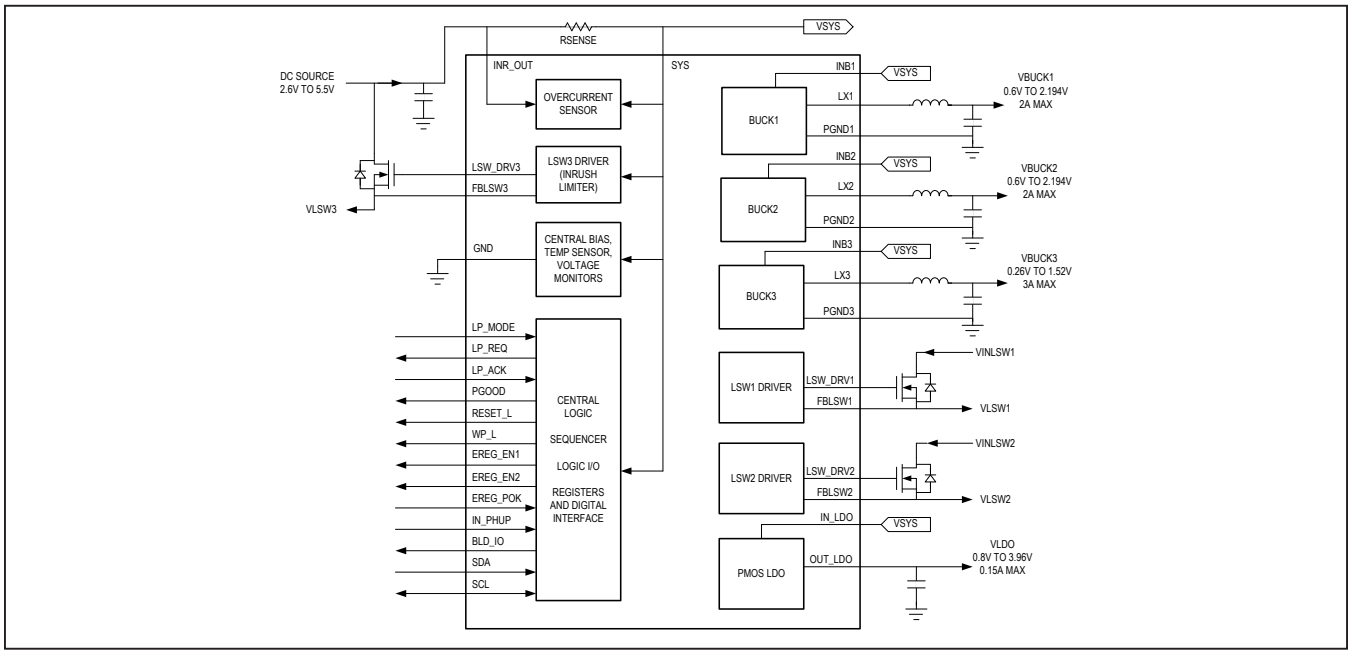
- Solid-State Drive Systems
- Handheld Devices
- Gaming Consoles
- Drones
- Automation Systems
- Cameras

Benefits and Features

- Highly Integrated
  - Three Buck Regulators
    - Integrated High-Accuracy Brownout Comparators
  - One Low-Dropout Linear Regulator
    - Low-Input Voltage
  - Two Dedicated Load Switch Controllers
  - One Inrush-Current Limiter, Configurable to be Load Switch 3 Controller Using OTP
  - Two External Regulator Enable Outputs
  - Voltage Monitor for Backup Power Control
- Highly Flexible and Configurable
  - I2C-Compatible Interface
  - Factory OTP Options Available
  - Flexible Power Sequencer
  - Configurable Sleep State Control
- Small Size
  - 40-Pin, 5mm x 5mm x 0.8mm, 0.4mm Pitch TQFN
  - 70mm2 Total Solution Size

Ordering Information appears at end of data sheet.

Simplified Block Diagram



Absolute Maximum Ratings

Top
- IN_DRV to GND ..... -0.3V to +16.0V
- IN_SNS to GND (Note 1) ..... -0.3V to +6.0V
- INR_OUT to GND ..... -0.3V to +6.0V
- SYS to GND ..... -0.3V to +6.0V
- IN_PHUP to GND ..... -0.3V to +6.0V
- RESET_L to GND ..... -0.3V to V_{SYS}+0.3V
- LP_REQ to GND ..... -0.3V to V_{SYS}+0.3V
- LP_ACK to GND ..... -0.3V to V_{SYS}+0.3V
- LP_MODE to GND ..... -0.3V to V_{SYS}+0.3V
- WP_L to GND (Note 2) ..... -0.3V to V_{H_INT}
- PGOOD to GND (Note 2) ..... -0.3V to V_{H_INT}
- EREG_EN1 to GND (Note 2) ..... -0.3V to V_{H_INT}
- EREG_EN2 to GND ..... -0.3V to 6.0V
- EREG_POK to GND ..... -0.3V to V_{SYS}+0.3V
- BLD_IO to GND (Note 2) ..... -0.3V to +6.0V
- WP_L Sink Current 35mA
- RESET_L Sink Current 35mA
- PGOOD Sink Current 35mA
- EREG_EN1 Sink Current 35mA
- EREG_EN2 Sink Current 35mA
- LP_REQ Sink Current 35mA
- DGND to GND ..... -0.3V to +0.3V

LDO
- IN_LDO to GND ..... -0.3V to +6.0V
- OUT_LDO to GND ..... -0.3V to V_{IN_LDO}+0.3V

Buck
- INB1, INB2, INB3 to SYS ..... -0.3V to +0.3V
- INB1 to PGND1 ..... -0.3V to +6.0V
- INB2 to PGND2 ..... -0.3V to +6.0V
- INB3 to PGND3 ..... -0.3V to +6.0V
- LX1 to PGND1 (Note 3) ..... -0.3V to V_{INB1}+0.3V
- LX2 to PGND2 (Note 3) ..... -0.3V to V_{INB2}+0.3V
- LX3 to PGND3 (Note 3) ..... -0.3V to V_{INB3}+0.3V
- LX1, LX2 RMS Current per pin (T_J = +110°C) (RMS current per pin (T_J = +110°C)) 1.7A
- LX3 RMS Current per pin (T_J = +110°C) (RMS current per pin (T_J = +110°C)) 3.0A
- FBB1, FBB2, FBB3 to GND ..... -0.3V to V_{SYS}+0.3V
- PGND1, PGND2, PGND3 to GND ..... -0.3V to +0.3V

I^2C
- SDA, SCL to GND ..... -0.3V to $V_{IN\_VIO\_I2C}$+0.3V
- SDA Sink Current 35mA

Load Switch
- LSW_DRV1 to GND ..... -0.3V to +16.0V
- LSW_DRV2 to GND ..... -0.3V to +16.0V
- FBLSW1 to GND ..... -0.3V to V_{SYS}+0.3V
- FBLSW2 to GND ..... -0.3V to V_{SYS}+0.3V

Continuous Power Dissipation (Multilayer Board)
- T_A = +70°C, derate 35.70mW/°C above +70°C ..... mW to 2857.1mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: IN_SNS voltage ramp rates greater than 2.8V/µs trigger the internal ESD device and should be avoided. The ESD device recovers if exposed to an excessive ramp rate.

Note 2: V_{H_INT} is the maximum voltage of V_{SYS} and V_{IN_PHUP}.

Note 3: The specified voltage limitation is for steady state conditions. Dead times of a few nano seconds exist during the dynamic BUCK regulator transitions from inductor charging to inductor discharging and vice versa. These dead times allow internal clamping diodes to PGNDx and INBx to forward bias (Vf~1V). When the LXx waveform is observed on a high-bandwidth oscilloscope (≥100MHz), the LXx transition edges are commonly seen with 1.5V spikes. These spikes are due to (1) the internal clamping diode forward voltage and (2) the high rate of current change through the current loop's inductance (V = L x di/dt). Designs must follow the recommended printed circuit board (PCB) layout in order to minimize this current loop's inductance.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

PACKAGE CODE	T4055+1C
Outline Number	21-0140
Land Pattern Number	90-0016
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	45°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics—Global Resources

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
OFF State Quiescent Current	I_{QSYS_OFF}	$V_{SYSUVLO} < V_{SYS} < V_{SYS\_RESET}$ (rising), OTP_INT_PU = 1, all regulators are disabled. This includes any central bias currents disabled (EREG_EN1 pulled to V_{SYS})		86	135	µA
DEVSLP State Quiescent Current	I_{QSYS_DEVSLP}	V_{SYS} = 3.3V, $V_{SYS} > V_{SYS\_RESET}$, OTP_INT_PU = 0, PMIC in DEVSLP State, Buck2, Buck3, LDO enabled in low-power mode. No load on all regulators. All other regulators disabled		70	125	µA
		V_{SYS} = 5V, $V_{SYS} > V_{SYS\_RESET}$, OTP_INT_PU = 0, PMIC in DEVSLP state, Buck2, Buck3, LDO enabled in low-power mode. No load on all regulators. All other regulators disabled		90	155	
Buck Quiescent Supply Current	I_{QSYS_BUCK}	V_{SYS} = 5V, $V_{SYS} > V_{SYS\_RESET}$, all bucks enabled in normal-power mode and skip mode		233	420	µA

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS AND REFERENCE CURRENT GENERATOR						
Operating Voltage Range	V_{SYS}		2.6		5.5	V
Quiescent Supply Current	I_{QCBRG}	V_{SYS} > $V_{SYSUVLO}$ (rising)		25		µA
Shutdown Supply Current		V_{SYS} < $V_{SYSUVLO}$ (falling)		0.1		µA
Bias Enable time	t_{BIASOK}			100		µs
POR COMPARATOR (INTERNAL)						
Quiescent Supply Current	I_{QSYS_POR}			1		µA
POR Undervoltage-Lockout Threshold	V_{POR}	V_{SYS} falling		1.33		V
POR Threshold Hysteresis	V_{HYS_POR}	V_{SYS} rising		160		mV
Response Time		100mV overdrive		300		µs
POR to UVLO Delay	$t_{PORUVLO}$	V_{SYS} rising across POR (1V to 2V)		100		µs
		V_{SYS} falling across POR		50		
SYS UNDERVOLTAGE-LOCKOUT COMPARATOR						
Quiescent Supply Current	I_{QSYS_UVLO}			1		µA
SYS Undervoltage-Lockout Threshold	$V_{SYSUVLO}$	V_{SYS} falling	2.00	2.10	2.25	V
SYS Undervoltage-Lockout Hysteresis	V_{INUVLO_HYS}			400		mV
SYS Undervoltage-Lockout Response Time	$t_{SYSUVLO}$	100mV overdrive, falling edge		150		µs
SYS RESET COMPARATOR						
Quiescent Supply Current	I_{QSYS_RESET}			3		µA
Reset Falling Threshold Range	V_{SYS_RESET}	Programmed by SYSRST[3:0]	2650		4150	mV
Reset Threshold Step Size				100		mV
Reset Threshold Hysteresis Range	$V_{SYSRESET\_HYS}$	Programmed by SYSRSTHYS[1:0]	150		300	mV
Reset Threshold Hysteresis Step Size				50		mV
Reset Comparator Response Time	$t_{SYSRESET}$			5		µs
Reset Comparator Accuracy		SYSRSTTH[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF	-2.5		+2.5	%

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS BROWNOUT COMPARATOR						
Brownout Falling Threshold Range	V_{SYS_BO}	Programmed by SYSBOTH[3:0]	2800		4300	mV
Brownout Threshold Step Size				100		mV
Brownout Threshold Hysteresis Range	$V_{SYS\_BO\_HYS}$	Programmed by SYSBOHYS[1:0]	150		300	mV
Brownout Threshold Hysteresis Step Size				50		mV
Brownout Comparator Response Time	t_{SYSBO}	SYS_BO_PR[1:0] = 0b00 (fast), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/µs		1.04		µs
		SYS_BO_PR[1:0] = 0b01 (med-fast), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/µs		1.14		
		SYS_BO_PR[1:0] = 0b10 (med-slow), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/µs		1.30		
		SYS_BO_PR[1:0] = 0b11 (slow), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/µs		1.68		
Brownout Comparator Response Time (DEVSLP)	t_{SYSBO}	PMIC in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/µs		3.53		µs
Quiescent Supply Current	I_{QSYS_BO}	SYS_BO_PR[1:0] = 0b00 (fast), PMIC not in DEVSLP state		13.4		µA
		SYS_BO_PR[1:0] = 0b01 (med-fast), PMIC not in DEVSLP state		10.4		
		SYS_BO_PR[1:0] = 0b10 (med-slow), PMIC not in DEVSLP state		7.4		
		SYS_BO_PR[1:0] = 0b11 (slow), PMIC not in DEVSLP state		4.4		
Quiescent Supply Current (DEVSLP)	I_{QSYS_BO}	PMIC in DEVSLP state		1.3		µA
Brownout Comparator Accuracy		SYSBO[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF, PMIC is not in DEVSLP state	-2.5		+2.5	%
Brownout Comparator Accuracy (DEVSLP)		SYSBO[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF, PMIC is in DEVSLP state	-2.5		+2.5	%
Brownout Timer Period	t_{BO}	T_BO_EN = 1		100		ms

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Clock Frequency	CLK32K	V_{SYS} = 5V		31.5		kHz
Oscillator Tolerance		V_{SYS} = 3.3V	-10		+10	%
		V_{SYS} = 5V	-10		+10	
WP_L OUTPUT (OPEN DRAIN)						
WP_L Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
WP_L Open Leakage Current		V_{SYS} = V_{WP_L} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = V_{WP_L} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
WP_L Falling Edge Time		C_{WP_L} = 25pF, V_{WP_L} = 1.8V ≥ 0		25		ns
WP_L Output Deassert Delay Time	t_{WPDLY}	WP_L_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		0		µs
		WP_L_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		WP_L_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		WP_L_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
WP_L Output Assert Delay Time				0		µs
WP_L Pullup Resistance	$R_{PU\_WP\_L}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
RESET_L OUTPUT (OPEN DRAIN)						
RESET_L Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
RESET_L Open Leakage Current		V_{SYS} = V_{RESET_L} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = V_{RESET_L} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
RESET_L Falling Edge Time		C_{RESET_L} = 25pF, V_{RESET_L} falling from 1.8V ≥ 0		25		ns

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET_L Output Deassert Delay Time	t_{RSTDLY}	RST_L_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		0		µs
		RST_L_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		RST_L_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		RST_L_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
RESET_L Output Assert Delay Time				0		µs
RESET_L Pullup Resistance	$R_{PU\_RESET\_L}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
PGOOD OUTPUT (OPEN DRAIN)						
PGOOD Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
PGOOD Open Leakage Current		V_{SYS} = V_{PGOOD} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = V_{PGOOD} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
PGOOD Falling Edge Time		C_{PGOOD} = 25pF, V_{PGOOD} = 1.8V ≥ 0		25		ns
PGOOD Output Assert Delay Time	$t_{PGOODDLY}$	PG_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		31.5		µs
		PG_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		PG_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		PG_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
PGOOD Output Deassert Delay Time				0		µs
PGOOD Pullup Resistance	R_{PU_PGOOD}	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LP_MODE INPUT						
LP_MODE I/O Pad Operating Voltage	V_{SYS}		2.6		5.5	V
LP_MODE Input-Low Voltage	V_{IL}				0.4	V
LP_MODE Input-High Voltage	V_{IH}		1.4			V
LP_MODE Input Hysteresis	V_{HYS}			50		mV
LP_MODE Input Leakage Current		V_{SYS} = V_{IN_VIO} = 5.5V, V_{LP_MODE} = 0V and 5.5V, T_A = +25°C		0.001	1	µA
		V_{SYS} = V_{IN_VIO} = 5.5V, V_{LP_MODE} = 0V and 5.5V, T_A = +85°C		0.01		
LP_MODE Debounce	t_{LPMD_DBNC}	Debounce applies to rising and falling edge. Does not account for oscillator tolerance (Note 4)		95	127	µs
LP_MODE I/O Pad Undervoltage Lockout	$V_{SYSUVLO}$	V_{SYS} falling		2.1		V
LP_MODE Mask Deassertion Timer	t_{LPMD_MSK}		16	20	25	ms
LP_ACK INPUT						
I/O Pad Operating Voltage	V_{SYS}		2.6		5.5	V
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		1.4			V
Input Hysteresis	V_{HYS}			50		mV
Input Leakage Current		V_{SYS} = 5.5V, V_{LP_ACK} = 0V and 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = 5.5V, V_{LP_ACK} = 0V and 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
LP_ACK Pullup Resistance	$R_{PU\_LP\_ACK}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LP_REQ OUTPUT (OPEN DRAIN)						
LP_REQ Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
LP_REQ Open Leakage Current		V_{SYS} = V_{LP_REQ} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = V_{LP_REQ} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
LP_REQ Falling Edge Time		C_{LP_REQ} = 25pF, V_{LP_REQ} = 1.8V ≥ 0		25		ns
LP_REQ Delay	t_{LPREQ_LOW}	LP_REQ_T_EN = 0, PMIC in master mode (OTP_SLP_MSTRSLV = 0), applies during DevSlp exit sequence		31.75		µs
		LP_REQ_T_EN = 1, PMIC in master mode (OTP_SLP_MSTRSLV = 0), applies during DevSlp exit sequence		20		ms
LP_REQ Pullup Resistance	$R_{PU\_LP\_REQ}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
EREG_ENx OUTPUT (OPEN DRAIN)						
EREG_EN1 Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
EREG_EN2 Output-Voltage Low	V_{OL}	I_{SINK} = 10mA			0.4	V
EREG_ENx Open Leakage Current		V_{SYS} = V_{EREG_ENx} = 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = V_{EREG_ENx} = 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
EREG_ENx Falling Edge Time		C_{EREG_ENx} = 25pF, V_{EREG_ENx} = 1.8V ≥ 0		25		ns
EREG_EN1 Pullup Resistance	$R_{PU\_EREG\_ENx}$	Pulled up to V_{H_INT}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
EREG_EN2 Pullup Resistance	$R_{PU\_EREG\_ENx}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
EREG_POK INPUT						
I/O Pad Operating Voltage	V_{SYS}		2.6		5.5	V
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		1.4			V
Input Hysteresis	V_{HYS}			50		mV

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current		V_{SYS} = 5.5V, V_{EREG_POK} = 0V and 5.5V, T_A = +25°C, OTP_INT_PU[0] = 0b0		0.001	1	µA
		V_{SYS} = 5.5V, V_{EREG_POK} = 0V and 5.5V, T_A = +85°C, OTP_INT_PU[0] = 0b0		0.01		
EREG_POK Pullup Resistance	$R_{PU\_EREG\_POK}$	Pulled up to V_{IN_VIO}, OTP_INT_PU[0] = 0b1	50	100	170	kΩ
THERMAL MONITORS						
Quiescent Supply Current	I_{QTM}			1.5		µA
Shutdown Supply Current				0.1		µA
Thermal Overload	T_{JOVLD}	T_J rising, 15°C hysteresis		165		°C
Response Time		5°C overdrive		10		µs
FLEXIBLE POWER SEQUENCER						
Power-Up Sequence Enable Delay	t_{FPSDON}	Measured from internal FPSxEN = 1 to start of sequence (based on a 31.5kHz clock)		63.492		µs
Power-Down Sequence Enable Delay	$t_{FPSDOFF}$	Measured from internal FPSxEN = 0 to start of sequence (based on a 31.5kHz clock)		95.240		µs
Flexible Power Sequencer Event Period	t_{FPS_PU}, t_{FPS_PD}	MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b000		31		µs
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b001		63		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b010		127		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b011		253		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b100		508		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b101		984		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b110		1936		
		MSTRxUPF[2:0] = MSTRxDNF[2:0] = 0b111		3904		

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.6V, V_{IO} = 1.8V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Down Sequence Delay	t_{PD_DLY}	PD_DLY[1:0] = 0b00		0		ms
		PD_DLY[1:0] = 0b01		1.0		
		PD_DLY[1:0] = 0b10		1.5		
		PD_DLY[1:0] = 0b11		2.0		
BLD_IO						
Maximum Bleed Time	t_{BLEED_MAX}			20	22	ms
Minimum Bleed Time	t_{BLEED_MIN}			31.5		µs
Bleed Threshold		BLD_IO falling		90	100	mV
Bleed Resistance	R_{BLEED}	BLD_IO = 0.3V		20	27	Ω
BLD_IO Input Leakage Current		V_{SYS} = 5.5V, V_{BLD_IO} = 0V and 5.5V, T_A = +85°C		0.01		µA
		V_{SYS} = 5.5V, V_{BLD_IO} = 0V and 5.5V, T_A = +25°C		0.001	1	
ON/OFF CONTROLLER						
Hiccup Counter Limit	HICCUP_CNT_LIM			7		counts
IN_PHUP						
Operating Voltage Range	V_{IN_PHUP}		2.4		5.5	V
IN_PHUP Supply Current	I_{IN_PHUP}	V_{SYS} = V_{IN_PHUP} = 5.5V, T_A = +25°C		5.0		µA

Note 4: The LP_MODE debounce period has a variation due to the variability associated with quantizing an asynchronous input signal. Additionally, while measuring the period from a valid LP_MODE edge to a subsequent event, such as LP_REQ assertion, there is one more clock cycle (CLK32K) of delay observed in a real system.

Electrical Characteristics—Inrush Control

(V_{IN_SNS} = 5.0V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_{IN}		2.1		5.5	V
IN Undervoltage-Lockout Threshold	V_{INUVLO}	V_{IN} rising		2.3	2.55	V
IN Undervoltage-Lockout Hysteresis	V_{INUVLO_HYS}			200		mV
IN Undervoltage-Lockout Response Time	t_{INUVLO}	V_{IN} rising (V_{IN} = V_{INUVLO} + 100mV)		39		µs
IN Overvoltage-Lockout Threshold	V_{INOVLO}	V_{IN} rising	5.70	5.87	6.10	V
IN Overvoltage-Lockout Hysteresis	V_{INOVLO_HYS}			80		mV
IN Overvoltage-Lockout Response Time	t_{INOVLO}	V_{IN} rising (V_{IN} = V_{INOVLO} + 50mV)		8		µs
Leakage	$I_{LKG\_VIN\_DRV}$	V_{IN} = 5.5V, V_{IN_DRV} = 0V and 11V, T_A = +25°C		0.001	1	µA
		V_{IN} = 5.5V, V_{IN_DRV} = 0V and 11V , T_A = +85°C		0.01		
Supply Current (Soft-Start)	$I_{Q\_IN\_SS}$	V_{IN_DRV}-VINR_OUT < V_{IN_SNS} (soft-start state), OTP_GDRV_FREQ = 0b111 (800kHz), V_{IN_SNS} = 3.3V		85		µA
		V_{IN_DRV}-VINR_OUT < V_{IN_SNS} (soft-start state), OTP_GDRV_FREQ = 0b111 (800kHz), V_{IN_SNS} = 5V		138		
Supply Current (Steady-State)	I_{IN}	V_{IN_DRV}-VINR_OUT = V_{IN_SNS} (steady state), t_{SS_DONE} expired, f_{GDRV} = 12.5kHz, V_{IN_SNS} = 3.3V		26		µA
		V_{IN_DRV}-VINR_OUT = V_{IN_SNS} (steady state), t_{SS_DONE} expired, f_{GDRV} = 12.5kHz, V_{IN_SNS} = 5V		37		
NMOS SWITCH DRIVER						
Gate Drive ON Voltage	$V_{IN\_DRV\_ON}$	V_{IN} = 5V; Voltage with respect to ground when external MOSFET is being driven to it's fully ON state	8.5		11	V
Gate Drive Current	I_{GDRV_INRUSH}	V_{IN} = 3.3V, 1X gate drive frequency setting	1.8	3.0	4.2	µA
4x Gate Drive Oscillator Frequency	f_{GDRV_4X}	OTP_INR_FREQ[2:0] = 0b111, V_{IN} = 3.3V, V_{IN} = 5V		720		kHz

Electrical Characteristics—Inrush Control (continued)

(V_{IN_SNS} = 5.0V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2x Gate Drive Oscillator Frequency	f_{GDRV_2X}	OTP_INR_FREQ[2:0] = 0b110, V_{IN} = 3.3V, V_{IN} = 5V		360		kHz
1x Gate Drive Oscillator Frequency	f_{GDRV_1X}	OTP_INR_FREQ[2:0] = 0b101 (nominal gate drive strength), V_{IN} = 3.3V, V_{IN} = 5V	120	180	240	kHz
0.5x Gate Drive Oscillator Frequency	$f_{GDRV\_0.5X}$	OTP_INR_FREQ[2:0] = 0b100, V_{IN} = 3.3V, V_{IN} = 5V		90		kHz
0.25x Gate Drive Oscillator Frequency	$f_{GDRV\_0.25X}$	OTP_INR_FREQ[2:0] = 0b011, V_{IN} = 3.3V, V_{IN} = 5V		45		kHz
0.125x Gate Drive Oscillator Frequency	$f_{GDRV\_0.125X}$	OTP_INR_FREQ[2:0] = 0b010, V_{IN} = 3.3V, V_{IN} = 5V	15	23	32	kHz
0.0625x Gate Drive Oscillator Frequency	$f_{GDRV\_0.0625X}$	OTP_INR_FREQ[2:0] = 0b001, V_{IN} = 3.3V, V_{IN} = 5V		11.25		kHz
0.03125x Gate Drive Oscillator Frequency	$f_{GDRV\_0.03125X}$	OTP_INR_FREQ[2:0] = 0b000, V_{IN} = 3.3V, V_{IN} = 5V		5.625		kHz
Gate Drive Discharge Resistance	R_{GDRV_DIS}	Resistance from INR_DRV to INR_OUT, $V_{INR\_DRV-INR\_OUT}$ = 4V		74		Ω
		Resistance from INR_DRV to INR_OUT, $V_{INR\_DRV-INR\_OUT}$ = 3.3V		100		
TIMING						
Start-Up Delay	t_{EN_INRUSH}	Time from V_{IN} rising above V_{INUVLO} to the internal charge pump being enabled. Duration is based on the gate drive oscillator frequency (f_{GDRV}) selected by OTP_INR_FREQ[2:0]		128		cycles of f_{GDRV}
Soft-Start Done Time	t_{SS_1}	Duration from MOSFET drive circuit being enabled (subsequent to startup delay) to the point when the IN_SS_DONE (internal signal) is asserted allowing a power-up sequence to occur. Based on default gate drive frequency (f_{GDRV}) selected by OTP_INR_FREQ[2:0]		512		cycles of f_{GDRV}
Gate Drive Idle Time	t_{SS_DONE}	Duration from MOSFET drive circuit being enabled (subsequent to the startup delay) to the point when the gate drive oscillator frequency folds back to the 12.5kHz setting (idle gate drive). Based on default gate drive frequency (f_{GDRV}) selected by OTP_INR_FREQ[2:0]		1024		cycles of f_{GDRV}

Electrical Characteristics—Current Sense Amplifier

(V_{SYS} = 3.3V, C_{LOAD} = 10pF, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT OVERCURRENT						
Input Overcurrent Threshold		2.25A setting, V_{SYS} = 3.3V	-6.5		+6.5	%
CSA Debounce Timer		OTP_CSA_DBNC = 0		100		µs
		OTP_CSA_DBNC = 1		50		
Overcurrent-Sense Comparator Threshold 1	V_{OC_THR}	Overcurrent limit, CSTH_OPT[1:0] = 0b00		30		mV
Overcurrent-Sense Comparator Threshold 2	V_{OC_THR}	Overcurrent limit, CSTH_OPT[1:0] = 0b01		35		mV
Overcurrent-Sense Comparator Threshold 3	V_{OC_THR}	Overcurrent-limit, CSTH_OPT[1:0] = 0b10		40		mV
Overcurrent-Sense Comparator Threshold 4	V_{OC_THR}	Overcurrent limit, CSTH_OPT[1:0] = 0b11		45		mV

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Input Voltage Range	V_{INBx}		2.6		5.5	V
Shutdown Supply Current	I_{QSHDN_BUCKx}	(Note 5)		0.1		µA
Supply Quiescent Current	$I_{Q\_SKIP\_NM\_BUCKx}$	No switching, no load, (Note 6), V_{SYS} = 3.3V		19	30	µA
		No switching, no load, (Note 6), V_{SYS} = 5V		19	30	
	$I_{Q\_FPWM\_BUCKx}$	FPWM mode (switching at fixed frequency), no load, V_{SYS} = 3.3V		10		mA
		FPWM mode (switching at fixed frequency), no load, V_{SYS} = 5V		10		
	$I_{Q\_SKIP\_LPM\_BUCKx}$	Low-power mode (no switching), no load, (Note 6), V_{SYS} = 3.3V		5	9	µA
		Low-power mode (no switching), no load, (Note 6), V_{SYS} = 5V		5	9	

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT_BUCKx}	Programmable in 6.25mV steps with BUCK1VOUT[7:0] and BUCK2VOUT[7:0]	0.600		2.194	V
Output Voltage Accuracy	$V_{OUT\_ACC\_NM\_BUCKx}$	FPWM mode, normal mode, no load, V_{OUT_BUCK1} = 1.800V	-2		+2	%
	$V_{OUT\_ACC\_LPM\_BUCKx}$	Low-power mode, no load, V_{OUT_BUCK1} = 1.800V	-4		+4	
	$V_{OUT\_ACC\_NM\_BUCKx}$	FPWM mode, normal mode, no load, V_{OUT_BUCK2} = 1.200V	-2		+2	
	$V_{OUT\_ACC\_LPM\_BUCKx}$	Low-power mode, no load, V_{OUT_BUCK2} = 1.200V	-4		+4	
OUTPUT CURRENT						
Maximum Output Current	$I_{OUT\_MAX\_NM\_BUCKx}$	RMS, normal mode, L = 1µH	2000			mA
	$I_{OUT\_MAX\_LPM\_BUCKx}$	RMS, low-power mode, L = 1µH		10		
PMOS Peak Current Limit	I_{LIMP}	V_{SYS} = 3.6V	2300	2875	4200	mA
		V_{SYS} = 5V	2300	2875	4200	
NMOS Valley Current Limit	I_{LIMV}	V_{SYS} = 3.6V		2125		mA
		V_{SYS} = 5V		2125		
NMOS Negative Current Limit	I_{LIMN}	V_{SYS} = 3.6V		800		mA
		V_{SYS} = 5V		800		
PERFORMANCE PARAMETERS						
Line Regulation		V_{SYS} = V_{INBx} = 2.6V to 5.5V		0.2		%/V
Load Regulation		Load = 0 to 1A, FPWM mode		0.125		%/A
Load Transient Response		FPWM mode, V_{OUT_BUCKx} = default, L = 1µH, C_{OUT} = 12µF effective Δ I_{OUT} = 0.2A–2A, Δt = 3µs		88		mV
		Skip mode, V_{OUT_BUCKx} = default, L = 1µH, C_{OUT} = 12µF effective Δ I_{OUT} = 10mA to 0.7A, Δt = 3µs,		90		
Switching Frequency	f_{SW}	V_{SYS} = 3.3V	1.8	2	2.2	MHz
Dead Time	t_{DEAD}	V_{SYS} = 3.3V		2.0		ns
Switching Frequency	f_{SW}	V_{SYS} = 5V	1.8	2	2.2	MHz

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dead Time	t_{DEAD}	V_{SYS} = 5V		2.0		ns
Soft-Start Slew Rate		Fixed for buck 1		6.5		mV/µs
		Fixed for buck 2		17		
Output Voltage Ramp-Up Slew Rate		Fixed for buckx (Notes 5, 8, 9), C_{OUT} = 22µF		40		mV/µs
Output Voltage Ramp-Down Slew Rate		Fixed for buck 1, 2 (Notes 5, 8), C_{OUT} = 22µF, BUCKxFPWMEN = 1 (x = 1, 2), no load		18		mV/µs
PMOS ON Resistance	R_{ON_PCH}	V_{SYS} = $V_{INBUCKx}$ = 3.6V, I_{OUT} = 150mA		100	150	mΩ
		V_{SYS} = $V_{INBUCKx}$ = 5V, I_{OUT} = 150mA		100	150	
NMOS ON Resistance	R_{ON_NCH}	V_{SYS} = $V_{INBUCKx}$ = 3.6V, I_{OUT} = 150mA		60	100	mΩ
		V_{SYS} = $V_{INBUCKx}$ = 5V, I_{OUT} = 150mA		60	100	
NMOS Zero-Crossing Threshold	I_{ZX}	Threshold to determine transition from PWM to SKIP mode		20		mA
Output Voltage Ripple in Skip Mode		V_{OUT_BUCKx} = 1.0V, L = 1µH, C_{OUT} = 12µF effective, no load (Note 5)		40		mV_{P-P}
Output Voltage Ripple in PWM Mode		V_{OUT_BUCKx} = 1.0V, L = 1µH, C_{OUT} = 12µF effective, I_{LOAD} = 0.5 x $I_{OUT\_MAX\_BUCKx}$ (Note 5)		5		mV_{P-P}
LX Leakage	$I_{L\_LX\_25C}$	V_{LXx} = 5.5V or 0V, T_A = +25°C		0.1	1	µA
	$I_{L\_LX\_85C}$	V_{LXx} = 5.5V or 0V, T_A = +85°C (Note 5)		1		
Output Active Discharge Resistance	R_{DISCHG_BUCKx}	Resistance from FBBx to PGNDx, output disabled, (Note 7)		100		Ω
Nominal Output Inductance	L_{NOM}			1.0		µH
Minimum Effective Output Capacitance	$C_{OUT\_EFF\_MIN}$	0mA < I_{OUT} < 2000mA	18			µF
Light Load Efficiency	Eff_{LIGHT}	Low-power mode, I_{OUT} = 0.5mA, V_{OUT_BUCKx} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 22µF (Note 5)		75		%

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Typical Load Efficiency	Eff_{IOUT_TYP}	I_{OUT} = 0.25 x $I_{OUT\_MAX\_BUCKx}$, V_{OUT_BUCKx} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 22µF (Note 5)		85		%
Maximum Load Efficiency	EFF_{IOUT_MAX}	I_{OUT} = $I_{OUT\_MAX\_BUCKx}$, V_{OUT} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 22µF (Note 5)		70		%
Turn-On Delay Time	$t_{ON\_DLY\_BUCKx}$	EN signal to LX switching with bias ON		30		µs
Maximum Duty Cycle		V_{OUT_BUCKx} / V_{IN_BUCKx} expressed as %		90		%
BROWNOUT COMPARATOR						
Output Brownout Threshold	V_{BO_BUCKx}	Normal-power mode, falling threshold, BUCKx_BO_THR[1:0] = 0b00		75		%
		Normal-power mode, falling threshold, BUCKx_BO_THR[1:0] = 0b01		80		
		Normal-power mode, falling threshold, BUCKx_BO_THR[1:0] = 0b10		85		
		Normal-power mode, falling threshold, BUCKx_BO_THR[1:0] = 0b11		90.7		
Output Brownout Accuracy		Normal-power mode. V_{OUT_BUCKx} = 1.0V (VOUT_BUCKx[7:0] = 0 x 40)	-4.0		+4.0	%
Output Brownout Threshold (Low-Power Mode)	V_{BO_BUCKx}	Falling threshold, low-power mode		86.0		%
Output Brownout Accuracy		Low-power mode. V_{OUT_BUCKx} = 1.0V (VOUT_BUCKx[7:0] = 0 x 40)	-4		+4	%
Output Brownout Hysteresis Range	$V_{BO\_HYS\_BUCKx}$	2-bit control over I^2C. Max rising threshold limited to 96%	5		20	%
Brownout Voltage Hysteresis Programming Step Size		Programmable with BUCKx_BO_HYS[1:0]		5		%
Output Brownout Hysteresis (Low-Power Mode)	$V_{BO\_HYS\_BUCKx\_LPM}$			5		%

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Brownout Response Time	t_{BO_BUCKx}	BUCKx_BO_PR[1:0] = 0b00 (fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.04		µs
		BUCKx_BO_PR[1:0] = 0b01 (med-fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.14		
		BUCKx_BO_PR[1:0] = 0b10 (med-slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.30		
		BUCKx_BO_PR[1:0] = 0b11 (slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.68		
		Buck in low-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		3.18		
Output Brownout Supply Current	$I_{QNM\_BO\_BUCKx}$	Normal-power mode, BUCKx_BO_PR[1:0] = 0b00 (fast)		13.4		µA
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b01 (med-fast)		10.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b10 (med-slow)		7.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b11 (slow)		4.4		
	$I_{QLPM\_BO\_BUCKx}$	Low-power mode		1.3		

Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV COMPARATOR						
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCKx_OV_THR = 1, referenced to output voltage setting		116.6		%
Output OV Hysteresis		BUCKx_OV_THR = 1		9.1		%
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCKx_OV_THR = 0, referenced to output voltage setting		108.3		%
Output OV Hysteresis		BUCKx_OV_THR = 0		2.8		%
Output OV Trip Level (Low-Power Mode)	$V_{OUTBUCKx\_OV}$	Rising edge, low-power mode		108.3		%
Output OV hysteresis (Low-Power Mode)		Low-power mode		2.8		%
Output Over-Voltage Response Time	t_{OV_BUCKx}	Normal-power mode, 100mV over-drive with rising slew rate of 150mV/µs. Time from V_{OUT_BUCKx} rising to PGOOD pin falling (Note 5)		1.68		µs
Output Over-Voltage Supply current	$I_{Q\_OV\_BUCKx}$	Normal-power mode		4.4		µA
Output Over-Voltage Response Time (Low-Power Mode)	t_{OV_BUCKx}	Low-power mode, 100mV over-drive with rising slew rate of 150mV/µs. Time from V_{OUT_BUCKx} rising to PGOOD pin falling (Note 5)		3.18		µs
Output Over-Voltage Supply Current (Low-Power Mode)	$I_{Q\_OV\_BUCKx}$	Low-power mode		1.3		µA

Note 5: Design guidance only and is not production tested.
Note 6: Individual buck Iq is not production tested. It is covered by a combined test by turning on all bucks.
Note 7: There is an n-channel MOSFET in series with the output active-discharge resistance. This NMOS requires V_{SYS} > 1.2V to be enhanced.
Note 8: The ramp down slew rate when the output voltage is decreased through I^2C is a function of the negative current limit and the output capacitance. With no load, forced PWM mode and 22µF output capacitor, the ramp-down slew rate is dv/dt = i / C = 0.4A / 22µF = 18mV/µs.
Note 9: DVS and soft-start ramp rates can be expected to vary by up to 30%.

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Input Voltage Range	$V_{INBUCK3}$		2.6		5.5	V
Shutdown Supply Current	I_{QSHDN_BUCK3}	(Note 10)		0.1		µA
Supply Quiescent Current	$I_{Q\_SKIP\_NM\_BUCK3}$	No switching, no load (Note 10)		26	40	µA
	$I_{Q\_FPWM\_BUCK3}$	FPWM mode, no load (Note 10)		10		mA
	$I_{Q\_SKIP\_LPM\_BUCK3}$	Low-power mode (no switching), no load (Note 10)		10	19	µA
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT_BUCK3}	I²C programmable in 10mV Steps (BUCK3VOUT[6:0] = 0x01 to 0x7F)	0.26		1.52	V
Output Voltage Accuracy	$V_{OUT\_ACC\_NM\_BUCK3}$	FPWM mode, normal mode, no load, T_A = +25°C, V_{OUT_BUCK3} = 1.0V	-2		+2	%
	$V_{OUT\_ACC\_LPM\_BUCK3}$	Low-power mode, no load, T_A = +25°C, V_{OUT_BUCK3} = 1.000V	-4		+4	
PERFORMANCE PARAMETERS						
Switching Frequency	f_{SW}	V_{SYS} = 3.3V	1.8	2	2.2	MHz
		V_{SYS} = 5V	1.8	2	2.2	
Line Regulation		$V_{INBUCK3}$ = 2.6V to 5.5V, V_{OUT_BUCK3} = 1.0V		0.2		%/V
Load Regulation		V_{OUT_BUCK3} = 1.0V, (Note 10), load = 0 to 1A, FPWM mode		0.125		%/A
Load Transient Response (Droop)		Skip mode, V_{OUT} = default, L = 1µH, C_{OUT} = 28µF effective ΔI_{OUT} = 20mA to 500mA, Δt = 0.8µs (Note 10)		45		mV
		Skip mode, V_{OUT} = default, L = 1µH, C_{OUT} = 28µF effective ΔI_{OUT} = 20mA to 3A, Δt = 4.8µs (Note 10)		70		
Soft-Start Slew Rate		BUCK3SSRAMP = 0		2.5		mV/µs
		BUCK3SSRAMP = 1		10		
Output Voltage Ramp-Up/Down Slew Rate (DVS)				10		mV/µs

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMOS ON Resistance	R_{ON_PCH}	V_{SYS} = $V_{INBUCK3}$ = 5V, I_{OUT} = 150mA		60	90	mΩ
		V_{SYS} = $V_{INBUCK3}$ = 3.6V, I_{OUT} = 150mA		60	90	
NMOS ON Resistance	R_{ON_NCH}	V_{SYS} = $V_{INBUCK3}$ = 5V, I_{OUT} = 150mA		35	60	mΩ
		V_{SYS} = $V_{INBUCK3}$ = 3.6V, I_{OUT} = 150mA		35	60	
NMOS Zero-Crossing Threshold	I_{ZX_SKIP}	SKIP mode		20		mA
	I_{ZX_PWM}	PWM mode		20		
Output Voltage Ripple In Skip Mode		V_{OUT_BUCK3} = 1.0V, L = 1µH, C_{OUT} = 28µF effective, no load (Note 10)		15		mV
Output Voltage Ripple In PWM Mode		V_{OUT_BUCK3} = 1.0V, L = 1µH, C_{OUT} = 28µF effective, I_{LOAD} = 0.5 x $I_{OUT\_MAX\_BUCK3}$ (Note 10)		5		mV
LX Leakage	$I_{L\_LX\_25C}$	$V_{LXBUCK1}$ = 5.5V or 0V, T_A = +25°C		0.1	1	µA
	$I_{L\_LX\_85C}$	$V_{LXBUCK1}$ = 5.5V or 0V, T_A = +85°C (Note 10)		1		
Output Active Discharge Resistance	R_{DISCHG_BUCK3}	Resistance from FBB3 to PGND3, output disabled		100		Ω
Nominal Output Inductance	L_{NOM}			1.0		µH
Minimum Effective Output Capacitance	$C_{OUT\_EFF\_MIN}$	0mA < I_{OUT} < 3000mA		28		µF
Turn-On Delay Time	$t_{ON\_DLY\_BUCK1}$	EN signal to LX switching with bias ON		200		µs
Light Load Efficiency	Eff_{LIGHT}	Low-power mode, I_{OUT} = 0.5mA, V_{OUT_BUCKx} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 3 x 22µF (Note 10)		75		%
Typical Load Efficiency	Eff_{IOUT_TYP}	I_{OUT} = 0.25 x $I_{OUT\_MAX\_BUCKx}$, V_{OUT_BUCKx} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 3 x 22µF (Note 10)		88		%
Maximum Load Efficiency	EFF_{IOUT_MAX}	I_{OUT} = $I_{OUT\_MAX\_BUCKx}$, V_{OUT} = 1.0V, L = 1µH, DCR_L = 50mΩ, C_{OUT} = 3 x 22µF (Note 10)		77		%

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CURRENT						
Maximum Output Current	$I_{OUT\_MAX\_NM\_BUCK3}$	RMS, normal mode	3000			mA
	$I_{OUT\_MAX\_LPM\_BUCK3}$	RMS, low-power mode		10		
PMOS Peak Current Limit	I_{LIMP}	T_A = -40°C to +85°C, V_{SYS} = 3.6V	3825	4250	4675	mA
NMOS Valley Current Limit	I_{LIMV}			3750		mA
NMOS (Negative) Current Limit	I_{LIMN}			2000		mA
BROWNOUT COMPARATOR						
Output Brownout Threshold	V_{BO_BUCK3}	Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b00		77		%
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b01		81		
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b10		85.7		
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b11		91		
Output Brownout Accuracy		Normal-power mode. V_{OUT_BUCK3} = 1.0V (VOUT_BUCK3[7:0] = 0x4B)	-4.5		+4.5	%
Output Brownout Threshold (Low-Power Mode)	V_{BO_BUCKx}	Falling threshold, low-power mode		86.0		%
Output Brownout Accuracy		Low-power mode, V_{OUT_BUCK3} = 1.0V (VOUT_BUCK3[7:0] = 0x4B)	-4		+4	%
Output Brownout Hysteresis Range	$V_{BO\_HYS\_BUCKx}$	2-Bit control over I^2C. Max rising threshold limited to 96%	5		20	%
Brownout Voltage Hysteresis Programming Step Size		Programmable with BUCKx_BO_HYS[1:0]		5		%
Output Brownout Hysteresis (Low-Power Mode)	$V_{BO\_HYS\_BUCKx\_LPM}$			5		%

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Brownout Response Time	t_{BO_BUCKx}	BUCKx_BO_PR[1:0] = 0b00 (fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.04		µs
		BUCKx_BO_PR[1:0] = 0b01 (med-fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.14		
		BUCKx_BO_PR[1:0] = 0b10 (med-slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.30		
		BUCKx_BO_PR[1:0] = 0b11 (slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		1.68		
		Buck in Low-power mode, 100mV under-drive with falling slew rate of 150mV/µs. Time from V_{OUT_BUCKx} falling to PGOOD pin falling		3.18		
Output Brownout Supply Current	$I_{QNM\_BO\_BUCKx}$	Normal-power mode, BUCKx_BO_PR[1:0] = 0b00 (fast)		13.4		µA
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b01 (med-fast)		10.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b10 (med-slow)		7.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b11 (slow)		4.4		
	$I_{QLPM\_BO\_BUCKx}$	Low-power mode		1.3		

Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

(V_{SYS} = 5.0V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV COMPARATOR						
Output OV Trip Level	$V_{OUTBUCK3\_OV}$	Rising edge, BUCK3_OV_THR = 1		117.1		%
Output OV hysteresis		BUCK3_OV_THR = 1		8.6		%
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCK3_OV_THR = 0		108.5		%
Output OV Hysteresis		BUCK3_OV_THR = 0		3.9		%
Output OV Trip Level (Low-Power Mode)	$V_{OUTBUCK3\_OV}$	Rising edge, low-power mode		108.3		%
Output OV Hysteresis (Low-Power Mode)		Low-power mode		3.9		%
Output Over-Voltage Response Time	t_{OV_BUCK3}	Buck in normal-power mode, 100mV over-drive with rising slew rate of 150mV/µs. Time from V_{OUT_BUCK3} rising to PGOOD pin falling (Note 10)		1.68		µs
Output Over-Voltage Supply current	$I_{Q\_OV\_BUCKx}$	Buck in normal-power mode		4.4		µA
Output Over-Voltage Response Time (Low-Power Mode)	t_{OV_BUCKx}	Buck in low-power mode, 100mV over-drive with rising slew rate of 150mV/µs. Time from V_{OUT_BUCKx} rising to PGOOD pin falling (Note 10)		3.18		µs
Output Over-Voltage Supply current (Low-Power Mode)	$I_{Q\_OV\_BUCK3}$	Buck in low-power mode		1.3		µA

Note 10: Design guidance only and is not production tested.

Electrical Characteristics—Load Switch Driver (LSW1/2)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. x is used to represent multiple instances of similar resources, for this section x = 1, 2 unless specified for e.g., LSWx represents LSW1, LSW2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current	$I_{SYS\_LSW\_SS}$	V_{INLSWx} = V_{SYS} = 5V, LSWxDRV_FREQ=0b111 (800kHz), $C_{OUTLSWx}$ = 20µF		68		µA
Supply Voltage Range	V_{SYS}		2.6		5.5	V
Supply Current	$I_{SYS\_LSW\_SS}$	V_{INLSWx} = V_{SYS} = 3.3V, LSWxDRV_FREQ = 0b111 (1.6MHz), $C_{OUTLSWx}$ = 20µF		43		µA
		V_{INLSWx} = V_{SYS} = 5V, LSWxDRV_FREQ = 0b101 (400kHz), $C_{OUTLSWx}$ = 20µF		20		
Leakage	$I_{LKG\_LSWx\_DRV}$	VSYS = 5.5V, V_{LSWx_DRV} = 0V and 11V, T_A = +25°C		0.001	1	µA
		V_{SYS} = 5.5V, V_{LSWx_DRV} =0 V and 11V, T_A = +85°C		0.01		
NMOS SWITCH DRIVER						
Gate Drive Voltage	V_{LSWx_DRV}	V_{SYS} = 5V	8.5		11	V
Gate Drive Current	I_{LSWx_DRV}	V_{SYS} = 3.3V, 1X gate drive frequency setting (LSWx_DRV_FREQ[2:0] = 0b101), $C_{OUTLSWx}$ = 20µF	1.85	3.7	5.55	µA
4x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_4X}$	LSWxDRV_FREQ[2:0] = 0b111, V_{SYS} = 3.3V, V_{SYS} = 5V		1600		kHz
2x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_2X}$	LSWx_DRV_FREQ[2:0] = 0b110, V_{SYS} = 3.3V, V_{SYS} = 5V		800		kHz
1x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_1X}$	LSWx_DRV_FREQ[2:0] = 0b101 (nominal gate drive strength), V_{SYS} = 3.3V, V_{SYS} = 5V	200	400	600	kHz
0.5x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.5X}$	LSWx_DRV_FREQ[2:0] = 0b100, V_{SYS} = 3.3V, V_{SYS} = 5V		200		kHz
0.25x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.25X}$	LSWx_DRV_FREQ[2:0] = 0b011, V_{SYS} = 3.3V, V_{SYS} = 5V		100		kHz
0.125x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.125X}$	LSWx_DRV_FREQ[2:0] = 0b010, V_{SYS} = 3.3V, V_{SYS} = 5V	25	50	75	kHz
0.0625x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.0625X}$	LSWx_DRV_FREQ[2:0] = 0b001, V_{SYS} = 3.3V, V_{SYS} = 5V		25		kHz

Electrical Characteristics—Load Switch Driver (LSW1/2) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. x is used to represent multiple instances of similar resources, for this section x = 1, 2 unless specified for e.g., LSWx represents LSW1, LSW2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
0.03125x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.03125X}$	LSWx_DRV_FREQ[2:0] = 0b000, VSYS = 3.3V, V_{SYS} = 5V		12.50		kHz
Output Active Discharge Resistance	R_{DISCHG_LSW}		50	100	150	Ω
Gate Drive Discharge Resistance	$R_{LSW\_GDRV\_DIS}$	Resistance from LSWx_DRV to FBLSWx, $V_{LSWx\_DRV-FBLSWx}$ = 4V		74		Ω
		Resistance from LSWx_DRV to FBLSWx, $V_{LSWx\_DRV-FBLSWx}$ = 3.3V		100		
TIMING						
Soft-Start Done Time	$t_{SS\_DONE\_LSW}$	Duration from MOSFET drive circuit being enabled to the internal soft-start done signal being asserted. Based on default gate drive frequency ($f_{LSWx\_DRV\_FREQ}$) selected by LSWx_DRV_FREQ[2:0] to program the default gate drive frequency		256		cycles of $f_{LSWx\_DRV\_FREQ}$
POWER-OK COMPARATOR						
Output Power-OK Threshold	$V_{LSWx\_OUT\_POK\_INT}$	Rising edge, input to the load switch is either one of the three internal buck regulator outputs or V_{SYS} as selected by LSWx_INP_EXT	0.85 x V_{IN_LSWx}	0.90 x V_{IN_LSWx}	0.95 x V_{IN_LSWx}	V
Output Power-OK Hysteresis				3		%
Power-OK Response Time		V_{SYS} = 3.3V, V_{INLSWx} = 1.8V, LSWx is enabled, 100mV under-drive with falling slew rate of 150mV/µs		1.20		µs
Power-OK Comparator Active Current	$I_{Q\_POK\_LSWx}$	V_{SYS} = 3.3V, V_{INLSWx} = 1.8V, LSWx is enabled		1.1		µA

Electrical Characteristics—Load Switch Driver (LSW3)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. This section is applicable when OTP_INRUSH_DISABLE = 1 and LSW_OTP_SEL = 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_{SYS}		2.6		5.5	V
Supply Current	$I_{SYS\_LSW\_SS}$	V_{INLSW3} = V_{SYS} = 3.3V, OTP_INR_FREQ[2:0] = 0b111 (720kHz), $C_{OUTLSW3}$ = 20µF		40		µA
		V_{INLSW3} = V_{SYS} = 5V, OTP_INR_FREQ[2:0] = 0b111 (720kHz), $C_{OUTLSW3}$ = 20µF		67		
Leakage	$I_{LKG\_LSW3\_DRV}$	V_{SYS} = 5.5V, V_{INR_DRV} = 0V and 11V, T_A = +25°C		0.001	1	µA
		V_{SYS} = 5.5V, V_{INR_DRV} = 0V and 11V, T_A = +85°C		0.01		
NMOS SWITCH DRIVER						
Gate Drive Voltage	V_{LSW3_DRV}	V_{SYS} = 5V	8.5		11	V
Gate Drive Current	I_{LSW3_DRV}	V_{SYS} = 3.3V, 1X gate drive frequency setting (OTP_INR_FREQ[2:0] = 0b101), $C_{OUTLSW3}$ = 20µF	1.8	3	4.2	µA
4x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_4X}$	OTP_INR_FREQ[2:0] = 0b111, V_{SYS} = 3.3V, V_{SYS} = 5V		720		kHz
2x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_2X}$	OTP_INR_FREQ[2:0] = 0b110, V_{SYS} = 3.3V, V_{SYS} = 5V		360		kHz
1x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_1X}$	OTP_INR_FREQ[2:0] = 0b101 (nominal gate drive strength), V_{SYS} = 3.3V, V_{SYS} = 5V	120	180	240	kHz
0.5x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.5X}$	OTP_INR_FREQ[2:0] = 0b100, V_{SYS} = 3.3V, V_{SYS} = 5V		90		kHz
0.25x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.25X}$	OTP_INR_FREQ[2:0] = 0b011, V_{SYS} = 3.3V, V_{SYS} = 5V		45		kHz
0.125x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.125X}$	OTP_INR_FREQ[2:0] = 0b010, V_{SYS} = 3.3V, V_{SYS} = 5V	15	23	32	kHz
0.0625x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.0625X}$	OTP_INR_FREQ[2:0] = 0b001, V_{SYS} = 3.3V, V_{SYS} = 5V		11.25		kHz

Electrical Characteristics—Load Switch Driver (LSW3) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. This section is applicable when OTP_INRUSH_DISABLE = 1 and LSW_OTP_SEL = 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
0.03125x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.03125X}$	OTP_INR_FREQ[2:0] = 0b000, V_{SYS} = 3.3V, V_{SYS} = 5V		5.625		kHz
Gate Drive Discharge Resistance	$R_{LSW\_GDRV\_DIS}$	Resistance from LSW3_DRV to FBLSW3, $V_{LSW3\_DRV-FBLSW3}$ = 4V		74		Ω
		Resistance from LSWx_DRV to FBLSWx, $V_{LSWx\_DRV-FBLSWx}$ = 3.3V		100		
TIMING						
Soft-Start Done Time	$t_{SS\_DONE\_LSW}$	Duration from MOSFET drive circuit being enabled to the internal soft-start done signal being asserted. Based on default gate drive frequency ($f_{LSW3\_DRV\_FREQ}$) selected by (OTP_INR_FREQ[2:0], to program the default gate drive frequency		512		cycles of $f_{LSW3\_DRV\_FREQ}$
POWER-OK COMPARATOR						
Output Power-OK Threshold	$V_{LSW3\_OUT\_POK\_INT}$	Rising edge, input to the load switch is either one of the four internal buck regulator outputs or V_{SYS} as selected by LSW3_INP_EXT	0.85 x V_{IN_LSW3}	0.90 x V_{IN_LSW3}	0.95 x V_{IN_LSW3}	V
Output Power-OK Hysteresis				3		%
Power-OK Response Time		V_{SYS} = 3.3V, V_{INLSWx} = 1.8V, LSWx is enabled, 100mV under-drive with falling slew rate of 150mV/µs		1.20		µs
Power-OK Comparator Active Current	$I_{Q\_POK\_LSWx}$	V_{SYS} = 3.3V, V_{INLSWx} = 1.8V, LSWx is enabled		1.1		µA

Electrical Characteristics—Linear Regulator

(V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 1.8V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Input Voltage Range	V_{IN_LDO}	Guaranteed by Output Voltage Accuracy tests (Notes 11, 12)	1.7		V_{SYS}	V
LDO Shutdown IN_LDO Current	I_{IN_LDO}	Current measured into IN_LDO, LDO output disabled, V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V. Production tested in combination with other blocks as shown in the *OFF State Quiescent Current* parameter of the *Electrical Characteristics—Linear Regulator* table		<0.1	1	µA
LDO Shutdown SYS Current	I_{SYS}	Current measured into IN_LDO, LDO output disabled, V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V. Production tested in combination with other blocks as shown in the global resources "*OFF State Quiescent Current*" parameter		<0.1		µA
LDO Normal Mode Quiescent Supply IN_LDO Current (Not in Dropout)	I_{IN_LDO}	Normal mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 2.5V, I_{OUT_LDO} = 0mA. Production tested in a combination with all other blocks as shown in the global resources "*ON State Quiescent Current*" parameter		16	20	µA
LDO Normal Mode Quiescent Supply SYS Current (Not in Dropout)	I_{SYS}	Normal mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 2.5V, I_{OUT_LDO} = 0mA. Production tested in combination with other blocks as shown in the global resources "*ON State Quiescent Current*" parameter		5	7	µA
LDO Normal Mode Quiescent Supply IN_LDO Current (In Dropout)	I_{IN_LDO}	Normal mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, V_{SYS} = 3.6V, V_{IN_LDO} = 2.0V, $V_{OUT\_LDO\_TARGET}$ = 2.5V, I_{OUT_LDO} = 0mA (Note 13)		20		µA
LDO Normal Mode Quiescent Supply SYS Current (In Dropout)	I_{SYS}	Normal mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, V_{SYS} = 3.6V, V_{IN_LDO} = 2.0V, $V_{OUT\_LDO\_TARGET}$ = 2.5V, I_{OUT_LDO} = 0mA (Note 13)		5		µA

Electrical Characteristics—Linear Regulator (continued)

(V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 1.8V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO Low-Power Mode Quiescent Supply IN_LDO Current (Not in Dropout)	I_{IN_LDO}	Low-power mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 2.5V, I_{OUT_LDO} = 0mA. Production tested in combination with other blocks as shown in the global resources "*DEVSLP State Quiescent Current*" parameter		2	3	µA
LDO Low-Power Mode Quiescent Supply SYS Current (Not in Dropout)	I_{SYS}	Low-power mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 2.5V, I_{OUT_LDO} = 0mA.		2	3	µA
LDO Low-Power Mode Quiescent Supply IN_LDO Current (In Dropout)	I_{IN_LDO}	Low-power mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, V_{SYS} = 3.6V, V_{IN_LDO} = 2.0V, $V_{OUT\_LDO\_TARGET}$ = 2.5V, I_{OUT_LDO} = 0mA (Note 13)		1.5		µA
LDO Low-Power Mode Quiescent Supply SYS Current (In Dropout)	I_{SYS}	Low-power mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, V_{SYS} = 3.6V, V_{IN_LDO} = 2.0V, $V_{OUT\_LDO\_TARGET}$ = 2.5V, I_{OUT_LDO} = 0mA (Note 13)		2.5		µA
Maximum Output Current	I_{OUT_LDO}	Normal-power mode (Note 14)	150			mA
		Low-power mode (Note 14)	5			
Output Current Limit		Normal-power mode, V_{OUT_LDO} set for 3.2V and loaded down to 90% of set output voltage (Note 15)	165	300		mA
		Low-power mode, V_{OUT_LDO} set for 3.2V and loaded down to 90% of set output voltage		40		
Output Capacitance for Stability	C_{LDO_OUT}	ESR must be less than 200mΩ, ESL is less than 20nH	1.1	2.2	20	µF
OUTPUT VOLTAGE RANGE						
Minimum Programmable Output Voltage		TV_LDO[6:0] = 0b0000000		0.8		V
Maximum Programmable Output Voltage		TV_LDO[6:0] = 0b1111111		3.975		V
Output DAC Bits				7		Bits
Output DAC LSB Size				25		mV

Electrical Characteristics—Linear Regulator (continued)

(V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 1.8V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC CHARACTERISTICS						
Output Voltage Accuracy		V_{SYS} = 5.5V, V_{IN_LDO} = 1.7V, V_{OUT_LDO} = 0.8V, I_{OUT_LDO} = 150mA, normal-power mode	-2		+2	%
		V_{SYS} = 5.5V, V_{IN_LDO} = 1.7V, V_{OUT_LDO} = 0.8V, I_{OUT_LDO} = 5mA, low-power mode	-6.5		+6.5	
		V_{SYS} = 2.8V, V_{IN_LDO} = 2.8V, V_{OUT_LDO} = 2.5V, I_{OUT_LDO} = 150mA, normal-power mode	-2		+2	
		V_{SYS} = 2.8V, V_{IN_LDO} = 2.8V, V_{OUT_LDO} = 2.5V, I_{OUT_LDO} = 5mA, low-power mode	-6.5		+6.5	
		V_{SYS} = 5.5V, V_{IN_LDO} = 5.5V, V_{OUT_LDO} = 3.975V, I_{OUT_LDO} = 0.1mA, normal-power mode	-2		+2	
		V_{SYS} = 5.5V, V_{IN_LDO} = 5.5V, V_{OUT_LDO} = 3.975V, I_{OUT_LDO} = 0.1mA, low-power mode	-6.5		+6.5	
Line Regulation		V_{SYS} = 5.5V, V_{IN_LDO} = 1.7V to 5.5V, V_{OUT_LDO} = 0.8V, I_{OUT_LDO} = 0.1mA, normal-power mode		0.05		%/V
		V_{SYS} = 5.5V, V_{IN_LDO} = 1.7V to 5.5V, V_{OUT_LDO} = 0.8V, I_{OUT_LDO} = 0.1mA, low-power mode		0.05		
		V_{SYS} = 5.5V, V_{IN_LDO} = 4.4V to 5.5V, V_{OUT_LDO} = 3.975V, I_{OUT_LDO} = 0.1mA, normal-power mode		0.05		
		V_{SYS} = 5.5V, V_{IN_LDO} = 4.4V to 5.5V, V_{OUT_LDO} = 3.975V, I_{OUT_LDO} = 0.1mA, low-power mode		0.05		
Load Regulation		V_{SYS} = 5.5V, V_{IN_LDO} = 1.7V, V_{OUT_LDO} = 0.8V, I_{OUT_LDO} = 0.1mA to 150mA, normal-power mode		0.5		%
		V_{SYS} = 5.5V, V_{IN_LDO} = 1.7V, V_{OUT_LDO} = 0.8V, I_{OUT_LDO} = 0.1mA to 5mA, low-power mode		0.5		
		V_{SYS} = 5.5V, V_{IN_LDO} = 3.975V, V_{OUT_LDO} = 0.8V, I_{OUT_LDO} = 0.1mA to 150mA, normal-power mode		0.5		
		V_{SYS} = 5.5V, V_{IN_LDO} = 3.975V, V_{OUT_LDO} = 0.8V, I_{OUT_LDO} = 0.1mA to 5mA, low-power mode		0.5		

Electrical Characteristics—Linear Regulator (continued)

(V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 1.8V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Noise		Normal-power mode, f = 10Hz to 100kHz, I_{LDO_OUT} = 15mA, V_{SYS} = 2.7V, V_{IN_LDO} = 1.7V, V_{LDO} = 0.8V		100		μV_{RMS}
		Normal-power mode, f = 10Hz to 100kHz, I_{LDO_OUT} = 15mA, V_{SYS} = 2.7V, V_{IN_LDO} = 1.7V, V_{LDO} = 1.0V		150		
		Normal-power mode, f = 10Hz to 100kHz, I_{LDO_OUT} = 15mA, V_{SYS} = 2.7V, V_{IN_LDO} = 2.7V, V_{LDO} = 2.0V		200		
		Normal-power mode, f = 10Hz to 100kHz, I_{LDO_OUT} = 15mA, V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{LDO} = 3.0V		300		
		Normal-power mode, f = 10Hz to 100kHz, I_{LDO_OUT} = 15mA, V_{SYS} = 5.5V, V_{IN_LDO} = 5.5V, V_{LDO} = 3.975V		400		
DYNAMIC CHARACTERISTICS						
Power-Supply Rejection Ratio	PSRR	Normal-power mode, V_{SYS} = 3.6V, V_{IN_LDO} = 2.8V+20mVpp, f = 10Hz to 10kHz, V_{OUT_LDO} = 1.8V, I_{OUT_LDO} = 15mA		60		dB
Line Transient		Normal-power mode, V_{OUT_LDO} = 1.2V, I_{OUT_LDO} = 1mA, V_{SYS} = V_{IN_LDO} = 3.6V to 3.2V to 3.6V with 5µs transition times		5		mV
		Normal-power mode, V_{OUT_LDO} = 1.2V, I_{OUT_LDO} = 1mA, V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V to 3.2V to 3.6V with 5µs transition times		5		
Load Transient		Normal-power mode, V_{OUT_LDO} = 2.5V, I_{OUT_LDO} = 1mA to 75mA to 1mA with 1µs transition times, C_{OUT_LDO} = 2.2µF		±5		%
		Normal-power mode, V_{OUT_LDO} = 2.5V, I_{OUT_LDO} = 1mA to 75mA to 1mA with 1µs transition times, C_{OUT_LDO} = 10µF		±3		
Output Over-Shoot During Startup				50		mV
TIMING CHARACTERISTICS						
Maximum Turn-On Delay		From the LDO receiving an enable signal to when the output voltage starts to rise		20		µs
Maximum Soft-Start Time		V_{OUT_LDO} from 10% to 90% of 2.5V final value		40		µs

Electrical Characteristics—Linear Regulator (continued)

(V_{SYS} = 3.6V, V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 1.8V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER STAGE CHARACTERISTCIS						
Dropout Voltage	V_{LDO_DO}	Normal-power mode, V_{SYS} = 3.6V, 3.3V programmed output voltage, V_{IN_LDO} = 3.1V, I_{OUT_LDO} = 150mA (Note 13)		100	200	mV
		Normal-power mode, V_{SYS} = 3.6V, 1.8V programmed output voltage, V_{IN_LDO} = 1.7V, I_{OUT_LDO} = 150mA (Note 13)		100		
Disabled Output Impedance	R_{AD_LDO}	Regulator disabled, active-discharge enabled (ADE_LDO = 1) (Note 16)	50	100	150	Ω
Disabled Output Leakage Current		Regulator disabled, active-discharge disabled (ADE_LDO = 0), V_{SYS} = V_{IN_LDO} = 5.5V, V_{OUT_LDO} = 5.5V and 0V, T_A = +25°C (Note 17)	-1.0	±0.1	+1.0	µA
POWER-OK COMPARATOR						
Output Power-OK Trim Level		Rising edge, V_{OUT_LDO} = 2.0V	82.5	87.5	92.5	%
Output Power-OK Hysteresis		V_{OUT_LDO} = 2.0V		3		%

Note 11: When the input voltage is within the specified range, the LDO tries to regulate the output voltage. However, the regulator may be in dropout. For example, if the output voltage is fixed at 1.85V and a 1.7V input is provided, the output is 1.7V minus the dropout voltage (V_{LDO} = V_{IN_LDO}-V_{LDO_DO}). To achieve the specified output voltage, the input voltage must be the output voltage plus the dropout voltage (V_{IN_LDO} ≥ V_{LDO} + $V_{LDO\_DO\_MAX}$).

Note 12: V_{IN_LDO} must be lower than or equal to V_{SYS}. The V_{SYS} maximum operating voltage range is 5.5V. For example, if V_{SYS} is 4.2V, then the maximum voltage for V_{IN_LDO} is 4.2V. Similarly, if V_{SYS} is 5.5V, then the maximum voltage for V_{IN_LDO} is 5.5V.

Note 13: The dropout voltage is the difference between the input voltage and the output voltage, when the input voltage is inside the specified "input voltage" range but below the "output voltage" set point. For example, if the output voltage set point is 1.85V, the input voltage is 1.7V, and the actual output voltage is 1.65V, then the dropout voltage is 50mV (V_{LDO_DO} = V_{IN_LDO}-V_{OUT_LDO}).

Note 14: The "Maximum Output Current" is guaranteed by the "Output Voltage Accuracy" tests.

Note 15: Current limit is provided for thermal concerns as a system fail safe feature, minor (50mA) oscillations of current when the LDO is at current limit are normal. Over process corner current limit is not expected to exceed 560mA.

Note 16: There is an n-channel MOSFET in series with the output active discharge resistance. This NMOS requires V_{SYS} > 1.2V to be enhanced.

Note 17: Guaranteed by design and characterization but not directly production tested. The ability to disconnect the active discharge resistance is functionally checked in a production test.

Electrical Characteristics—I²C Interface

(T_A = -40°C to +85°C (unless otherwise specified), V_{IO} = 1.8V, V = 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
VIO Voltage Range	$V_{IN\_VIO\_I2C}$		1.7		3.6	V
SDA AND SCL I/O STAGE						
SCL, SDA Input HIGH Voltage	V_{IH}	$V_{IN\_VIO\_I2C}$ = 1.7V to 3.6V	0.7 x $V_{IN\_VIO\_I2C}$			V
SCL, SDA Input LOW Voltage	V_{IL}	$V_{IN\_VIO\_I2C}$ = 1.7V to 3.6V			0.3 x $V_{IN\_VIO\_I2C}$	
SCL, SDA Input Hysteresis	V_{HYS}			0.1 x $V_{IN\_VIO\_I2C}$		V
SCL, SDA Input Leakage Current	I_I	$V_{IN\_VIO\_I2C}$ = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output LOW Voltage	V_{OL}	IOL = 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL}	t_{OF}	(Note 18)			120	ns
Internal Pullup	R_{PU_SDA}, R_{PU_SCL}	OTP_INT_PU[0] = 0b0		Open		kΩ
		Pulled up to $V_{IN\_VIO\_I2C}$, OTP_INT_PU[0] = 0b1	2.5	5.0	7.5	
WATCHDOG TIMER						
Watchdog Timer Period	t_{WD}			35		ms
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST-MODE PLUS) (Note 18)						
Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
SCL LOW Period	t_{LOW}		0.5			µs
SCL HIGH Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs

Electrical Characteristics—I²C Interface (continued)

(T_A = -40°C to +85°C (unless otherwise specified), V_{IO} = 1.8V, V = 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DATA Hold Time	t_{HD_DAT}	Receive mode	0			µs
DATA Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Data Valid Time	t_{VD_DAT}	Transmit mode			0.45	µs
Data Valid Acknowledge Time	t_{VD_ACK}				0.45	µs
Bus Capacitance	C_B				550	pF
Pulse Width of Suppressed Spikes	t_{SP}			50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 100pF) (Note 18)						
Clock Frequency	f_{SCL}				3.4	MHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
SCL LOW Period	t_{LOW}		160			ns
SCL HIGH Period	t_{HIGH}		60			ns
DATA Hold Time	t_{HD_DAT}		0			ns
DATA Setup Time	t_{SU_DAT}		10			ns
SCL Rise Time	t_{rCL}	T_A = +25°C (Note 18)	10		40	ns
Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit	t_{rCL1}	T_A = +25°C (Note 18)	10		80	ns
SCL Fall Time	t_{fCL}	T_A = +25°C (Note 18)	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C (Note 18)	10		80	ns
SDA Fall Time	t_{fDA}	T_A = +25°C (Note 18)			80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}			10		ns

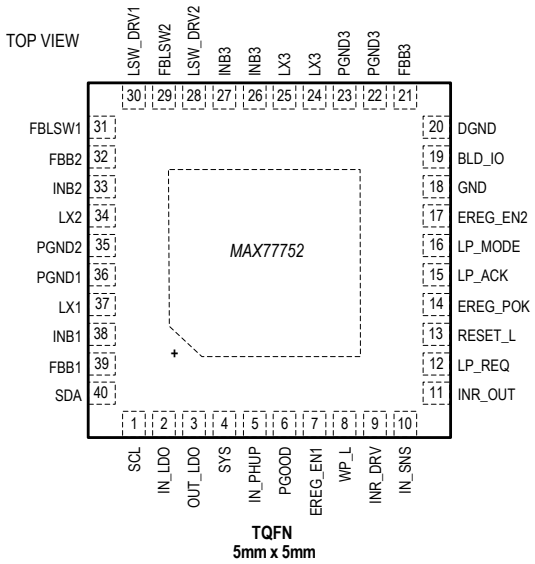
Electrical Characteristics—I²C Interface (continued)

(T_A = -40°C to +85°C (unless otherwise specified), V_{IO} = 1.8V, V = 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 400pF) (Note 18)						
Clock Frequency	f_{SCL}				1.7	MHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
SCL LOW Period	t_{LOW}		320			ns
SCL HIGH Period	t_{HIGH}		120			ns
DATA Hold Time	t_{HD_DAT}		0			ns
DATA Setup Time	t_{SU_DAT}		10			ns
SCL Rise Time	t_{rCL}	T_A = +25°C (Note 18)	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge bit	t_{rCL1}	T_A = +25°C (Note 18)	20		160	ns
SCL Fall Time	t_{fCL}	T_A = +25°C (Note 18)	20		80	ns
SDA Rise Time	t_{rDA}	T_A = +25°C (Note 18)	20		160	ns
SDA Fall Time	t_{fDA}	T_A = +25°C (Note 18)			160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}			10		ns

Note 18: Minimum typical and maximum values are guaranteed by design. Not production tested.

Pin Configuration



Pin Description

PIN	NAME	FUNCTION	TYPE
TOP			
9	INR_DRV	External Inrush FET Gate Drive. Inrush MOSFET Gate Driver. When using the inrush control feature, connect INR_DRV to the gate of an external NMOS. If the inrush feature is not required, this pin can also be configured as LSW3_DRV using LSW_OTP_SEL = 1. If either use cases do not apply, leave INR_DRV unconnected or connect to ground ONLY after ensuring that the inrush controller is disabled by the appropriate OTP option.	Analog Output
10	IN_SNS	Input Voltage Sense (Preswitch). Input Voltage Sense. When using the inrush control feature, connect IN_SNS to the drain of an external n-channel MOSFET. When the inrush control feature is not needed, connect IN_SNS to V_{SYS}.	Power Input
11	INR_OUT	Inrush Control Output Sense. This pin must be connected to the source of the inrush control MOSFET. If the inrush controller is not required, this pin can also be configured as FBLSW3 by setting LSW_OTP_SEL = 1. If either use cases do not apply, then this pin must be connected to the SYS node.	Power Input
4	SYS	System Power Input. SYS is the voltage sense input for the inrush controller, system voltage monitors, and other analog circuits. Connect SYS to the same power source as that meant for the voltage regulators in the PMIC. When using the inrush control feature, connect SYS to the source of an external n-channel MOSFET whose drain is connected to the main power input. When the inrush control feature is not needed, connect SYS to IN_SNS. Regardless of the inrush controller configuration, SYS must connect to the buck regulator power inputs (INB1, INB2, INB3).	Power Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
18	GND	Ground. GND carries ground current for "quiet" control circuits. GND also carries the current for the OTP programming circuit when the programming sequence is executed.	Ground
8	WP_L	Write Protect (Open Drain, Active Low) to memory. Connect this pin to the appropriate pin on the memory. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal V_{IN_VIO} node.	Digital Output
15	LP_ACK	Low-Power Mode Acknowledge from controller. Connect LP_ACK to the appropriate pin on the controller. LP_ACK acknowledges the LP_REQ output signal in master mode (OTP_SLP_MSTRSLV = 0) by asserting high, which initiates the transition to DevSlp state. LP_ACK initiates the transition to DevSlp state independently in slave mode (OTP_SLP_MSTRSLV = 1) by asserting high. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal V_{IN_VIO} node.	Digital Input
13	RESET_L	Reset Output (Open Drain, Active Low) to controller. Connect to the reset input of the controller. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal node.	Digital Output
6	PGOOD	Power Good Output (Open Drain, Active High). PGOOD indicates the status of all regulators controlled by the PMIC (internal and external) and asserts LOW if any regulator's individual Power-OK (POK) signal is deasserted. Additionally, it also asserts low if the system voltage (V_{SYS}) falls below the brownout threshold. Connect PGOOD to the appropriate pin on the controller. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal node.	Digital Output
7	EREG_EN1	External Regulator #1 Enable Output. EREG_EN1 is an open-drain output with optional internal pullup resistor. EREG_EN1 is typically used to drive the enable pin of an external regulator.	Digital Output
17	EREG_EN2	External Regulator #2 Enable Output. EREG_EN2 is an open-drain output with optional internal pullup resistor. EREG_EN2 is typically used to drive the enable pin of an external regulator.	Digital Output
14	EREG_POK	External Regulator Power-OK Input. EREG_POK is a digital input. In the typical application, EREG_POK is derived from the POK outputs of the external regulators that are enabled/disabled by EREG_EN1 and EREG_EN2.	Digital Input
16	LP_MODE	Low-Power Mode Input to PMIC from Connector in Master Mode (OTP_SLP_MSTRSLV = 0). When in slave mode (OTP_SLP_MSTRSLV = 1), it is recommended to connect LP_MODE to ground or to a power supply such that it is logic high. Open-Drain Output. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal node.	Digital Input
12	LP_REQ	Open-Drain (Active High) Output. Low-power mode request to controller in master mode in alternate mode (OTP_SLP_MSTRSLV = 0). Open-Drain Output. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal node.	Digital Output

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
20	DGND	Digital Ground. DGND carries ground current for digital circuits such as the I²C.	Ground
19	BLD_IO	BLD_IO Pin is a Dedicated Open-Drain Input/Output Pin. In an application, this active-low input discharges the supply rail during a powerup cycle. This pin also senses the voltage on the pin it is connected to, and the function is to discharge a rail lower than 100mV. Connect this pin to GND when this feature is not required in the system.	Analog I/O
5	IN_PHUP	IN_PHUP is a Dedicated Analog Input Pin. This pin is connected to the output of the power holdup IC. In case of a power-fail event, the voltage on this pin drives the internal logic block to sustain the holdup function by maintaining the logic levels of the appropriate pins.	Power Input
LDO			
2	IN_LDO	Input Power for LDO (150mA). Bypass with a 2.2µF ceramic capacitor to GND with the following parasitic constraints (including capacitor and PCB parasitics) of ESR<100mΩ and ESL<30nH. If the LDO is not used, it is recommended to connect IN_LDO to OUT_LDO and connect them to ground.	Power Input
3	OUT_LDO	150mA PMOS LDO Output. Bypass with a 2.2µF capacitor to GND. If the LDO is not used, it is recommended to either ground OUT_LDO or leave it unconnected.	Power output
BUCK			
38	INB1	BUCK1 Power Input. INB1 is the shared drain connection of BUCK1's main power FET. Connect both INB1 pins together and to the power input to the system. INB1 is a critical discontinuous current node that requires careful PCB layout.	Power Input
37	LX1	BUCK1 Switching Node. Connect the required inductor between LX and the output capacitor. Both LX1 pins must be connected together. LX1 is a critical node that requires careful PCB layout.	Power I/O
36	PGND1	BUCK1 Power Ground are Internally Combined. PGND1 is the source connection of BUCK1's synchronous rectifier. PGND1 is a critical discontinuous current node that requires careful PCB layout.	Ground
39	FBB1	BUCK1 Output Voltage Feedback Node. Connect FBB1 to the local output capacitor at the buck output. In addition to setting the output-voltage regulation threshold, FBB1 can also be programmed to discharge the output capacitor when the converter is shutdown. FBB1 is a critical analog input that requires careful PCB layout.	Analog Input
33	INB2	BUCK2 Power Input. INB2 is the shared drain connection of BUCK2's main power FET. Connect both INB2 pins together and to the power input to the system. INB2 is a critical discontinuous current node that requires careful PCB layout.	Power Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
34	LX2	BUCK2 Switching Node. Connect the required inductor between LX and the output capacitor. LX2 is a critical node that requires careful PCB layout.	Power I/O
35	PGND2	BUCK2 Power Ground are Internally Combined. PGND2 is the source connection of BUCK2's synchronous rectifier. PGND2 is a critical discontinuous current node that requires careful PCB layout.	Ground
32	FBB2	BUCK2 Output Voltage Feedback Node. Connect FBB2 to the local output capacitor at the buck output. In addition to setting the output-voltage regulation threshold, FBB2 can also be programmed to discharge the output capacitor when the converter is shutdown. FBB2 is a critical analog input that requires careful PCB layout.	Analog Input
26,27	INB3	BUCK3 Power Input. INB3 is the drain connection of BUCK3's main power FET. Connect to the power input to the system. INB3 is a critical discontinuous current node that requires careful PCB layout.	Power Input
24,25	LX3	BUCK3 Switching Node. Connect the required inductor between LX and the output capacitor. LX3 is a critical node that requires careful PCB layout.	Power I/O
21	FBB3	BUCK3 Output Voltage Feedback Node. Connect FBB3 to the local output capacitor at the Buck output. In addition to setting the output voltage regulation threshold, FBB3 may also be programmed to discharges the output capacitor when the converter is shutdown. FBB3 is a critical analog input that requires careful PCB layout.	Analog Input
22, 23	PGND3	BUCK3 Power Ground. PGND2 is the shared source connection of BUCK3's synchronous rectifier. Connect both PGND3 pins together. PGND3 is a critical discontinuous current node that requires careful PCB layout.	Ground
I²C			
40	SDA	Serial Interface Data Bidirectional Open Drain. An optional 5kΩ internal pullup resistor is available which is pulled up to an internal $V_{IN\_VIO\_I2C}$ node. If the part is in Off state due to HICCUP_CNT_EXPIRE = 1, the I²C power switches from V_{FBB1} to V_{IN_PHUP}. Otherwise, the pin is in Hi-Z state during Off condition.	Digital I/O
1	SCL	Serial Interface Port 0 Clock Input. Open-Drain Output. An optional 5kΩ internal pullup resistor is available which is pulled up to an internal $V_{IN\_VIO\_I2C}$ node. If the part is in Off state due to HICCUP_CNT_EXPIRE = 1, the I²C power switchs from V_{FBB1} to V_{IN_PHUP}. Otherwise, the pin is in Hi-Z state during Off condition.	Digital Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
LOAD SWITCH			
30	LSW_DRV1	Gate Drive for Load Switch 1. Connect to the gate of an external n-channel MOSFET used as the load switch. If the load switch is not used, LSW_DRV1 must be left unconnected.	Analog Output
28	LSW_DRV2	Gate Drive for LSW2. Connect to the gate of an external n-channel MOSFET used as the load switch. If the load switch is not used, LSW_DRV2 must be left unconnected.	Analog Output
31	FBLSW1	Feedback Input for Load-Switch Controller 1. FBLSW1 is an analog input to the load-switch controller which is used to control soft-start of the load switch and is the input to the output voltage monitor. Connect FBLSW1 to the output (source-side of n-channel MOSFET) of the load switch. If the load switch is not used, FBLSW1 can be left unconnected or tied to ground.	Analog Input
29	FBLSW2	Feedback Input for Load-Switch Controller 2. FBLSW2 is an analog input to the load-switch controller which is used to control soft-start of the load switch and is the input to the output voltage monitor. Connect FBLSW2 to the output (source-side of n-channel MOSFET) of the load switch. If the load switch is not used, FBLSW2 can be left unconnected or tied to ground.	Analog Input

Detailed Description—Software Recommendations

Advice for optimizing software is provided throughout this data sheet within the context of the hardware descriptions. This section is dedicated to software recommendations and provides system level software guidance in order to optimally utilize the features of this device.

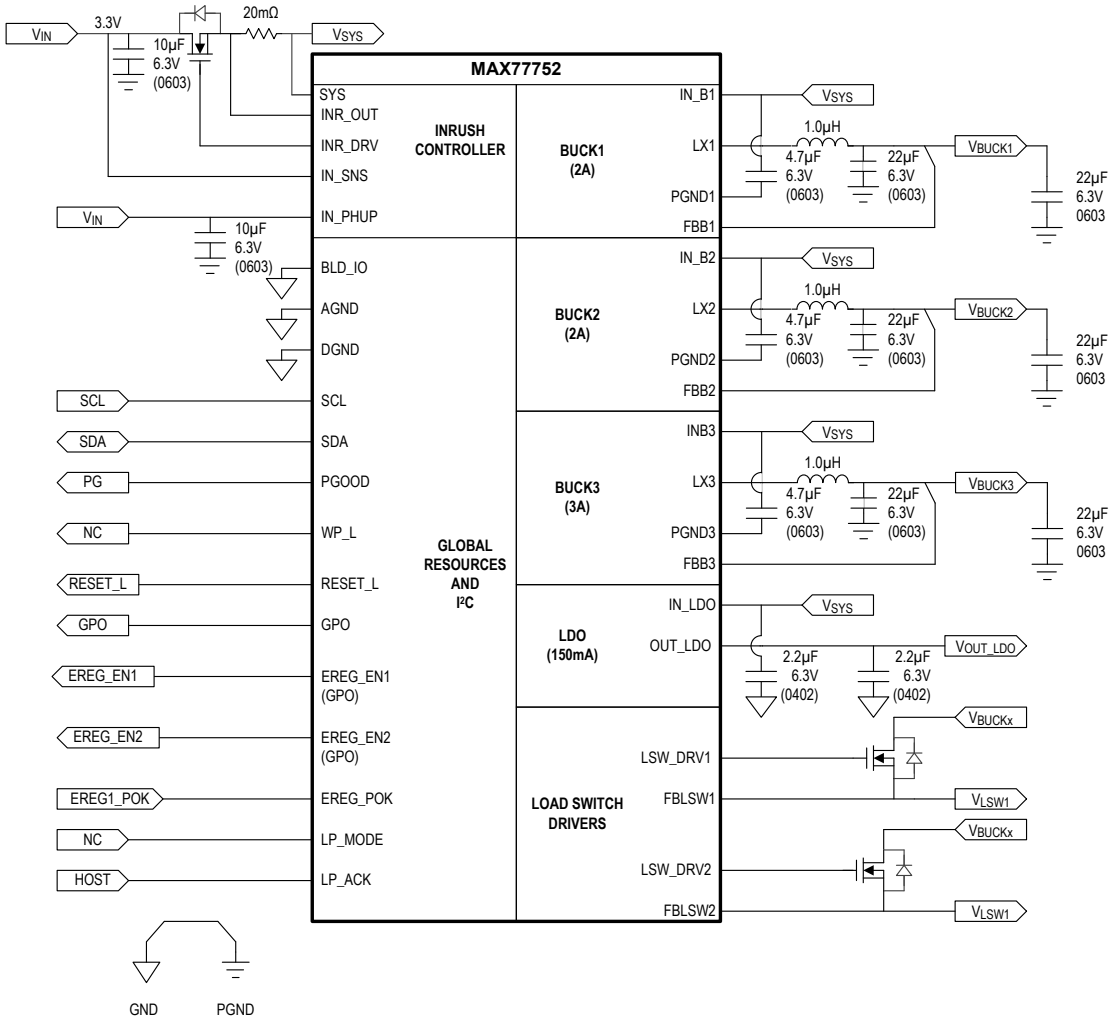
OFF to ON Software Initialization

The system processor typically runs a set of initialization code each time a transition from the OFF to the ON state occurs, the reset output is deasserted (RESET_L = 1), and the PGOOD is asserted (PGOOD = 1).

The following are recommended software steps within this initialization code:

1) Read the interrupt bits:
    1) Interrupt bits set at this point in time can indicate an issue that previously caused a shutdown.
2) Check the values of CID0, CID1, CID2, CID3, and CID4. Consider reporting these values if the product has some form of serial number checking utility. If the SBT bits do not read an appropriate value, then flag the product as bad and do not ship it. Only values of 0b011 and 0b101 should be shipped as production units. If the DRV bits do not match with what was intended for the given product, then flag that product as bad and do not ship it. This device has many OTP options and the DRV bits are set differently for each set of options. If parts got mixed up in the warehouse (i.e., A version confused for C version), then this step helps catch that mistake.
3) Set/Clear the mask bits as deemed appropriate for the target platform.

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX77752AETL+	-40°C to +85°C	40 TQFN	MAX77752AETL+
MAX77752BETL+	-40°C to +85°C	40 TQFN	MAX77752BETL+

+ Denotes a lead(Pb)-free/RoHS-compliant package.

For a copy of the register map and for further questions, contact techsupport@maximintegrated.com.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—
1	1/18	Added conditions statement to the *Electrical Characteristics—Current Sense Amplifier* table	14
2	1/18	Removed SSD and NAND from *Pin Description* table, added new part variant to *Ordering Information* table	38, 42

