2A, 5.5V, Low I_Q ACOT Synchronous Step-Down Converter

General Description

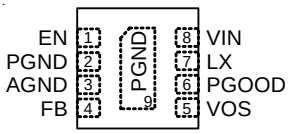
The RT5715 is a full featured 5.5V, 2A, Advanced Constant-On-Time (ACOT) synchronous step-down converter with two integrated MOSFETs. The advanced COT operation allows transient responses to be optimized over a wide range of loads, and output capacitors to efficiently reduce external component count. The RT5715 provides up to 2.7MHz switching frequency to minimize the size of output inductor and capacitors. The RT5715 is available in the WDFN-8SL 2x2 package.

Applications

- Mobile Phones and Handheld Devices
- STB, Cable Modem, and xDSL Platforms
- WLAN ASIC Power / Storage (SSD and HDD)
- General Purpose for POL LV Buck Converter

Pin Configurations

(TOP VIEW)



WDFN-8SL 2x2

Features

- **2.5V to 5.5V Input Voltage Range**
- **Advanced COT Control loop design**
- **Fast Transient Response**
- **Internal 100mΩ and 80mΩ Synchronous Rectifier**
- **Highly Accurate V_{OUT} Regulation Over Load/Line Range**
- **Robust Loop Stability with Low-ESR C_{OUT}**

Ordering Information

RT5715 □□

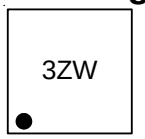
- Package Type
  QW : WDFN-8SL 2x2 (W-Type)
  (Exposed Pad-Option 2)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

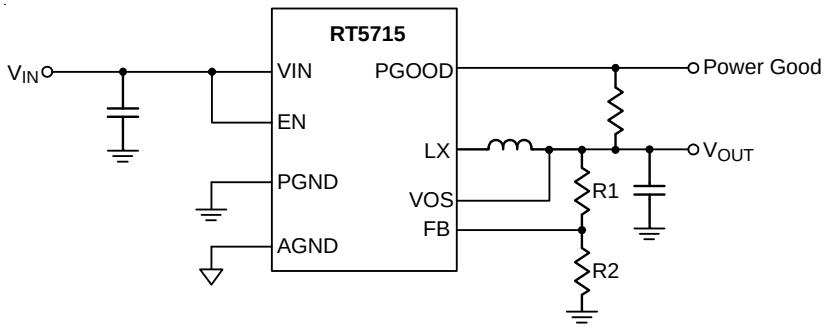
Marking Information



3Z : Product Code

W : Date Code

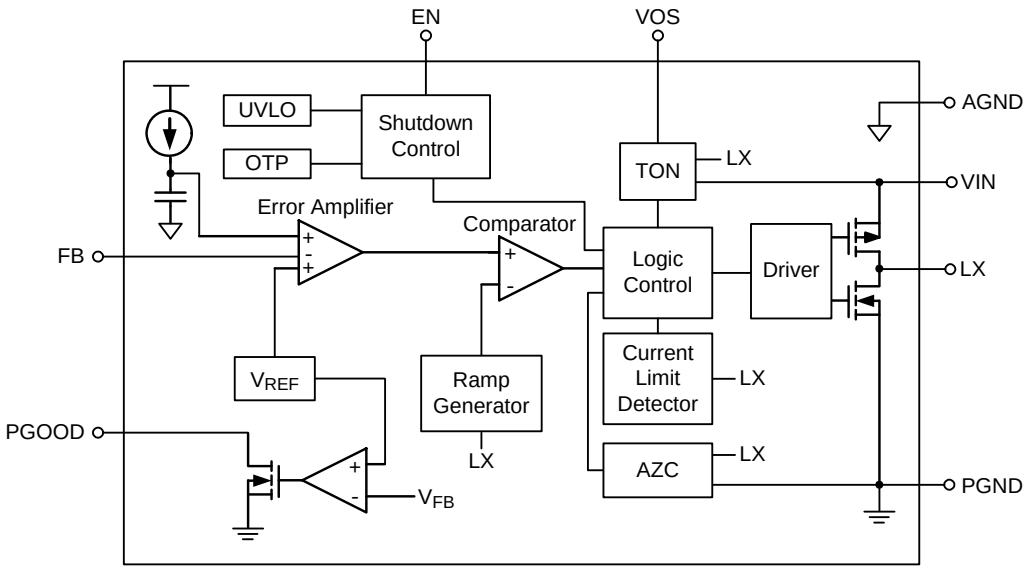
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable Control Input. Pull High to Enable.
2, 9 (Exposed Pad)	PGND	Power Ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
3	AGND	Analog Ground. Should be electrically connected to GND close to the device.
4	FB	Feedback Voltage Input.
5	VOS	Output Voltage Sense Pin for the Internal Control Loop. Must be connected to output.
6	PGOOD	Power Good Open-Drain Output. This pin is pulled to low if the output voltage is below regulation limits. Can be left floating if not used.
7	LX	Switch Node. The Source of the internal high-side power MOSFET, and Drain of the internal low-side (synchronous) rectifier MOSFET.
8	VIN	Power Input Supply Voltage, 2.5V to 5.5V.

Function Block Diagram



Operation

The RT5715 is a low voltage synchronous step-down converter that can support input voltage ranging from 2.5V to 5.5V and the output current can be up to 2A. The RT5715 uses ACOT™ mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation :

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{OSC}}$$ where f_{OSC} is nominal 2.7MHz

Under-Voltage Protection (UVLO)

The UVLO continuously monitors the VCC voltage to make sure the device works properly. When the VCC is high enough to reach the UVLO high threshold voltage, the step-down converter softly starts or pre-bias to its regulated output voltage. When the VCC decreases to its low threshold voltage, the device shuts down.

Power Good

When the output voltage is higher than PGOOD rising threshold, the PGOOD flag is high.

Output Under-Voltage Protection (UVP)

When the output voltage is lower than 66% reference voltage after soft-start, the UVP is triggered.

Over-Current Protection (OCP)

The RT5715 senses the current signal when the high-side and low-side MOSFET turns on. As a result, The OCP is a cycle-by-cycle current limit. If an over-current condition occurs, the converter turns off the next on pulse until inductor current drops below the OCP limit. If the OCP is continually activated and the load current is larger than the current provided by the converter, the output voltage drops. Also, when the output voltage triggers the UVP also, the current will drop to ZC and trigger the re-soft start sequence.

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time is 150µs.

Over-Temperature Protection (OTP)

The RT5715 has an over-temperature protection. When the device triggers the OTP, the device shuts down until the temperature is back to normal.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to (V_{IN} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8SL 2x2 ---------- 1.538W
- Package Thermal Resistance (Note 2)
  WDFN-8SL 2x2, θ_{JA} ---------- 65°C/W
  WDFN-8SL 2x2, θ_{JC} ---------- 8°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Under-Voltage Lockout Threshold		V_{UVLO}	V_{CC} Rising	2.28	2.35	2.48	V
Under-Voltage Lockout Hysteresis		V_{UVLOHY}		--	400	--	mV
Shutdown Supply Current		I_{SHDN}	EN = 0V	--	--	1	μA
Quiescent Current		I_Q	Active, V_{FB} = 0.5V, No Switching	--	30	--	μA
Voltage Reference		V_{REF}		0.4455	0.45	0.4545	V
Current Limit	High-Side	I_{LIM}	Peak Current	2.5	3.2	4	A
	Low-Side		Valley Current	2	2.4	2.9	
Power Good Threshold		V_{PGTH}	V_{OUT} Falling Referenced to V_{OUT} Nominal	–15	–10	–5	%
Power Good Hysteresis		V_{PGHY}	Hysteresis Referenced to V_{OUT} Nominal	--	5	--	%
Power Good Leakage Current		I_{PG}	V_{PG} = 5V	--	0.01	0.1	μA
Power Good Low Level Voltage		V_{PGL}	I_{sink} = 500μA	--	--	0.3	V
Enable Rising Threshold		V_{ENR}	Rising	1	--	--	V
Enable Falling Threshold		V_{ENF}	Falling	--	--	0.4	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Switch On-Resistance	High-Side	$R_{P\text{-}MOSFET}$		--	100	--	mΩ
	Low-Side	$R_{N\text{-}MOSFET}$		--	80	--	
Thermal Shutdown Temperature				--	150	--	°C
Thermal Shutdown Hysteresis				--	20	--	°C
Switching Frequency		f_{OSC}		--	2.7	--	MHz
Output Discharge Resistor				--	1	--	kΩ

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package. The copper area is 70mm^2 connected with IC exposed pad.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

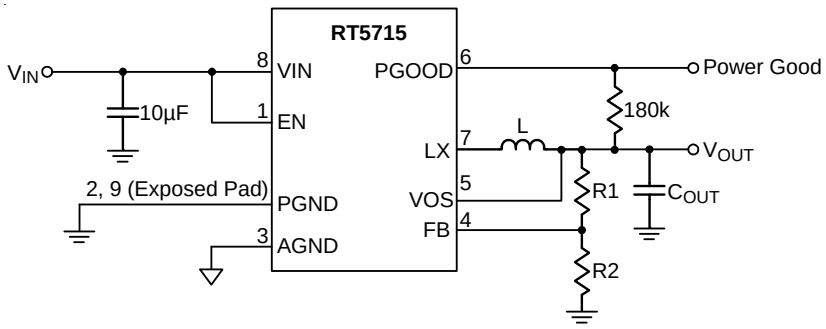
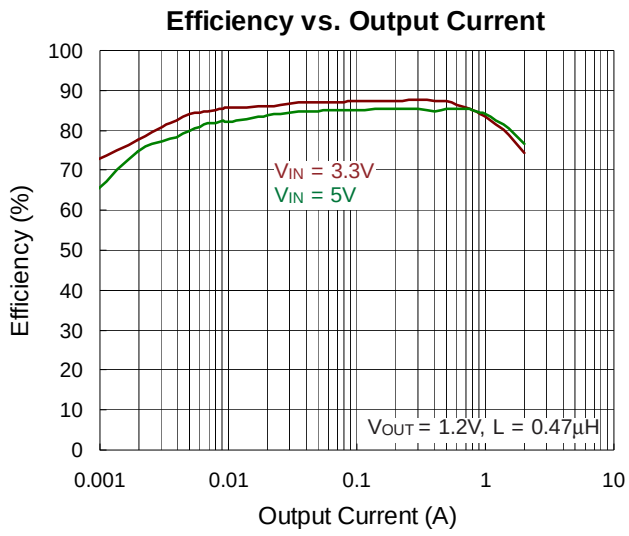
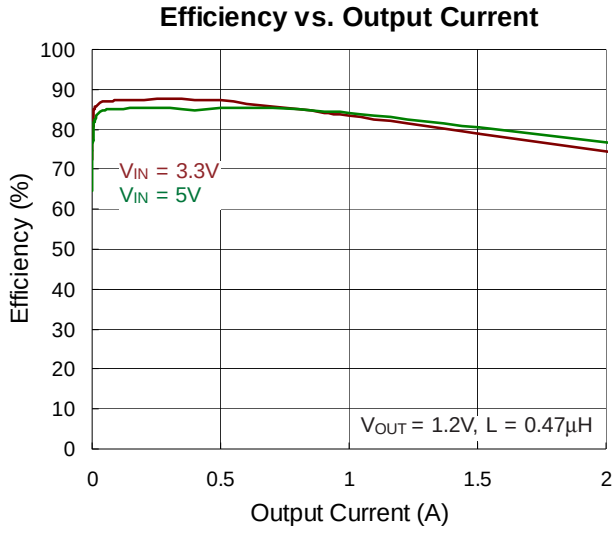


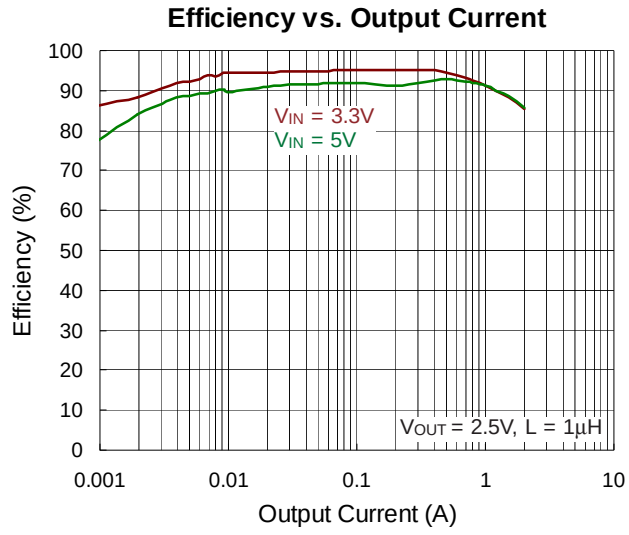
Table 1. Suggested Component Values

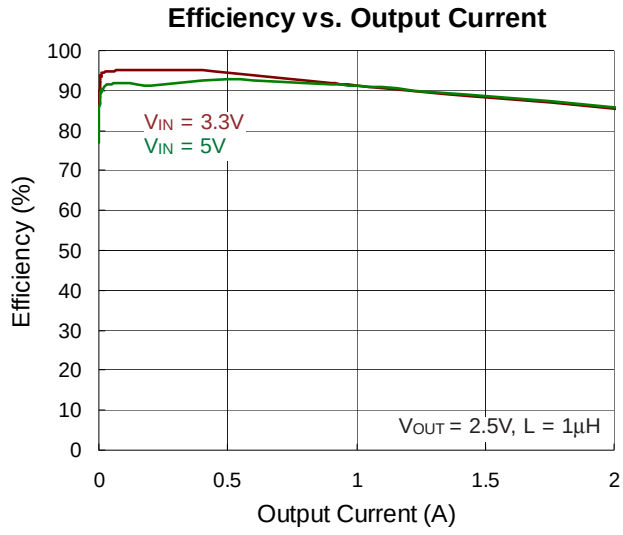
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)
1.2V	65.3	39.2	0.47	22
1.8V	117.6	39.2	1	22
2.5V	178.6	39.2	1	22
3.3V	248.3	39.2	1	22

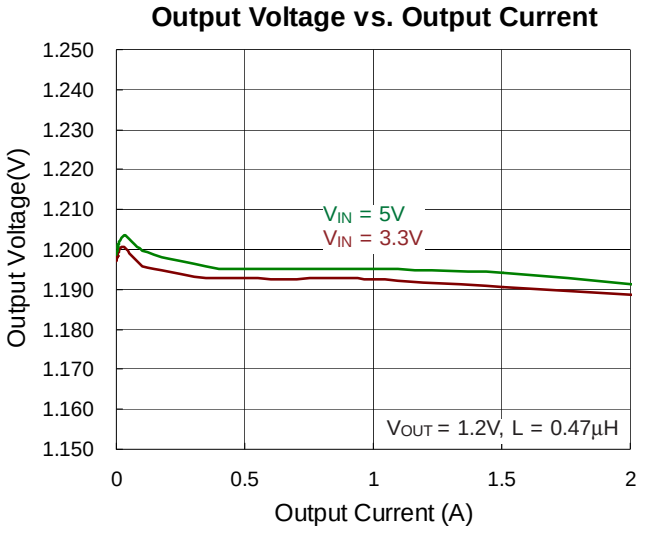
Typical Operating Characteristics

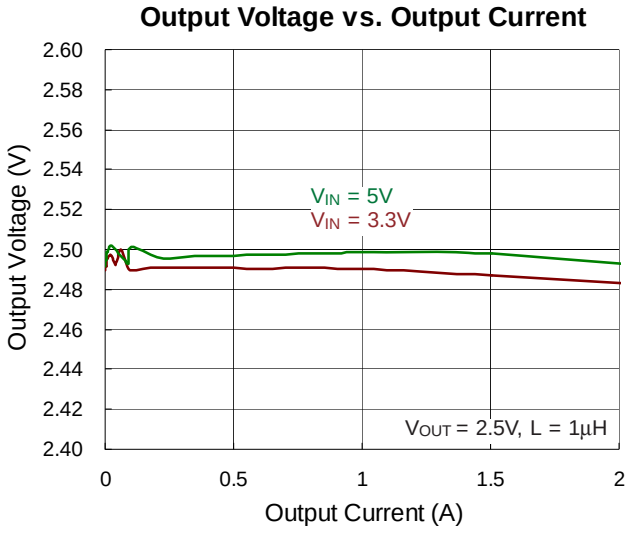




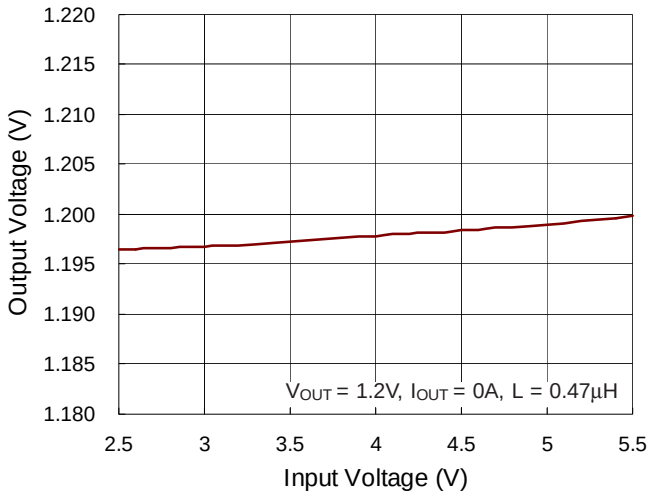




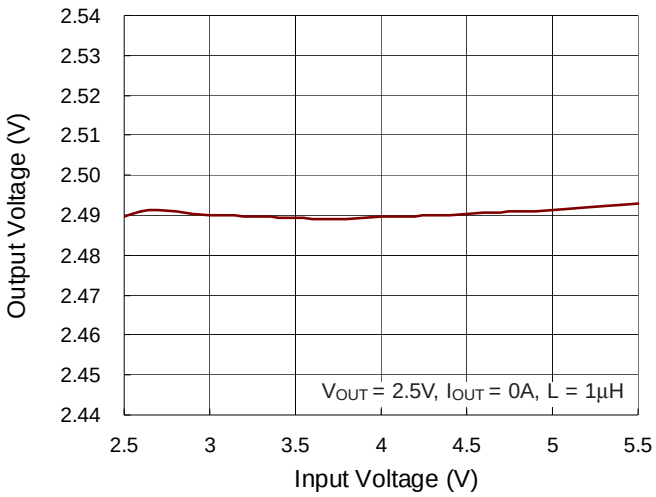




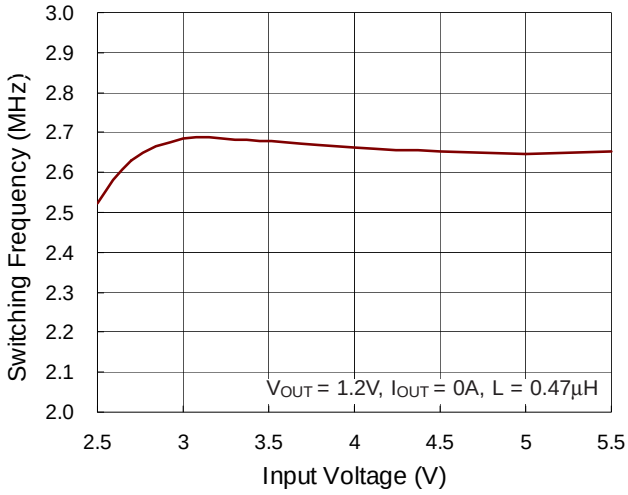
Output Voltage vs. Input Voltage



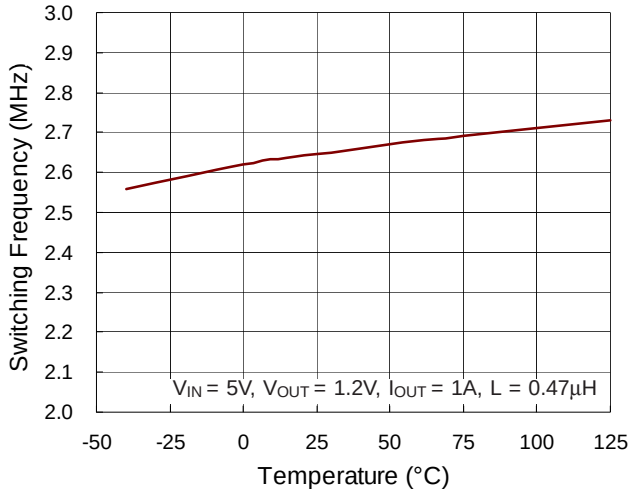
Output Voltage vs. Input Voltage



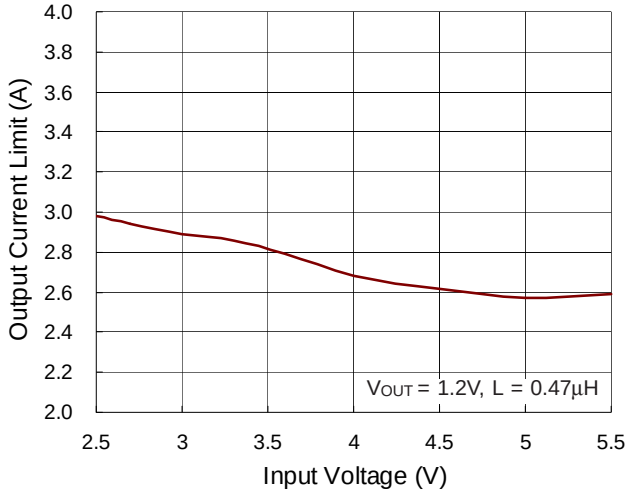
Switching Frequency vs. Input Voltage



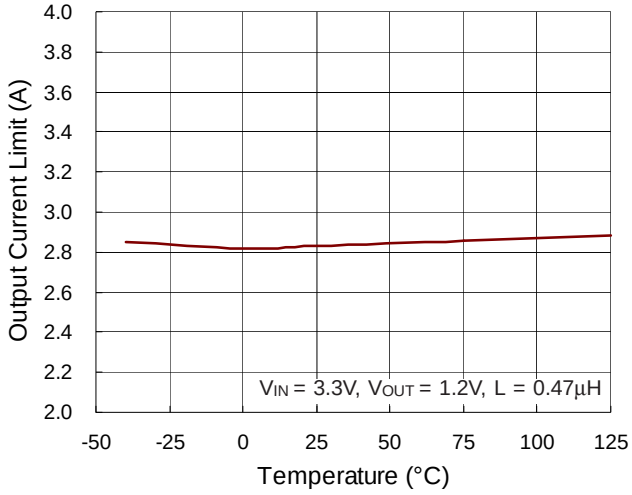
Switching Frequency vs. Temperature



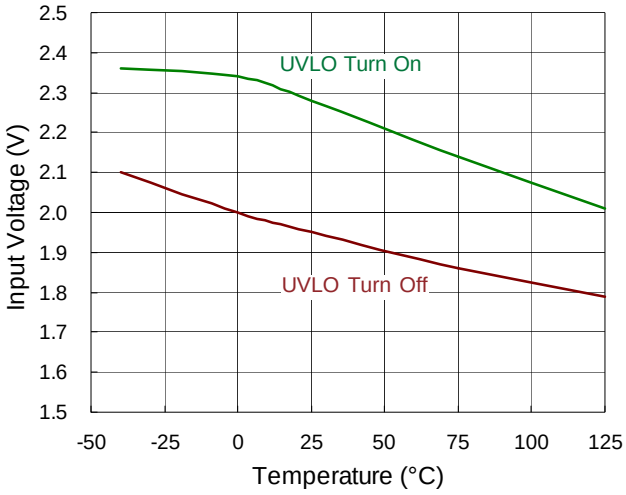
Output Current Limit vs. Input Voltage



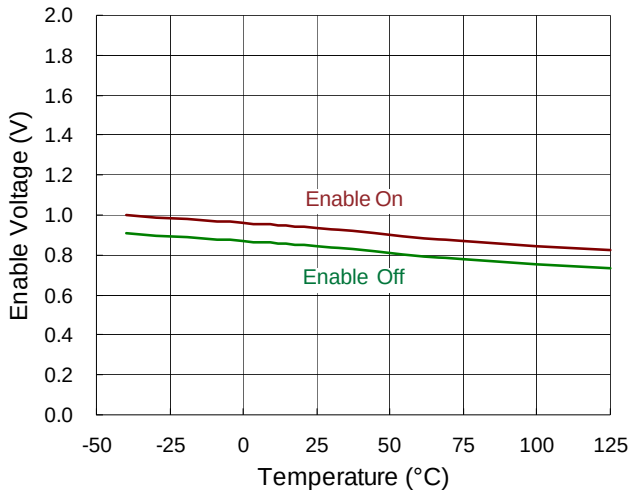
Output Current Limit vs. Temperature



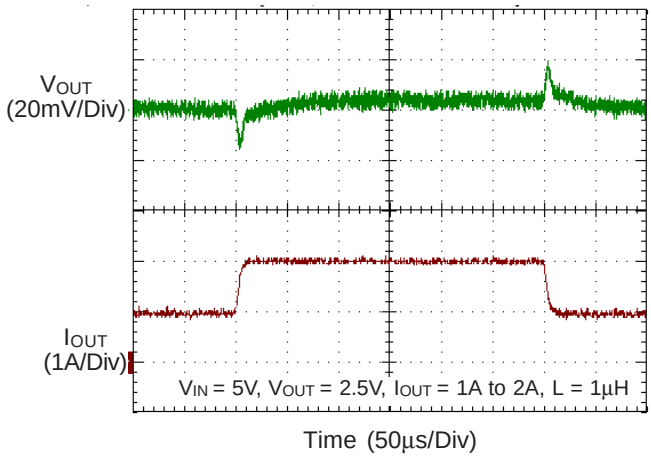
Input Voltage vs. Temperature



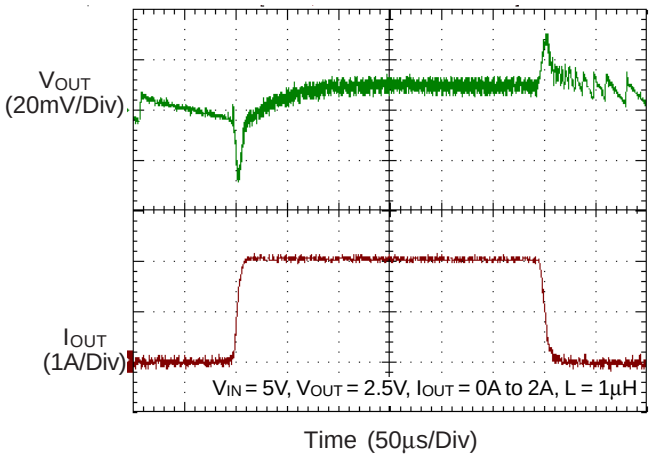
Enable Threshold vs. Temperature



Load Transient Response



Load Transient Response



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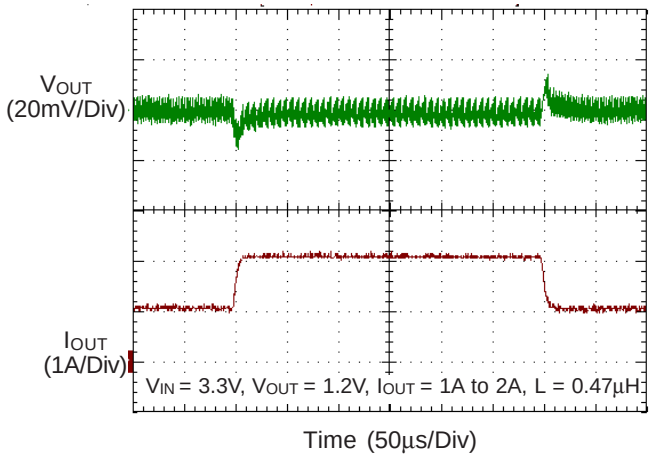
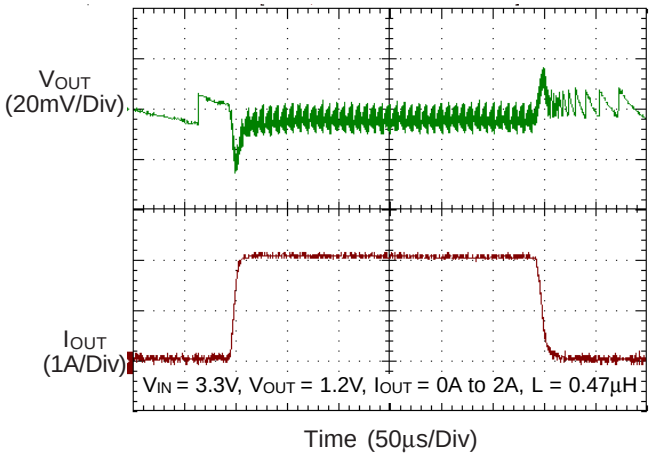
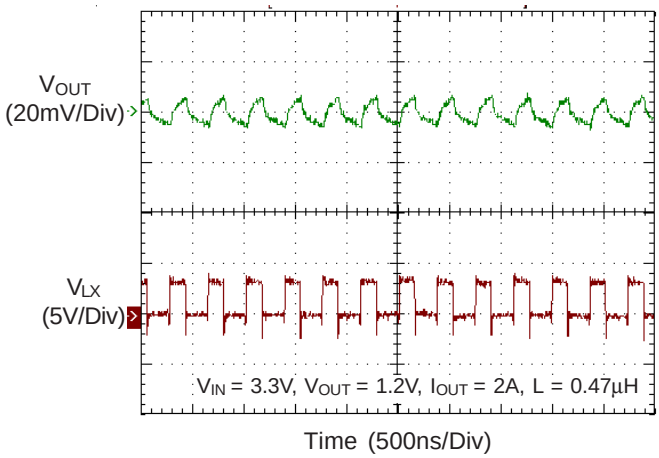


Load Transient Response



Voltage Ripple



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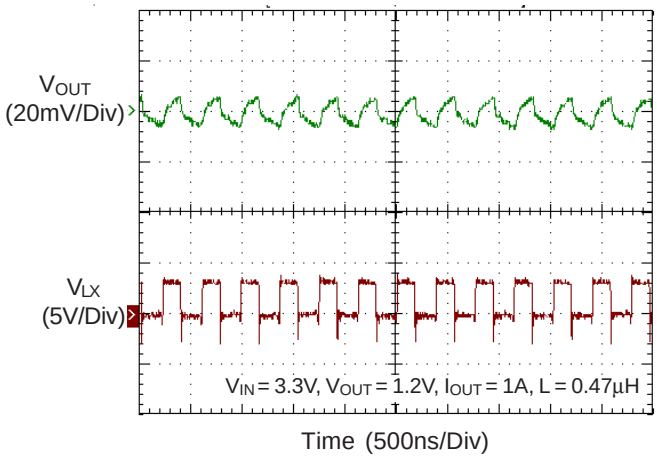
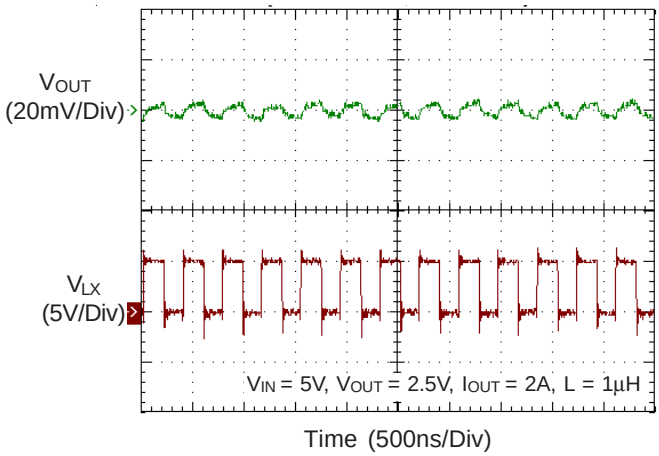
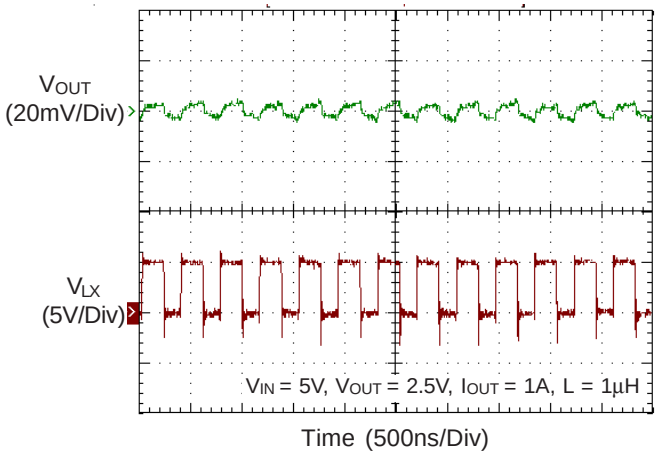


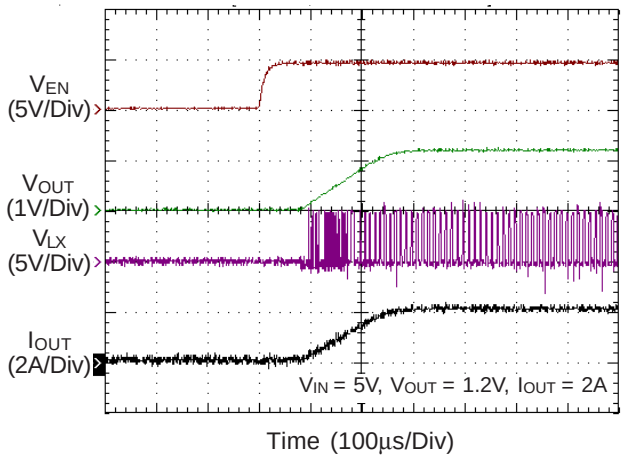
Voltage Ripple



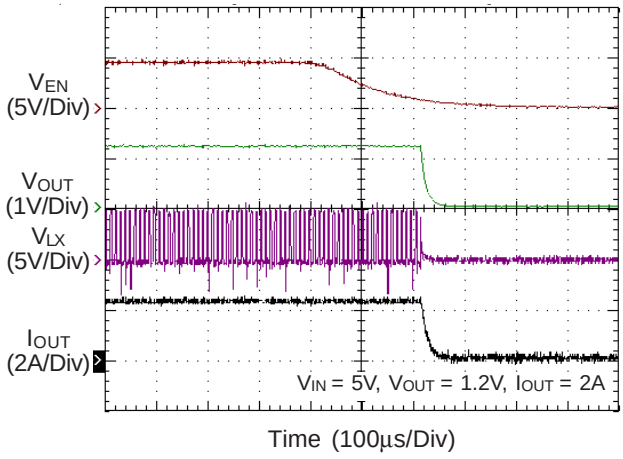
Voltage Ripple



Power On from VIN



Power Off from VIN



Application Information

The RT5715 is a single-phase step-down converter. Advance Constant-on-Time (ACOT) with fast transient response. An internal 0.45V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (2.7MHz) oscillator and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection and over temperature protection.

Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \times (1+\frac{R1}{R2})$$

where VREF equals to 0.45V typical. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

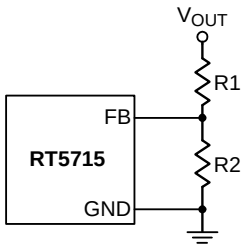


Figure 1. Setting the Output Voltage

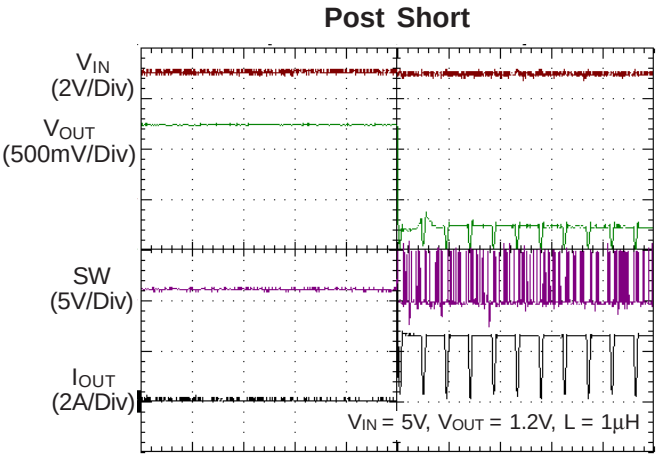
Low Supply Operation

The RT5715 is designed to operate down to an input supply voltage of 2.5V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-Channel and N-Channel power switches increases. The user should calculate the power dissipation when the RT5715 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Under Voltage Protection (UVP)

Hiccup Mode

For the RT5715, it provides Hiccup Mode Under Voltage Protection (UVP). When the output voltage is lower than 66% reference voltage after soft-start, the UVP is triggered. If the UVP condition remains for a period, the RT5715 will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.



C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst case condition is commonly used for design because even significant deviations do not result in much difference. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR, but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects.

The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Table 2. Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
MuRata	GRM31CR71A106KA01	10μF	1206
MuRata	GRM31CR71A226KA01	22μF	1206

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-8SL 2x2 packages, the thermal resistance, θ_{JA}, is 65°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (65°C/W) = 1.538W for WDFN-8SL 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

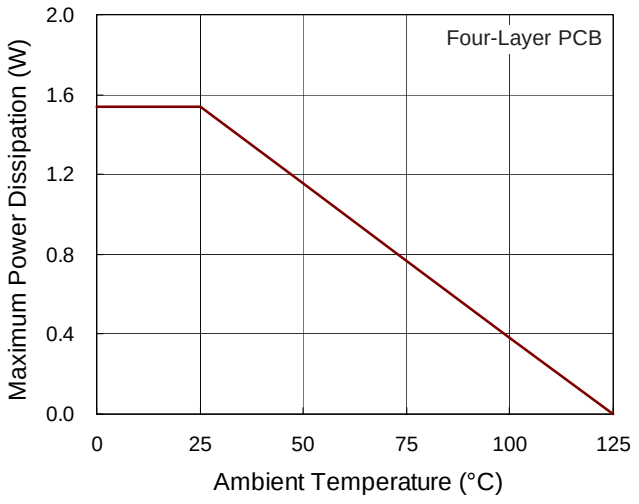


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT5715.

- Connect the terminal of the input capacitor(s), C_{IN}, as close as possible to the VIN pin. This capacitor provides the AC current into the internal power MOSFETs.
- LX node experiences high frequency voltage swing and should be kept within a small area. Keep all sensitive small-signal nodes away from the LX node to prevent stray capacitive noise pick up.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND, or any other DC rail in the system).
- Connect the FB pin directly to the feedback resistors. The resistive voltage divider must be connected between V_{OUT} and GND.

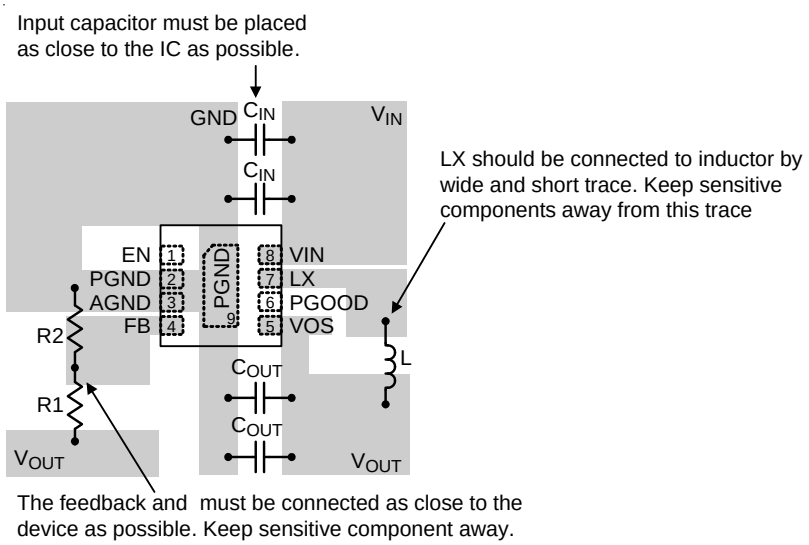
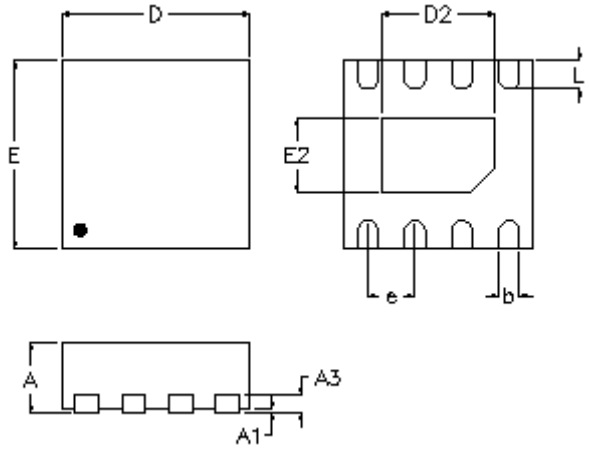
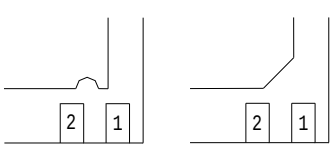


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		1.900	2.100	0.075	0.083
D2	Option1	1.150	1.250	0.045	0.049
	Option2	1.550	1.650	0.061	0.065
E		1.900	2.100	0.075	0.083
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e		0.500		0.020	
L		0.250	0.350	0.010	0.014

W-Type 8SL DFN 2x2 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789