MAX20330

Programmable OVP Controller with VBUS Short Detection

General Description

The MAX20330 is an overvoltage controller with the VBUS impedance detection function. The device drives an external low R_{ON} path for the device that requires a flexible and adjustable OVLO threshold. The VBUS impedance detection can detect the soft short on VBUS and warn the user about the potential connector overheating.

The MAX20330 is designed to drive a single or dual back-to-back external N-channel MOSFET with a low R_{ON} (10mΩ max). An external TVS can be used to protect the device from a high energy surge if necessary.

The device is available in an 8-bump (0.35mm pitch, 1.77mm x 1.03mm) wafer-level package (WLP) and operate over the -40ºC to +85°C extended temperature range.

Applications

- Smart Phones
- Tablets
- Phablets
- Desktops

Benefits and Features

- Protects High-Power Portable Devices
  - Wide Operating Input Voltage Protection Range: 2.7V to 36V
  - Ultra-Fast Turn-Off Time: 100nsec
  - Built-In Charge Pump to Drive External N-MOSFET
- Flexible Overvoltage Protection Design
  - I^2C Adjustable Overvoltage Protection Trip Level
  - Wide Adjustable OVLO Threshold Range from 4V to 24V (168 steps)
  - Preset Internal Accurate OVLO Thresholds: 6.8V±2%
- Additional Protection Features Increase System Reliability
  - VBUS Short Detection
  - Soft-Start to Minimize In-Rush Current
  - Internal 15ms Startup Debounce
  - Thermal Shutdown Protection
- Space-Saving
  - 8 Bump 0.35mm Pitch 1.77mm x 1.03mm WLP

***Ordering Information** appears at end of data sheet.*

19-100269; Rev 0; 3/18

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
VBUS to GND (Note 1) .....-0.3V to +40V
GATE to GND..... -0.3V to min (VBUS + 0.3V, 40V)
OUT to GND.....-0.3V to min (GATE + 0.3V, 40V)
GATE to OUT .....-0.3V to +6V
SDA, SCL, $\overline{INT}$, V_{CC} to GND.....-0.3V to +6V
Continuous Current into all pins.....±0.1A

Continuous Power Dissipation (T_A = +70ºC)
WLP (derate 10.9mW/ºC above +70ºC).....872mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....91.72°C/W

Note 1: The external TVS clamp voltage should be below the abs max of MAX20330.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{BUS} = 2.7V to 36V, V_{CC} = 2.6V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VBUS							
VBUS Startup Voltage	V_{BUS_ST}				2.7	2.75	V
VBUS Supply Current	I_{VBUS}	V_{BUS} = 4.2V, I_{OUT} = 0mA			250	400	µA
VBUS Pull Down Resistor	R_{PD}	Enabled by I^2C		0.5	1	2	kΩ
OUT PROGRAMMABLE PROTECTION							
VBUS OVLO Range		Shutdown		4		24	V
Internal Overvoltage Trip Level	V_{OVLO_R}	VBUS rising		-2	Programmable	+2	%
Internal Overvoltage Trip Hysteresis	V_{OVLO_F}	VBUS falling			0.2		%
VBUS OVLO Resolution		4V – 8V [63]			63.5		mV
		8V – 16V [63]			127		
		12V – 24V [63]			190.5		
V_{CC}							
V_{CC} Voltage Range	V_{CC}			2.6	3.3	5.5	V
V_{CC} Supply Current	I_{VCC}	V_{CC} = 4.2V, manual detection mode (I_{SRC} = 0mA)			125	200	µA
V_{CC} Shutdown Current		V_{CC} = 4.2V, VBUS floating, ENb = 1			2.8	5	µA
GATE							
Maximum Gate On Voltage	V_{GON}	GATE external leakage <1µA		min (VBUS, 5V)			V
			VBUS = 2.75V	2.43			
			VBUS = 5V, 23V	4.6		5.4	
Gate Off	V_{GOFF}					0.5	V
Soft-Start Comparator	V_{SS_THR}			220	300	380	mV

Electrical Characteristics (continued)

(V_{BUS} = 2.7V to 36V, V_{CC} = 2.6V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ID CURRENT SOURCE						
Current Source Accuracy			-5		+5	%
Current Source Open Voltage	V_{OVSO}	I_{ID} = 2µA			2	V
Current Source	I_{ID}			2		µA
				6		
				18		
				54		
				162		
				2500		
Average Current Source	I_{ID_AVG}	162µA max current, IS_PERIOD ≥ 130x, ISRC_MAN = 0			2	µA
ADC						
Resolution				8		bit
Voltage step				5.9		mV
Full-Scale Error			-2		+2	%
Noise Filtering				100		µs
Full Scale				1.5		V
DIGITAL SIGNALS (SDA, SCL, $\overline{INT}$)						
Output Low Voltage	V_{OL}	V_{IO} = 3.3V, I_{SINK} = 3mA			0.4	V
Leakage Current		V_{IO} = 2.6V, open-drain			1	µA
Input Logic-High	V_{IH}		1.3			V
Input Logic-Low	V_{IL}				0.4	V
Input Leakage Current	I_{BUS_LEAK}	V_{IN} = 0V, V_{IN} = 2.6V	-1		+1	µA
TIMING CHARACTERISTICS						
VBUS Debounce Time	t_{DEB}	VBUS = 4.3V to charge pump on (OUT = 10% of VBUS), R_{LOAD} = 100Ω, C_{LOAD} = 10µF		Programmable		ms
VBUS Soft-Start Time	t_{SS}	IGATE = 4µA (typ)		50		ms
VBUS Fast OVP Turn Off Response Time	t_{OFF}	From VBUS > V_{OVLO_R} to $V_{GATE_TO_SOURCE}$ = 0.5V, $C_{GATE_TO_OUT}$ = 4nF		100		ns
Programmable Time Accuracy			-10		+10	%
I^2C Maximum Clock Frequency				400		kHz

Electrical Characteristics (continued)

(V_{BUS} = 2.7V to 36V, V_{CC} = 2.6V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL PROTECTION						
Thermal Shutdown				125		°C
Thermal Shutdown Hysteresis				20		°C

Note 3: All devices are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design.

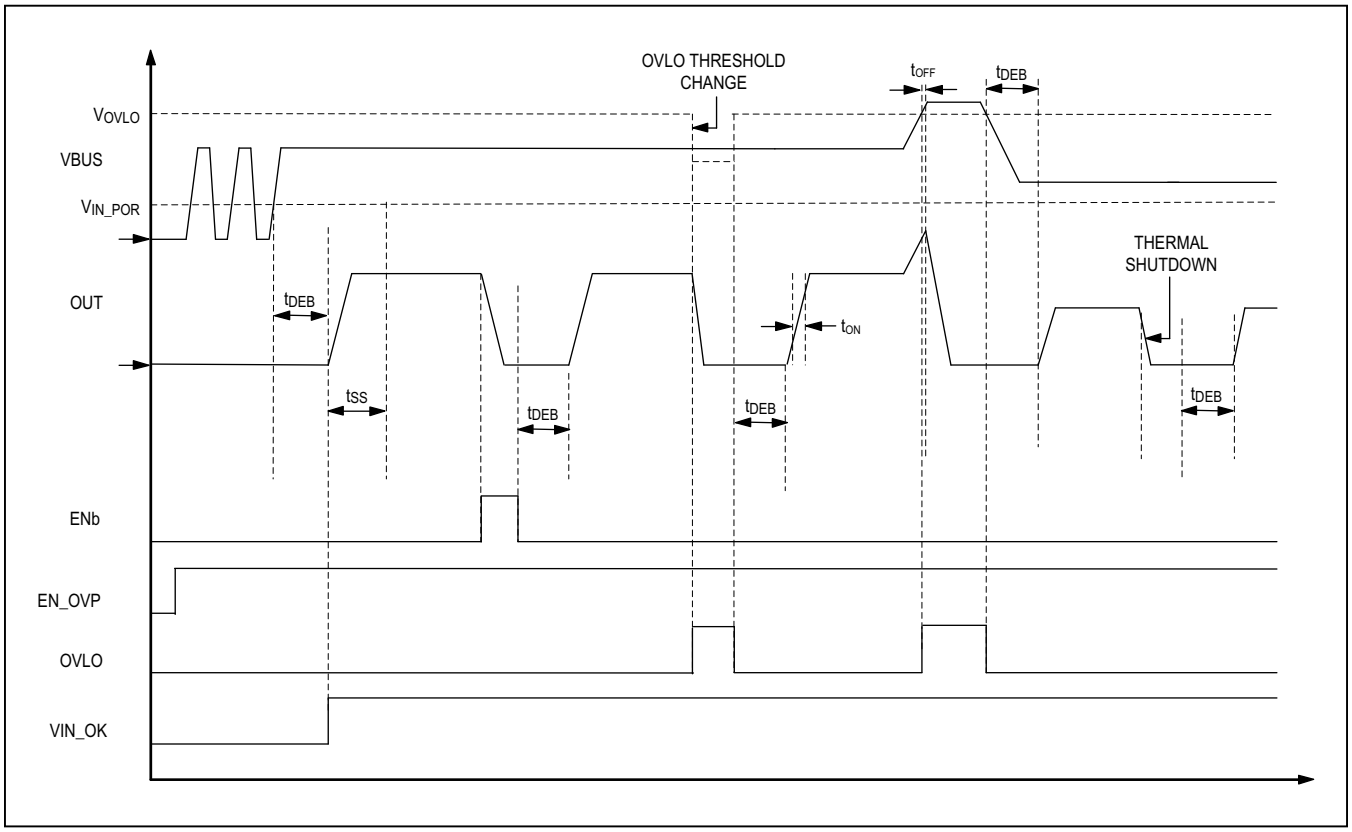
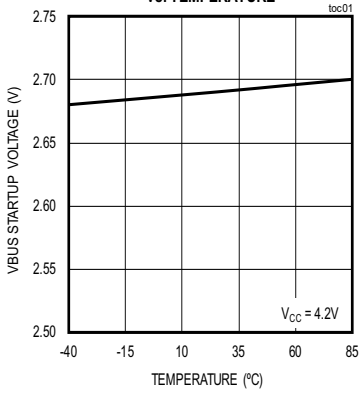


Figure 1. Timing Diagram

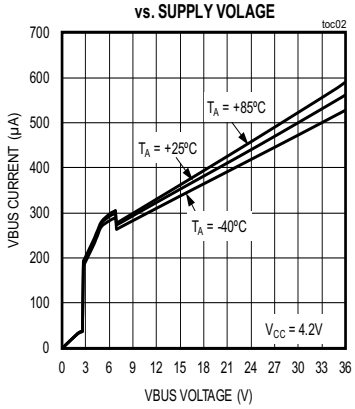
Typical Operating Characteristics

(V_{CC} = 4.2V, T_A = +25°C, unless otherwise noted.)

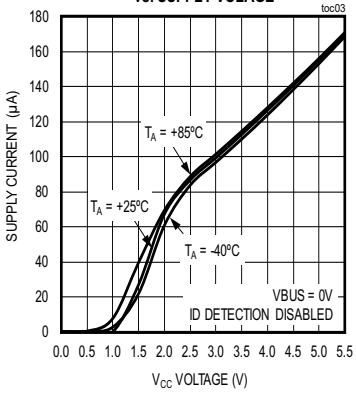
VBUS STARTUP VOLTAGE vs. TEMPERATURE



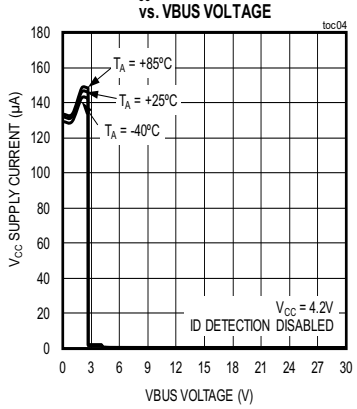
VBUS SUPPLY CURRENT vs. SUPPLY VOLAGE



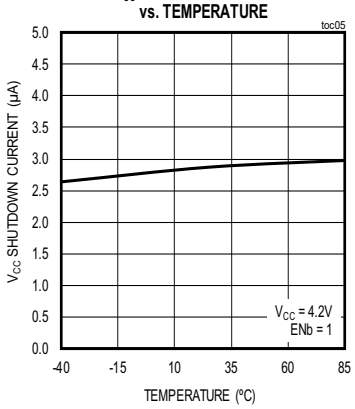
VCC SUPPLY CURRENT vs. SUPPLY VOLAGE



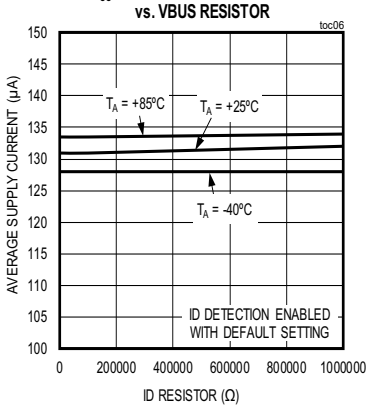
VCC SUPPLY CURRENT vs. VBUS VOLTAGE



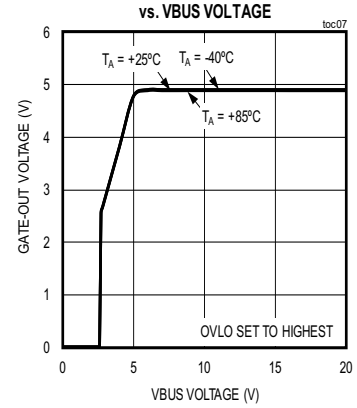
VCC SHUTDOWN CURRENT vs. TEMPERATURE



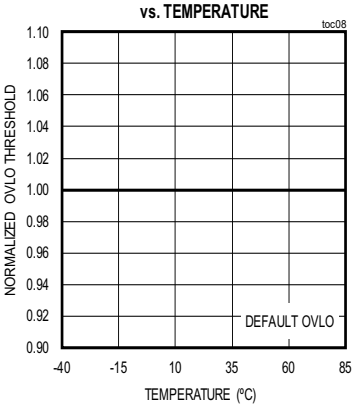
VCC AVERAGE SUPPLY CURRENT vs. VBUS RESISTOR



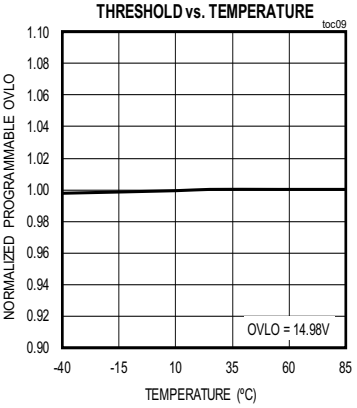
GATE-OUT VOLTAGE vs. VBUS VOLTAGE



NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



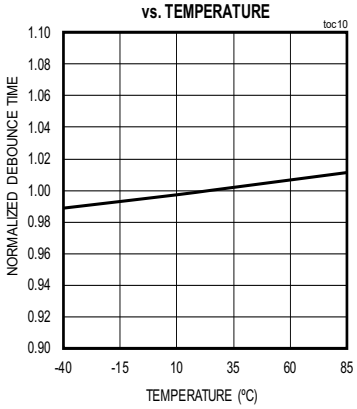
NORMALIZED PROGRAMMABLE OVLO THRESHOLD vs. TEMPERATURE



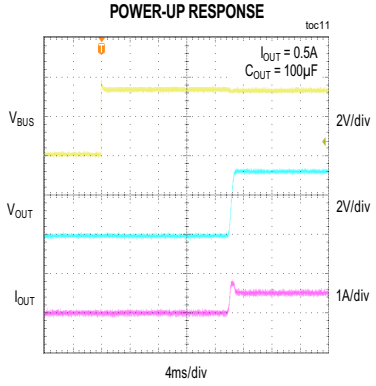
Typical Operating Characteristics (continued)

(V_{CC} = 4.2V, T_A = +25°C, unless otherwise noted.)

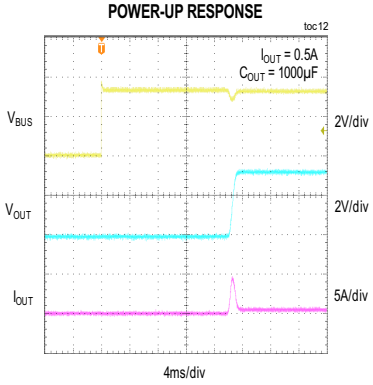
NORMALIZED DEBOUNCE TIME vs. TEMPERATURE



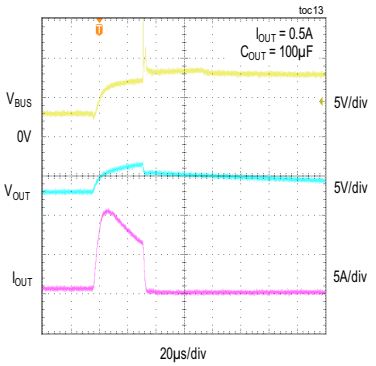
POWER-UP RESPONSE



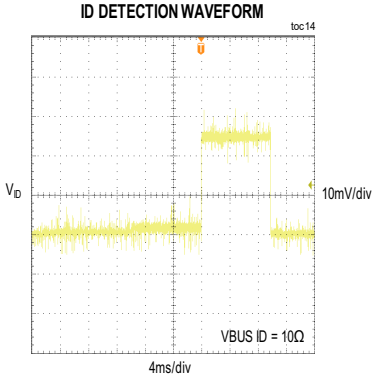
POWER-UP RESPONSE



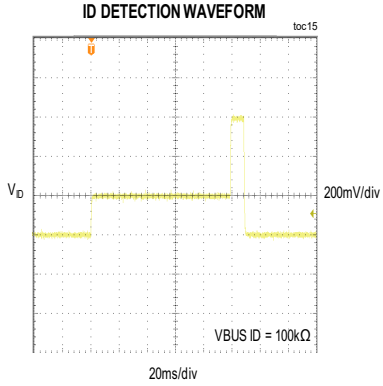
OVERVOLTAGE FAULT RESPONSE



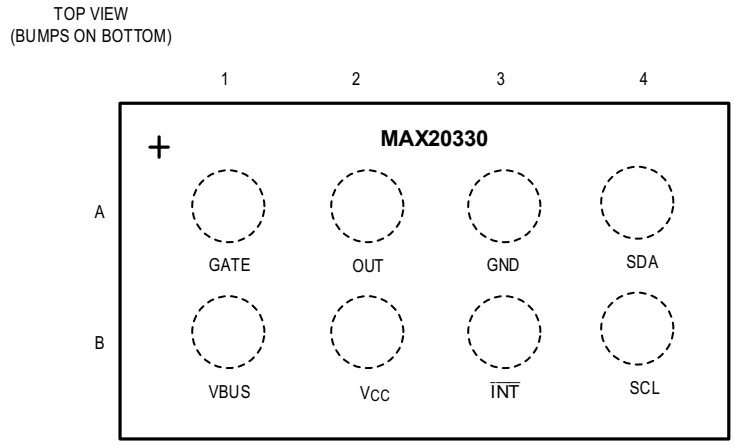
ID DETECTION WAVEFORM



ID DETECTION WAVEFORM



Bump Configuration



Bump Description

BUMP	NAME	FUNCTION
A1	GATE	Gate Drive Output for External N-FET
A2	OUT	Output Voltage to the Battery Terminal. Output of internal switch.
A3	GND	Ground
A4	SDA	I^2C Data Line. Connect SDA to an external pullup resistor.
B1	VBUS	VBUS Input. For proper ESD and surge protection, place the external TVS and a 0.1µF capacitor on VBUS.
B2	V_{CC}	Supply for the I^2C Digital Block. Bypass V_{CC} to ground with a 0.1µF capacitor as close to the device as possible.
B3	$\overline{INT}$	Interrupt Output.
B4	SCL	I^2C Clock. Connect SCL to an external pullup resistor.

Functional Diagram

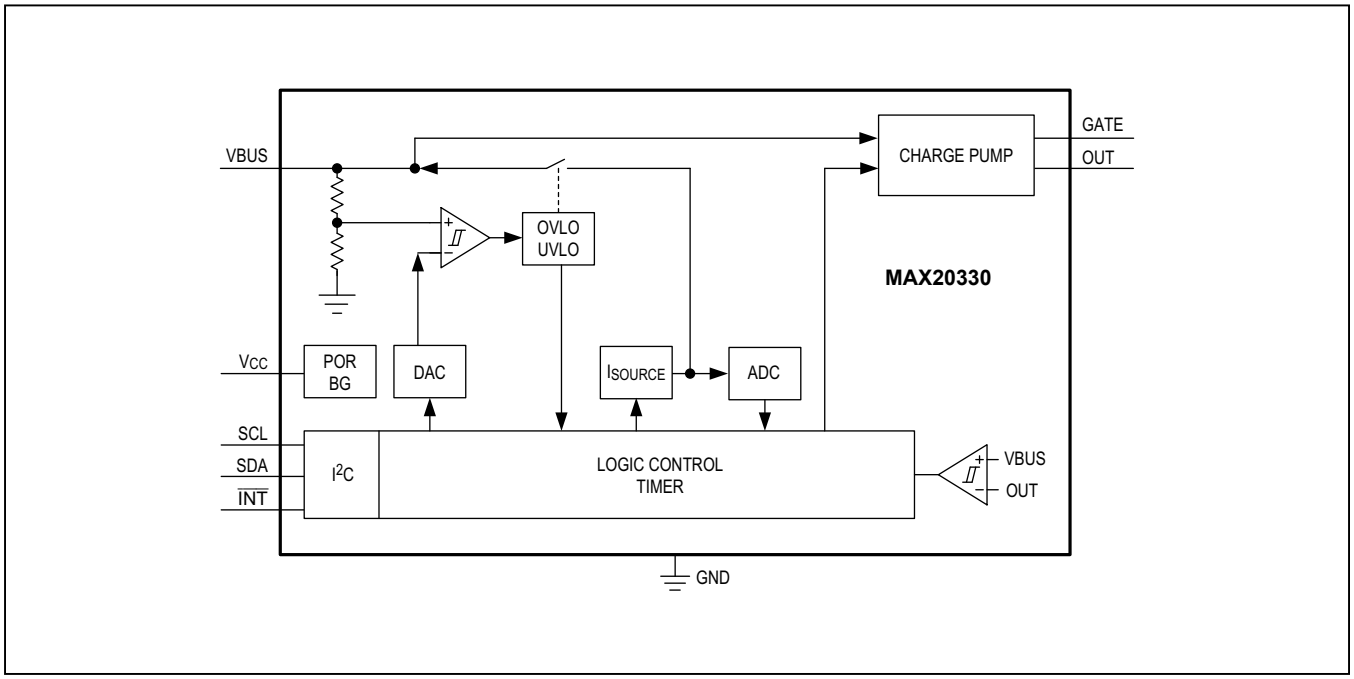


Table 1. Register Map

ADDRESS	NAME	TYPE	DEFAULT	DESCRIPTION
0x00	CHIP ID	Read Only	0x00	Device ID Register
0x01	CONTROL 1	RW	0x88	System Control 1
0x02	STATUS	Read Only	0x00	Status Register
0x03	INTERRUPT	Clear on Read	0x00	Interrupt Register
0x04	MASK	RW	0xFF	Mask Register
0x05	SET_OVLO	RW	0x2C	OVLO Threshold
0x06	I_SRC	RW	0x01	Current Source Threshold
0x07	I_SRC_TMR	RW	0x1B	Current Source On-Timer
0x08	CONTROL 2	RW	0x3C	System Control 2
0x0A	ACCDET_REF	RW	0xF0	Accessory Detection Threshold
0x0B	ISRC_ADC	Read Only	0x00	Current Source Output
0x0C	VBUS_ADC	Read Only	0x00	Current Source Output

Table 2. Detailed Register Map

CHIP ID 0X00 (READ ONLY)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	CHIP_ID				CHIP_REV			
Reset Value	0	0	0	0	0	0	0	0
Description	Chip ID and Revision							
CONTROL 1 0x01 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	EN_OVP	EN_IS	RFU	VBUS_DET		VBUSADC_EN	RFU	ENb
Reset Value	1	0	0	0	1	0	0	0
EN_OVP	OVP Enable (EN_OVP and EN_IS can not be “1” at the same time) 0 = OVP disabled 1 = OVP enabled (default)							
EN_IS	Current Source (I_SRC) Enable 0 = I_SRC disabled (default) 1 = I_SRC enabled							
RFU	Reserved for future use							
VBUS_DET	VBUS Debounce Time (t_{DEB}) 00 = 1ms or min time for power-up 01 = 15ms (default) 10 = 30ms 11 = 60ms							
VBUSADC_EN	One Time ADC for VBUS. The bit is cleared after the measurement. EN_OVP = 1 is required to run one time ADC for VBUS. 0 = VBUS ADC is disabled 1 = VBUS ADC is enabled							
ENb	Device Active Low Enable. Reset at VBUS rising edge. 0 = device is in active mode (default) 1 = device is in sleep mode							

Table 2. Detailed Register Map (continued)

STATUS 0x02 (Read Only)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	VIN_OK	RFU	EOC	TP_OUT	ACC_ DET	THERM_ SHDN	OUT_ SHRT	OVLO
Reset Value	0	0	0	0	0	0	0	0
VIN_OK	VIN (VBUS) is above 2.7V (typ) 0 = VBUS is below 2.7V (typ) 1 = VBUS is above 2.7V (typ)							
RFU	Reserved for future use							
EOC	End of ADC Conversion 0 = no conversion since last read 1 = new ADC data since last read							
TP_OUT	Timer Period Out 0 = timer period not expired 1 = timer period expired							
ACC_DET	Accessory Detection Status 0 = no change 1 = accessory detected							
THERM_SHDN	Thermal Shutdown 0 = no thermal shutdown 1 = thermal shutdown							
OUT_SHRT	OUT does not reach 90% of VBUS within Soft Start Time 0 = OUT ok 1 = OUT not ok							
OVLO	Overvoltage Shutdown 0 = no OVP shutdown 1 = OVP shutdown							

Table 2. Detailed Register Map (continued)

INTERRUPT 0x03 (Clear on Read)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	VIN_OKi	RFU	EOCi	TP_OUTi	ACC_ DETi	THERM_ SHDNi	OUT_ SHRTi	OVLOi
Reset Value	0	0	0	0	0	0	0	0
VIN_OKi	VIN (VBUS) is above 2.7V (typ) interrupt 0 = interrupt not occurred 1 = interrupt occurred							
RFU	Reserved for future use							
EOCi	ADC EOC interrupt 0 = interrupt not occurred 1 = interrupt occurred							
TP_OUTi	Timer Period OUT interrupt 0 = interrupt not occurred 1 = interrupt occurred							
ACC_DETi	Accessory Detection interrupt 0 = interrupt not occurred 1 = interrupt occurred							
THERM_SHDNi	Thermal Shutdown interrupt 0 = interrupt not occurred 1 = interrupt occurred							
OUT_SHRTi	OUT does not reach 90% of VBUS within soft-start time interrupt 0 = interrupt not occurred 1 = interrupt occurred							
OVLOi	Overvoltage shutdown interrupt 0 = interrupt not occurred 1 = interrupt occurred							

Table 2. Detailed Register Map (continued)

MASK 0x04 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	VIN_OKm	RFU	EOCm	TP_ OUTm	ACC_ DETm	THERM_ SHDNm	OUT_ SHRTm	OVLOm
Reset Value	1	1	1	1	1	1	1	1
VIN_OKm	VIN (VBUS) is above 2.7V (typ) interrupt 0 = not masked 1 = masked							
RFU	Reserved for future use							
EOCm	ADC EOC interrupt 0 = not masked 1 = masked							
TP_OUTm	Timer Period OUT interrupt 0 = not masked 1 = masked							
ACC_DETm	Accessory Detection interrupt 0 = not masked 1 = masked							
THERM_SHDNm	Thermal Shutdown interrupt 0 = not masked 1 = masked							
OUT_SHRTm	OUT does not reach 90% of VBUS within soft start time interrupt 0 = not masked 1 = masked							
OVLOm	Overvoltage shutdown interrupt 0 = not masked 1 = masked							
SET_OVLO 0x05 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	SET_OVLO							
Reset Value	0	0	1	0	1	1	0	0
SET_OVLO	OVLO Threshold Set (8 bit resolution) 0000,0000 – 0011, 1111: 4V-8V [63 steps] (1.59% resolution) 0100,0000 – 0111,1111: 8V-16V [63 steps] 1000,0000 – 1011,1111: 12V-24V [63 steps] 1100,0000 – 1111,1111: 12V-24V [63 steps] Default: 6.8V							

Table 2. Detailed Register Map (continued)

I_SRC 0x06 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU	I_SRC_MON			RFU	I_SRC_SET		
Reset Value	0	0	0	0	0	0	0	1
RFU	Reserved for future use.							
I_SRC_MON (Read Only)	Current source monitor 000 = off 001 = 2µA 010 = 6µA 011 = 18µA 100 = 54µA 101 = 162µA 110 = 2500µA 111 = reserved							
I_SRC_SET	Current source set In auto mode, it is the maximum current source set. Above this value, the auto ID detection is skipped. In manual mode, it is the fixed current source set. 000 = off 001 = 2µA (default) 010 = 6µA 011 = 18µA 100 = 54µA 101 = 162µA 110 = 2500µA 111 = reserved							
I_SRC_TMR 0x07 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU		IS_PERIOD		IS_INIT_SET	IS_TDET		
Reset Value	0	0	0	1	1	0	1	1
RFU	Reserved for future use.							
IS_PERIOD	Repeat period, off period 00 = 4x 01 = 130x (default) 10 = 250x 11 = 1600x							
IS_INIT_SET	Set the initial value different from IS_PERIOD and IS_TDET for the ID detection auto-mode 0 = use IS_PERIOD and IS_TDET for the initial check (2µA) 1 = use IS_PERIOD = 00 and IS_TDET = 101 as the initial value. If the current source needs to increase, then use the programmed IS_PERIOD and IS_TDET value for the current source larger than 2µA. (default)							
IS_TDET	Current source on time for detection 000 = 2500µs 001 = 3500µs 010 = 4000µs 011 = 10000µs (default) 100 = 40000µs 101 = 100000µs 110 = 400000µs 111 = 1sec							

Table 2. Detailed Register Map (continued)

CONTROL2 0x08 (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	RFU	EN_ VBPD	VBPD_TMR		AUT_ISRC_SCL		ISRC_ MAN	ISRC_ST
Reset Value	0	0	1	1	1	1	0	0
RFU	Reserved for future use.							
EN_VBPD	1kΩ VBUS pulldown enable bit. The bit is cleared after pull down time expires. 0 = pull down disabled (default) 1 = pull down enabled							
VBPD_TMR	VBUS pull down discharge window 00 = 5ms 01 = 15ms 10 = 30ms 11 = 60ms (default)							
AUT_ISRC_SCL	Automatic scaling for impedance detection reference 00 = 10% of full ADC scale 01 = 20% of full ADC scale 10 = 30% of full ADC scale 11 = 40% of full ADC scale (default)							
ISRC_MAN	Current source manual detection 0 = automatic scaling for detection when ENb = 0 (default) 1 = manual detection when ENb = 0, fixed based on I_SRC and ISRC_TMR register values (register 0x06 and 0x07)							
ISRC_ST	Current source manual start and ADC conversion. The bit is cleared after one impedance detection. 0 = disable (default) 1 = start one manual impedance detection							
ACCDET_REF 0x0A (Read/Write)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	ACC_DET_TH							
Reset Value	1	1	1	1	0	0	0	0
ACC_DET_TH	Accessory Detection Threshold Accessory is detected (ACC_DET = 1) if ADC_1 (0x0B) final reading is lower than ACC_DET_TH							

Table 2. Detailed Register Map (continued)

ISRC_ADC 0x0B (Read Only)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	ADC_1							
Reset Value	0	0	0	0	0	0	0	0
ADC_1	ID ADC: 0V to 1.5V Voltage step 5.9mV (typ)							
VBUS_ADC 0x0C (Read Only)								
BIT	7	6	5	4	3	2	1	0
BIT NAME	ADC_2							
Reset Value	0	0	0	0	0	0	0	0
ADC_2	VBUS ADC: 3V to 30V Voltage step 118mV (typ) Write 1 to VBUSADC_EN for one time VBUS ADC							

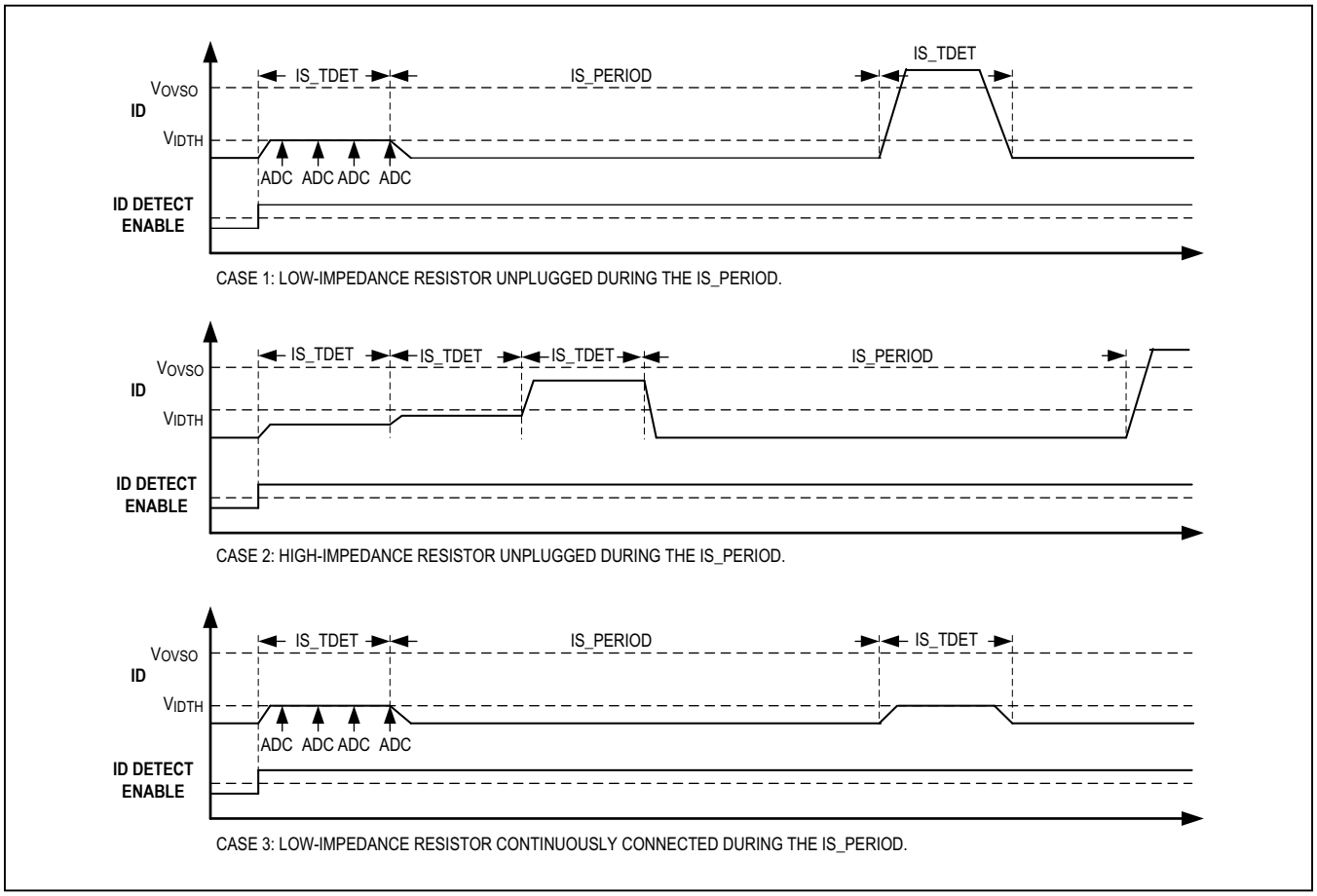


Figure 2. Current Source On-Time Timing Diagram (IS_INIT_SET = 0)

Detailed Description

The MAX20330 features the overvoltage protection to the charger input VBUS line when a travel adapter (TA) is used. The MAX20330 uses the external N-MOSFET with R_{ON} lower than 10mΩ and V_{DS} rating at or higher than +30V. The device protects the battery and low voltage systems against voltage faults up to $40V_{DC}$. The external TVS could be used to further protect the device from surges. If the input voltage exceeds the overvoltage threshold, the external N-FET is disconnected from the input to prevent damage to the protected components. In addition to the OVP controller function, the MAX20330 also provides the accessory ID detection as well as VBUS short detection when the device is not in OVP mode (EN_OVP = 0).

ENb Bit

The MAX20330 is enabled by default. When disabled as VBUS is available, the part will remain enabled sinking current from VBUS.

36VDC (40V Abs Max) Withstanding

The MAX20330 can withstand the DC voltage up to 40V. If 40V input is expected, it is recommended to use the external TVS that clamps the surge to 40V or below.

OVLO

OUT is connected to VBUS when VBUS is between UVLO threshold and OVLO threshold. When VBUS goes above overvoltage lockout threshold (SET_OVLO 0x05), OUT is disconnected from VBUS, the OVLO bit is set high. When VBUS drops below SET_OVLO threshold, the OVLO bit is deasserted and the debounce time starts counting. After the debounce time, OUT follows VBUS again.

UVLO/POR

The VBUS has min operating voltage of 2.7V. The ADC works when V_{CC} voltage is 2.6V or higher. The device disables the external FET unless VBUS is higher than UVLO threshold. When the device is operating with I^2C ENb bit = 0 (default), if the UVLO happens, the device shuts down the switch immediately.

Safe Turn-On Protection

When the switch turns on, if the OUT is below V_{SS_THR} of VBUS after soft start time out, it shuts down the output.

Fast Turn-Off Time

The MAX20330 provides 100ns turn off response time and can switch off an external N-MOSFET.

VBUS ID/Short Detection

The MAX20330 can check the VBUS impedance with automatic scaling for the best resolution using the different current resources. The current source can be turned on only when the OVP function is disabled (EN_OVP = 0). The ID open load voltage is 2V max. When the VBUS is soft shorted to ground, it can be detected and warn the user. Also, VBUS can be actively discharged by I^2C command. This is useful when the OVP IC blocks the VBUS from discharged by the PMIC or by the USB type C controller during power down operation.

Thermal Shutdown

Thermal shutdown circuitry protects the devices from overheating. The switches turn off when the junction temperature exceeds +125°C (typ). The switches turn on again after the device temperature drops by approximately 20°C (typ).

Application Information

I²C Interface

When in I²C mode, the MAX20330 operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX20330 and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX20330 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high-to-low while SCL is high (Figure 4). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

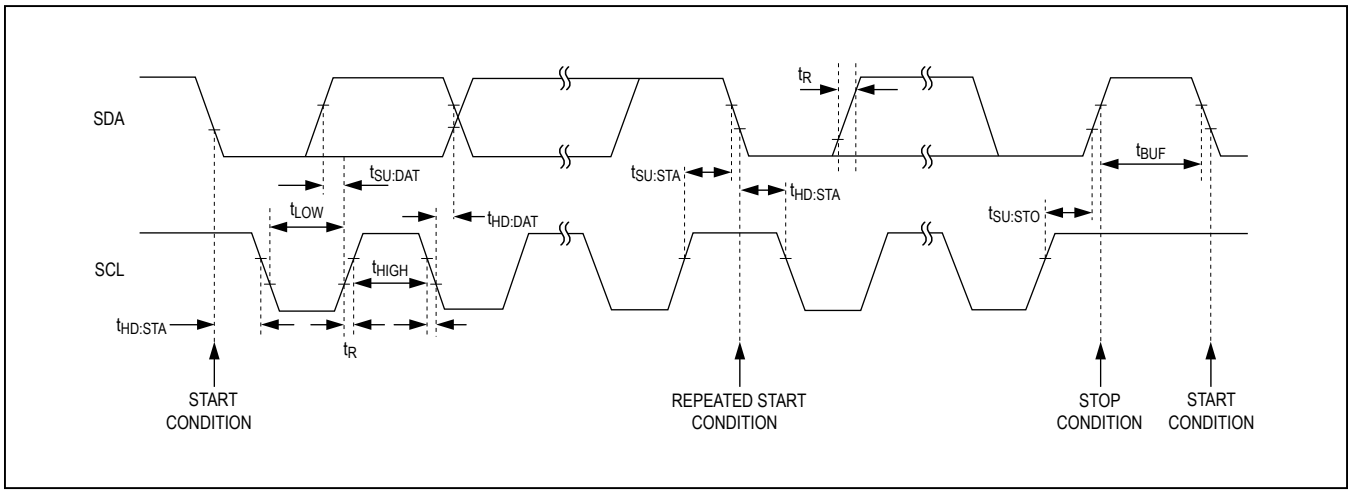


Figure 3. I²C Interface Timing Details

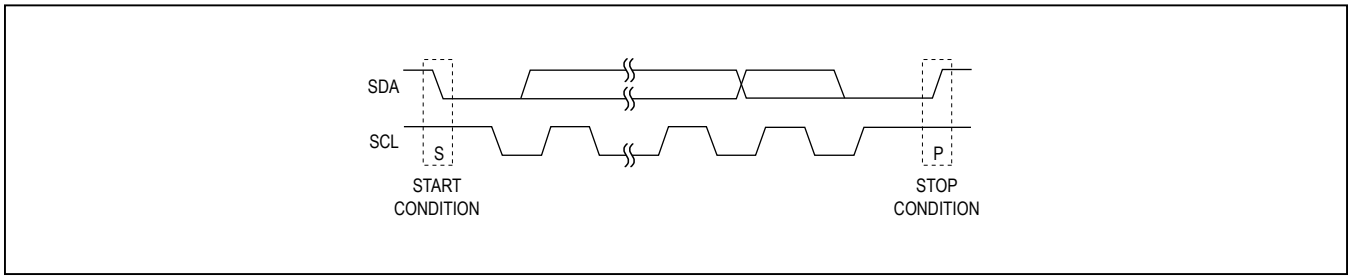


Figure 4. Start and Stop Conditions

Bit Transfer

One data bit is transferred during each clock pulse (Figure 5).The data on SDA must remain stable while SCL is high. Changes in SDA while SCK is high and stable are considered control signals (see *Start and Stop Conditions*)

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 6), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX20330, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the device did not pull SDA low, a not acknowledge is indicated.

Slave Address

The MAX20330 features a 7-bit slave address: 0010 111. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

Bus Reset

The MAX20330 resets the bus with the I^{2}C start condition for reads. When the R/$\overline{W}$ bit is set to 1, the device transmits data to the master, thus the master is reading from the device.

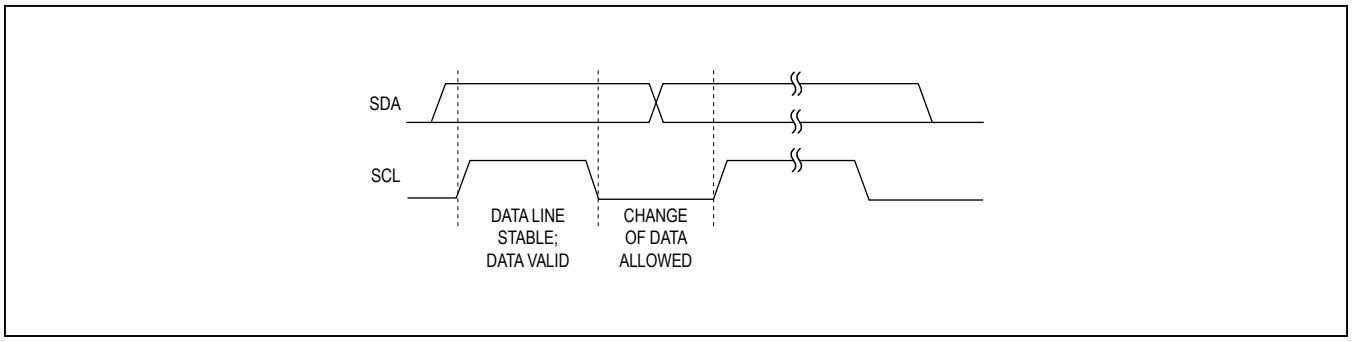


Figure 5. Bit Transfer

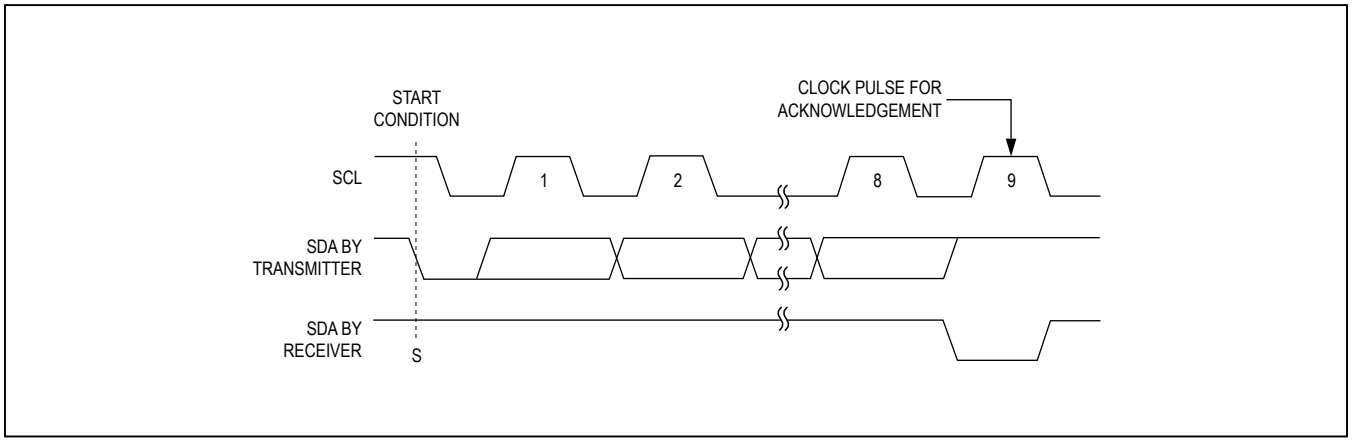


Figure 6. Acknowledge

Format for Writing

A write to the MAX20330 comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, then the device takes no further action beyond storing the register address. Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 7). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrement (Figure 8).

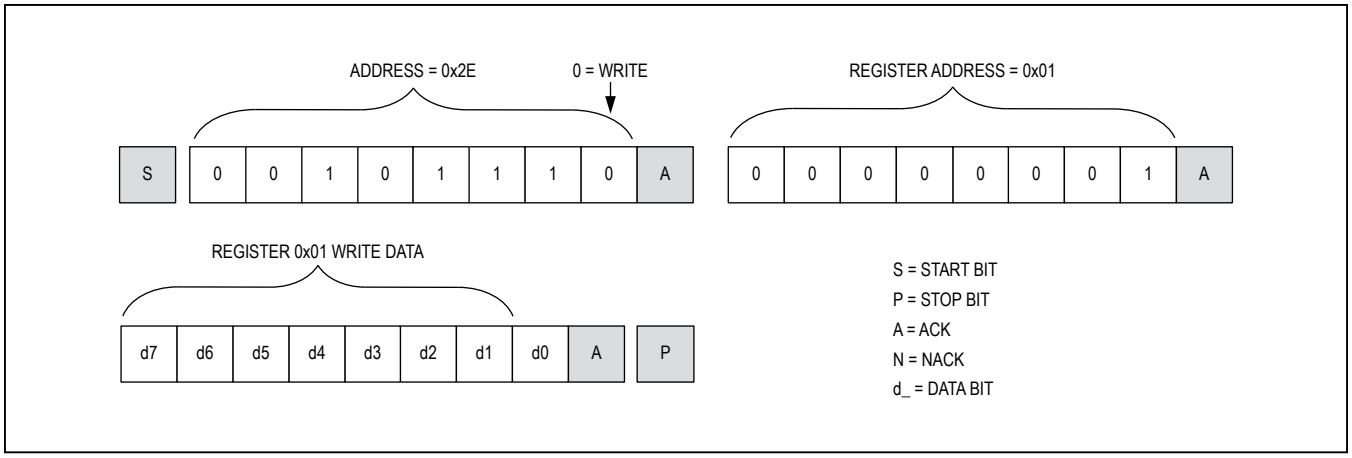


Figure 7. Format for I²C Write

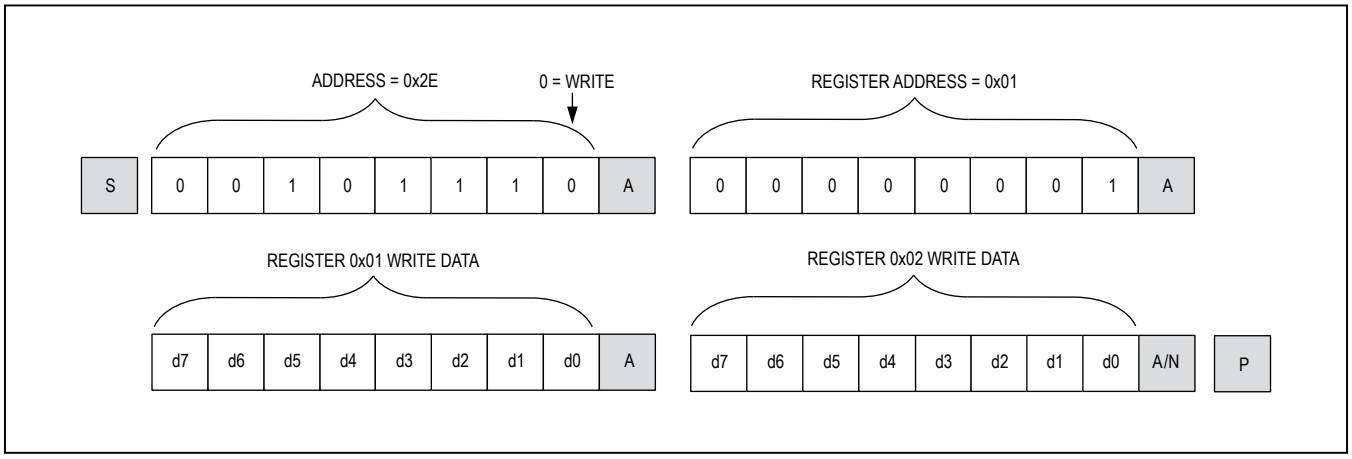


Figure 8. Format for Writing to Multiple Registers

Format for Reading

The MAX20330 is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 9). The master can now read consecutive bytes from the device, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 10). Once the master sounds a NACK, the MAX20330 stops sending valid data.

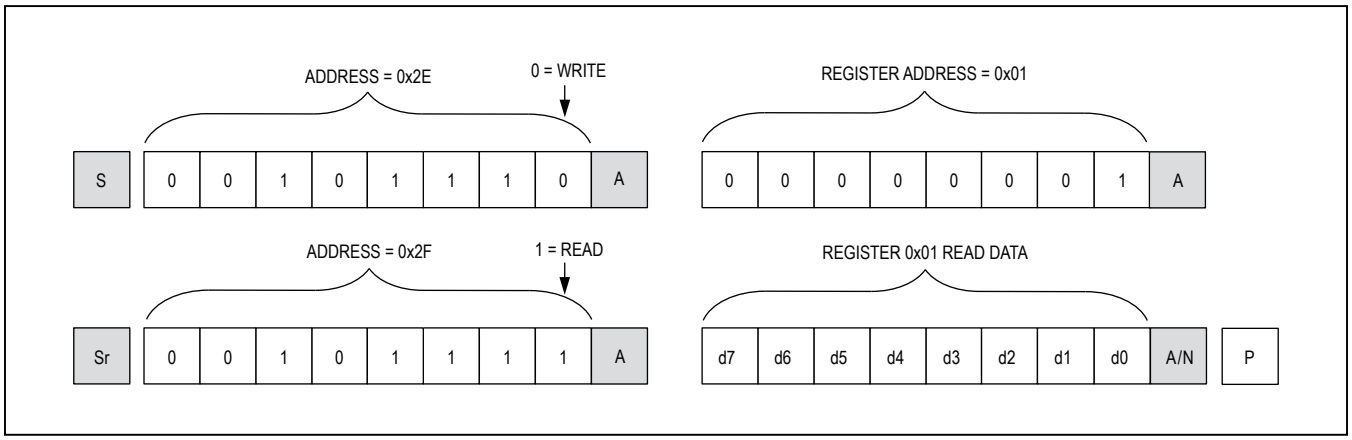


Figure 9. Format for Reads (Repeated Start)

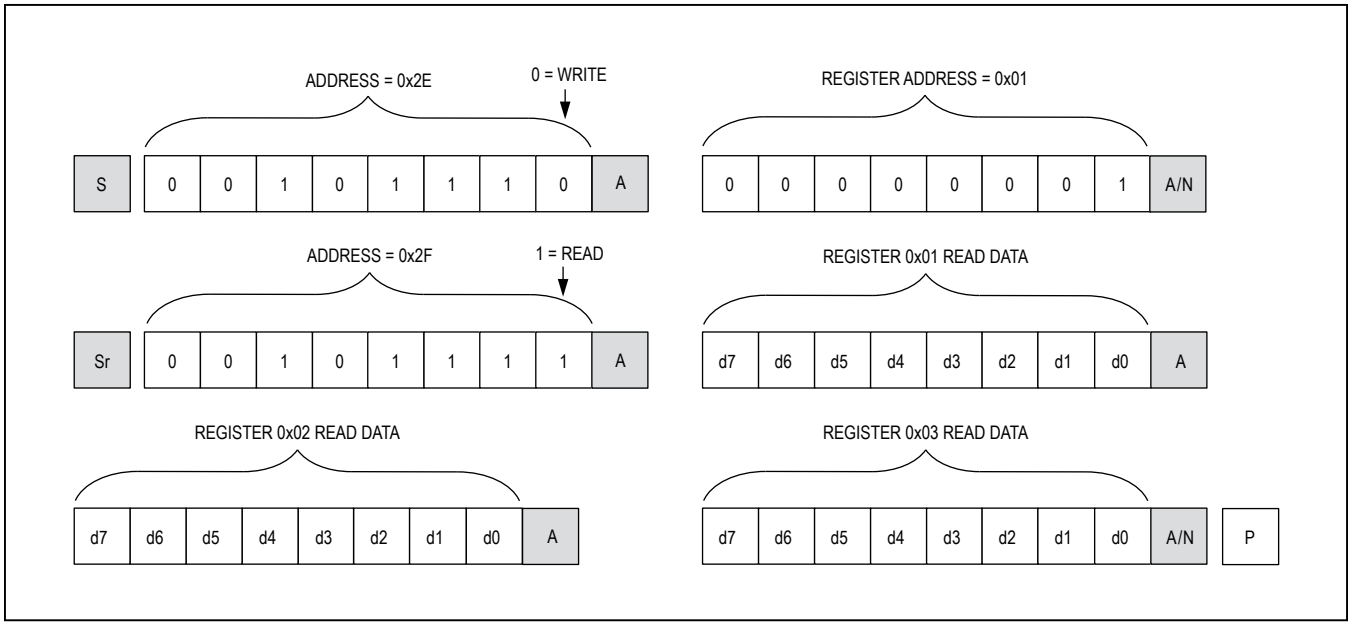
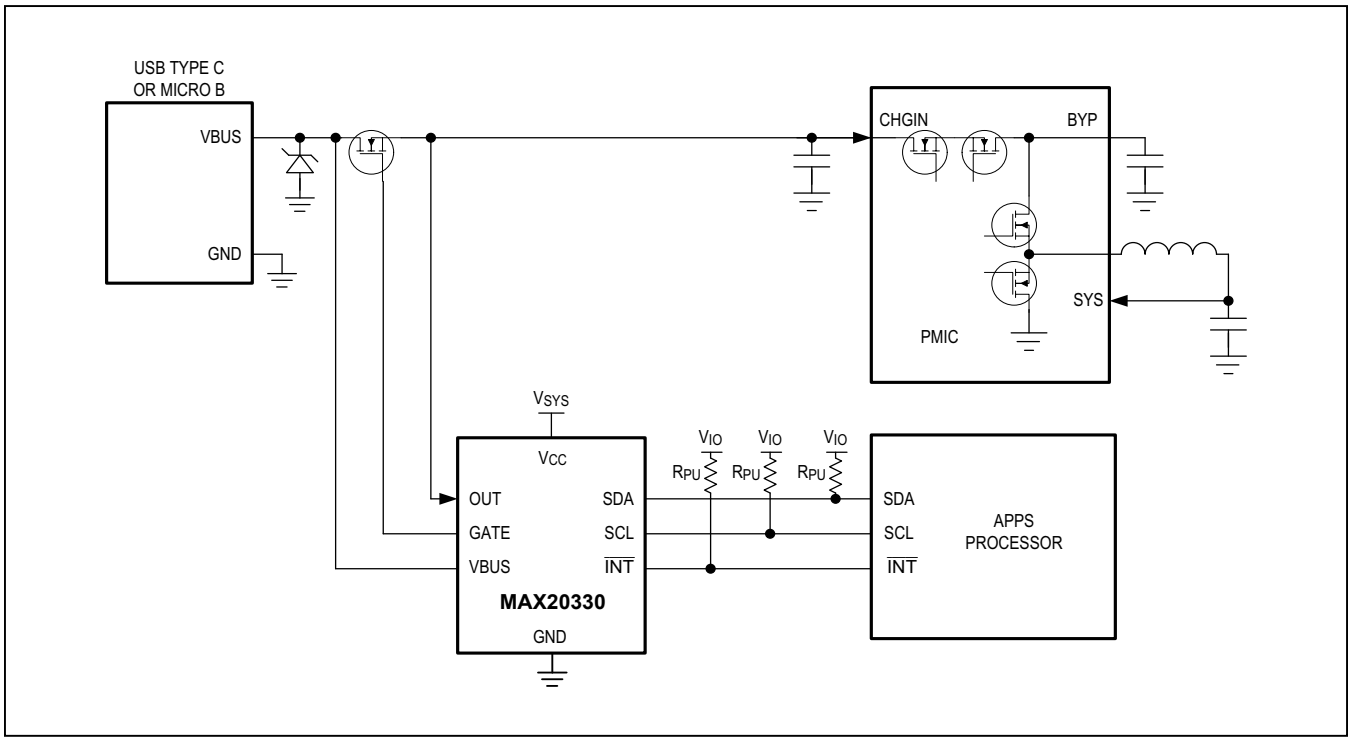
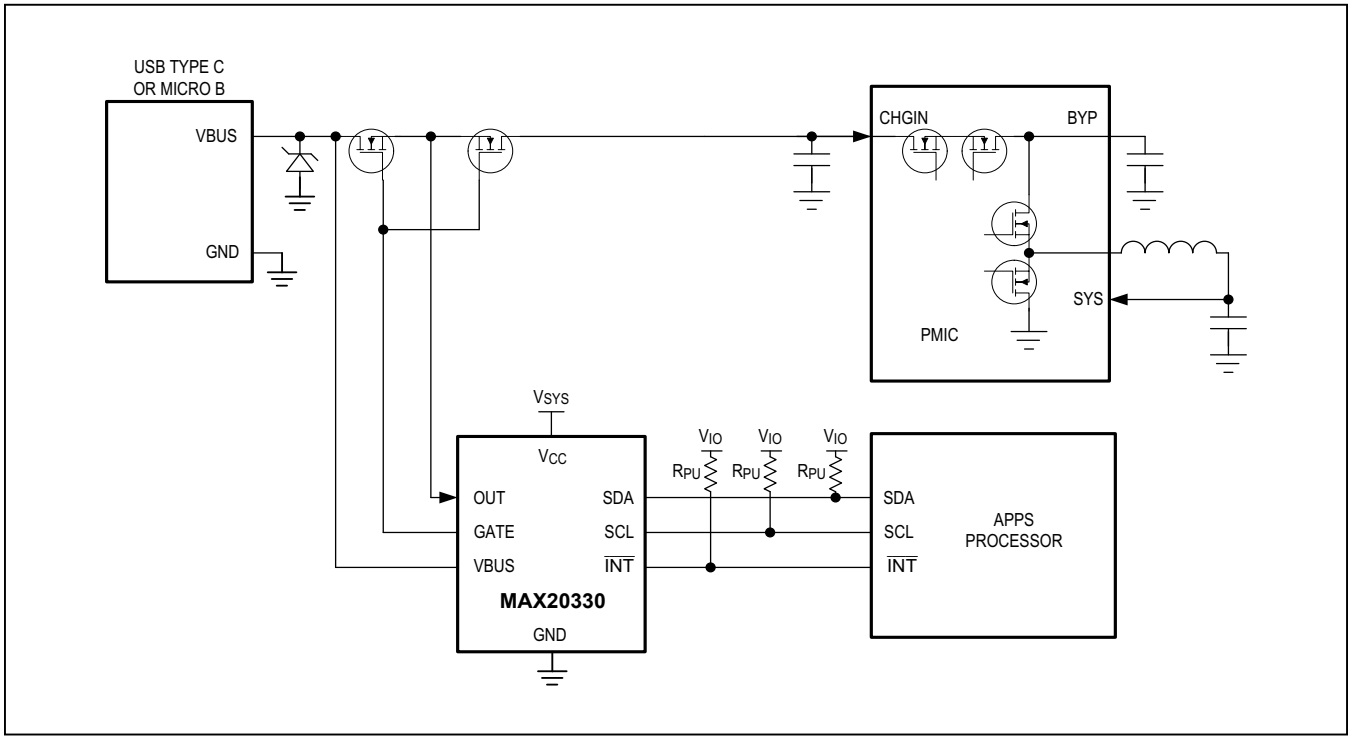


Figure 10. Format for Reading Multiple Registers

Typical Application Circuits





Ordering Information

PART	TOP MARK	TEMP RANGE	PIN-PACKAGE
MAX20330EWA+T	CA	-40°C TO +85°C	8 WLP

+ Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 WLP	W81B1+1	**21-100229**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—

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