Description

The 9ZXL0831E / 9ZXL0851E are second-generation enhanced performance DB800ZL differential buffers. The parts are pin-compatible upgrades to the 9ZXL0831A and 9ZXL0851A, while offering a much improved phase jitter performance. A fixed external feedback maintains low drift for critical QPI/UPI applications.

PCIe Clocking Architectures Supported

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Application

- Servers
- Storage
- Networking
- SSDs

Output Features

- 8 Low-Power (LP) HCSL output pairs (0831E)
- 8 Low-Power (LP) HCSL output pairs with 85Ω Zout (0851E)

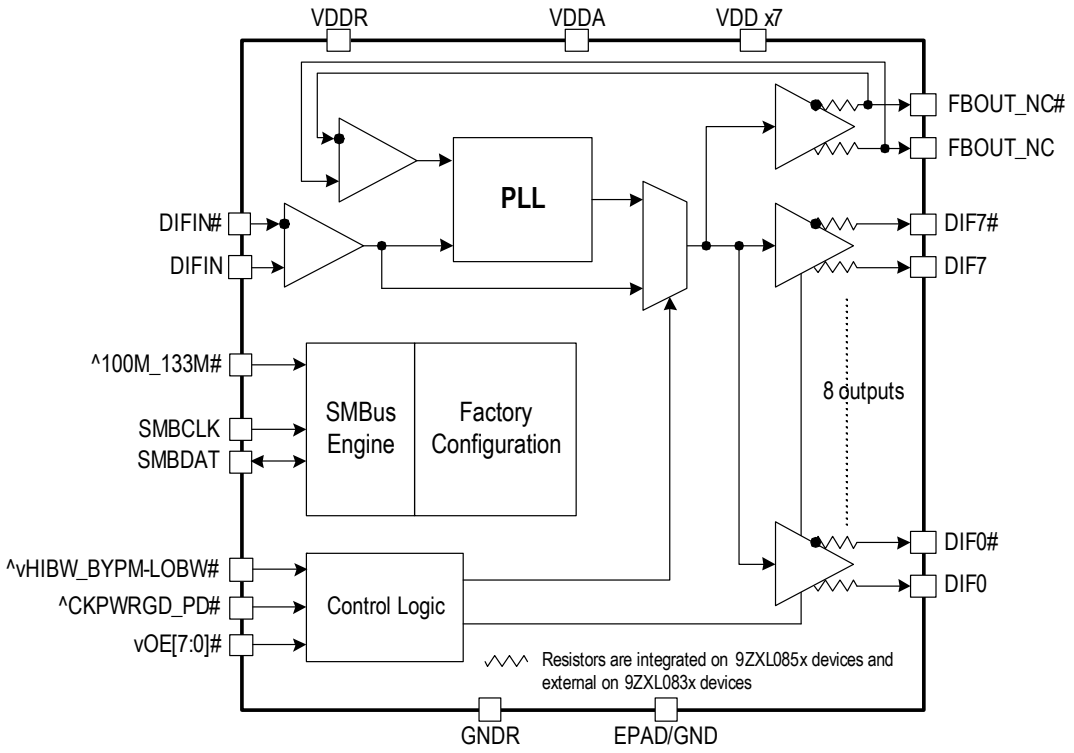
Features

- LP-HCSL outputs; eliminate 16 resistors, save 27mm^2 of area (0831E)
- LP-HCSL outputs with 85Ω Zout; eliminate 32 resistors, save 64mm^2 of area (0851E)
- 8 OE# pins; hardware control of each output
- Selectable PLL BW; minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of PLL bandwidth and bypass; change mode without power cycle
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- 100MHz & 133.33MHz PLL mode; UPI and legacy QPI support
- 6 × 6 mm 48-VFQFPN package; small board footprint

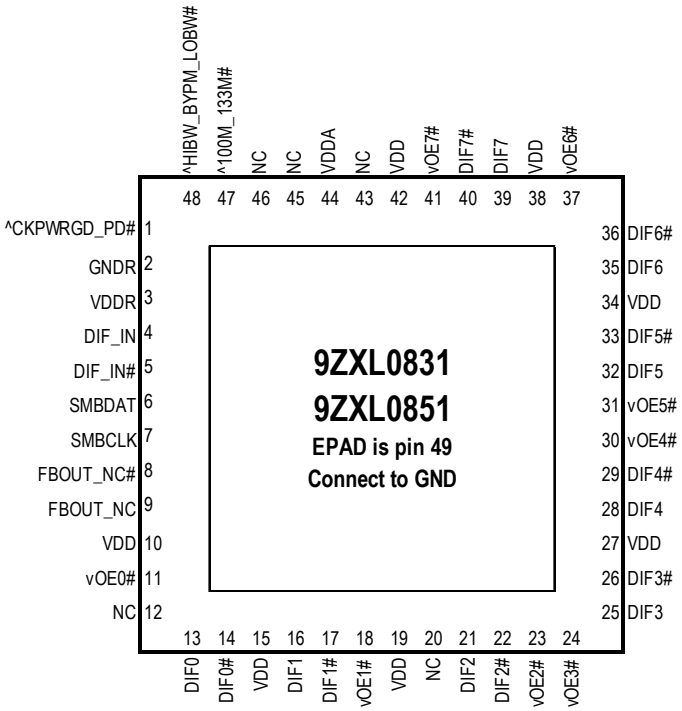
Key Specifications

- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps
- Input-to-output delay: Fixed at 0ps
- Input-to-output delay variation < 50ps
- Phase jitter: PCIe Gen4 < 0.5ps rms
- Phase jitter: QPI/UPI > = 9.6GB/s < 0.2ps rms
- Phase jitter: IF-UPI < 1.0ps rms

Block Diagram



Pin Assignments



48-VFQFPN, 6 x 6 mm, 0.4mm pitch

Power Management Table

CKPWRGD_PD#	DIF_IN	SMBus EN bit	OE[x]#	DIF[x]	PLL State if not in Bypass Mode
0	X	X	X	Low/Low	OFF
1	Running	0	0	Low/Low	ON
		0	1	Low/Low	ON
		1	0	Running	ON
		1	1	Low/Low	ON

PLL Operating Mode Table

HiBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

PLL Operating Mode Readback Table

HiBW_BypM_LoBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

SMBus Address

Address	+ Read/Write bit
1101100	x

Power Connections

Pin Number		Description
VDD	GND	
44	49	Analog PLL
3	2	Analog input
10,15,19, 27,34,38,42	49	DIF clocks

Functionality at Power Up (PLL Mode)

100M_133M#	DIF_IN MHz	DIF[x]
1	100.00	DIF_IN
0	133.33	DIF_IN

Pin Descriptions

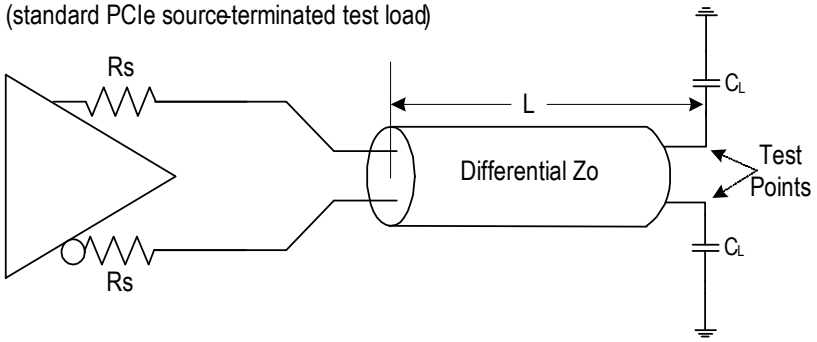
Pin #	Pin Name	Type	Description
1	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
2	GNDR	GND	Analog ground pin for the differential input (receiver).
3	VDDR	PWR	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
4	DIF_IN	IN	HCSL true input.
5	DIF_IN#	IN	HCSL complementary input.
6	SMBDAT	I/O	Data pin of SMBUS circuitry
7	SMBCLK	IN	Clock pin of SMBUS circuitry
8	FBOUT_NC#	OUT	Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
9	FBOUT_NC	OUT	True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
10	VDD	PWR	Power supply, nominally 3.3V.
11	vOE0#	IN	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
12	NC	N/A	No connection.
13	DIF0	OUT	Differential true clock output.
14	DIF0#	OUT	Differential complementary clock output.
15	VDD	PWR	Power supply, nominally 3.3V.
16	DIF1	OUT	Differential true clock output.
17	DIF1#	OUT	Differential complementary clock output.
18	vOE1#	IN	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
19	VDD	PWR	Power supply, nominally 3.3V.
20	NC	N/A	No connection.
21	DIF2	OUT	Differential true clock output.
22	DIF2#	OUT	Differential complementary clock output.
23	vOE2#	IN	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
24	vOE3#	IN	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
25	DIF3	OUT	Differential true clock output.
26	DIF3#	OUT	Differential complementary clock output.
27	VDD	PWR	Power supply, nominally 3.3V.
28	DIF4	OUT	Differential true clock output.
29	DIF4#	OUT	Differential complementary clock output.
30	vOE4#	IN	Active low input for enabling output 4. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
31	vOE5#	IN	Active low input for enabling output 5. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
32	DIF5	OUT	Differential true clock output.
33	DIF5#	OUT	Differential complementary clock output.
34	VDD	PWR	Power supply, nominally 3.3V.
35	DIF6	OUT	Differential true clock output.
36	DIF6#	OUT	Differential complementary clock output.
37	vOE6#	IN	Active low input for enabling output 6. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
38	VDD	PWR	Power supply, nominally 3.3V.

Pin Descriptions (cont.)

Pin #	Pin Name	Type	Description
39	DIF7	OUT	Differential true clock output.
40	DIF7#	OUT	Differential complementary clock output.
41	vOE7#	IN	Active low input for enabling output 7. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.
42	VDD	PWR	Power supply, nominally 3.3V.
43	NC	N/A	No connection.
44	VDDA	PWR	Power supply for PLL core.
45	NC	N/A	No connection.
46	NC	N/A	No connection.
47	^100M_133M#	LATCHED IN	3.3V Input to select operating frequency. This pin has an internal 120kohm pull-up resistor. See Functionality Table for definition.
48	^HIBW_BYPM_LOBW#	LATCHED IN	Tri-level input to select High BW, Bypass or Low BW Mode. Has an internal 120kohm pull up resistor. See PLL Operating Mode Table for details.
49	EPAD	PWR	Ground

Test Loads

Low-Power HCSL Output Test Load
(standard PCIe source-terminated test load)



Parameters for Low-Power HCSL Output Test Load

Device	Rs (Ω)	Zo (Ω)	L (Inches)	CL (pF)
9ZXL083x	27	85	10	2
	33	100	10	2
9ZXL085x*	Internal	85	10	2
	7.5	100	10	2

*Contact factory for versions of this device with Zo=100Ω

Alternate Terminations

The LP-HCSL output can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for termination schemes for LVPECL, LVDS, CML and SSTL.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL0831E / 9ZXL0851E. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx				3.9	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5	V	1,3
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD Protection	ESD prot	Human Body Model	2500			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 3.9V.

Electrical Characteristics–DIF_IN Clock Input Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage - DIF_IN	V_{CROSS}	Cross over voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	µA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–SMBus

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	at I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	at V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max V_{IL} - 0.15V) to (Min V_{IH} + 0.15V)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min V_{IH} + 0.15V) to (Max V_{IL} - 0.15V)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			500	kHz	5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

Electrical Characteristics–Input/Supply/Common Output Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
VDDx	Supply Voltage	Supply voltage for core and analog	3.135	3.3	3.465	V	
VDDIO	Output Supply Voltage	Supply voltage for DIF outputs, if present	0.9975	1.05	3.465	V	
T_{AMB}	Ambient Operating Temperature	Industrial range (T_{IND})	-40	25	85	°C	
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus, tri-level inputs	2		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus, tri-level inputs	GND - 0.3		0.8	V	
V_{IH}	Input High Voltage	Tri-level inputs	2.2		V_{DD} + 0.3	V	
V_{IL}	Input Mid Voltage	Tri-level inputs	1.2	VDD/2	1.8	V	
V_{IL}	Input Low Voltage	Tri-level inputs	GND - 0.3		0.8	V	
I_{IN}	Input Current	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}	-5		5	µA	
I_{INP}		Single-ended inputs V_{IN} = 0 V; inputs with internal pull-up resistors V_{IN} = V_{DD}; inputs with internal pull-down resistors	-50		50	µA	
F_{ibyp}	Input Frequency	V_{DD} = 3.3 V, Bypass Mode	1		400	MHz	
F_{ipll}		V_{DD} = 3.3 V, 100MHz PLL Mode	98.5	100.00	102.5	MHz	
F_{ipll}		V_{DD} = 3.3 V, 133.33MHz PLL Mode	132	133.33	135	MHz	
L_{pin}	Pin Inductance				7	nH	1
C_{IN}	Capacitance	Logic inputs, except DIF_IN	1.5		5	pF	1
C_{INDIF_IN}		DIF_IN differential clock inputs	1.5		2.7	pF	1,4
C_{OUT}		Output pin capacitance			6	pF	1
T_{STAB}	Clk Stabilization	From V_{DD} power-up and after input clock stabilization or de-assertion of PD# to 1st clock		1.0	1.8	ms	1,2
$f_{MODINPCIe}$	Input SS Modulation Frequency PCIe	Allowable frequency for PCIe applications (Triangular modulation)	30		33	kHz	
$t_{LATOE\#}$	OE# Latency	DIF start after OE# assertion DIF stop after OE# deassertion	4	5	10	clocks	1,2,3
t_{DRVPD}	Tdrive_PD#	DIF output enable after PD# de-assertion		49	300	µs	1,3
t_F	Tfall	Fall time of control inputs			5	ns	2
t_R	Trise	Rise time of control inputs			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

Electrical Characteristics–Current Consumption

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
I_{DDA}	Operating Supply Current	V_{DDA}, PLL Mode at 100MHz		37	45	mA	1
I_{DD}	Operating Supply Current	All other V_{DD} pins at 100MHz		55	68	mA	
I_{DDAPD}	Powerdown Current	V_{DDA}, CKPWRGD_PD# = 0		3	4	mA	1
I_{DDPD}	Powerdown Current	All other V_{DD} pins, CKPWRGD_PD# = 0		1	2	mA	

[1.] Includes VDDR if applicable.

Electrical Characteristics–HCSL/LP-HCSL Outputs

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
dV/dt	Slew Rate	Scope averaging on.	2	2.9	4	1 – 4	V/ns	1, 2, 3
ΔdV/dt	Slew Rate Matching	Single-ended measurement.		7.1	20	20	%	1, 4, 7
Vmax	Max Voltage	Measurement on single-ended signal using absolute value (scope averaging off).	660	792	850	1150	mV	7
Vmin	Min Voltage		-150	-35	150	-300		7
Vcross_abs	Crossing Voltage (abs)	Scope averaging off.	250	372	550	250 – 550	mV	1, 5, 7
Δ-Vcross	Crossing Voltage (var)	Scope averaging off.		15	140	140	mV	1, 6, 7

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Electrical Characteristics–Skew and Differential Jitter Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units	Notes
t_{SPO_PLL}	CLK_IN, DIF[x:0]	Input-to-output skew in PLL Mode at 100MHz, nominal temperature and voltage	-100	-21.3	100	ps	1,2,4,5,8
t_{PD_BYP}	CLK_IN, DIF[x:0]	Input-to-output skew in Bypass Mode at 100MHz, nominal temperature and voltage	2	2.6	4	ns	1,2,3,5,8
t_{DSPO_PLL}	CLK_IN, DIF[x:0]	Input-to-output skew variation in PLL Mode at 100MHz, across voltage and temperature	-50	0.0	50	ps	1,2,3,5,8
t_{DSPO_BYP}	CLK_IN, DIF[x:0]	Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T_{AMB} = 0 to 70°C	-250		250	ps	1,2,3,5,8
		Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T_{AMB} = -40°C to 105°C	-350		350	ps	1,2,3,5,8
t_{DTE}	CLK_IN, DIF[x:0]	Random differential tracking error between two 9ZX devices in Hi BW Mode		3	5	ps (rms)	1,2,3,5,8
t_{DSSTE}	CLK_IN, DIF[x:0]	Random differential spread spectrum tracking error between two 9ZX devices in Hi BW Mode		23	50	ps	1,2,3,5,8
t_{SKEW_ALL}	DIF[x:0]	Output-to-output skew across all outputs, common to PLL and Bypass Mode, at 100MHz			50	ps	1,2,3,8
$j_{peak\text{-}hibw}$	PLL Jitter Peaking	LOBW#_BYPASS_HIBW = 1	0	1.3	2.5	dB	7,8
$j_{peak\text{-}lobw}$	PLL Jitter Peaking	LOBW#_BYPASS_HIBW = 0	0	1.3	2	dB	7,8
pll_{HIBW}	PLL Bandwidth	LOBW#_BYPASS_HIBW = 1	2	2.6	4	MHz	8,9
pll_{LOBW}	PLL Bandwidth	LOBW#_BYPASS_HIBW = 0	0.7	1.0	1.4	MHz	8,9
t_{DC}	Duty Cycle	Measured differentially, PLL Mode	45	50.3	55	%	1
t_{DCD}	Duty Cycle Distortion	Measured differentially, Bypass Mode at 100MHz	-1	0	1	%	1,10
$t_{jcyc\text{-}cyc}$	Jitter, Cycle to Cycle	PLL Mode		14	50	ps	1,11
		Additive jitter in Bypass Mode		0.1	5	ps	1,11

Notes for preceding table:

[1] Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device.

[5] Measured with scope averaging on to find mean value.

[6] t is the period of the input clock.

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform.

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
$t_{jphPCIeG1-CC}$	Phase Jitter, PLL Mode	PCIe Gen 1		13.4	30	86	ps (p-p)	1, 2, 3
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)		0.2	0.7	3	ps (rms)	1, 2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)		1.0	1.5	3.1	ps (rms)	1, 2
$t_{jphPCIeG3-CC}$		PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.2	0.4	1	ps (rms)	1, 2
$t_{jphPCIeG4-CC}$		PCIe Gen 4 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.2	0.4	0.5	ps (rms)	1, 2
$t_{jphPCIeG1-CC}$	Additive Phase Jitter, Bypass mode	PCIe Gen 1		0.01	0.06	Not Applicable	ps (p-p)	1, 2, 3, 4
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)		0.01	0.06		ps (rms)	1, 2, 3, 4
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz)		0.01	0.06		ps (rms)	1, 2, 3, 4
$t_{jphPCIeG3-CC}$		PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.01	0.06		ps (rms)	1, 2, 3, 4
$t_{jphPCIeG4-CC}$		PCIe Gen 4 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.01	0.06		ps (rms)	1, 2, 3, 4

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Independent Reference (IR) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Industry Limit	Units	Notes
$t_{jphPCIeG2-SRIS}$	Phase Jitter, PLL Mode	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.9	1.1	2	ps (rms)	1, 2, 5
$t_{jphPCIeG3-SRIS}$		PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.6	0.65	0.7	ps (rms)	1, 2, 5
$t_{jphPCIeG2-SRIS}$	Additive Phase Jitter, Bypass mode	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.01	0.05	Not Applicable	ps (rms)	2, 4, 5
$t_{jphPCIeG3-SRIS}$		PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.01	0.05		ps (rms)	2, 4, 5

Notes for PCIe Filtered Phase Jitter tables (CC) and (IR)

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel-supplied Clock Jitter Tool, when driven by 9SQL495x or equivalent with spread on and off.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] For RMS values, additive jitter is calculated by solving for b [$b = sqrt(c^2 - a^2)$], where "a" is rms input jitter and "c" is rms total jitter.

[5] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev 4.0 version 0.7 draft, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates.

Electrical Characteristics–Filtered Phase Jitter Parameters - QPI/UPI

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
t_{jphQPI_UPI}	Phase Jitter, PLL Mode	QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.14	0.30	0.5	ps (rms)	1, 2
		QPI & UPI (100MHz, 8.0Gb/s, 12UI)		0.07	0.13	0.3	ps (rms)	1, 2
		QPI & UPI (100MHz, ?9.6Gb/s, 12UI)		0.06	0.1	0.2	ps (rms)	1, 2
$t_{jphIF-UPI}$		IF-UPI		0.1 0.17	0.14 0.2	1	ps (rms)	1, 4, 5
t_{jphQPI_UPI}	*Additive* Phase Jitter, Bypass mode	QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.0	0.01	Not Applicable	ps (rms)	1, 2, 3
		QPI & UPI (100MHz, 8.0Gb/s, 12UI)		0.0	0.01		ps (rms)	1, 2, 3
		QPI & UPI (100MHz, ?9.6Gb/s, 12UI)		0.0	0.01		ps (rms)	1, 2, 3
$t_{jphIF-UPI}$		IF-UPI		0.06	0.07		ps (rms)	1, 4

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel-supplied Clock Jitter Tool, when driven by 9SQL495x or equivalent with spread on and off.

[3] For RMS values, additive jitter is calculated by solving for b [$b = sqrt(c^2 - a^2)$], where "a" is rms input jitter and "c" is rms total jitter.

[4] Calculated from phase noise analyzer when driven by Wenzel Associates source with Intel-specified brick-wall filter applied.

[5] Top number is when the buffer is in Low BW mode, bottom number is when the buffer is in High BW mode.

Electrical Characteristics–Unfiltered Phase Jitter Parameters - 12kHz to 20MHz

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Industry Limit	Units	Notes
$t_{jph12k-20MHi}$	Phase Jitter, PLL Mode	PLL High BW, SSC OFF, 100MHz		171	225	Not Applicable	fs (rms)	1, 2
$t_{jph12k-20MLo}$	Phase Jitter, PLL Mode	PLL Low BW, SSC OFF, 100MHz		184	225		fs (rms)	1, 2
$t_{jph12k-20MByp}$	*Additive* Phase Jitter, Bypass Mode	Bypass Mode, SSC OFF, 100MHz		107	125		fs (rms)	1, 2, 3

[1] Applies to all outputs when driven by Wenzel Associates source.

[2] 12kHz to 20MHz brick wall filter.

[3] For RMS values, additive jitter is calculated by solving for b [$b = sqrt(c^2 - a^2)$], where "a" is rms input jitter and "c" is rms total jitter.

Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Frequency MHz	Measurement Window							Units	Notes
		1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1 Clock		
		-c2c jitter AbsPer Minimum	-SSC Short-Term Average Minimum	- ppm Long-Term Average Minimum	0 ppm Period Nominal	+ ppm Long-Term Average Maximum	+SSC Short-Term Average Maximum	+c2c jitter AbsPer Maximum		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3
	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2,4

Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Frequency MHz	Measurement Window							Units	Notes
		1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1 Clock		
		-c2c jitter AbsPer Minimum	-SSC Short-Term Average Minimum	- ppm Long-Term Average Minimum	0 ppm Period Nominal	+ ppm Long-Term Average Maximum	+SSC Short-Term Average Maximum	+c2c jitter AbsPer Maximum		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3
	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2,4

Notes:

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (+/-100ppm). The buffer itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, 100MHz PLL Mode or Bypass Mode.

[4] Driven by CPU output of main clock, 133MHz PLL Mode or Bypass Mode.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: PLL Mode and Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	48	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latch
Bit 6	48	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latch
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2		PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode Readback Table		1
Bit 1		PLL Mode 0	PLL Operating Mode 1	RW			1
Bit 0	47	100M_133M#	Frequency Select Readback	R	133MHz	100MHz	Latch

Note: Setting bit 3 to '1' allows the user to override the latch value from pin 5 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. If the user changes these bits, a warm reset of the system will have to be accomplished.

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	32/33	DIF_5_En	Output Enable	RW	Low/Low	OE# Pin Control	1
Bit 6	28/29	DIF_4_En	Output Enable	RW			1
Bit 5	25/26	DIF_3_En	Output Enable	RW			1
Bit 4	21/22	DIF_2_En	Output Enable	RW			1
Bit 3		Reserved					0
Bit 2	16/17	DIF_1_En	Output Enable	RW	Low/Low	OE# Pin Control	1
Bit 1	13/14	DIF_0_En	Output Enable	RW			1
Bit 0		Reserved					0

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2	39/40	DIF_7_En	Output Enable	RW	Low/Low	OE# Pin Control	1
Bit 1		Reserved					0
Bit 0	35/36	DIF_6_En	Output Enable	RW	Low/Low	OE# Pin Control	1

SMBus Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBus Table: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBus Table: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	E rev = 0100		0
Bit 6	-	RID2		R			1
Bit 5	-	RID1		R			0
Bit 4	-	RID0		R			0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	0831 is E5 Hex 0851 is F5 Hex		1
Bit 6	-	Device ID 6		R			1
Bit 5	-	Device ID 5		R			1
Bit 4	-	Device ID 4		R			x
Bit 3	-	Device ID 3		R			x
Bit 2	-	Device ID 2		R			x
Bit 1	-	Device ID 1		R			x
Bit 0	-	Device ID 0		R			x

SMBus Table: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	-	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			0

SMBus Table: Reserved Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

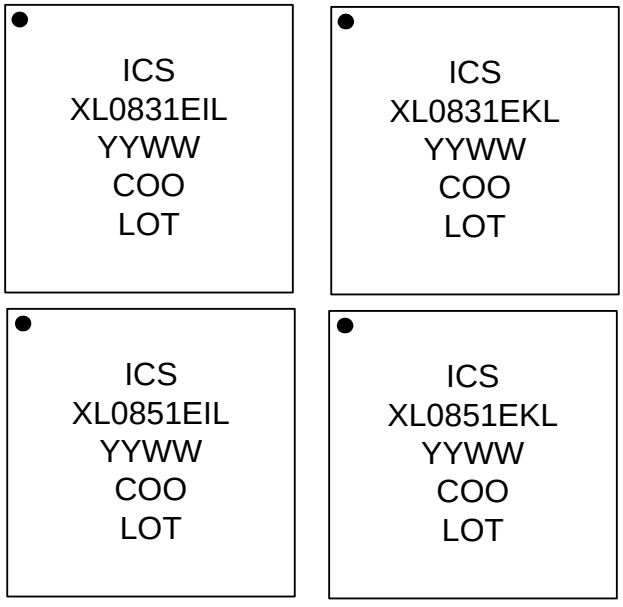
www.idt.com/document/psc/ndndg-48-package-outline-60-x-60-mm-body-040-mm-pitch-qfn-epad-size-420-x-420-mm

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
9ZXL0831EKILF	6 x 6 mm, 0.40mm pitch 48-VFQFPN	Tray	-40° to +85°C
9ZXL0831EKILFT	6 x 6 mm, 0.40mm pitch 48-VFQFPN	Reel	-40° to +85°C
9ZXL0851EKILF	6 x 6 mm, 0.40mm pitch 48-VFQFPN	Tray	-40° to +85°C
9ZXL0851EKILFT	6 x 6 mm, 0.40mm pitch 48-VFQFPN	Reel	-40° to +85°C
9ZXL0831EKKLF	6 x 6 mm, 0.40mm pitch 48-VFQFPN	Tray	-40° to +105°C
9ZXL0831EKKLFT	6 x 6 mm, 0.40mm pitch 48-VFQFPN	Reel	-40° to +105°C
9ZXL0851EKKLF	6 x 6 mm, 0.40mm pitch 48-VFQFPN	Tray	-40° to +105°C
9ZXL0851EKKLFT	6 x 6 mm, 0.40mm pitch 48-VFQFPN	Reel	-40° to +105°C

“LF” designates PB-free configuration, RoHS compliant.
“E” is the device revision designator (will not correlate with the datasheet revision).

Marking Diagrams



1. “I” denotes industrial temperature range
2. “K” denotes extended temperature range.
3. “L” denotes RoHS compliant package.
4. “YYWW” denotes the last two digits of the year and week the part was assembled.
5. “COO” denotes country of origin.
6. “LOT” denotes the lot number.

Revision History

Revision Date	Description of Change
August 14, 2018	Updated block diagram.
July 17, 2018	Corrected typos in Byte 1, bits 1 and 2.
April 12, 2018	Updated absolute maximum supply voltage rating and VIHSMB to 3.9V.
December 1, 2017	Removed “5V tolerant” reference in pins 6 and 7 descriptions.
September 29, 2017	Initial release.

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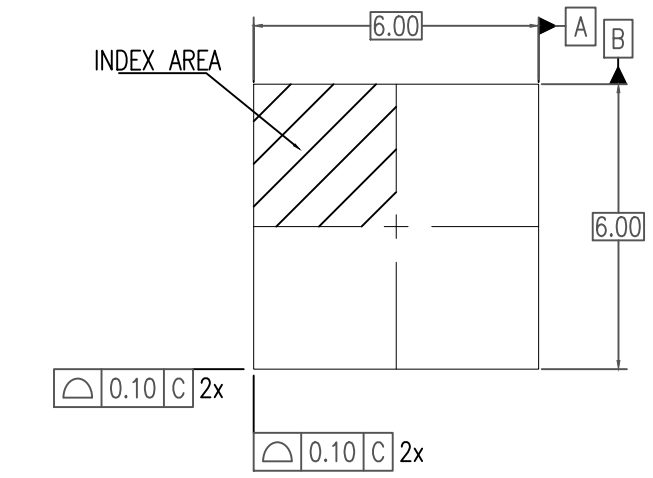
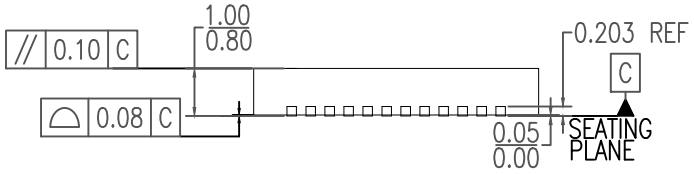
48-VFQFPN Package Outline Drawing

6.0 x 6.0 x 0.90 mm Body, Epad 4.2 x 4.2 mm, 0.40mm Pitch

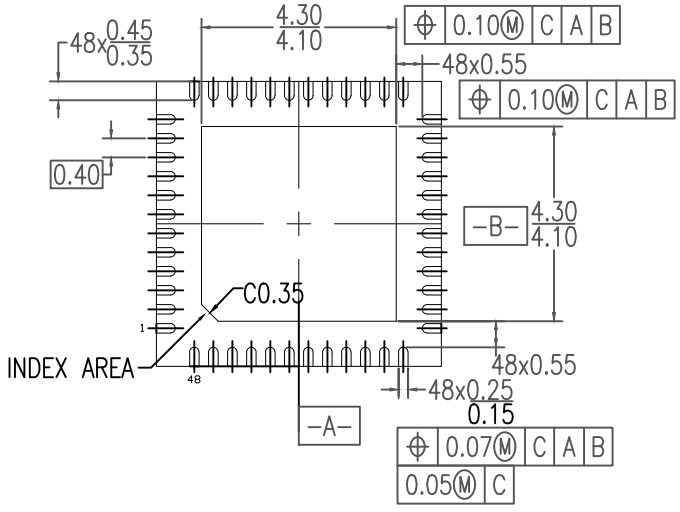
NDG48P2, PSC-4212-02, Rev 02, Page 1



TOP VIEW



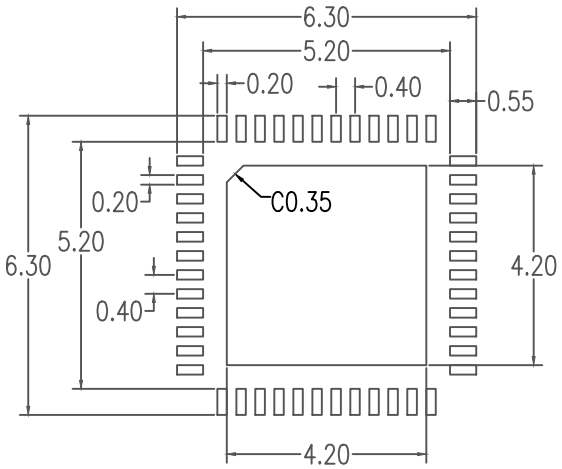
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
July 24, 2018	Rev 02	New Format Change QFN to VFQFPN, Recalculate Land Pattern
Sept 9, 2014	Rev 01	Add Chamfer