SLG46170

GreenPAK
Programmable Mixed-signal Matrix

Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8V (±5%) to 5V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 14-pin STQFN: 2 x 2.2 x 0.55 mm, 0.4 mm pit

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

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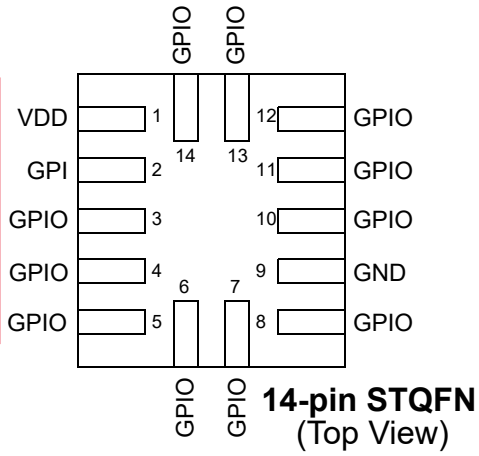
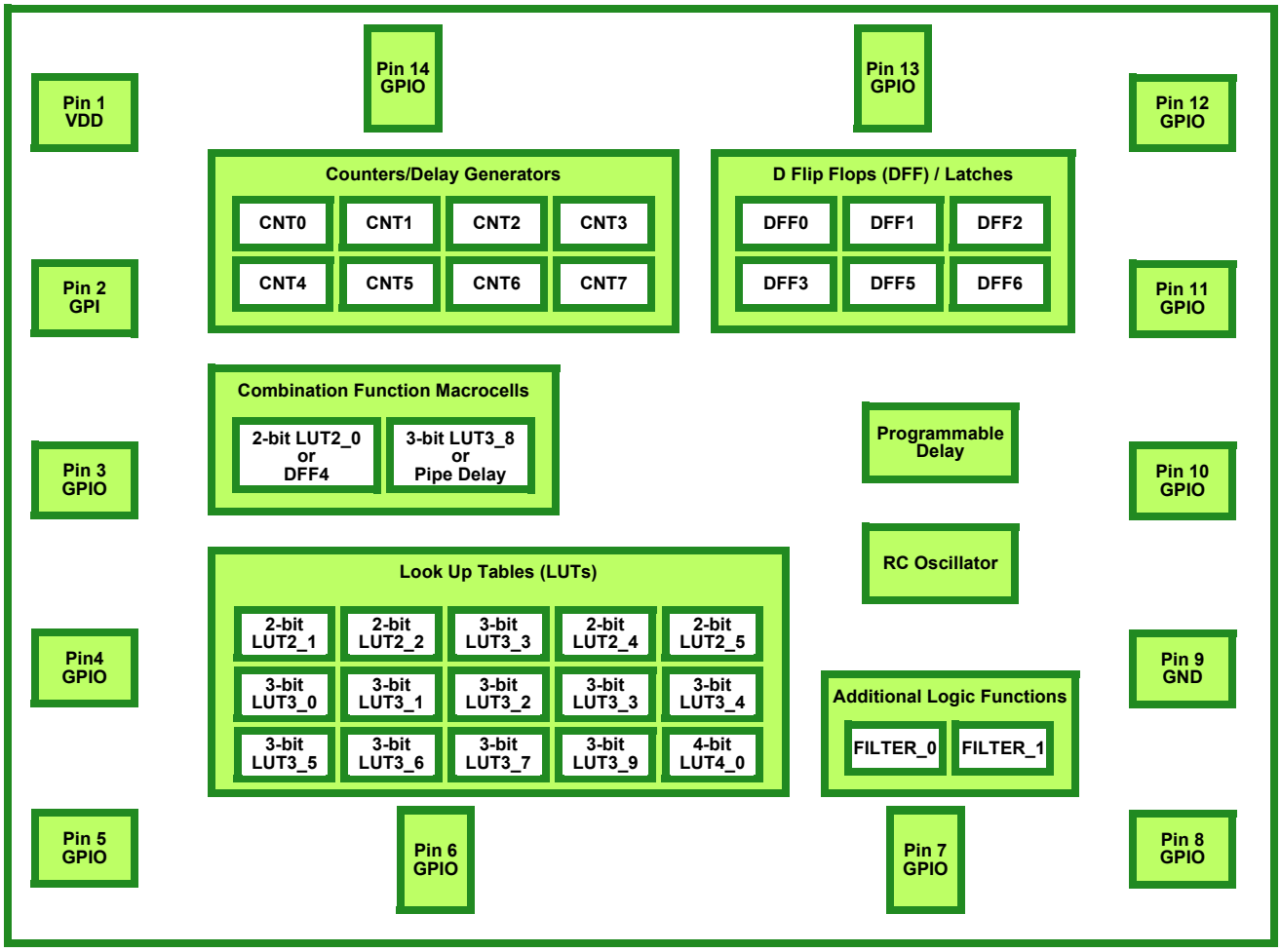
Pin Configuration



14-pin STQFN
(Top View)

Block Diagram



1.0 Overview

The SLG46170 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46170. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- Fifteen Combinatorial Look Up Tables (LUTs)
  - Five 2-bit LUTs
  - Nine 3-bit LUTs
  - One 4-bit LUT
- Two Combination Function Macrocells
  - One Selectable FF/Latch or 2-bit LUT
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 16 stage / 3 output
- Eight Counter / Delay Generators (CNT/DLY)
  - One 14-bit delay/counter
  - One 14-bit delay/counter with external clock/reset
  - Four 8-bit delays/counters
  - Two 8-bit delays/counters with external clock/reset
- Six D Flip-Flop / Latches (DFF)
- Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Functions – 2 Deglitch Filters
- RC Oscillator (RC OSC)

2.0 Pin Description

2.1 Functional and Programming Pin Description

Pin #	Pin Name	Function	Programming Function
1	VDD	Power Supply	Power Supply
2	GPI	General Purpose Input	V_{PP} (Programming Voltage)
3	GPIO	General Purpose I/O	N/A
4	GPIO	General Purpose I/O	N/A
5	GPIO	General Purpose I/O	N/A
6	GPIO	General Purpose I/O	N/A
7	GPIO	General Purpose I/O	N/A
8	GPIO	General Purpose I/O	N/A
9	GND	Ground	Ground
10	GPIO	General Purpose I/O	Programming Mode Control
11	GPIO	General Purpose I/O	Programming ID Pin
12	GPIO	General Purpose I/O	Programming SDIO Pin
13	GPIO	General Purpose I/O	Programming SRDWB Pin
14	GPIO	General Purpose I/O or External Clock	Programming SCL Pin

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46170's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

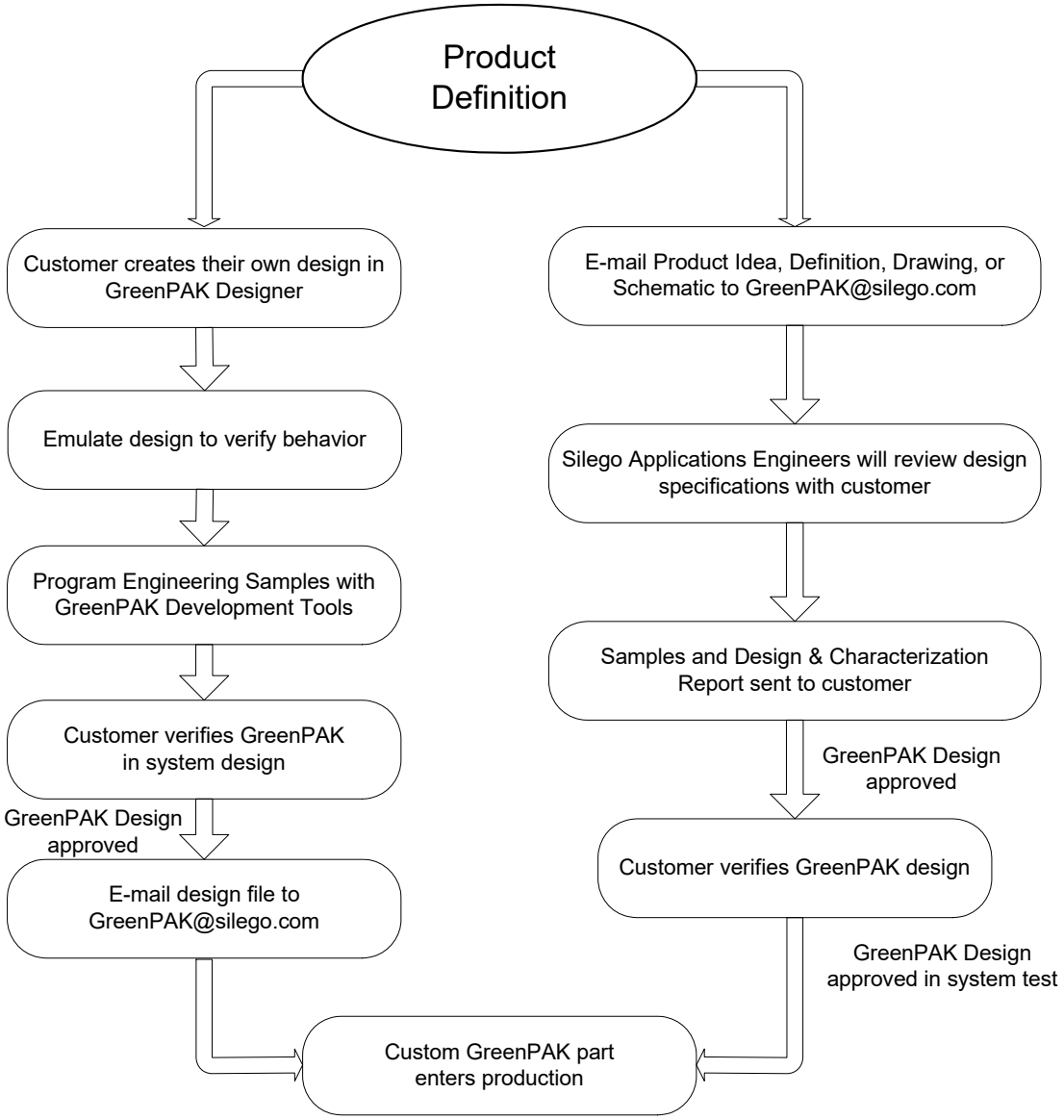


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46170V	14-pin STQFN
SLG46170VTR	14-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
	OD 1x	--	8	
	OD 2x	--	12	
	OD 4x	--	25	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8 V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	--	V
		Logic Input with Schmitt Trigger	1.270	--	--	V
		Low-Level Logic Input	0.980	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.690	1.789	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.794	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.008	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.004	0.010	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.005	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.003	0.010	V
		Open Drain NMOS 4X, I_{OL}= 100 µA	--	0.003	0.004	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD} - 0.2$	1.066	1.703	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD} - 0.2$	2.216	3.406	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.917	1.689	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.834	3.378	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.375	2.534	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	2.750	5.068	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.15 V	5.500	10.136	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.096	1.353	1.528	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.759	0.933	1.125	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	--	V
		Logic Input with Schmitt Trigger	2.130	--	--	V
		Low-Level Logic Input	1.130	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.735	3.120	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.870	3.210	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.130	0.228	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.060	0.108	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.080	0.147	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.040	0.080	V
		Open Drain NMOS 4X, I_{OL}= 3 mA	--	0.027	0.034	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	6.045	12.080	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.522	24.160	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.875	8.244	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	9.750	16.488	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	7.313	12.370	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	14.541	24.740	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.4 V	25.801	49.480	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.096	1.353	1.528	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.759	0.933	1.125	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.4 Electrical Characteristics (5 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.640	--	--	V
		Logic Input with Schmitt Trigger	3.160	--	--	V
		Low-Level Logic Input	1.230	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
I_{LGK}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.190	4.780	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.320	4.890	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.157	0.270	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.076	0.130	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.102	0.180	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.051	0.110	V
		Open Drain NMOS 4X, I_{OL}= 5 mA	--	0.035	0.045	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	22.080	34.040	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	41.690	68.080	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	7.215	11.580	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	13.831	23.160	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	10.820	17.380	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	17.343	34.760	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.4 V	30.964	69.520	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.096	1.353	1.528	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.759	0.933	1.125	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent	0.5	0.8	1.0	µA
		OSC 25 kHz, predivide = 1	3.2	5.1	7.3	µA
		OSC 25 kHz, predivide = 8	3.0	4.4	6.0	µA
		OSC 2 MHz, predivide = 1	38.5	78.2	136.2	µA
		OSC 2 MHz, predivide = 8	18.3	25.7	35.5	µA

5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital input to PP 1X	42	45	17	19	12	13	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	42	43	16	17	18	12	ns
tpd	Delay	Low Voltage Digital input to PP 1X	45	428	17	177	12	120	ns
tpd	Delay	Digital input to PMOS	42	-	17	-	12	-	ns
tpd	Delay	Digital input to NMOS	-	80	-	27	-	18	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	53	-	21	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	50	-	20	-	14	-	ns
tpd	Delay	LUT2bit(LATCH)	34	33	14	13	10	9	ns
tpd	Delay	LATCH(LUT2bit)	30	34	14	13	10	9	ns
tpd	Delay	LUT3bit(LATCH)	38	37	18	15	13	10	ns
tpd	Delay	LATCH+nRESET(LUT3bit)	45	42	21	17	15	12	ns
tpd	Delay	LUT4bit	28	33	14	13	10	9	ns
tpd	Delay	LUT2bt	19	26	10	10	7	7	ns
tpd	Delay	LUT3bit	28	34	14	13	10	9	ns
tpd	Delay	CNT/DLY	40	38	18	15	13	11	ns
tpd	Delay	P_DLY1C	380	377	166	163	123	120	ns
tpd	Delay	P_DLY2C	720	718	314	312	233	231	ns
tpd	Delay	P_DLY3C	1061	1060	462	460	343	341	ns
tpd	Delay	P_DLY4C	1396	1400	609	609	451	451	ns
tpd	Delay	Filter	200	200	78	78	53	53	ns
tpd	Delay	ACMP (5mV across inputs)	3000	3000	2000	2000	2000	2000	ns
tw	width	I/O with 1X push pull (min transmitted)	20	20	20	20	20	20	ns
tw	width	filter (min transmitted)	150	150	55	55	35	35	ns

5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
offset	25kHz	auto	19	14	12	µs
offset	2MHz	auto	7	4	4	µs
frequency settling time	25kHz	auto	19	14	12	µs

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
frequency settling time	2MHz	auto	14	14	14	µs
variable (CLK period)	25kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25kHz/2MHz	either	35	14	10	ns

5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay (typical).

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
time1	Width, 1 cell	mode:(any)edge detect, edge detect output	325	150	110	ns
time1	Width, 2 cell	mode:(any)edge detect, edge detect output	740	300	225	ns
time1	Width, 3 cell	mode:(any)edge detect, edge detect output	1020	450	340	ns
time1	Width, 4 cell	mode:(any)edge detect, edge detect output	1350	600	450	ns
time2	Delay, 1 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 2 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 3 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 4 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time1	Width, 1 cell	mode: delayed (any)edge detect, delayed edge detect output	340	150	110	ns
time1	Width, 2 cell	mode: delayed (any)edge detect, delayed edge detect output	670	300	220	ns
time1	Width, 3 cell	mode: delayed (any)edge detect, delayed edge detect output	1000	450	335	ns
time1	Width, 4 cell	mode: delayed (any)edge detect, delayed edge detect output	1340	600	450	ns
time2	Delay, 1 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 2 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 3 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 4 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	382	375	126	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	713	169	237	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	1045	318	350	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1370	466	460	ns
time2	Delay, 1 cell	mode: both edge delay, delayed edge detect output	900	613	250	ns
time2	Delay, 2 cell	mode: both edge delay, delayed edge detect output	1250	520	360	ns
time2	Delay, 3 cell	mode: both edge delay, delayed edge detect output	1600	680	480	ns
time2	Delay, 4 cell	mode: both edge delay, delayed edge detect output	1900	815	600	ns

5.9 Typical Pulse Width Performance

Table 5. Typical Pulse Width Performance.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width for Filter 0 and Filter 1	< 150	< 55	< 35	ns

5.10 OSC Specifications

Table 6. 25 kHz RC OSC frequency limits at T = 25 °C

Power Supply Range (VDD) V	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	24.069	25.960
3.3 V ±10%	24.397	25.620
5 V ±10%	24.048	25.962
2.5 V ... 4.5 V	24.214	25.868
1.71 V… 5.5 V	23.703	27.515

Table 7. 25 kHz RC OSC frequency error (error calculated relative to nominal value) at T = 25 °C

Power Supply Range (VDD) V	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-3.73%	3.84%
3.3 V ±10%	-2.41%	2.48%
5 V ±10%	-3.81%	3.85%
2.5 V ... 4.5 V	-3.14%	3.47%
1.71 V… 5.5 V	-5.19%	10.06%

5.10.1 2 MHz RC Oscillator

Table 8. 2 MHz RC OSC frequency limits at T = 25 °C

Power Supply Range (VDD) V	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.855	2.133
3.3 V ±10%	1.911	2.089
5 V ±10%	1.873	2.130
2.5 V ... 4.5 V	1.894	2.110
1.71 V… 5.5 V	1.760	2.164

Table 9. 2 MHz RC OSC frequency error (error calculated relative to nominal value) at T = 25 °C

Power Supply Range (VDD) V	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-7.25%	6.67%
3.3 V ±10%	-4.44%	4.43%
5 V ±10%	-6.33%	6.50%
2.5 V ... 4.5 V	-5.28%	5.52%
1.71 V… 5.5 V	-12.00%	8.19%

5.10.2 OSC Power On delay

Table 10. Oscillators Power On delay at T=(-40..+85) °C, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On"

Power Supply Range (VDD) V	RC OSC 2 MHz		RC OSC 25 kHz	
	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs
1.71	8.80	12.78	19.34	24.22
1.80	8.26	12.07	18.80	24.37
1.89	7.76	11.47	18.28	23.99
2.50	5.76	8.57	15.45	19.91
2.70	5.42	7.86	14.64	18.85
3.00	5.10	7.24	13.58	17.80
3.30	4.90	7.14	12.52	16.96
3.60	4.79	7.22	11.36	16.20
4.20	4.69	7.33	9.58	12.69
4.50	4.66	7.22	8.83	11.51
5.00	4.60	7.12	7.69	9.79
5.50	4.54	7.00	6.75	8.45

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs
- Push Pull Outputs
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- 40 mA Open Drain 4X Drive output

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Combinational Logic Look Up Tables (LUTs – 15 total)

- Five 2-bit Lookup Tables
- Nine 3-bit Lookup Tables
- One 4-bit Lookup Tables

6.4 Combination Function Macrocell (2 total)

- One Selectable FF/Latch or 2-bit LUT
- One Selectable Pipe Delay or 3-bit LUT

6.5 Delays/Counters (8 total)

- Two 14-bit delay/counters: Range 1-16384 clock cycles
- Four 8-bit delays/counters: Range 1-255 clock cycles
- Two 8-bit delays/counters with external clock/reset: Range 1-255 clock cycles

6.6 Digital Storage Elements (6 total)

- Six D Flip-Flops or Latches

6.7 Pipe Delay (Part of Combination Function Macrocell)

- 16 stage / 3 output
- One 1 stage fixed output
- Two 1-16 stage selectable outputs.

6.8 Programmable Delay

- 150 ns/300 ns/450 ns /600 ns @ 3.3 V
- Includes Edge Detection function

6.9 Additional Logic Functions (2 total)

- Two Deglitch filter macrocells

6.10 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First stage divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider (5): OSC/1, OSC/4, selectable (OSC/8, OSC/12, OSC/24, or OSC/64), OSC/3, and additional OSC/3 (from selectable output)

7.0 I/O Pins

The SLG46170 has a total of 12 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Normal Mode pin definitions are as follows:

- Pin 2: general purpose input
- Pin 3: general purpose input or output
- Pin 4: general purpose input or output
- Pin 5: general purpose input or output
- Pin 6: general purpose input or output
- Pin 7: general purpose input or output
- Pin 8: general purpose input or output
- Pin 10: general purpose input or output
- Pin 11: general purpose input or output
- Pin 12: general purpose input or output
- Pin 13: general purpose input or output
- Pin 14: general purpose input or output or external clock

Programming Mode pin definitions are as follows;

- Pin 1: Vdd power supply
- Pin 2: Vpp programming voltage
- Pin 9: ground
- Pin 10: programming mode control
- Pin 11: programming ID pin
- Pin 12: programming SDIO pin
- Pin 13: programming SRDWB pin
- Pin 14: programming SCL pin

Of the 12 user defined I/O pins on the SLG46170, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input.

7.2 Output Modes

Pins 3, 4, 5, 6, 7, 8, 10, 11, 12, 13 and 14 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 11. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	<845:844>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	<847:846>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 12. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	<857:855>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 3 Pull Up/Down Resistor Value Selection	<859:858>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	<860>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 3 Driver Strength Selection	<861>	0: 1X 1: 2X

7.4.3 PIN 4 Register Settings

Table 13. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control	<864:862>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 4 Pull Up/Down Resistor Value Selection	<866:865>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	<867>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 4 Driver Strength Selection	<868>	0: 1X 1: 2X

7.4.4 PIN 5 Register Settings

Table 14. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Mode Control	<871:869>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 5 Pull Up/Down Resistor Value Selection	<873:872>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull Up/Down Resistor Selection	<874>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 5 Driver Strength Selection	<875>	0: 1X 1: 2X

7.4.5 PIN 6 Register Settings

Table 15. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control	<878:876>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 6 Pull Up/Down Resistor Value Selection	<880:879>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	<881>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 6 Driver Strength Selection	<882>	0: 1X 1: 2X

7.4.6 PIN 7 Register Settings

Table 16. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Mode Control	<892:890>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 7 Pull Up/Down Resistor Value Selection	<894:893>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 7 Pull Up/Down Resistor Selection	<895>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 7 Driver Strength Selection	<896>	0: 1X 1: 2X

7.4.7 PIN 8 Register Settings

Table 17. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control	<899:897>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 8 Pull Up/Down Resistor Value Selection	<901:900>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	<902>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	<903>	0: 1X 1: 2X
PIN 8 4X Drive (4X, NMOS Open Drain) Selection	<904>	0: 4X Drive Off 1: 4X Drive On (if <897:899> = '101')

7.4.8 PIN 10 Register Settings

Table 18. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control	<936:934>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 10 Pull Up/Down Resistor Value Selection	<938:937>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	<939>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 10 Driver Strength Selection	<940>	0: 1X 1: 2X

7.4.9 PIN 11 Register Settings

Table 19. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Mode Control	<943:941>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 11 Pull Up/Down Resistor Value Selection	<945:944>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 11 Pull Up/Down Resistor Selection	<946>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 11 Driver Strength Selection	<947>	0: 1X 1: 2X

7.4.10 PIN 12 Register Settings

Table 20. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control	<950:948>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 12 Pull Up/Down Resistor Value Selection	<952:951>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull Up/Down Resistor Selection	<953>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 12 Driver Strength Selection	<954>	0: 1X 1: 2X

7.4.11 PIN 13 Register Settings

Table 21. PIN 13 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 13 Mode Control	<957:955>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 13 Pull Up/Down Resistor Value Selection	<959:958>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 13 Pull Up/Down Resistor Selection	<960>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 13 Driver Strength Selection	<961>	0: 1X 1: 2X

7.4.12 PIN 14 Register Settings

Table 22. PIN 14 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 14 Mode Control	<964:962>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 14 Pull Up/Down Resistor Value Selection	<966:965>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 14 Pull Up/Down Resistor Selection	<967>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 14 Driver Strength Selection	<968>	0: 1X 1: 2X

7.5 GPI IO Structure

7.5.1 GPI IO Structure (for Pin 2)

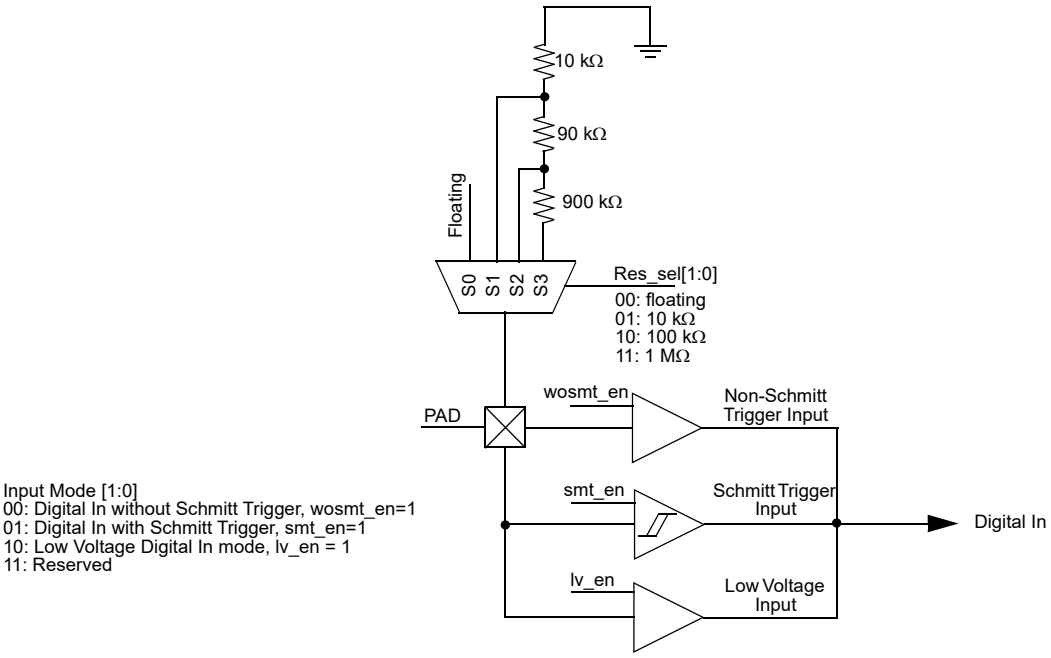


Figure 2. PIN 2 GPI IO Structure Diagram

7.6 Register OE IO Structure

7.6.1 Register OE IO Structure (for Pins 3, 4, 5, 6, 7, 10, 11, 12, 13, 14)

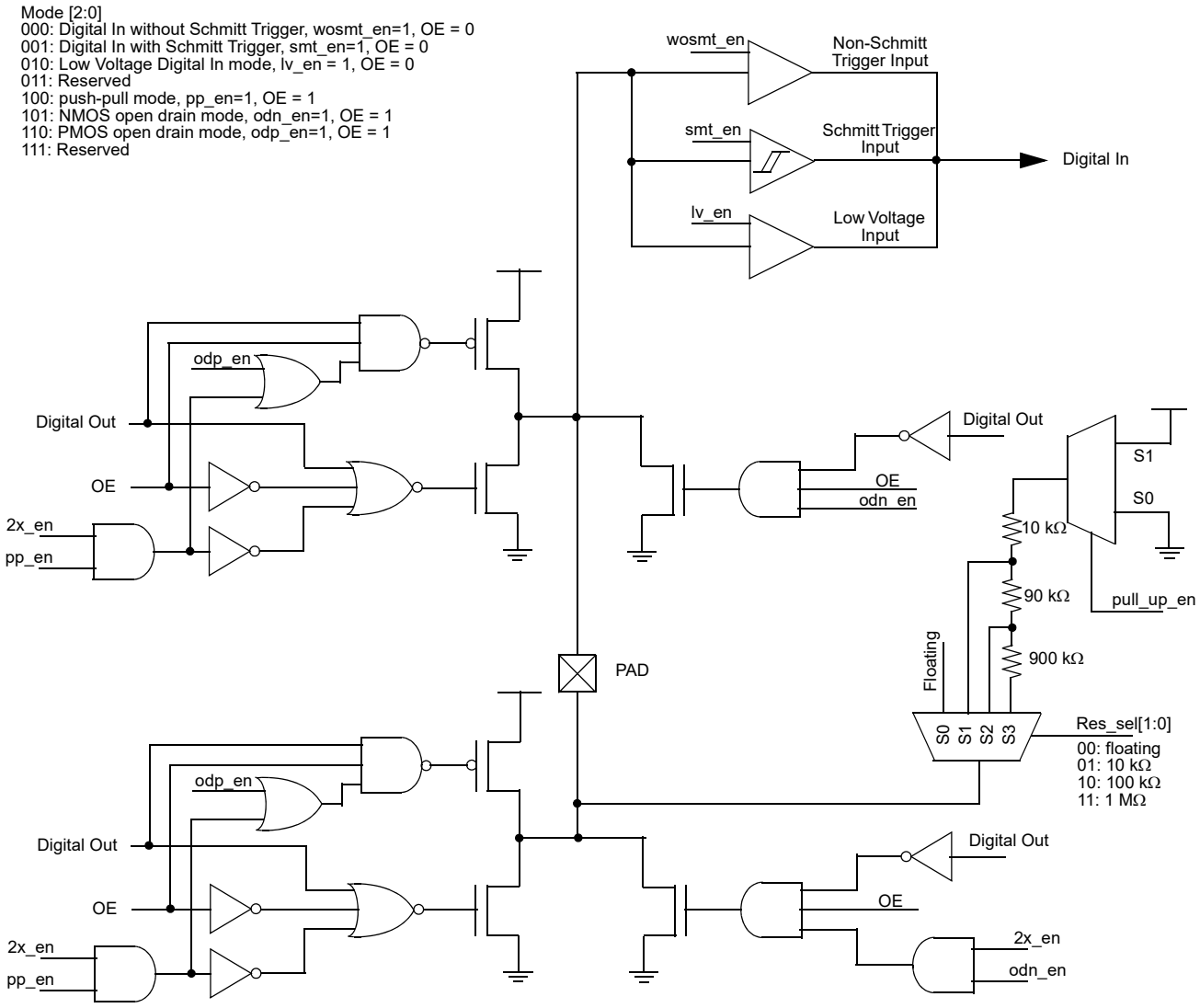


Figure 3. Register OE IO Structure Diagram

7.7 Register OE IO Structure with 4X Drive

7.7.1 Register OE IO Structure with 4X Drive (for Pin 8)

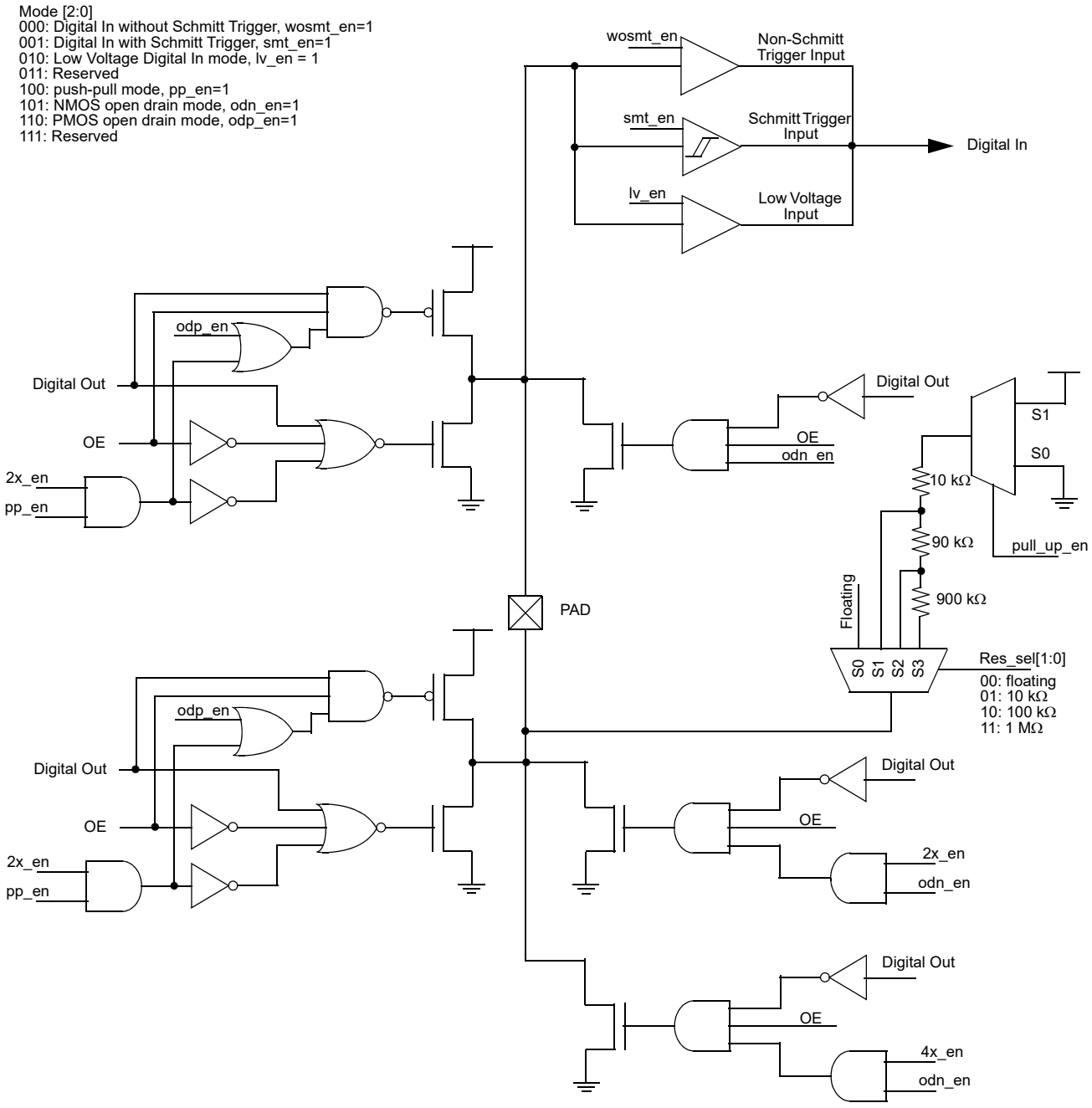


Figure 4. Register OE IO with 4X Drive Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46170 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46170 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 1024 register bits within the SLG46170 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 95 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including I/O pins, LUTs, other digital resources and V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

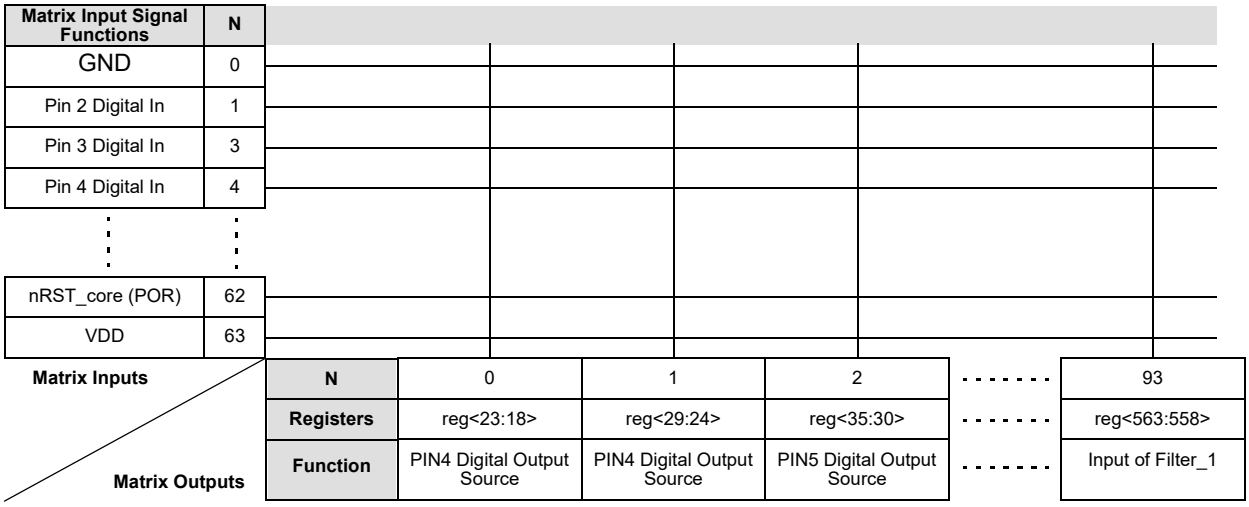


Figure 5. Connection Matrix

8.1 Matrix Input Table

Table 23. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	pin2 digital Input	0	0	0	0	0	1
2	Reserved	0	0	0	0	1	0
3	pin3 digital Input	0	0	0	0	1	1
4	pin4 digital Input	0	0	0	1	0	0
5	pin5 digital Input	0	0	0	1	0	1
6	pin6 digital Input	0	0	0	1	1	0
7	Reserved	0	0	0	1	1	1
8	pin7 digital Input	0	0	1	0	0	0
9	pin8 digital Input	0	0	1	0	0	1
10	counter/delay_0 output 14 bit	0	0	1	0	1	0
11	counter/delay_1 output 14 bit w/ ext CK and reset	0	0	1	0	1	1
12	counter/delay_2 output 8 bit w/ ext CK and reset	0	0	1	1	0	0
13	counter/delay_3 output 8 bit w/ ext CK and reset	0	0	1	1	0	1
14	counter/delay_4 output 8 bit	0	0	1	1	1	0
15	counter/delay_5 output 8 bit	0	0	1	1	1	1
16	counter/delay_6 output 8 bit	0	1	0	0	0	0
17	counter/delay _7 output 14 bit	0	1	0	0	0	1
18	DFF/LATCH_0 Q output with nRST or nSET	0	1	0	0	1	0
19	DFF/LATCH_0 nQ output with nRST or nSET	0	1	0	0	1	1
20	DFF/LATCH_1 output with nRST or nSET	0	1	0	1	0	0
21	DFF/LATCH_2 output with nRST or nSET	0	1	0	1	0	1
22	DFF/LATCH_3 output with nRST or nSET	0	1	0	1	1	0
23	DFF/LATCH_5 output	0	1	0	1	1	1
24	DFF/LATCH_6 output	0	1	1	0	0	0
25	LUT4_0 output	0	1	1	0	0	1
26	LUT3_0 output	0	1	1	0	1	0
27	LUT3_1 output	0	1	1	0	1	1
28	LUT3_2 output	0	1	1	1	0	0
29	LUT3_3 output	0	1	1	1	0	1
30	LUT3_4 output	0	1	1	1	1	0
31	LUT3_5 output	0	1	1	1	1	1
32	LUT3_6 output	1	0	0	0	0	0
33	LUT3_7 output	1	0	0	0	0	1
34	LUT3_8 output (1st stage pipe 1 delay output)	1	0	0	0	1	0
35	LUT3_9 output	1	0	0	0	1	1

Table 23. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
36	LUT2_0 output (DFF/LATCH_4 output)	1	0	0	1	0	0
37	LUT2_1 output	1	0	0	1	0	1
38	LUT2_2 output	1	0	0	1	1	0
39	LUT2_3 output	1	0	0	1	1	1
40	LUT2_4 output	1	0	1	0	0	0
41	LUT2_5 output	1	0	1	0	0	1
42	pipe1 delay output0	1	0	1	0	1	0
43	pipe1 delay output1	1	0	1	0	1	1
44	Edge detect output	1	0	1	1	0	0
45	Programmable delay with edge detector	1	0	1	1	0	1
46	internal oscillator output	1	0	1	1	1	0
47	internal oscillator divided by 4 output	1	0	1	1	1	1
48	internal oscillator divided by 8, 12, 24, 64 output	1	1	0	0	0	0
49	internal oscillator divided by 3 output	1	1	0	0	0	1
50	Reserved	1	1	0	0	1	0
51	Reserved	1	1	0	0	1	1
52	Reserved	1	1	0	1	0	0
53	Reserved	1	1	0	1	0	1
54	pin10 digital Input	1	1	0	1	1	0
55	pin11 digital Input	1	1	0	1	1	1
56	pin12 digital Input	1	1	1	0	0	0
57	pin13 digital Input	1	1	1	0	0	1
58	pin14 digital Input	1	1	1	0	1	0
59	filter_0 output	1	1	1	0	1	1
60	matrix input<48> divide by 3	1	1	1	1	0	0
61	filter_1 output	1	1	1	1	0	1
62	Reset_core (POR) as matrix input	1	1	1	1	1	0
63	VDD	1	1	1	1	1	1

8.2 Matrix Output Table

Table 24. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<5:0>	Reserved	0
reg<11:6>	Matrix Out: PIN3 Digital Output Source	1
reg<17:12>	Matrix Out: PIN4 Digital Output Source	2
reg<23:18>	Matrix Out: PIN5 Digital Output Source	3
reg<29:24>	Matrix Out: PIN6 Digital Output Source	4
reg<35:30>	Reserved	5
reg<41:36>	Matrix Out: PIN6 Digital Output Source	6
reg<47:42>	Matrix Out: PIN8 Digital Output Source (4X Drive)	7
reg<53:48>	Matrix Out: Input for Delay0 or Counter0 External Clock	8
reg<59:54>	Matrix Out: Input for Delay1 or Counter1 Reset Input	9
reg<65:60>	Matrix Out: Input for Counter1 External Clock or Delay1 External Clock	10
reg<71:66>	Matrix Out: Input for Delay2 or Counter2 Reset Input	11
reg<77:72>	Matrix Out: Input for Counter2 External Clock or Delay2 External Clock	12
reg<83:78>	Matrix Out: Input for Delay3 or Counter3 Reset Input	13
reg<89:84>	Matrix Out: Input for Counter3 External Clock or Delay3 External Clock	14
reg<95:90>	Matrix Out: Input for Delay4 or Counter4 External Clock	15
reg<101:96>	Matrix Out: Input for Delay5 or Counter5 External Clock	16
reg<107:102>	Matrix Out: Input for Delay6 or Counter6 External Clock	17
reg<113:108>	Matrix Out: Input for Delay7 or Counter7 External Clock	18
reg<119:114>	Matrix Out: Clock Input of DFF0	19
reg<125:120>	Matrix Out: Data Input of DFF0	20
reg<131:126>	Matrix Out: nRST (nSET) of DFF0	21
reg<137:132>	Matrix Out: Clock Input of DFF1	22
reg<143:138>	Matrix Out: Data Input of DFF1	23
reg<149:144>	Matrix Out: nRST (nSET) of DFF1	24
reg<155:150>	Matrix Out: Clock Input of DFF2	25
reg<161:156>	Matrix Out: Data Input of DFF2	26
reg<167:162>	Matrix Out: nRST (nSET) of DFF2	27
reg<173:168>	Matrix Out: Clock Input of DFF3	28
reg<179:174>	Matrix Out: Data Input of DFF3	29
reg<185:180>	Matrix Out: nRST (nSET) of DFF3	30
reg<191:186>	Matrix Out: Clock Input of DFF5	31
reg<197:192>	Matrix Out: Data Input of DFF5	32
reg<203:198>	Matrix Out: Clock Input of DFF6	33
reg<209:204>	Matrix Out: Data Input of DFF6	34
reg<215:210>	Matrix Out: In0 of LUT4_0	35
reg<221:216>	Matrix Out: In1 of LUT4_0	36

Table 24. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<227:222>	Matrix Out: In2 of LUT4_0	37
reg<233:228>	Matrix Out: In3 of LUT4_0	38
reg<239:234>	Matrix Out: In0 of LUT3_0	39
reg<245:240>	Matrix Out: In1 of LUT3_0	40
reg<251:246>	Matrix Out: In2 of LUT3_0	41
reg<257:252>	Matrix Out: In0 of LUT3_1	42
reg<263:258>	Matrix Out: In1 of LUT3_1	43
reg<269:264>	Matrix Out: In2 of LUT3_1	44
reg<275:270>	Matrix Out: In0 of LUT3_2	45
reg<281:276>	Matrix Out: In1 of LUT3_2	46
reg<287:282>	Matrix Out: In2 of LUT3_2	47
reg<293:288>	Matrix Out: In0 of LUT3_3	48
reg<299:294>	Matrix Out: In1 of LUT3_3	49
reg<305:300>	Matrix Out: In2 of LUT3_3	50
reg<311:306>	Matrix Out: In0 of LUT3_4	51
reg<317:312>	Matrix Out: In1 of LUT3_4	52
reg<323:318>	Matrix Out: In2 of LUT3_4	53
reg<329:324>	Matrix Out: In0 of LUT3_5	54
reg<335:330>	Matrix Out: In1 of LUT3_5	55
reg<341:336>	Matrix Out: In2 of LUT3_5	56
reg<347:342>	Matrix Out: In0 of LUT3_6	57
reg<353:348>	Matrix Out: In1 of LUT3_6	58
reg<359:354>	Matrix Out: In2 of LUT3_6	59
reg<365:360>	Matrix Out: In0 of LUT3_7	60
reg<371:366>	Matrix Out: In1 of LUT3_7	61
reg<377:372>	Matrix Out: In2 of LUT3_7	62
reg<383:378>	Matrix Out: In0 of LUT3_8 or Input of Pipe delay	63
reg<389:384>	Matrix Out: In1 of LUT3_8 or nRST of Pipe delay	64
reg<395:390>	Matrix Out: In2 of LUT3_8 or Clock of Pipe delay	65
reg<401:396>	Matrix Out: In0 of LUT3_9	66
reg<407:402>	Matrix Out: In1 of LUT3_9	67
reg<413:408>	Matrix Out: In2 of LUT3_9	68
reg<419:414>	Matrix Out: In0 of LUT2_0 or Clock Input of DFF4	69
reg<425:420>	Matrix Out: In1 of LUT2_0 or Data Input of DFF4	70
reg<431:426>	Matrix Out: In0 of LUT2_1	71
reg<437:432>	Matrix Out: In1 of LUT2_1	72
reg<443:438>	Matrix Out: In0 of LUT2_2	73
reg<449:444>	Matrix Out: In1 of LUT2_2	74
reg<455:450>	Matrix Out: In0 of LUT2_3	75

Table 24. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<461:456>	Matrix Out: In1 of LUT2_3	76
reg<467:462>	Matrix Out: In0 of LUT2_4	77
reg<473:468>	Matrix Out: In1 of LUT2_4	78
reg<439:474>	Matrix Out: In0 of LUT2_5	79
reg<485:480>	Matrix Out: In1 of LUT2_5	80
reg<491:486>	Matrix Out: Input for Programmable Delay & Edge Detector	81
reg<497:492>	Matrix Out: Power Down for Osc	82
reg<503:498>	Reserved	83
reg<509:504>	Reserved	84
reg<515:510>	Reserved	85
reg<521:516>	Reserved	86
reg<527:522>	Matrix Out: Pin10 Digital Output Source	87
reg<533:528>	Matrix Out: Pin11 Digital Output Source	88
reg<539:534>	Matrix Out: Pin12 Digital Output Source	89
reg<545:540>	Matrix Out: Pin13 Digital Output Source	90
reg<551:546>	Matrix Out: Pin14 Digital Output Source	91
reg<557:552>	Matrix Out: Input of Filter_0	92
reg<563:558>	Matrix Out: Input of Filter_1	93
reg<569:564>	Reserved	94

9.0 Combinatorial Logic

Combinatorial logic is supported via fifteen Lookup Tables (LUTs) within the SLG46170. There are five 2-bit LUTs, nine 3-bit LUTs, and one 4-bit LUT. The device also includes two Combination Function Macrocells that can be used as LUTs. For more details, please see Section 10.0 Combination Function Macrocells.

Inputs/Outputs for the fifteen LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

9.1 2-Bit LUT

The five 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

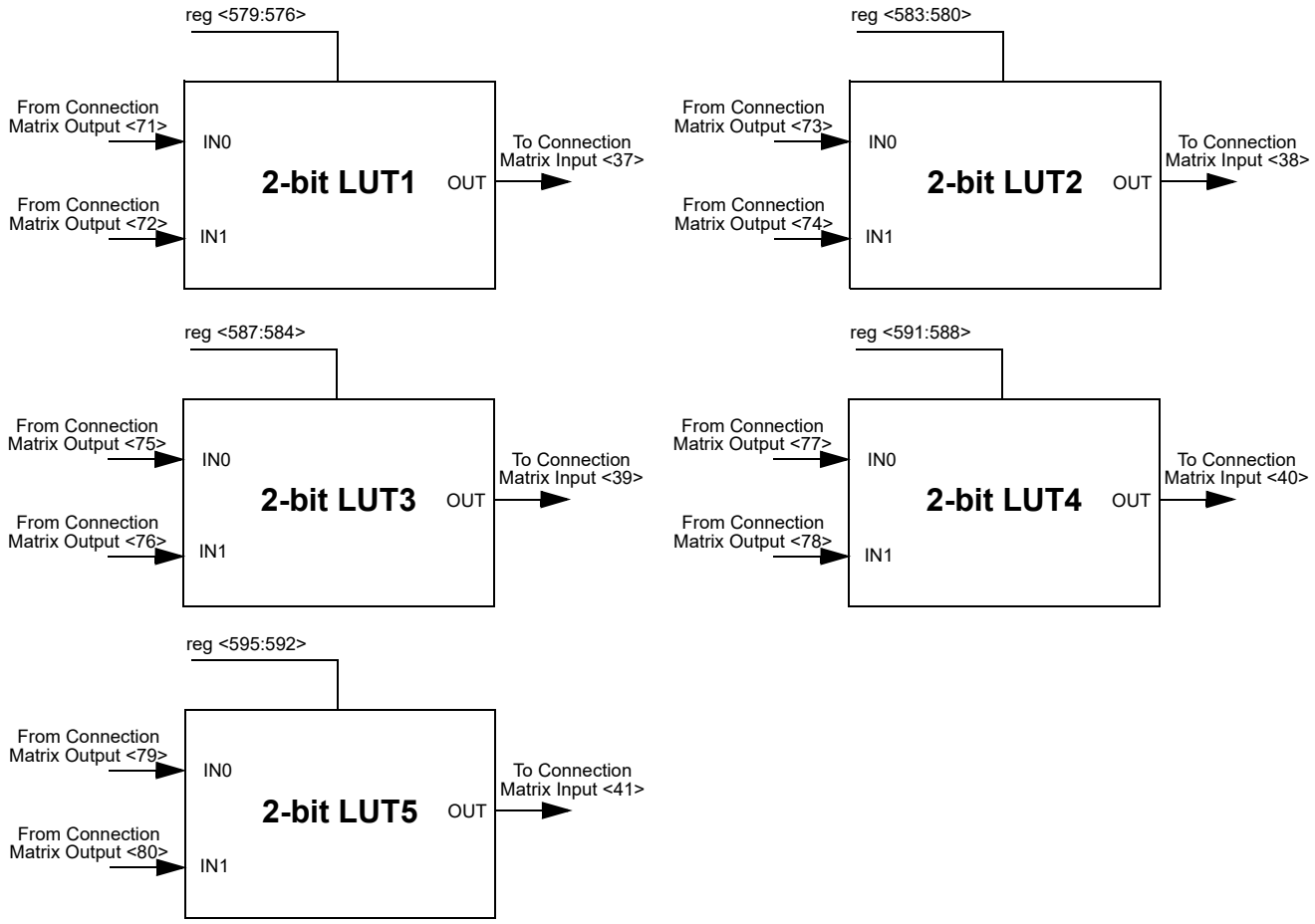


Figure 6. 2-bit LUTs

Table 25. 2-bit LUT1 Truth Table.

IN1	IN0	OUT
0	0	reg <576>
0	1	reg <577>
1	0	reg <578>
1	1	reg <579>

Table 26. 2-bit LUT2 Truth Table.

IN1	IN0	OUT
0	0	reg <580>
0	1	reg <581>
1	0	reg <582>
1	1	reg <583>

Table 27. 2-bit LUT3 Truth Table.

IN1	IN0	OUT
0	0	reg <584>
0	1	reg <585>
1	0	reg <586>
1	1	reg <587>

Table 28. 2-bit LUT4 Truth Table.

IN1	IN0	OUT
0	0	reg <588>
0	1	reg <589>
1	0	reg <590>
1	1	reg <591>

Table 29. 2-bit LUT5 Truth Table.

IN1	IN0	OUT
0	0	reg <592>
0	1	reg <593>
1	0	reg <594>
1	1	reg <595>

Each 2-bit LUT uses a 4-bit register signal to define their output functions;

2-Bit LUT1 is defined by reg<579:576>

2-Bit LUT2 is defined by reg<583:580>

2-Bit LUT3 is defined by reg<587:584>

2-Bit LUT4 is defined by reg<591:588>

2-Bit LUT5 is defined by reg<595:592

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 2-bit LUT logic cells.

Table 30. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

9.2 3-Bit LUT

The nine 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

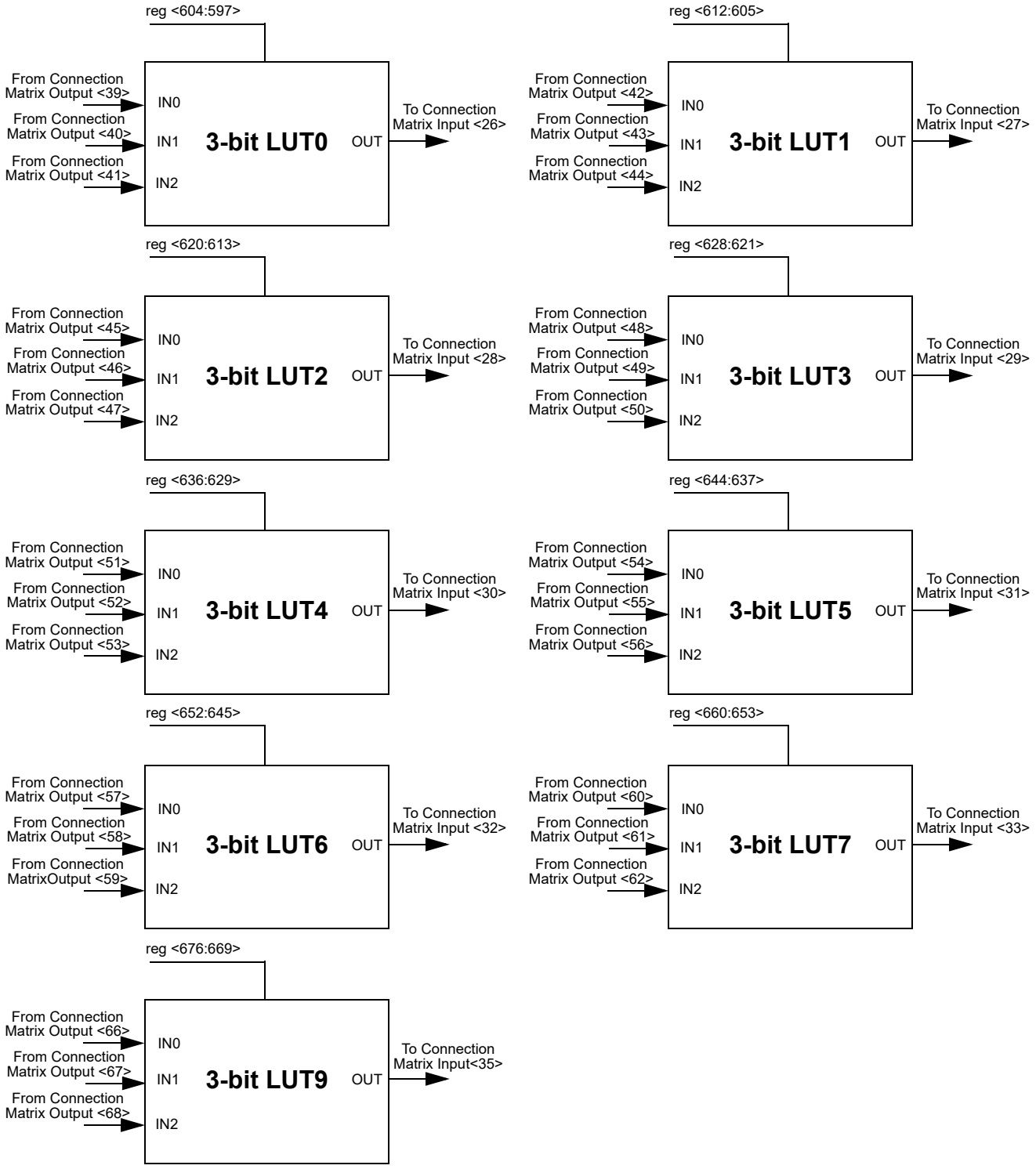


Figure 7. 3-bit LUTs

Table 31. 3-bit LUT0 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <597>
0	0	1	reg <598>
0	1	0	reg <599>
0	1	1	reg <600>
1	0	0	reg <601>
1	0	1	reg <602>
1	1	0	reg <603>
1	1	1	reg <604>

Table 32. 3-bit LUT1 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <605>
0	0	1	reg <606>
0	1	0	reg <607>
0	1	1	reg <608>
1	0	0	reg <609>
1	0	1	reg <610>
1	1	0	reg <611>
1	1	1	reg <612>

Table 33. 3-bit LUT2 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <613>
0	0	1	reg <614>
0	1	0	reg <615>
0	1	1	reg <616>
1	0	0	reg <617>
1	0	1	reg <618>
1	1	0	reg <619>
1	1	1	reg <620>

Table 34. 3-bit LUT3 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <621>
0	0	1	reg <622>
0	1	0	reg <623>
0	1	1	reg <624>
1	0	0	reg <625>
1	0	1	reg <626>
1	1	0	reg <627>
1	1	1	reg <628>

Table 35. 3-bit LUT4 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <629>
0	0	1	reg <630>
0	1	0	reg <631>
0	1	1	reg <632>
1	0	0	reg <633>
1	0	1	reg <634>
1	1	0	reg <635>
1	1	1	reg <636>

Table 36. 3-bit LUT5 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <637>
0	0	1	reg <638>
0	1	0	reg <639>
0	1	1	reg <640>
1	0	0	reg <641>
1	0	1	reg <642>
1	1	0	reg <643>
1	1	1	reg <644>

Table 37. 3-bit LUT6 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <645>
0	0	1	reg <646>
0	1	0	reg <647>
0	1	1	reg <648>
1	0	0	reg <649>
1	0	1	reg <650>
1	1	0	reg <651>
1	1	1	reg <652>

Table 38. 3-bit LUT7 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <653>
0	0	1	reg <654>
0	1	0	reg <655>
0	1	1	reg <656>
1	0	0	reg <657>
1	0	1	reg <658>
1	1	0	reg <659>
1	1	1	reg <660>

Table 39. 3-bit LUT9 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <669>
0	0	1	reg <670>
0	1	0	reg <671>
0	1	1	reg <672>
1	0	0	reg <673>
1	0	1	reg <674>
1	1	0	reg <675>
1	1	1	reg <676>

Each 3-bit LUT uses a 8-bit register signal to define their output functions;

3-Bit LUT1 is defined by reg<604:597>

3-Bit LUT2 is defined by reg<612:605>

3-Bit LUT3 is defined by reg<620:613>

3-Bit LUT4 is defined by reg<628:621>

3-Bit LUT5 is defined by reg<636:629>

3-Bit LUT6 is defined by reg<644:637>

3-Bit LUT7 is defined by reg<652:645>

3-Bit LUT8 is defined by reg<660:653>

3-Bit LUT9 is defined by reg<676:669>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six3-bit LUT logic cells.

Table 40. 3-bit LUT Standard Digital Functions.

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

9.3 4-Bit LUT

The one 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

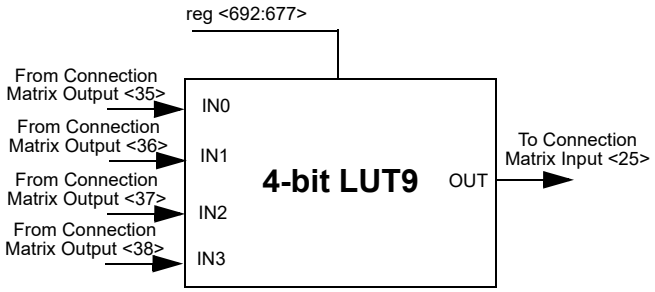


Figure 8. 2-bit LUTs

Table 41. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <677>
0	0	0	1	reg <678>
0	0	1	0	reg <679>
0	0	1	1	reg <680>
0	1	0	0	reg <681>
0	1	0	1	reg <682>
0	1	1	0	reg <683>
0	1	1	1	reg <684>
1	0	0	0	reg <685>
1	0	0	1	reg <686>
1	0	1	0	reg <687>
1	0	1	1	reg <688>
1	1	0	0	reg <689>
1	1	0	1	reg <690>
1	1	1	0	reg <691>
1	1	1	1	reg <692>

The 4-bit LUT uses a 16-bit register signal to define the output function;

4-Bit LUT0 is defined by reg<692:677>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within the 4-bit LUT logic cell.

Table 42. 4-bit LUT Standard Digital Functions.

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

10.0 Combination Function Macrocells

The SLG46170 has two combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells;

- One macrocell that can serve as either 2-bit LUT or as D Flip Flop
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay

Inputs/Outputs for the two combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR, Inverter, Buffer and MUX for 3-bit and 4-bit LUTs).

10.1 2-Bit LUT or D Flip Flop Macrocells

There is one macrocell that can serve as either a 2-bit LUT or as a D Flip Flop. When used to implement LUT function, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (D) and clock (clk) inputs for the Flip Flop, with the output going back to the connection matrix.

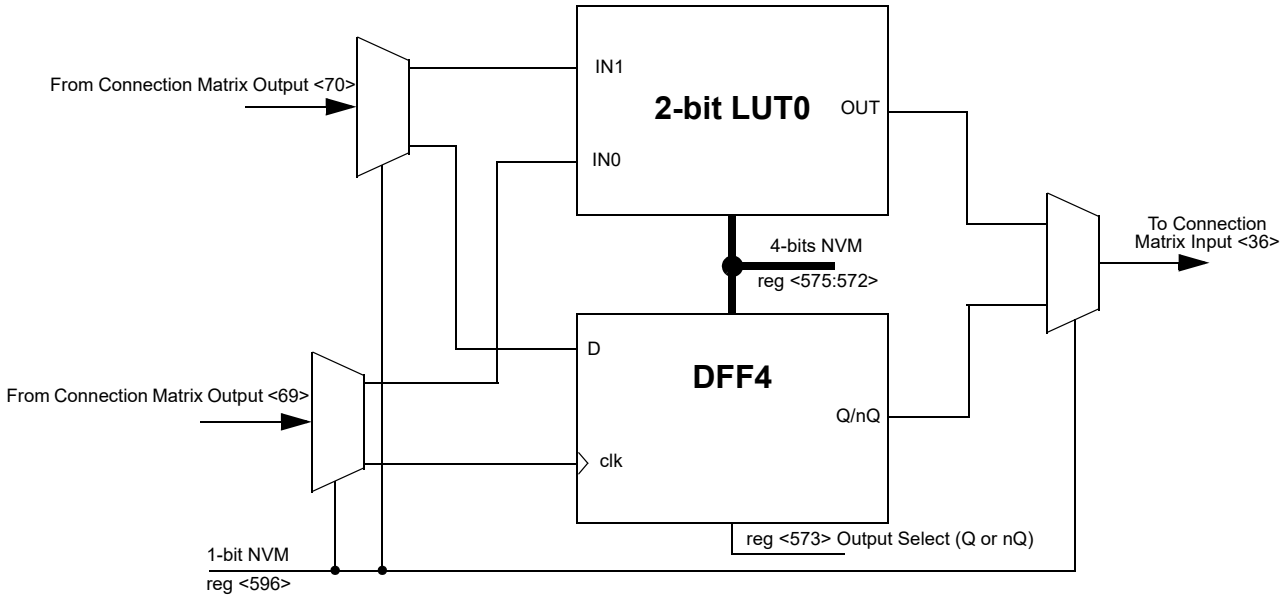


Figure 9. 2-bit LUT0 or DFF4

10.1.1 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

Table 43. 2-bit LUT0 Truth Table.

IN1	IN0	OUT
0	0	reg <572>
0	1	reg <573>
1	0	reg <574>
1	1	reg <575>

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by reg<575:572>

10.1.2 2-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 44. DFF4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_0 or DFF4 Select	596	0: LUT2_0 1: DFF4
DFF4 or Latch Select	572	0: DFF function 1: Latch function
DFF4 Output Select	573	0: Q output 1: nQ output
DFF4 Initial Polarity Select	574	0: Low 1: High

10.2 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (RST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (ONE PIPE OUT) is fixed at the output of the first flip-flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by reg <664:661> for OUT0 and reg <668:665> for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46170 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46722). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

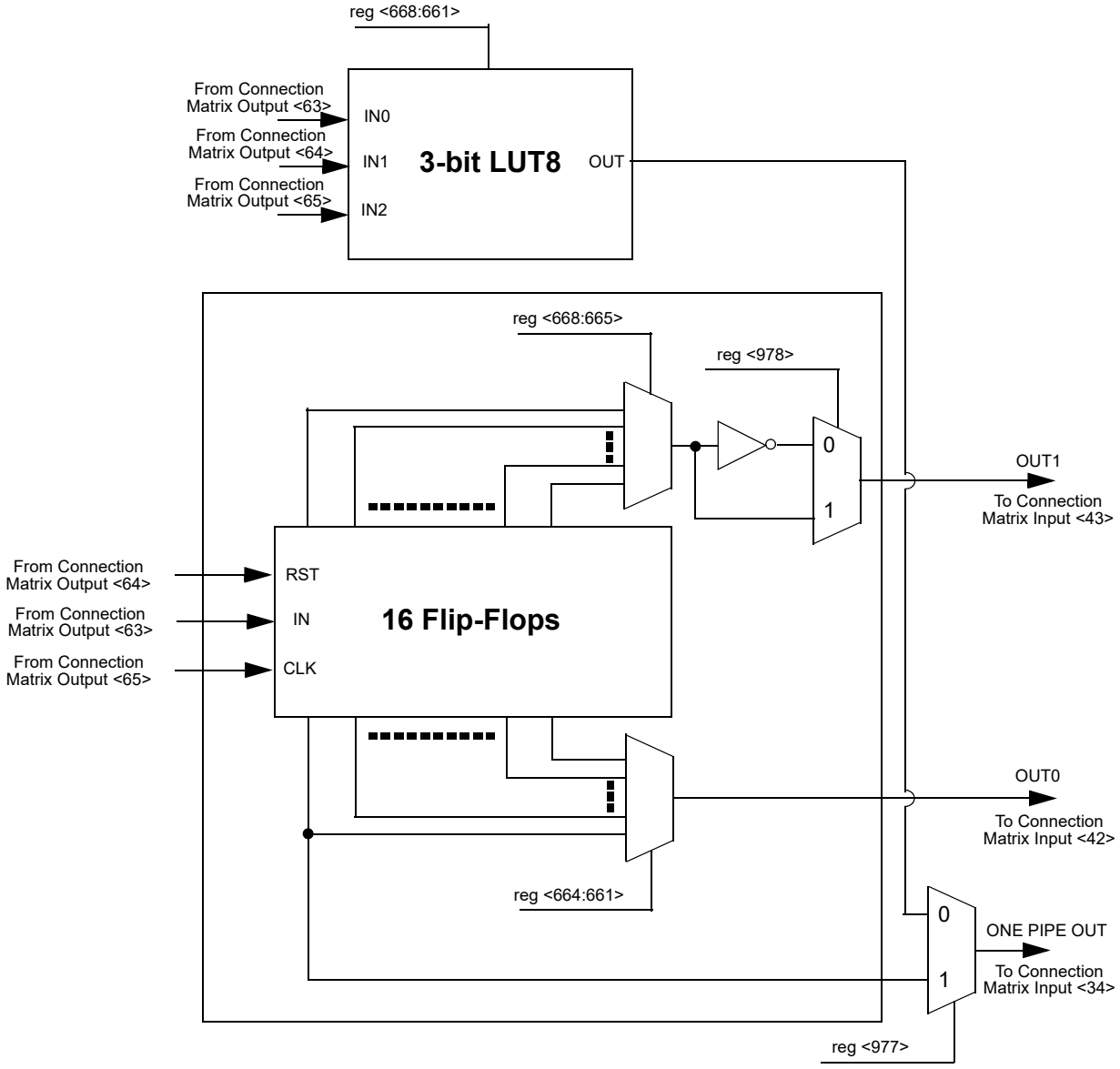


Figure 10. 3-bit LUT8 or Pipe Delay

10.2.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 45. 3-bit LUT8 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <661>
0	0	1	reg <662>
0	1	0	reg <663>
0	1	1	reg <664>
1	0	0	reg <665>
1	0	1	reg <666>
1	1	0	reg <667>
1	1	1	reg <668>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT8 is defined by reg<668:661>

10.2.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 46. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_8 or Pipe Delay Output Select	reg<977>	0: LUT3_8 1: 1 Pipe Delay Output
OUT0 select	reg<664:661>	
OUT1 select	reg<668:665>	
Pipe delay OUT1 Polarity Select Bit	reg<978>	0: Non-inverted 1: Inverted

11.0 Digital Storage Elements (DFFs/Latches)

There are six D Flip Flop / Latches (DFF/Latch logic cells within the SLG46170 available for design. The source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/Latch macrocells have user selection for initial state. DFF0 has the option to connect both the Q and Q Bar outputs to the connection matrix, DFF1, DFF2, DFF3, DFF5 and DFF6 can only connect the Q output to the matrix. The macrocells DFF0, DFF1, DFF2 and DFF3 have an additional input from the matrix that can serve as a nSet or nReset function to the macrocell.

Note that one of the Combination Function Macrocells (LUT 2_0 / DFF4) can also operate as a DFF or a 2-bit LUT please see Section *10.1 2-Bit LUT or D Flip Flop Macrocells* for the description of this Combination Function macrocell.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: if CLK = 0, then Q = D

if CLK = 1, then Q will not change

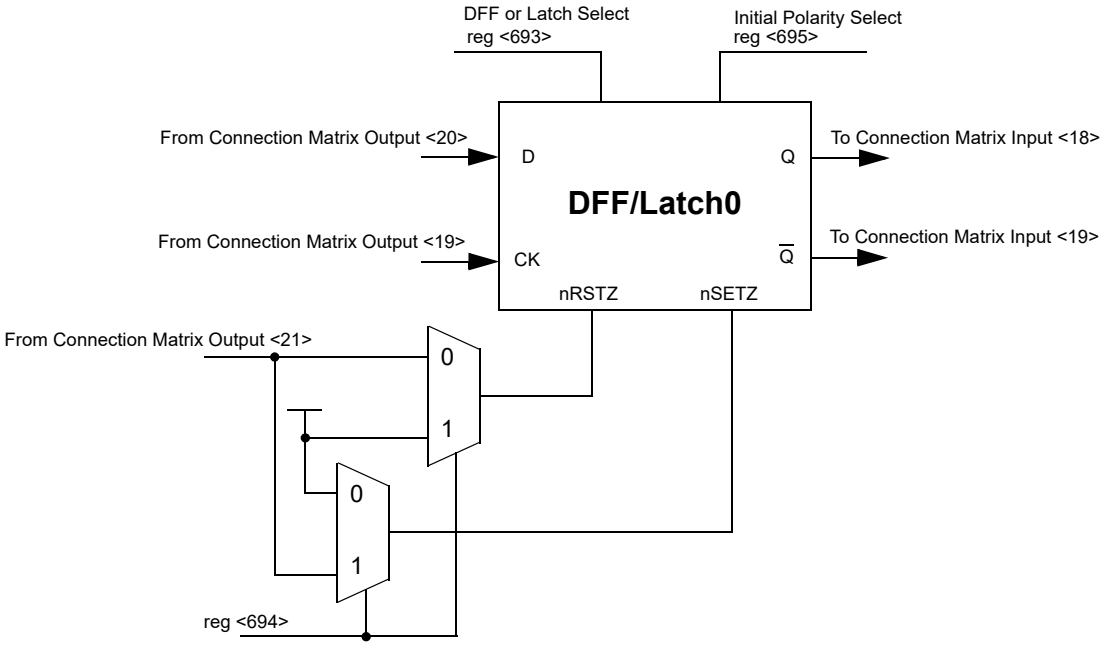


Figure 11. DFF/Latch0

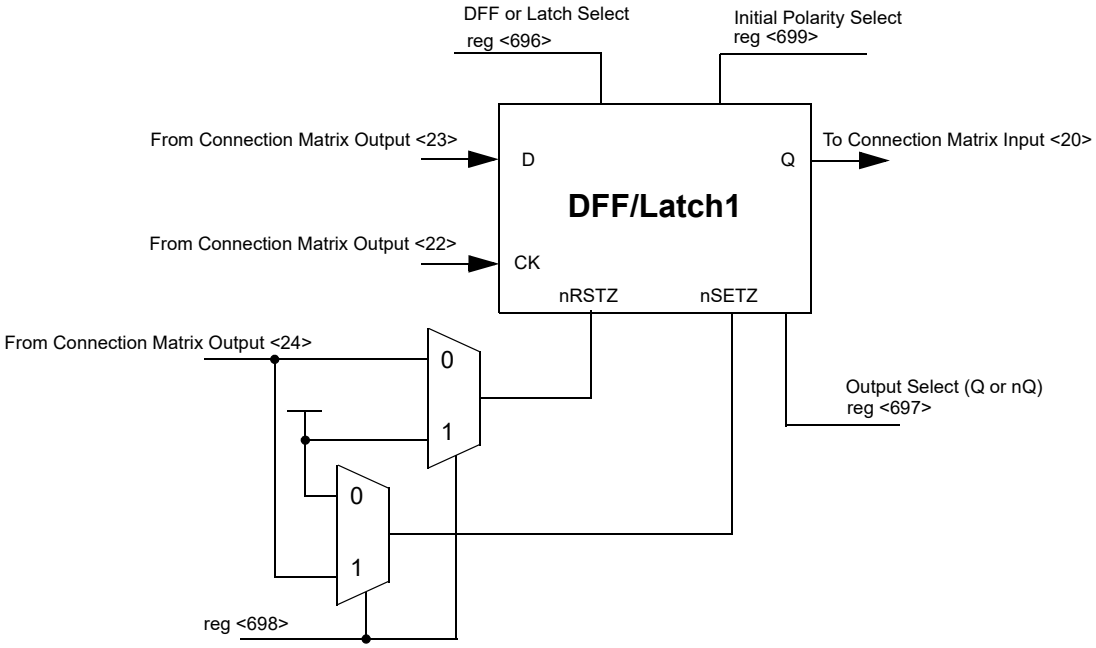


Figure 12. DFF/Latch1

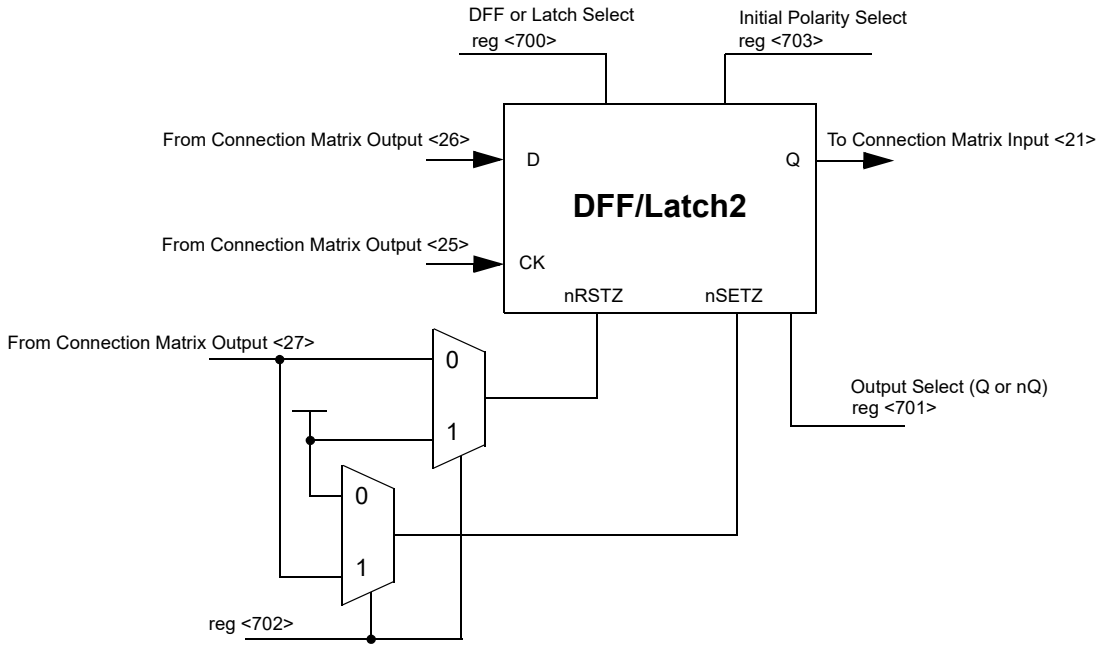


Figure 13. DFF/Latch2

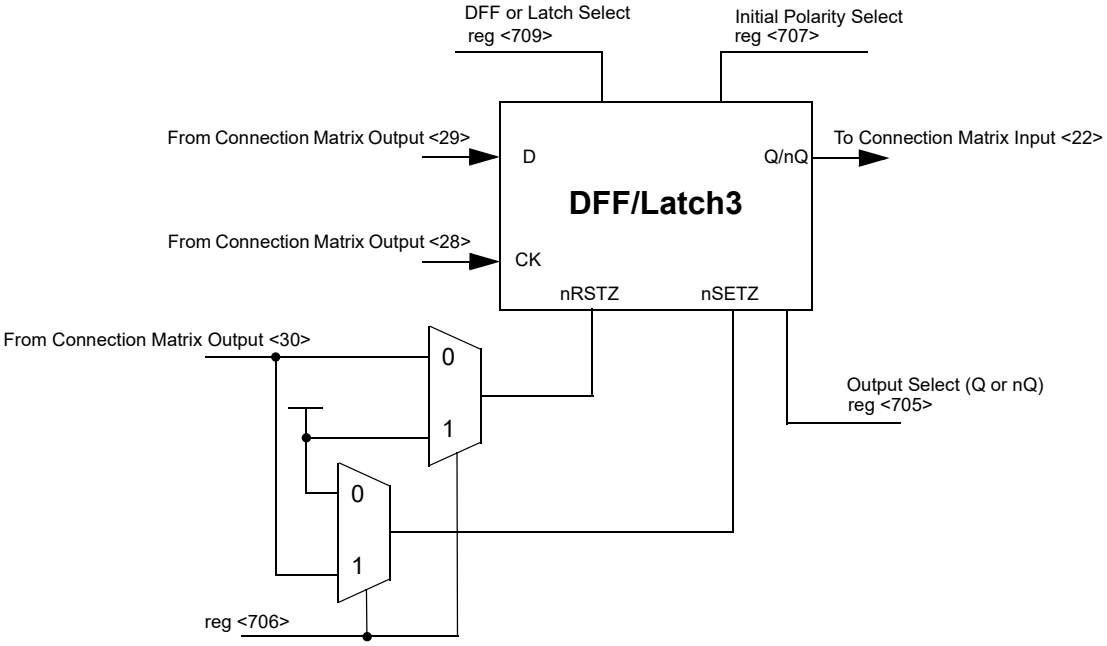


Figure 14. DFF/Latch3

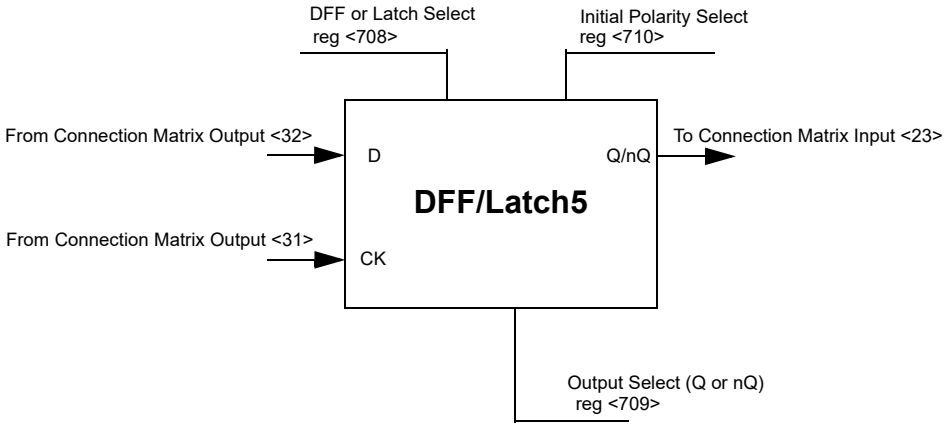


Figure 15. DFF/Latch5

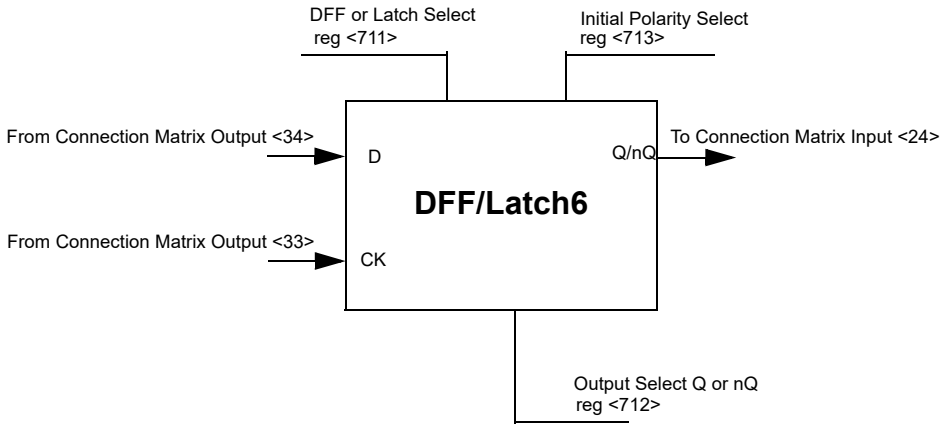


Figure 16. DFF/Latch6

11.1 Initial Polarity Operations

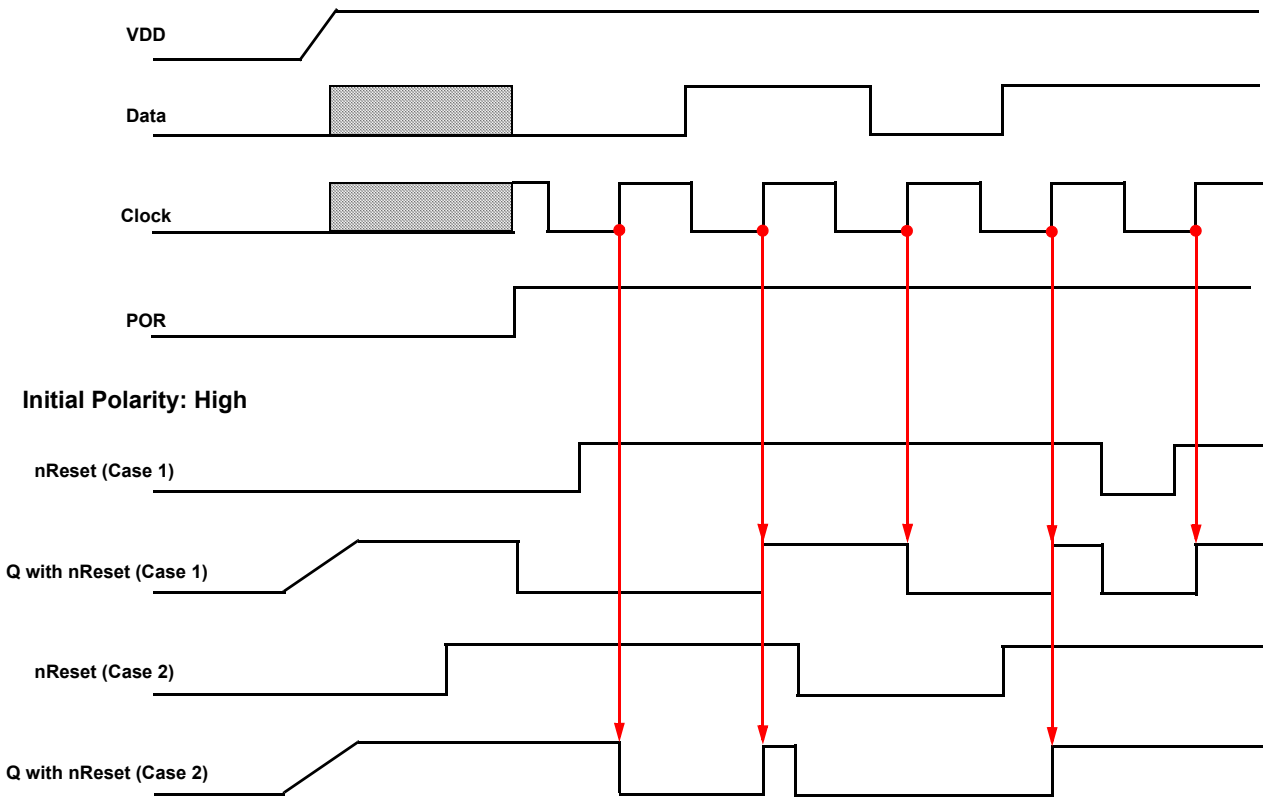


Figure 17. DFF Polarity Operations

12.0 Counters/Delay Generators (CNT/DLY)

There are eight configurable counters/delay generators in the SLG46170. Two of these counters/delay generators are 14-bit (CNT/DLY 0 and 1), and six of the counters/delay generators are 8-bit (CNT/DLY 2, 3, 4, 5, 6, 7). For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits.

Three of the counter/delay generator macrocells (CNT/DLY, 1,2,3) have two inputs from the connection matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source. Five of the counter/delay generator macrocells (CNT/DLY 0, 4, 5, 6, 7) have one input from the connection matrix, which has a shared function of either a Delay Input or an external clock input.

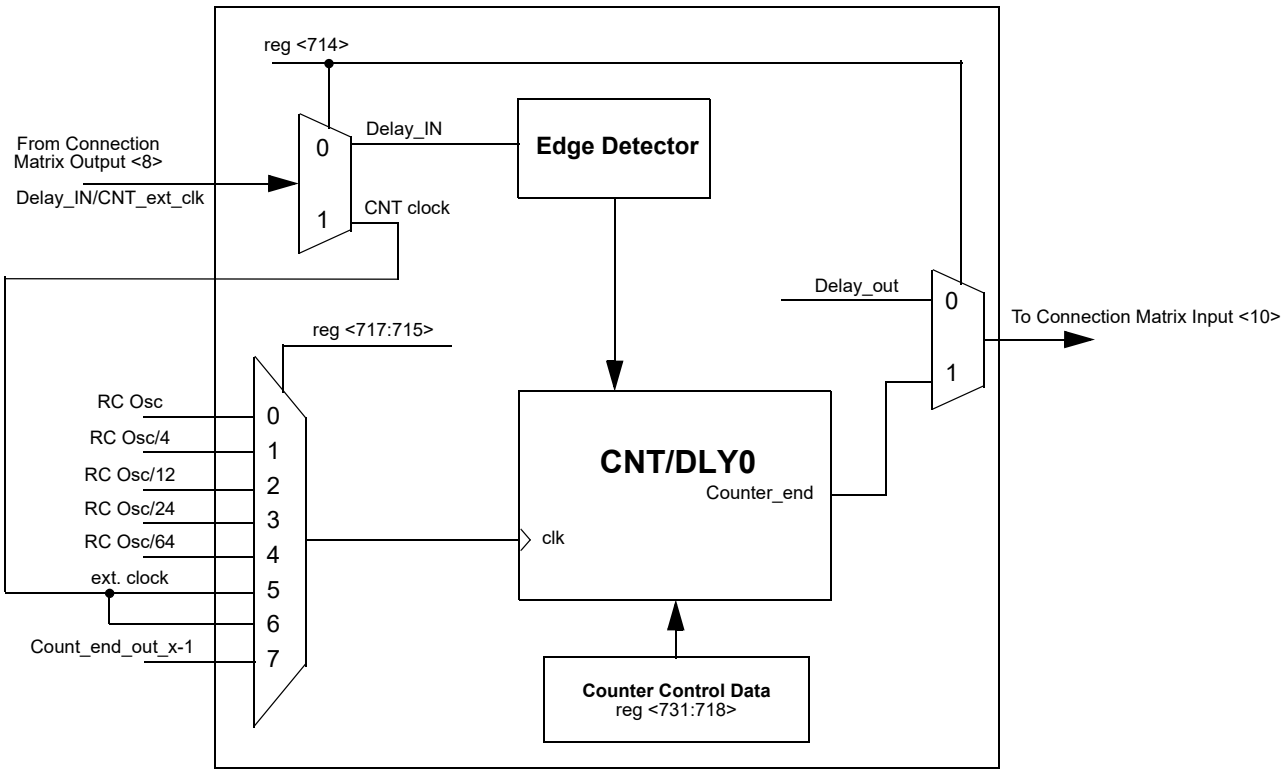


Figure 18. CNT/DLY0

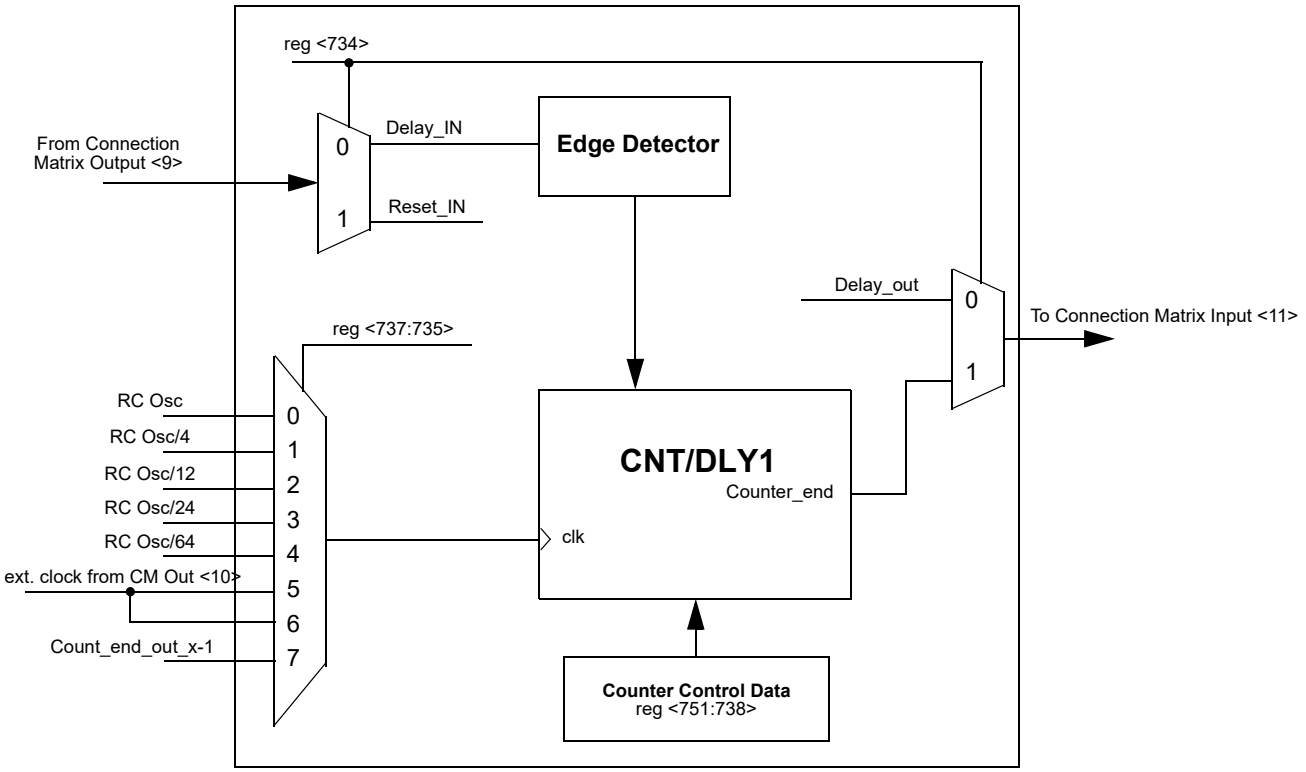


Figure 19. CNT/DLY1

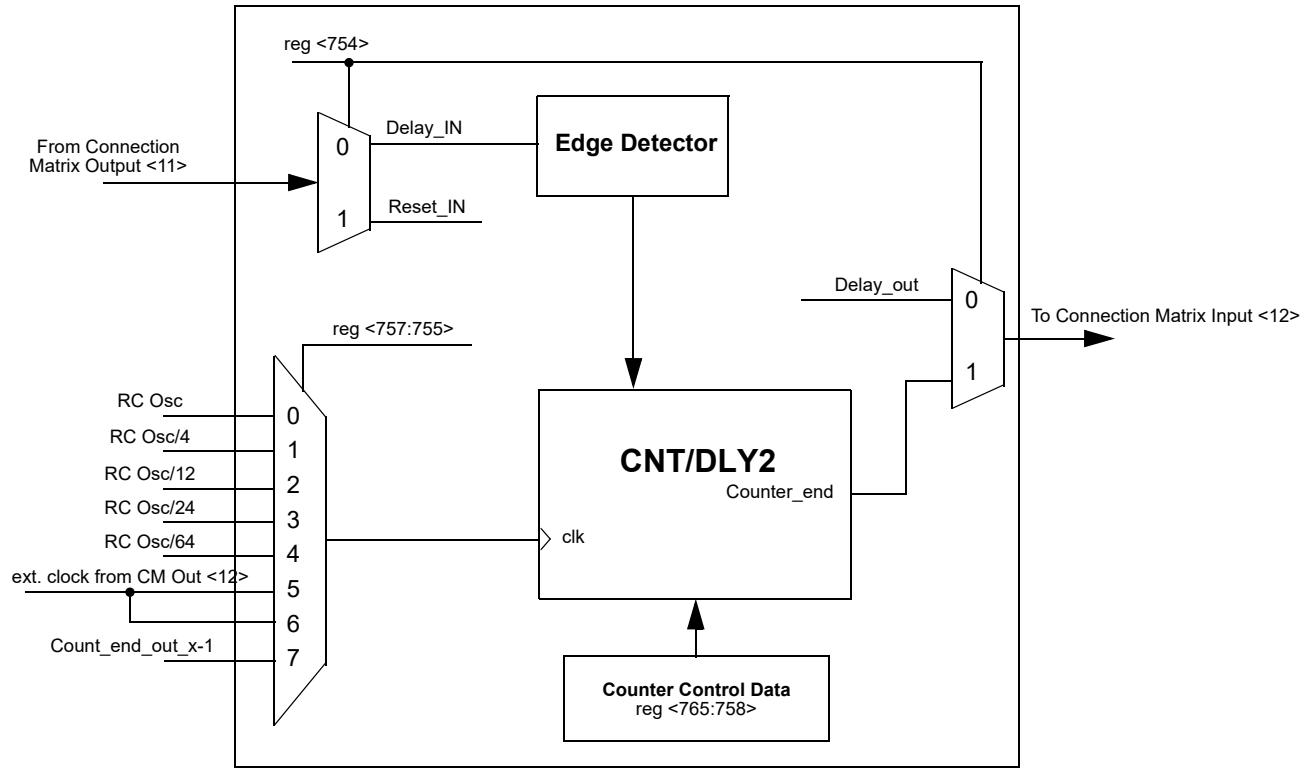


Figure 20. CNT/DLY2

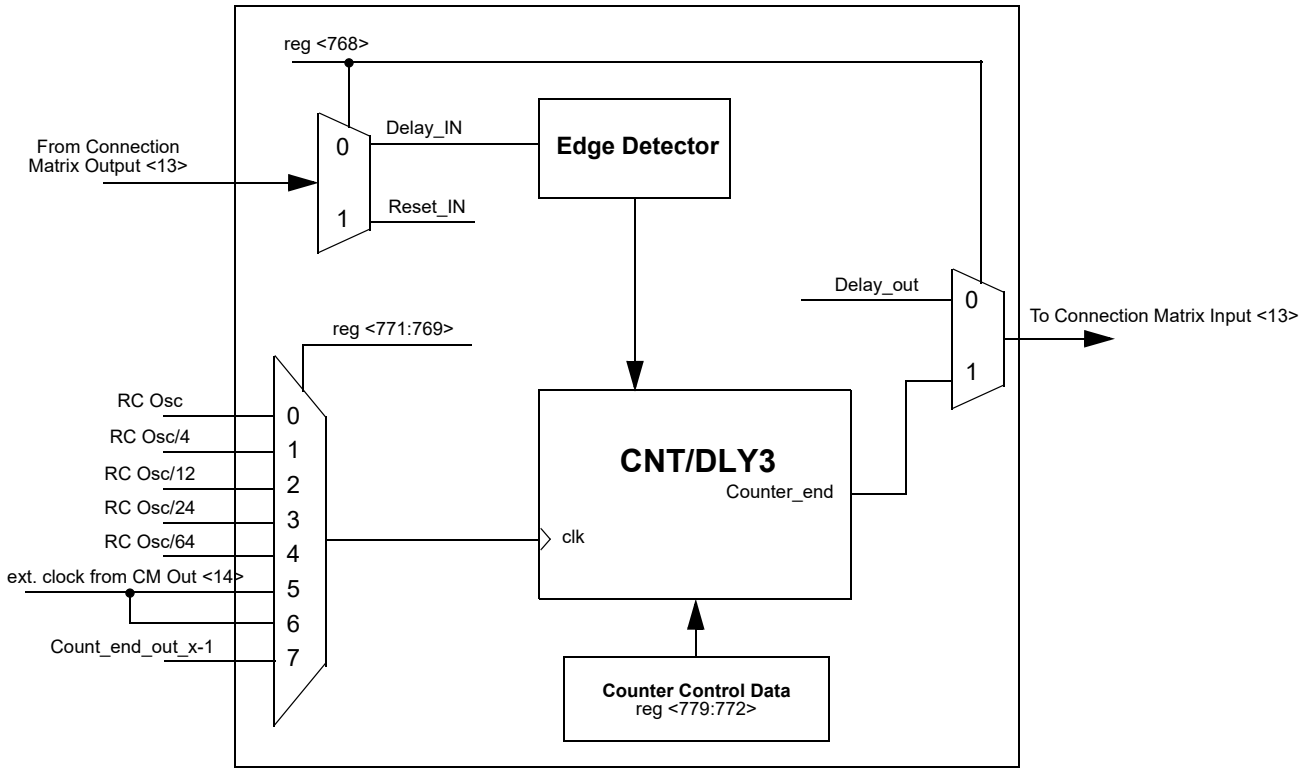


Figure 21. CNT/DLY3

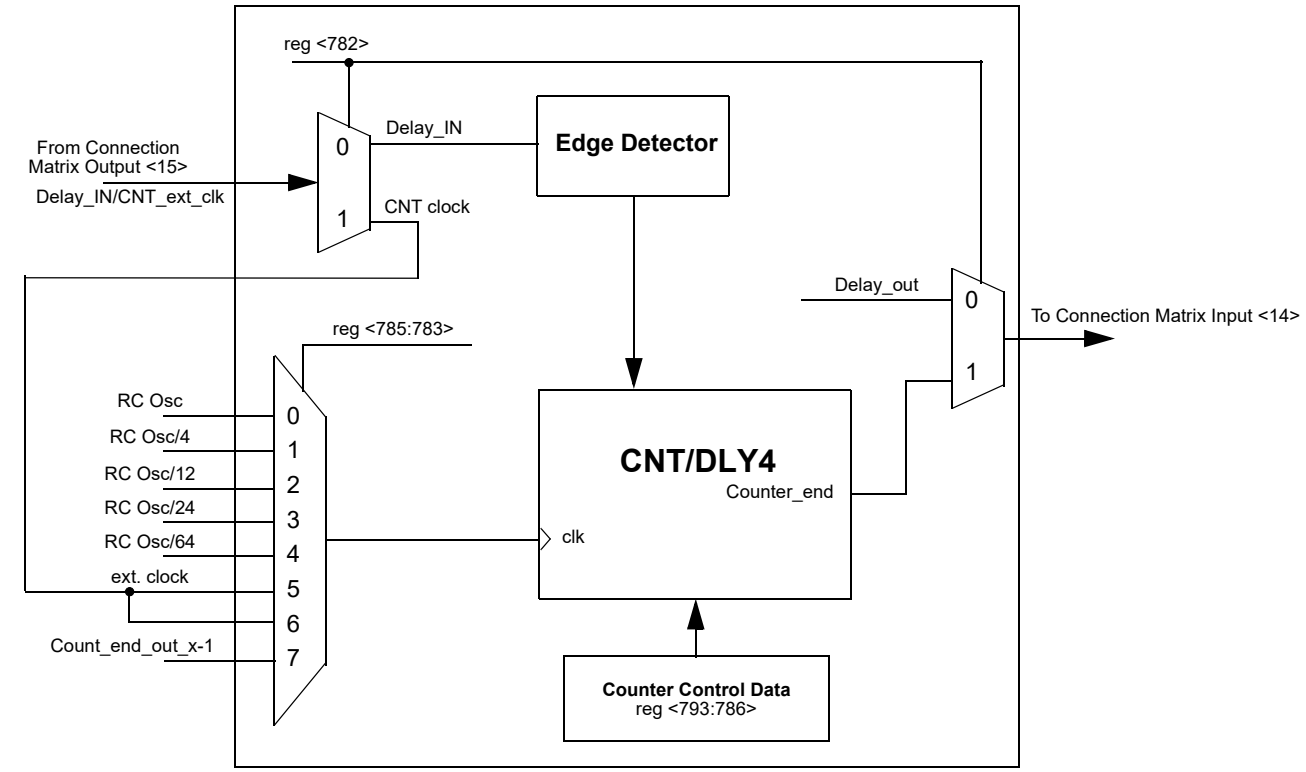


Figure 22. CNT/DLY4

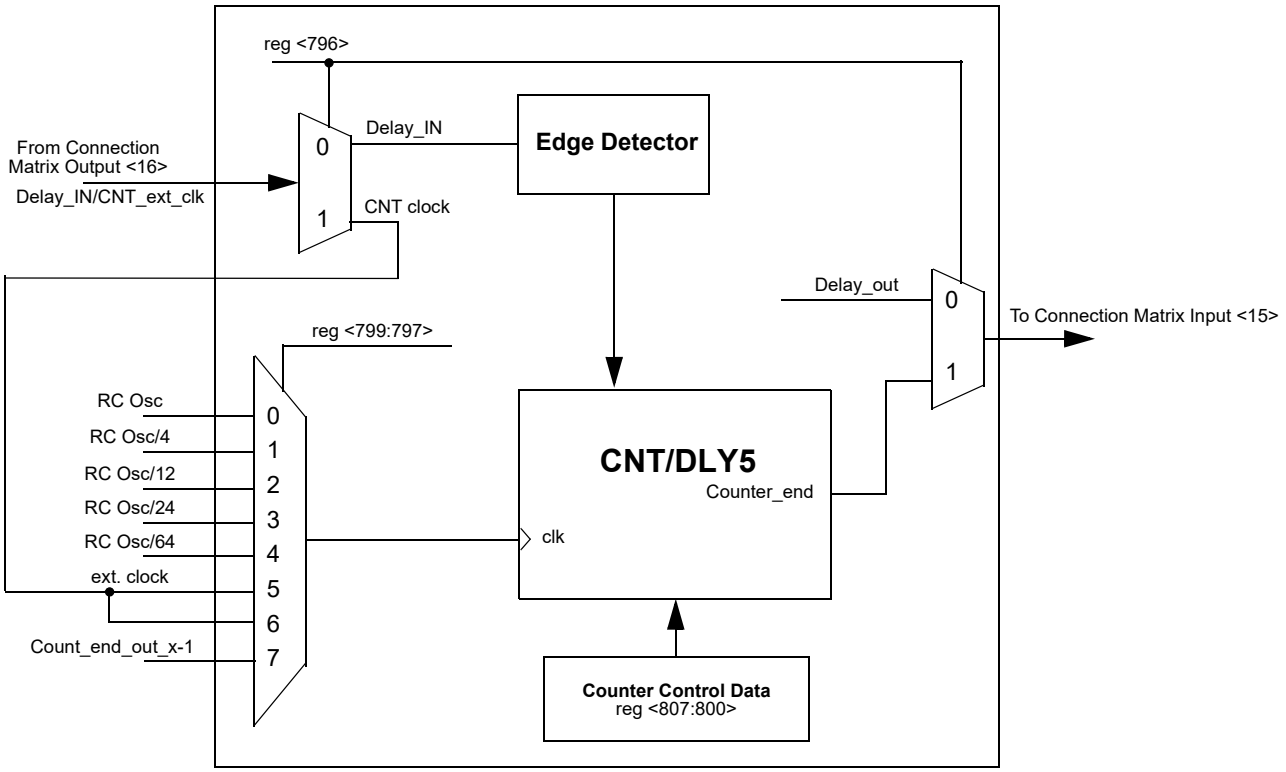


Figure 23. CNT/DLY5

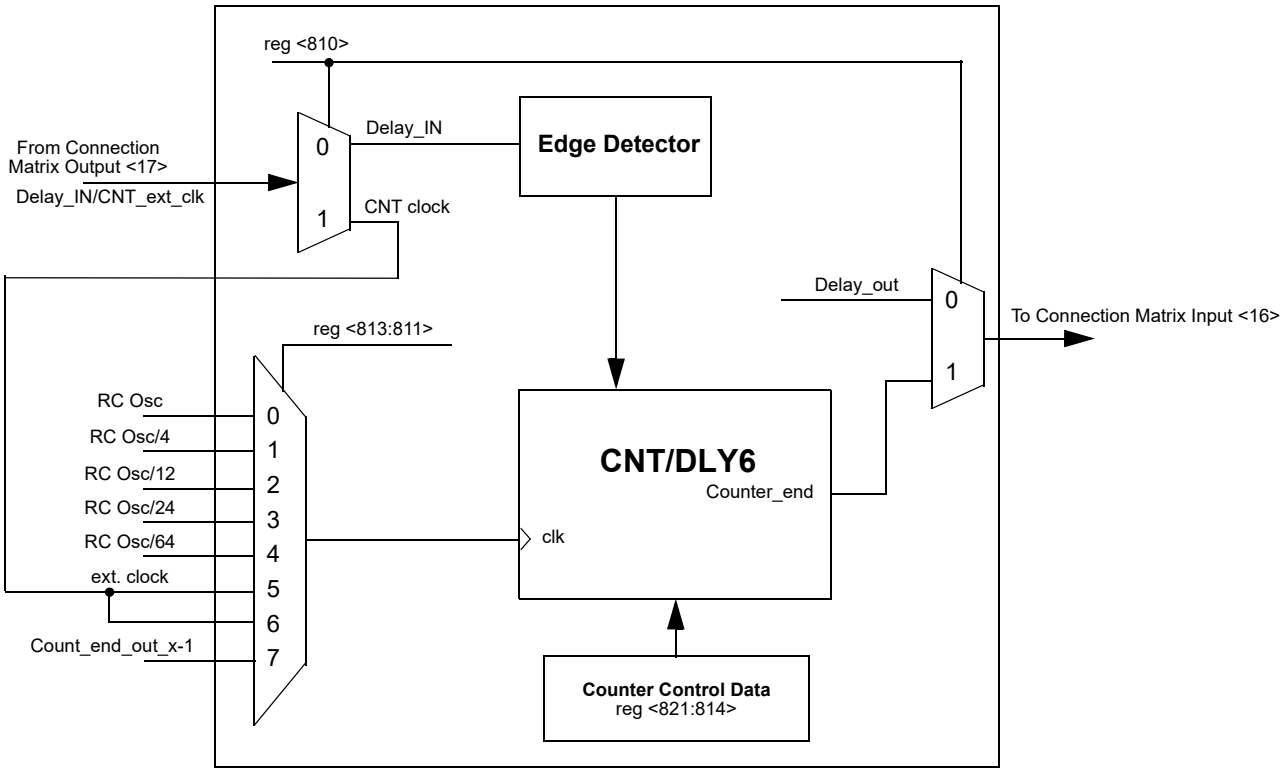


Figure 24. CNT/DLY6

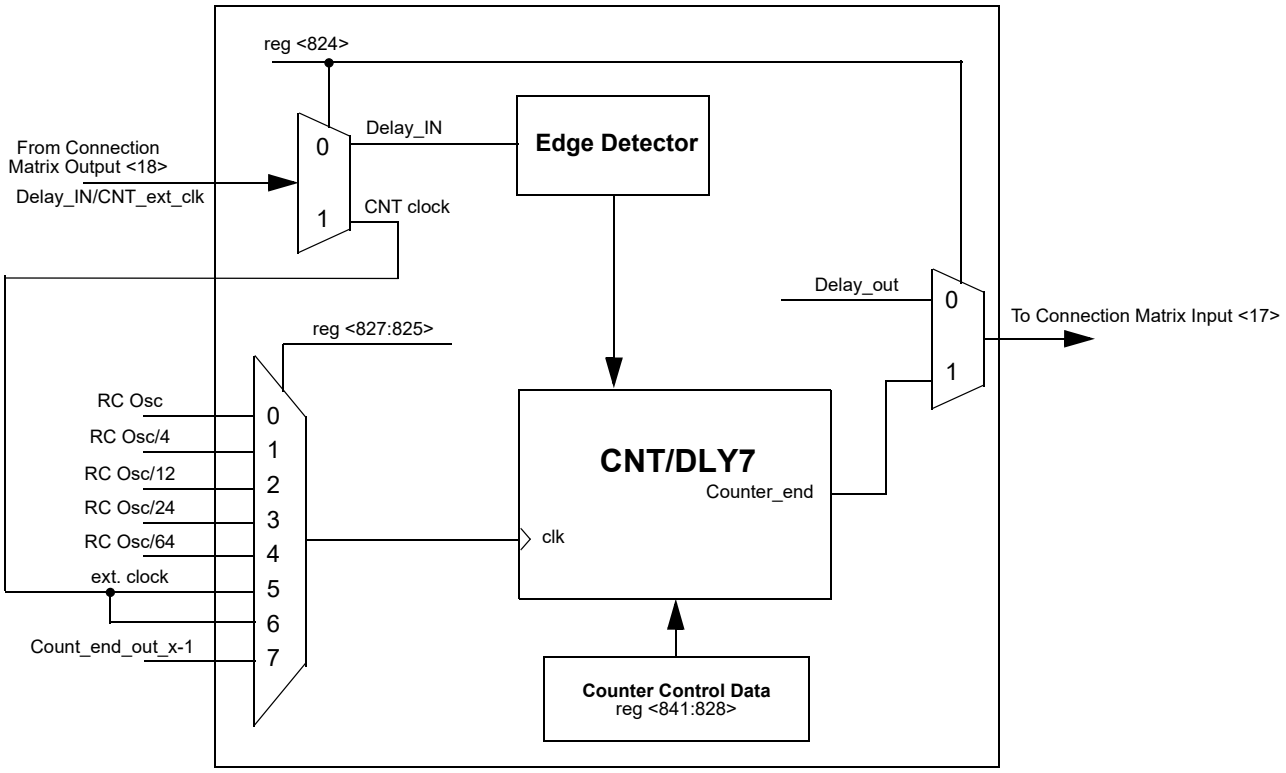


Figure 25. CNT/DLY7

12.1 CNT/DLY Timing Diagrams

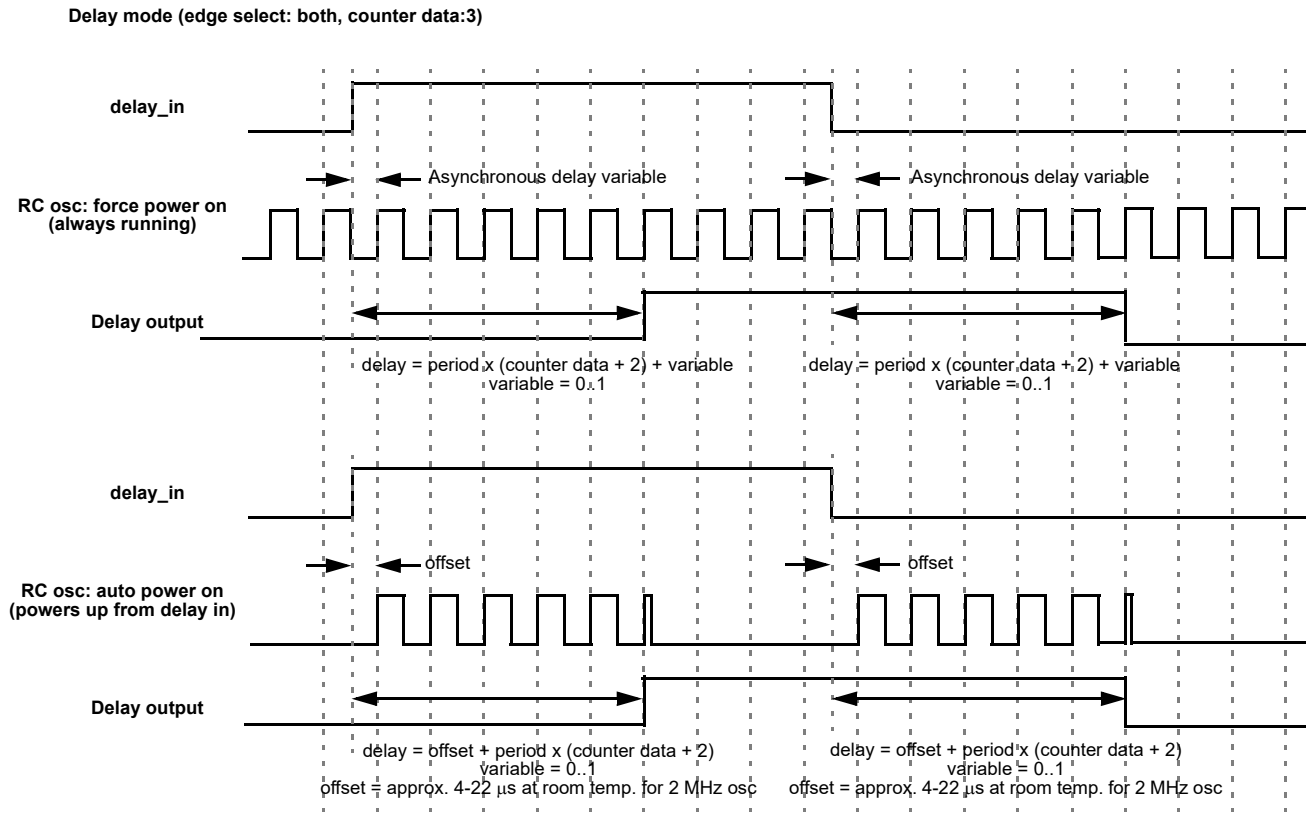


Figure 26. Delay Mode Timing

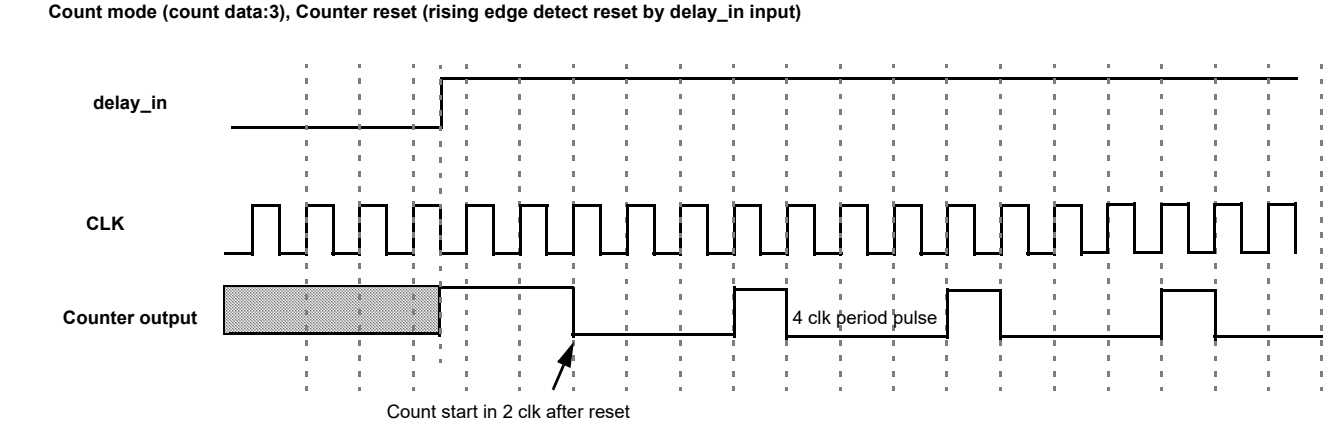


Figure 27. Counter Mode Timing

12.2 CNT/DLY0 Register Settings

Table 47. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay0 Mode Select	reg<714>	0: Delay Mode 1: Counter Mode
Counter/Delay0 Clock Source Select (external clock is only for counter mode)	reg<717:715>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter 7 Overflow
Counter0 Control Data/Delay0 Time Control	reg<731:718>	1-16384: (delay time = (counter control data +2) /freq)
Delay0 Mode Select	reg<733:732>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

12.3 CNT/DLY1 Register Settings

Table 48. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg<734>	0: Delay Mode 1: Counter Mode
Counter/Delay1 Clock Source select	reg<737:735>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter 0 Overflow
Counter1 Control Data/Delay1 Time Control	reg<751:738>	1-16384: (delay time = (counter control data +2) /freq)
Delay1 Mode Select or asynchronous counter reset	reg<753:752>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

12.4 CNT/DLY2 Register Settings

Table 49. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg<754>	0: Delay Mode 1: Counter Mode

Table 49. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Clock Source select	reg<757:755>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter 1 Overflow
Counter1 Control Data/Delay1 Time Control	reg<765:758>	1-256: (delay time = (counter control data +2) /freq)
Delay1 Mode Select or asynchronous counter reset	reg<767:766>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

12.5 CNT/DLY3 Register Settings

Table 50. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg<768>	0: Delay Mode 1: Counter Mode
Counter/Delay1 Clock Source select	reg<771:769>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter 2 Overflow
Counter1 Control Data/Delay1 Time Control	reg<779:772>	1-256: (delay time = (counter control data +2) /freq)
Delay1 Mode Select or asynchronous counter reset	reg<781:780>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

12.6 CNT/DLY4 Register Settings

Table 51. CNT/DLY4 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay4 Mode Select	reg<782>	0: Delay Mode 1: Counter Mode
Counter/Delay4 Clock Source Select (external clock is only for counter mode)	reg<785:783>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter 3 Overflow
Counter4 Control Data/Delay4 Time Control	reg<793:786>	1-256: (delay time = (counter control data +2) /freq)
Delay4 Mode Select	reg<795:794>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

12.7 CNT/DLY5 Register Settings

Table 52. CNT/DLY5 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay5 Mode Select	reg<796>	0: Delay Mode 1: Counter Mode
Counter/Delay5 Clock Source Select (external clock is only for counter mode)	reg<799:797>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter 4 Overflow
Counter5 Control Data/Delay5 Time Control	reg<807:800>	1-256: (delay time = (counter control data +2) /freq)
Delay5 Mode Select	reg<809:808>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

12.8 CNT/DLY6 Register Settings

Table 53. CNT/DLY6 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay6 Mode Select	reg<810>	0: Delay Mode 1: Counter Mode
Counter/Delay6 Clock Source Select (external clock is only for counter mode)	reg<813:811>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter 5 Overflow
Counter6 Control Data/Delay6 Time Control	reg<821:814>	1-256: (delay time = (counter control data +2) /freq)
Delay6 Mode Select	reg<823:822>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

12.9 CNT/DLY7 Register Settings

Table 54. CNT/DLY7 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay67 Mode Select	reg<824>	0: Delay Mode 1: Counter Mode
Counter/Delay7 Clock Source Select (external clock is only for counter mode)	reg<827:825>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter 6 Overflow
Counter6 Control Data/Delay7 Time Control	reg<841:828>	1-16384: (delay time = (counter control data +2) /freq)
Delay7 Mode Select	reg<843:842>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

13.0 Pipe Delay (PD)

The SLG46170 has a pipe delay logic cell that is shared with the 3-bit LUT8 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. Please see Section *10.2 3-Bit LUT or Pipe Delay Macrocell* for the description of this Combination Function macrocell.

14.0 Programmable Delay / Edge Detector

The SLG46170 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See the timing diagrams below for further information.

Note: *The input signal must be longer than the delay, otherwise it will be filtered out.*

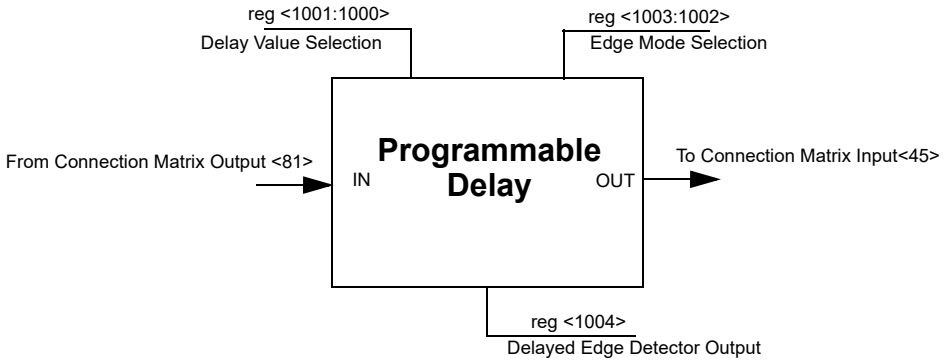


Figure 28. Programmable Delay

14.1 Programmable Delay Timing Diagram - Edge Detector Output

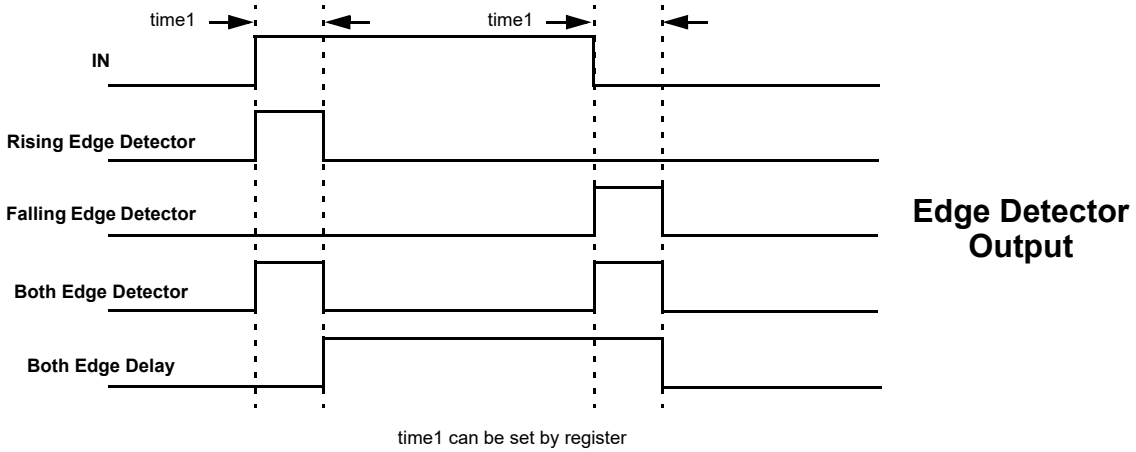


Figure 29. Edge Detector Output

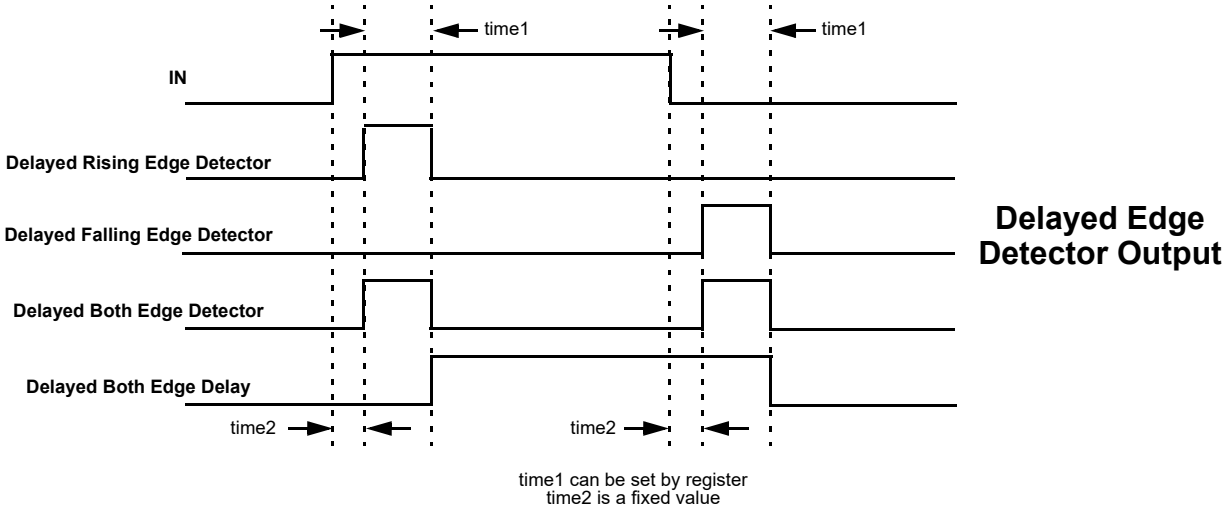


Figure 30. Delayed Edge Detector Output

Note: For delays and widths refer to Table 4.

14.2 Programmable Delay Timing Diagram - Glitch Filtering For Edge Detector Output

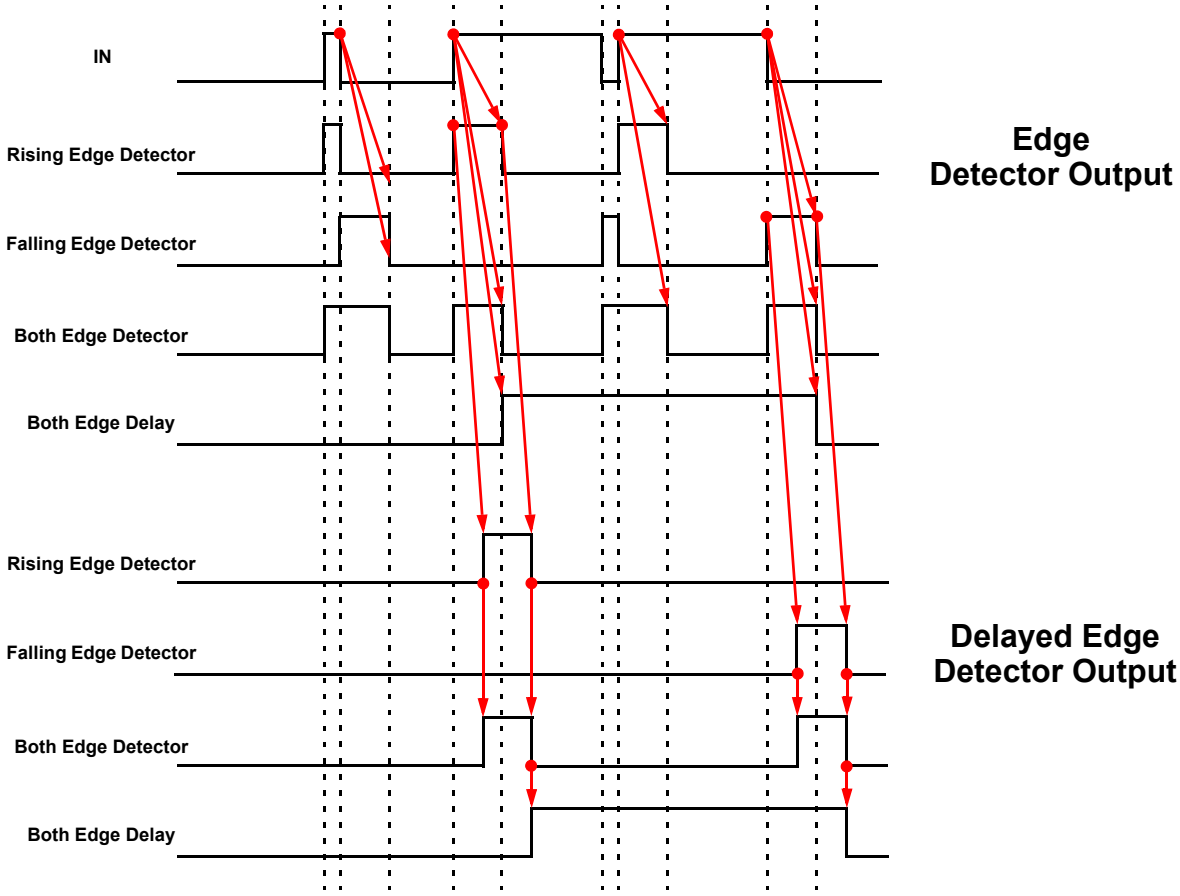


Figure 31. Glitch Filtering for Edge Detector Output

14.3 Programmable Delay Register Settings

Table 55. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition)	reg<1001:1000>	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
Select the edge mode of programmable delay & edge detector	reg<1003:1002>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Select edge detector output mode	reg<1004>	0: Edge Detector Output 1: Delayed Edge Detector Output

15.0 Additional Logic Functions

The SLG46170 has two additional logic functions that serve as deglitch filters.

15.1 Deglitch Filter

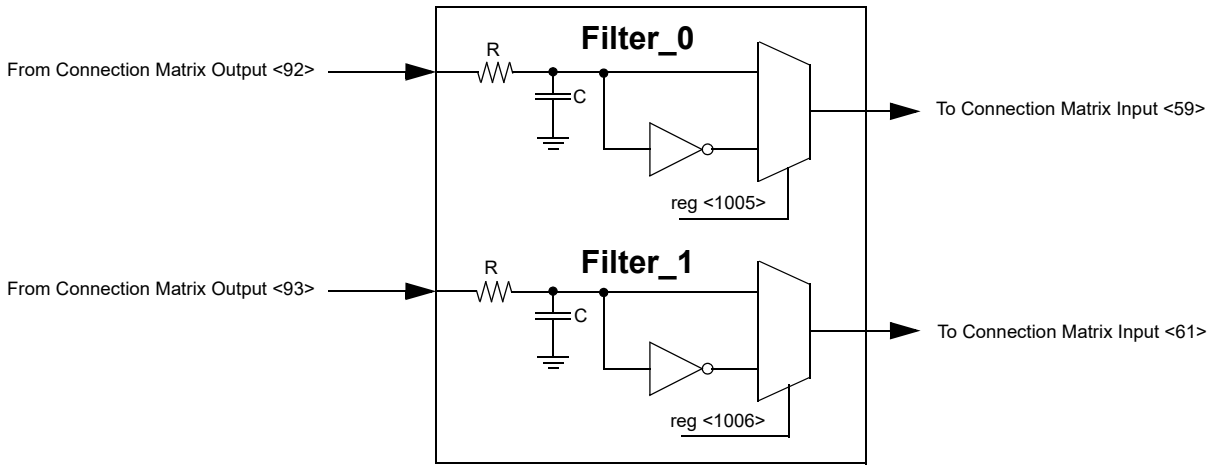


Figure 32. Deglitch Filter

16.0 RC Oscillator (RC Osc)

16.1 RC Oscillator Overview

The SLG46170 has two internal RC oscillators, one that runs at 25 kHz and one that runs at 2 MHz. The user can select one of these fundamental frequencies for the RC OSC Macrocell, or the fundamental frequency can also come from an external clock input (PIN 14). There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The first stage divider allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. The second stage divider has an input of one frequency from the first stage divider, and outputs five different frequencies on Connection Matrix Input lines <45>, <46>, <47>, <48>, and <49>. See *Figure 33* below for details of the frequencies for each of these five Connection Matrix Inputs.

If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH the oscillator will be turned off. The PWR DOWN signal has the highest priority.

The user can select two OSC POWER MODEs (reg<707>):

- If **AUTO POWER ON** <0> is selected, the OSC will run when the SLG46170 is powered on.
- If **FORCE POWER ON** <1> is selected, the OSC will run only when any macrocell that uses OSC is powered on.

OSC can be turned on by:

- Register control (force power on)
- Delay mode, when delay requires OSC
- CNT

16.2 RC OSC Block Diagram

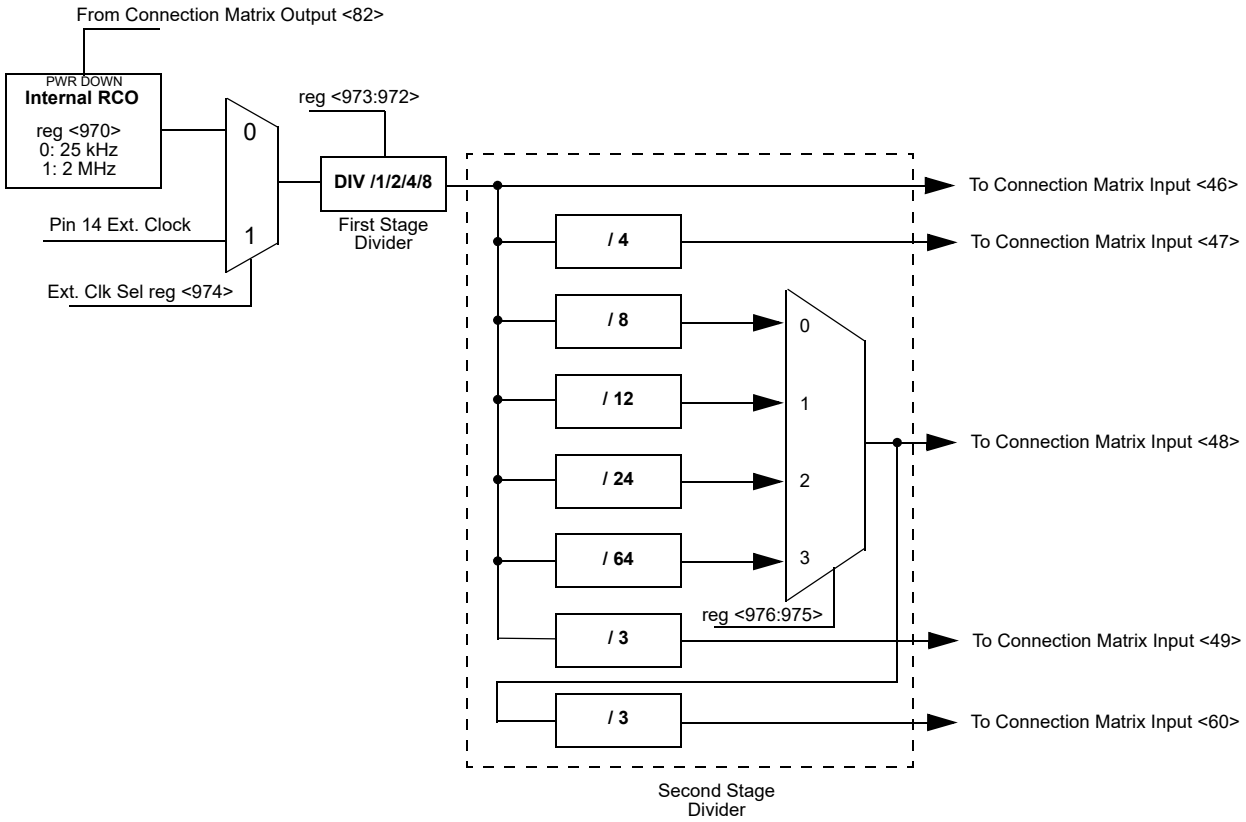


Figure 33. RC OSC Block Diagram

16.3 Oscillator Power On delay

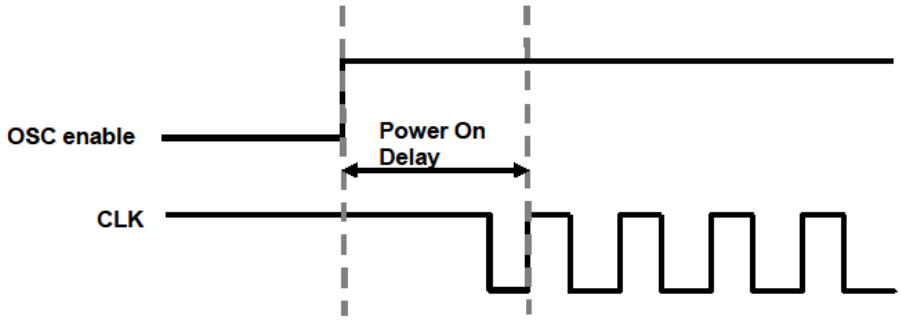


Figure 34. Oscillator Startup Diagram

Note 1: OSC power mode: "Auto Power On".

Note 2: 'OSC enable' signal appears when any macrocell that uses OSC is powered on.

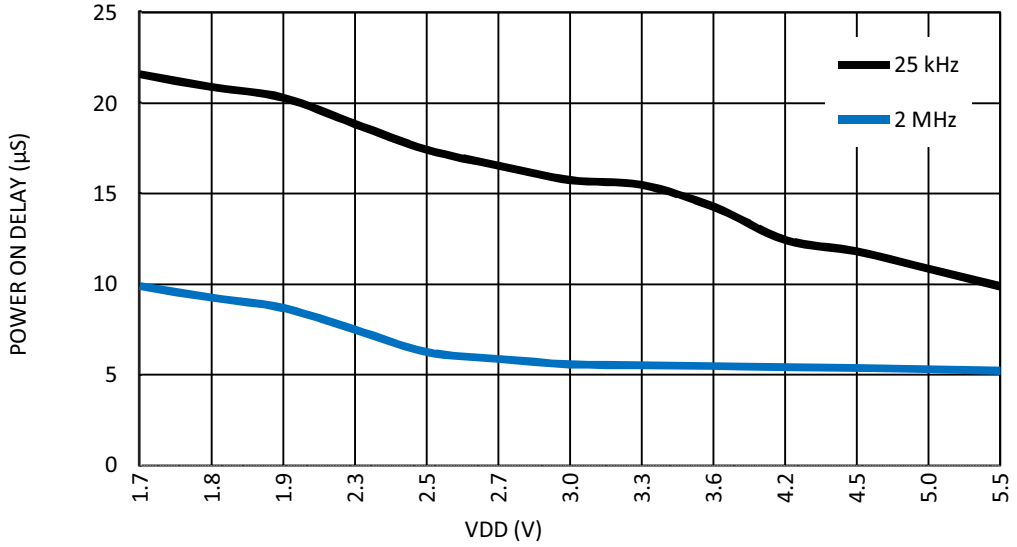


Figure 35. RC Oscillator Maximum Power On Delay vs. VDD at room temperature

16.4 Oscillator Accuracy

Note: OSC power setting: Force Power On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

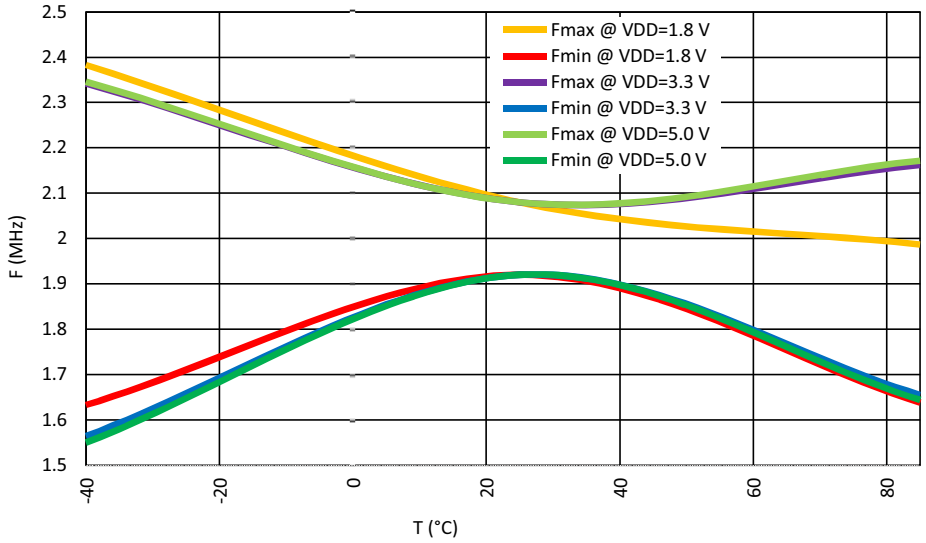


Figure 36. RC Oscillator Frequency vs. Temperature, RC OSC0=2 MHz

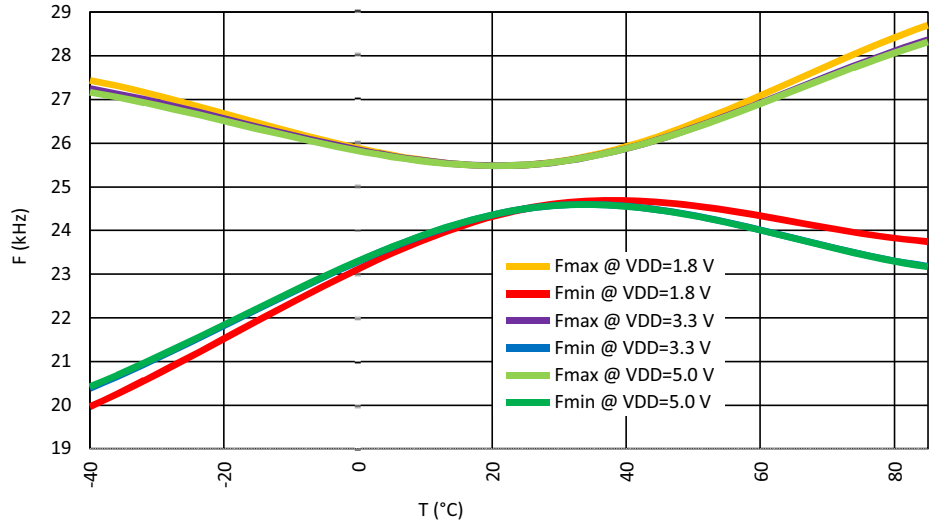


Figure 37. RC Oscillator Frequency vs. Temperature, RC OSC0=25 kHz

Note: For more information see section 5.10 OSC Specifications.

17.0 Power On Reset (POR)

17.1 POR Overview

The Power On Reset (POR) Macrocell will produce a high or “1” signal as an output when the device power supply (V_{DD}) rises to approximately 1.4 V. The typical internal delay for POR to release POR_IO will be 1 ms + α depending on the power slope, because there is adaptive power-up sequence. The next internal signal will be POR_CORE and then POR_IO_DLY, each of which is further delayed by approximately 1 µs. The rise of POR_IO_DLY will trigger the I/O pins to exit tri-state, and the device will become active.

17.2 POR Timing Diagram

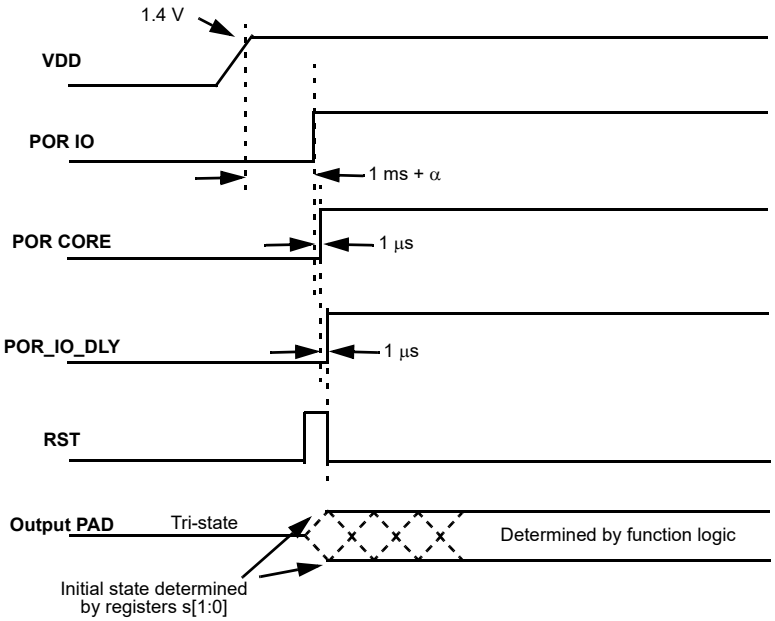


Figure 38. POR Timing Diagram

18.0 Appendix A - SLG46170 Register Definition

Register Bit Address	Signal Function	Register Bit Definition
reg<5:0>	Reserved	
reg<11:6>	Matrix Out	PIN3 Digital Output Source
reg<17:12>	Matrix Out	PIN4 Digital Output Source
reg<23:18>	Matrix Out	PIN5 Digital Output Source
reg<29:24>	Matrix Out	PIN6 Digital Output Source
reg<35:30>	Reserved	
reg<41:36>	Matrix Out	PIN7 Digital Output Source
reg<47:42>	Matrix Out	PIN8 Digital Output Source (4X Drive)
reg<53:48>	Matrix Out	Input for delay0 or Counter0 external clock
reg<59:54>	Matrix Out	Input for delay1 or counter1 reset input
reg<65:60>	Matrix Out	Input for Counter1 external clock or delay1 external clock
reg<71:66>	Matrix Out	Input for delay2 or counter2 reset input
reg<77:72>	Matrix Out	Input for Counter2 external clock or delay2 external clock
reg<83:78>	Matrix Out	Input for delay3 or counter3 reset input
reg<89:84>	Matrix Out	Input for Counter3 external clock or delay3 external clock
reg<95:90>	Matrix Out	Input for delay4 or Counter4 external clock
reg<101:96>	Matrix Out	Input for delay5 or Counter5 external clock
reg<107:102>	Matrix Out	Input for delay6 or Counter6 external clock
reg<113:108>	Matrix Out	Input for delay7 or Counter7 external clock
reg<119:114>	Matrix Out	Clock Input of DFF0
reg<125:120>	Matrix Out	Data Input of DFF0
reg<131:126>	Matrix Out	nRST (nSET) of DFF0
reg<137:132>	Matrix Out	Clock Input of DFF1
reg<143:138>	Matrix Out	Data Input of DFF1
reg<149:144>	Matrix Out	nRST (nSET) of DFF1
reg<155:150>	Matrix Out	Clock Input of DFF2
reg<161:156>	Matrix Out	Data Input of DFF2
reg<167:162>	Matrix Out	nRST (nSET) of DFF2
reg<173:168>	Matrix Out	Clock Input of DFF3
reg<179:174>	Matrix Out	Data Input of DFF3
reg<185:180>	Matrix Out	nRST (nSET) of DFF3
reg<191:186>	Matrix Out	Clock Input of DFF5
reg<197:192>	Matrix Out	Data Input of DFF5
reg<203:198>	Matrix Out	Clock Input of DFF6
reg<209:204>	Matrix Out	Data Input of DFF6
reg<215:210>	Matrix Out	In0 of LUT4_0
reg<221:216>	Matrix Out	In1 of LUT4_0
reg<227:222>	Matrix Out	In2 of LUT4_0

Register Bit Address	Signal Function	Register Bit Definition
reg<233:228>	Matrix Out	In3 of LUT4_0
reg<239:234>	Matrix Out	In0 of LUT3_0
reg<245:240>	Matrix Out	In1 of LUT3_0
reg<251:246>	Matrix Out	In2 of LUT3_0
reg<257:252>	Matrix Out	In0 of LUT3_1
reg<263:258>	Matrix Out	In1 of LUT3_1
reg<269:264>	Matrix Out	In2 of LUT3_1
reg<275:270>	Matrix Out	In0 of LUT3_2
reg<281:276>	Matrix Out	In1 of LUT3_2
reg<287:282>	Matrix Out	In2 of LUT3_2
reg<293:288>	Matrix Out	In0 of LUT3_3
reg<299:294>	Matrix Out	In1 of LUT3_3
reg<305:300>	Matrix Out	In2 of LUT3_3
reg<311:306>	Matrix Out	In0 of LUT3_4
reg<317:312>	Matrix Out	In1 of LUT3_4
reg<323:318>	Matrix Out	In2 of LUT3_4
reg<329:324>	Matrix Out	In0 of LUT3_5
reg<335:330>	Matrix Out	In1 of LUT3_5
reg<341:336>	Matrix Out	In2 of LUT3_5
reg<347:342>	Matrix Out	In0 of LUT3_6
reg<353:348>	Matrix Out	In1 of LUT3_6
reg<359:354>	Matrix Out	In2 of LUT3_6
reg<365:360>	Matrix Out	In0 of LUT3_7
reg<371:366>	Matrix Out	In1 of LUT3_7
reg<377:372>	Matrix Out	In2 of LUT3_7
reg<383:378>	Matrix Out	In0 of LUT3_8 or Input of Pipe delay
reg<389:384>	Matrix Out	In1 of LUT3_8 or nRST of Pipe delay
reg<395:390>	Matrix Out	In2 of LUT3_8 or Clock of Pipe delay
reg<401:396>	Matrix Out	In0 of LUT3_9
reg<407:402>	Matrix Out	In1 of LUT3_9
reg<413:408>	Matrix Out	In2 of LUT3_9
reg<419:414>	Matrix Out	In0 of LUT2_0 or Clock Input of DFF4
reg<425:420>	Matrix Out	In1 of LUT2_0 or Data Input of DFF4
reg<431:426>	Matrix Out	In0 of LUT2_1
reg<437:432>	Matrix Out	In1 of LUT2_1
reg<443:438>	Matrix Out	In0 of LUT2_2
reg<449:444>	Matrix Out	In1 of LUT2_2
reg<455:450>	Matrix Out	In0 of LUT2_3
reg<461:456>	Matrix Out	In1 of LUT2_3
reg<467:462>	Matrix Out	In0 of LUT2_4
reg<473:468>	Matrix Out	In1 of LUT2_4
reg<479:474>	Matrix Out	In0 of LUT2_5
reg<485:480>	Matrix Out	In1 of LUT2_5

Register Bit Address	Signal Function	Register Bit Definition
reg<491:486>	Matrix Out	Input for programmable delay & edge detector
reg<497:492>	Matrix Out	Power down for osc
reg<503:498>	Reserved	
reg<509:504>	Reserved	
reg<515:510>	Reserved	
reg<521:516>	Reserved	
reg<527:522>	Matrix Out	Pin10 Digital Output Source
reg<533:528>	Matrix Out	Pin11 Digital Output Source
reg<539:534>	Matrix Out	Pin12 Digital Output Source
reg<545:540>	Matrix Out	Pin13 Digital Output Source
reg<551:546>	Matrix Out	Pin14 Digital Output Source
reg<557:552>	Matrix Out	Input of filter_0
reg<563:558>	Matrix Out	Input of filter_1
reg<569:564>	Matrix Out	Reserved
reg<571:570>	Reserved	
reg<575:572>	LUT2_0 data or	
	reg<572> DFF4 or Latch select	0: DFF function 1: Latch function
	reg<573> DFF4 output select	0: Q output 1: nQ output
	reg<574> DFF4 initial polarity select	0: Low 1: High
reg<579:576>	LUT2_1 data	
reg<583:580>	LUT2_2 data	
reg<587:584>	LUT2_3 data	
reg<591:588>	LUT2_4 data	
reg<595:592>	LUT2_5 data	
reg<596>	LUT2_0 or DFF4 select	0: LUT2_0 1: DFF4
reg<604:597>	LUT3_0 data	
reg<612:605>	LUT3_1 data	
reg<620:613>	LUT3_2 data	
reg<628:621>	LUT3_3 data	
reg<636:629>	LUT3_4 data	
reg<644:637>	LUT3_5 data	
reg<652:645>	LUT3_6 data	
reg<660:653>	LUT3_7 data	
reg<668:661>	LUT3_8 data or pipe number select	
	reg<664: 661>: OUT0 select	
	reg<668: 665>: OUT1 select	
reg<676:669>	LUT3_9 data	

Register Bit Address	Signal Function	Register Bit Definition
reg<692:677>	LUT4_0 data	
reg<693>	DFF0 or Latch Select	0: DFF function 1: Latch function
reg<694>	DFF0 nRST/nSET select	0: nRST from matrix out 1: nSET from matrix out
reg<695>	DFF0 Initial polarity select	0: Low 1: High
reg<696>	DFF1 or Latch Select	0: DFF function 1: Latch function
reg<697>	DFF1 output select (Q or nQ)	0: Q output 1: nQ output
reg<698>	DFF1 nRST/nSET select	1: nSET from matrix out 0: nRST from matrix out
reg<699>	DFF1 Initial polarity select	0: Low 1: High
reg<700>	DFF2 or Latch Select	0: DFF function 1: Latch function
reg<701>	DFF2 output select (Q or nQ)	0: Q output 1: nQ output
reg<702>	DFF2 nRST/nSET select	1: nSET from matrix out 0: nRST from matrix out
reg<703>	DFF2 Initial polarity select	0: Low 1: High
reg<704>	DFF3 or Latch Select	0: DFF function 1: Latch function
reg<705>	DFF3 output select (Q or nQ)	0: Q output 1: nQ output
reg<706>	DFF3 nRST/nSET select	1: nSET from matrix out 0: nRST from matrix out
reg<707>	DFF3 Initial polarity select	0: Low 1: High
reg<708>	DFF5 or Latch Select	0: DFF function 1: Latch function
reg<709>	DFF5 output select (Q or nQ)	0: Q output 1: nQ output
reg<710>	DFF5 Initial polarity select	0: Low 1: High
reg<711>	DFF6 or Latch Select	0: DFF function 1: Latch function
reg<712>	DFF6 output select (Q or nQ)	0: Q output 1: nQ output
reg<713>	DFF6 Initial polarity select	0: Low 1: High
reg<714>	Counter/Delay0 mode select	0: Delay Mode 1: Counter Mode

Register Bit Address	Signal Function	Register Bit Definition
reg<717:715>	Counter/delay0 Clock Source Select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter 7 Overflow
reg<731:718>	Counter0 Control Data/Delay0 Time Control	1-16384: (delay time = (counter control data +2) /freq)
reg<733:732>	Delay0 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<734>	Counter/Delay1 mode select	0: Delay Mode 1: Counter Mode
reg<737:735>	Counter/delay1 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter 0 Overflow
reg<751:738>	Counter1 Control Data/Delay1 Time Control	1-16384: (delay time = (counter control data +2) /freq)
reg<753:752>	Delay1 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
reg<754>	Counter/Delay2 Mode selection	0: Delay Mode 1: Counter Mode
reg<757:755>	Counter/delay2 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter 1 Overflow
reg<765:758>	Counter2 Control Data/Delay2 Time Control	1-256: (delay time = (counter control data +2) /freq)
reg<767:766>	Delay2 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
reg<768>	Counter/Delay3 Mode selection	0: Delay Mode 1: Counter Mode

Register Bit Address	Signal Function	Register Bit Definition
reg<771:769>	Counter/delay3 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter 2 Overflow
reg<779:772>	Counter3 Control Data/Delay3 Time Control	1-256: (delay time = (counter control data +2) /freq)
reg<781:780>	Delay3 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
reg<782>	Counter/Delay4 Mode Selection	0: Delay Mode 1: Counter Mode
reg<785:783>	Counter/delay4 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter 3 Overflow
reg<793:786>	Counter4 Control Data/Delay4 Time Control	1-256: (delay time = (counter control data +2) /freq)
reg<795:794>	Delay4 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<796>	Counter/Delay5 Mode Selection	0: Delay Mode 1: Counter Mode
reg<799:797>	Counter/delay5 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter 4 Overflow
reg<807:800>	Counter5 Control Data/Delay5 Time Control	1-256: (delay time = (counter control data +2) /freq)
reg<809:808>	Delay5 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<810>	Counter/Delay6 Mode Selection	0: Delay Mode 1: Counter Mode

Register Bit Address	Signal Function	Register Bit Definition
reg<813:811>	Counter/delay6 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter 5 Overflow
reg<821:814>	Counter6 Control Data/Delay6 Time Control	1-256: (delay time = (counter control data +2) /freq)
reg<823:822>	Delay6 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<824>	Counter/Delay7 Mode Selection	0: Delay Mode 1: Counter Mode
reg<827:825>	Counter/Delay7 Mode Selection (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter 6 Overflow
reg<841:828>	Counter7 Control Data/Delay7 Time Control	1-16384:(delay time = (counter control data +2)/freq
reg<843:842>	Delay7 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
<845:844>	PIN2 mode control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
<847:846>	PIN2 pull down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<850:848>	Reserved	
<852:851>	Reserved	
<853>	Reserved	
<854>	Reserved	
<857:855>	PIN3 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<859:889>	PIN3 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
<860>	PIN3 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable

Register Bit Address	Signal Function	Register Bit Definition
<861>	PIN3 driver strength selection	0: 1X 1: 2X
<864:862>	PIN4 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<866:865>	PIN4 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<867>	PIN4 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<868>	PIN4 driver strength selection	0: 1X 1: 2X
<871:869>	PIN5 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<873:872>	PIN5 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<874>	PIN5 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<875>	PIN5 driver strength selection	0: 1X 1: 2X
<878:876>	PIN6 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<880:879>	PIN6 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<881>	PIN6 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<882>	PIN6 driver strength selection	0: 1X 1: 2X
<885:883>	Reserved	
<887:886>	Reserved	
<888>	Reserved	

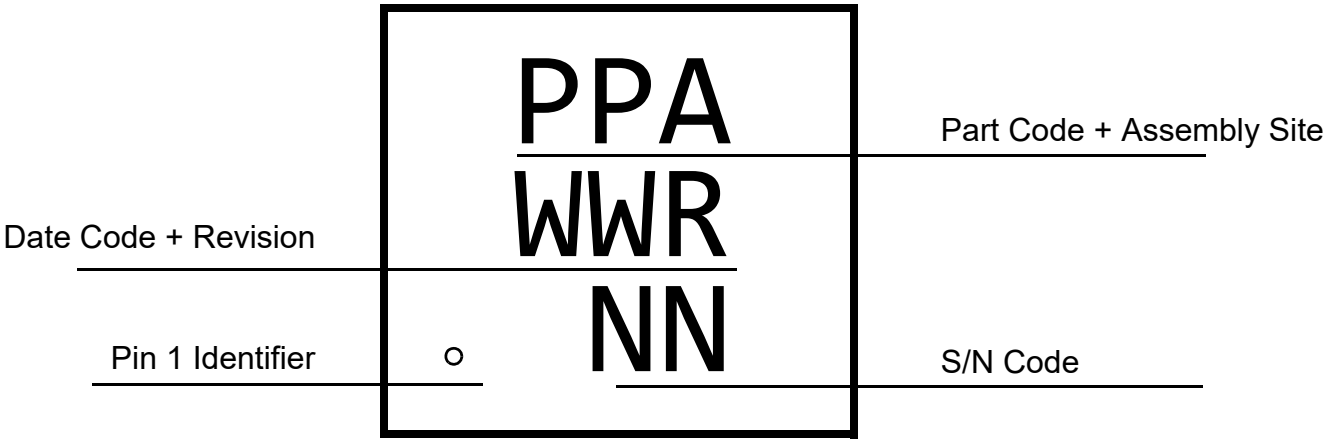
Register Bit Address	Signal Function	Register Bit Definition
<889>	Reserved	
<892:890>	PIN7 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<894:893>	PIN7 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
<895>	PIN7 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<896>	PIN7 driver strength selection	0: 1X 1: 2X
<899:897>	PIN8 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<901:900>	PIN8 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<902>	PIN8 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<903>	PIN8 driver strength selection	0: 1X 1: 2X
<904>	PIN8 4X Drive (4X, NMOS open drain) selection	0: 4X Drive off 1: 4X Drive on (if <899: 897> = 101)
<907:905>	Reserved	
<909:908>	Reserved	
<910>	Reserved	
<911>	Reserved	
<912>	Reserved	
<915:913>	Reserved	
<917:916>	Reserved	
<918>	Reserved	
<919>	Reserved	
<922:920>	Reserved	
<924:923>	Reserved	
<925>	Reserved	

Register Bit Address	Signal Function	Register Bit Definition
<926>	Reserved	
<929:927>	Reserved	
<931:930>	Reserved	
<932>	Reserved	
<933>	Reserved	
<936:934>	PIN10 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<938:937>	PIN10 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<939>	PIN10 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<940>	PIN10 driver strength selection	0: 1X 1: 2X
<943:941>	PIN11 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<945:944>	PIN11 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<946>	PIN11 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<947>	PIN11 driver strength selection	0: 1X 1: 2X
<950:948>	PIN12 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<952:951>	PIN12 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<953>	PIN12 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable

Register Bit Address	Signal Function	Register Bit Definition
<954>	PIN12 driver strength selection	0: 1X 1: 2X
<957:955>	PIN13 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<959:558>	PIN13 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<960>	PIN13 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<961>	PIN13 driver strength selection	0: 1X 1: 2X
<964:962>	PIN14 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
<966:965>	PIN14 pull up/down resistor value selection	00: floating 01: 10 K 10: 100 K 11: 1 M
<967>	PIN14 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
<968>	PIN14 driver strength selection	0: 1X 1: 2X
reg<969>	Force RC oscillator on	0: Auto Power on 1: Force Power on
reg<970>	RC Oscillator frequency control	0: 25 K 1: 2 M
reg<971>	Reserved	
reg<973:972>	Internal Oscillator frequency divider control	00: OSC/8 01: OSC/12 10: OSC/24 11: OSC/64
reg<974>	External Clock Source Select	0: Internal Oscillator 1: External Clock from Pin20
reg<976:975>	Osc clock pre-divider	00: Div1 01: Div2 10: Div4 11: Div8
reg<977>	LUT3_8 or pipe delay output select	0: Lut3_8 1: 1 pipe delay output
reg<978>	Pipe delay OUT1 polarity select bit	0: non-inverted 1: inverted

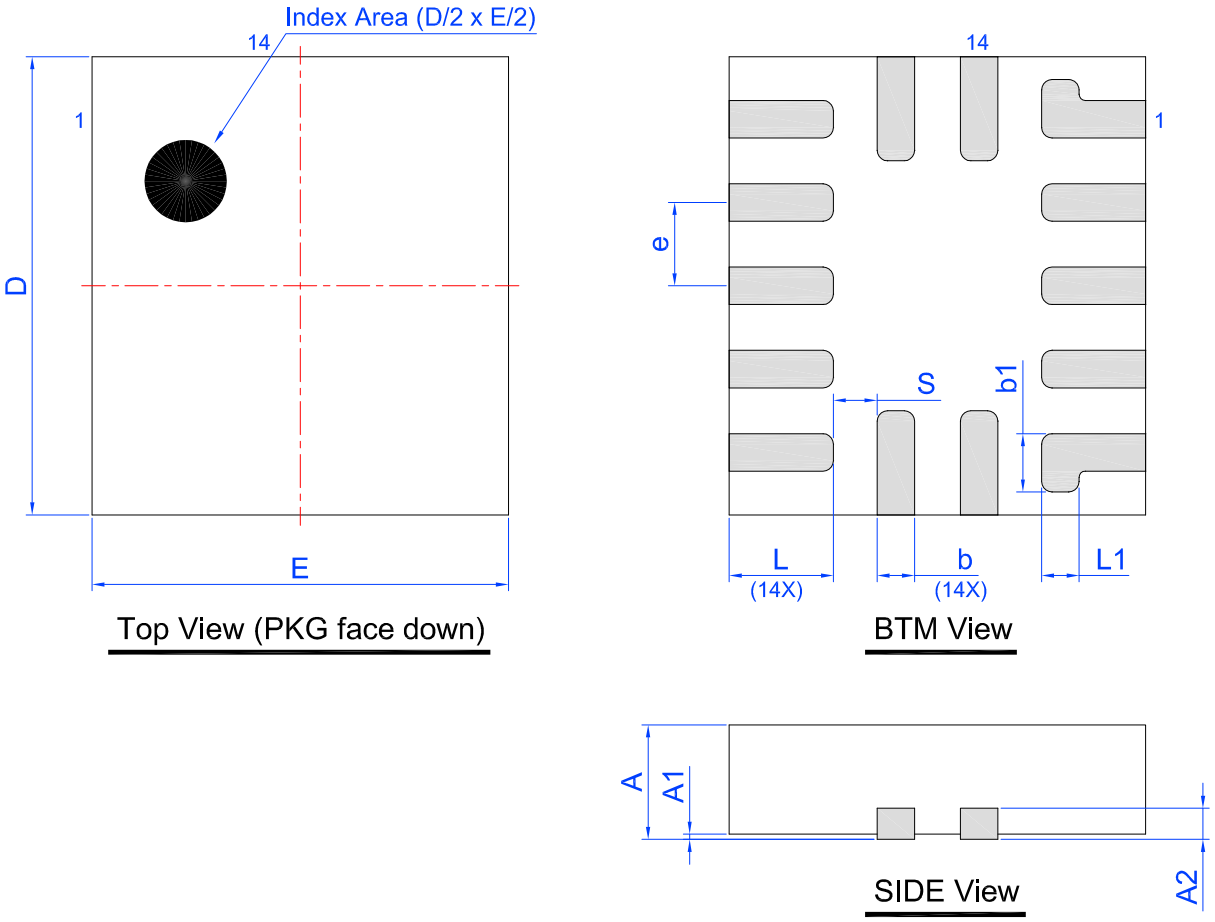
Register Bit Address	Signal Function	Register Bit Definition
reg<979>	NVM data read disable	0: Disable (program data can be read) 1: Enable (Program data cannot be read)
reg<980>	NVM power down	0: None (or programming enable) 1: Power Down (or programming disable)
reg<981>	GPIO quick charge enable	0: Disable 1: Enable
reg<983: 982>	Reserved	
reg<991:984>	Reserved	
reg<999:992>	8-bit Pattern ID	
reg<1001:1000>	Delay value select for programmable delay & edge detector (VDD 3.3V, typ)	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
reg<1003:1002>	Select the edge mode of programmable delay & edge detector	00: rising edge detector 01: falling edge detector 10: both edge detector 11: both edge delay
reg<1004>	Select edge detector output mode	0: edge detector output 1: delayed edge detector output
reg<1005>	Select polarity of filter_0 output	0: non-inverted 1: inverted
reg<1006>	Select polarity of filter_1 output	0: non-inverted 1: inverted
reg<1007>	Reserved	
reg<1013:1008 >	Reserved	
reg<1014>	Reserved	
reg<1015>	Reserved	
reg<1023:1016>	Reserved	

19.0 Package Top Marking System Definition



20.0 Package Drawing and Dimensions

STQFN 14L 2 x 2.2mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

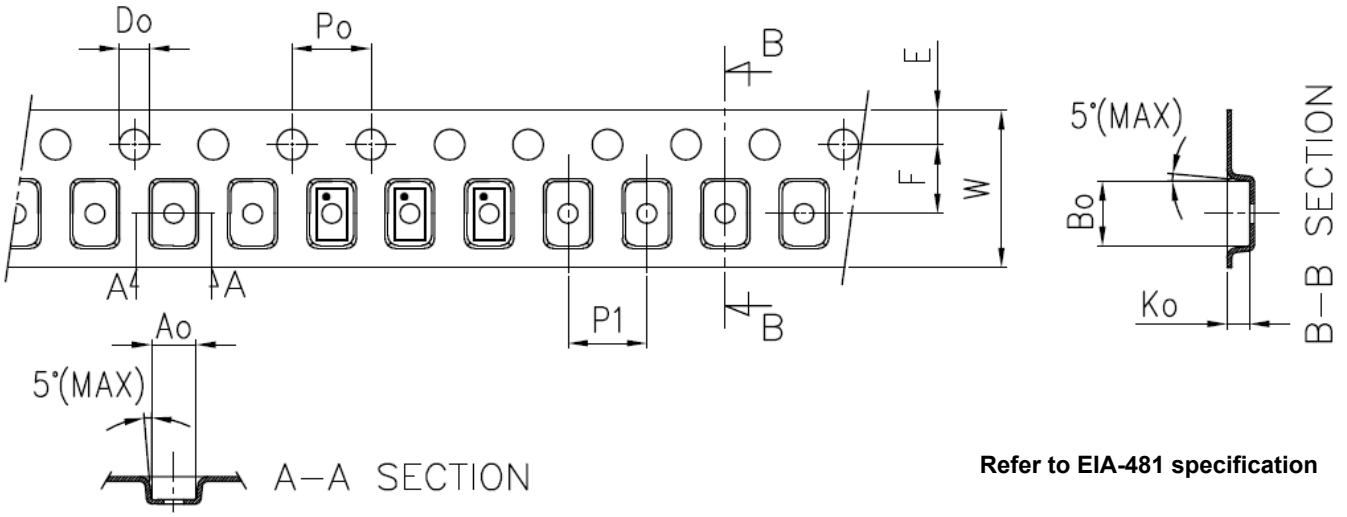
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.15	2.20	2.25
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.45	0.50	0.55
b	0.13	0.18	0.23	S	0.21 TYP		
e	0.40 BSC			b1	0.28 TYP		
				L1	0.18 TYP		

21.0 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 2x2.2 mm 0.4P COL	14	2 x 2.2 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

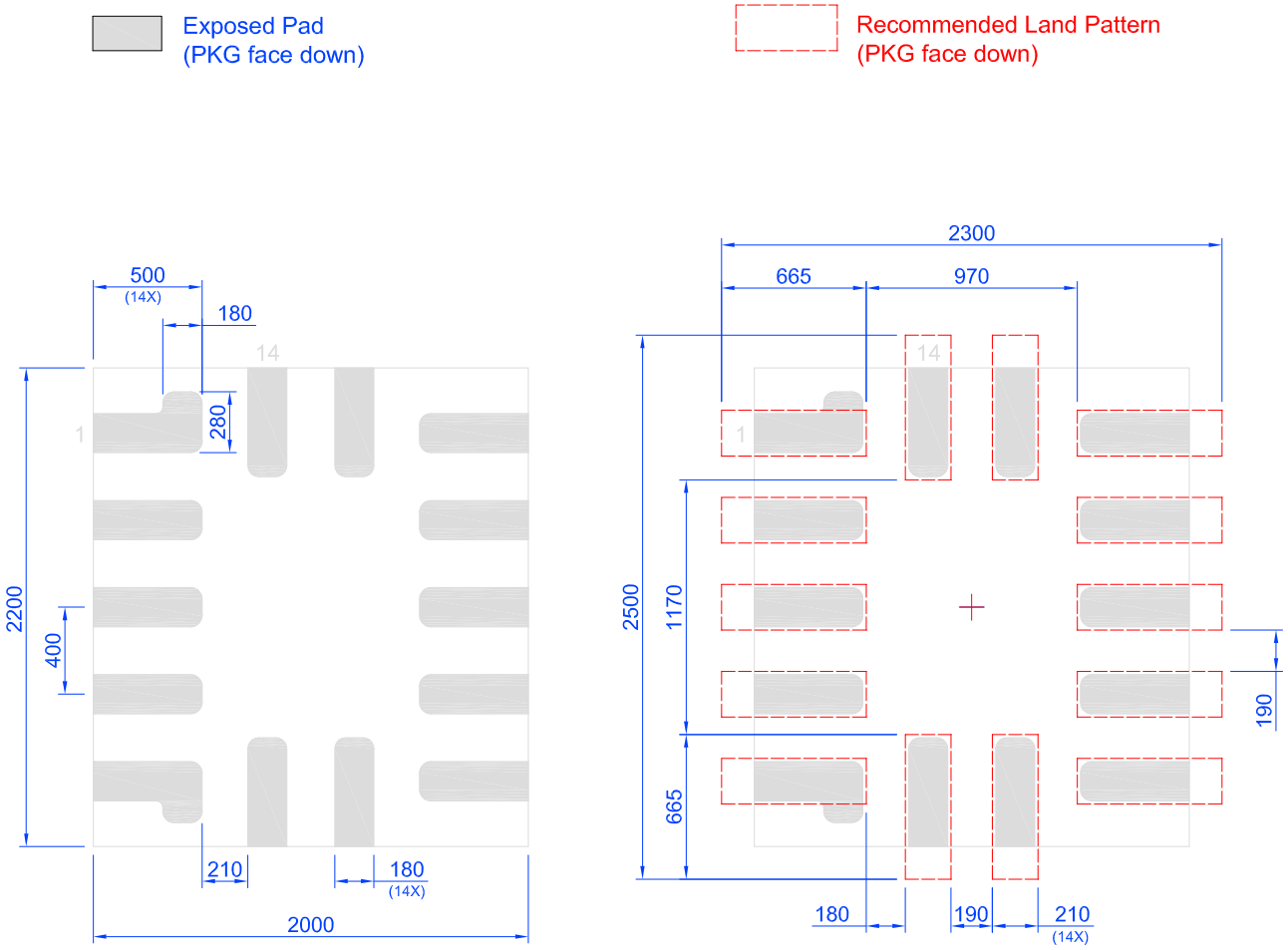
21.1 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 2x2.2 mm 0.4P COL	2.2	2.35	0.8	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

22.0 Recommended Landing Pattern



Unit:um

23.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.42 mm^3 (nominal). More information can be found at www.jedec.org.

24.0 Revision History

Date	Version	Change
10/10/2017	1.03	Updated Electrical Spec Fixed typos
7/5/2017	1.02	Fixed typos Updated Silego Website & Support Updated Section Programmable Delay / Edge Detector Updated Electrical Spec
10/20/2016	1.01	Removed references to GPAK families
9/28/2016	1.00	Production Release

Silego Website & Support

Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit our website.

Our Green product lines feature:

GreenPAK: Programmable Mixed Signal Matrix products
GreenFET1 / GreenFET3 / HFET1: MOSFET Drivers and ultra-small, low RDSon Load Switches
GreenCLK1 / GreenCLK2 / GreenCLK3: Crystal replacement technology

Products are also available for purchase directly from Silego at the Silego Online Store at http://www.silego.com/buy/.

Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send e-mail requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

Contact Your Local Sales Representative

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

Contact Silego Directly

Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following URL:

http://support.silego.com/

Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of world wide Silego Technology offices and representatives are all available at http://www.silego.com/

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