

Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

General Description

The MAX16807/MAX16808 are integrated, high-efficiency white or RGB LED drivers. They are designed for LCD backlighting and other LED lighting applications with multiple strings of LEDs. The MAX16807/MAX16808's current-mode PWM controller regulates the necessary voltage to the LED array. Depending on the input voltage and LED voltage range, it can be used with boost or buck-boost (SEPIC) topologies. The MAX16807/MAX16808 feature an 8V to 26.5V input voltage range. A wide range of adjustable frequency (20kHz to 1MHz) allows design optimization for efficiency and minimum board space.

The MAX16807/MAX16808 LED drivers include eight open-drain, constant-current-sinking LED driver outputs rated for 36V continuous operation. The LED current-control circuitry achieves $\pm 3\%$ current matching among strings and enables paralleling of outputs for LED string currents higher than 55mA. The output-enable pin is used for simultaneous PWM dimming of all output channels. Dimming frequency range is 50Hz to 30kHz and dimming ratio is up to 5000:1. The constant-current outputs are single resistor programmable and the LED current can be adjusted up to 55mA per output channel.

The MAX16807/MAX16808 operate either in stand-alone mode or with a microcontroller (μC) using an industry-standard, 4-wire serial interface. The MAX16808 includes circuitry that automatically detects open-circuit LEDs.

The MAX16807/MAX16808 include overtemperature protection, operate over the full -40°C to $+125^{\circ}\text{C}$ temperature range, and are available in a thermally enhanced, 28-pin TSSOP exposed paddle package.

Pin Configurations appear at end of data sheet.

Features

- ◆ Eight Constant-Current Output Channels (Up to 55mA Each)
- ◆ $\pm 3\%$ Current Matching Among Outputs
- ◆ Paralleling Channels Allows Higher Current per LED String
- ◆ Outputs Rated for 36V Continuous Voltage
- ◆ Output-Enable Pin for PWM Dimming (Up to 30kHz)
- ◆ One Resistor Sets LED Current for All Channels
- ◆ Wide Dimming Ratio Up to 5000:1
- ◆ Low Current-Sense Reference (300mV) for High Efficiency
- ◆ 8V to 26.5V Input Voltage or Higher with External Biasing Devices
- ◆ Open LED Detection (MAX16808)
- ◆ 4-Wire Serial Interface to Control Individual Output Channels

Applications

LCD White or RGB LED Backlighting:
LCD TVs, Desktop, and Notebook Panels
Automotive Navigation, Heads-Up,
and Infotainment Displays
Industrial and Medical Displays
Ambient, Mood, and Accent Lighting

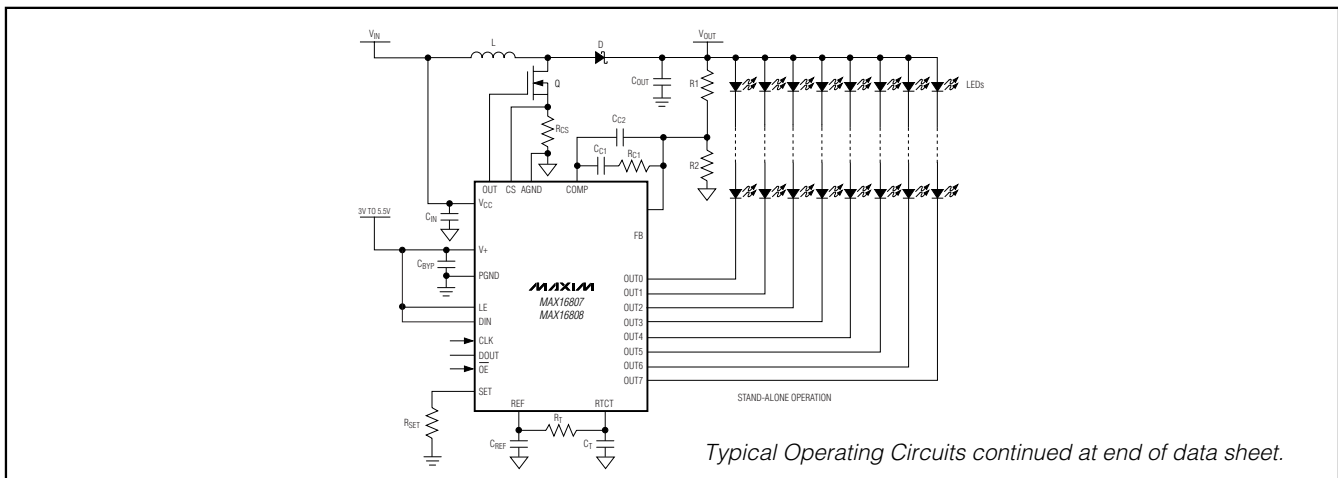
Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|--------------|---|--------------|----------|
| MAX16807AUI+ | -40°C to $+125^{\circ}\text{C}$ | 28 TSSOP-EP* | U28ME-1 |
| MAX16808AUI+ | -40°C to $+125^{\circ}\text{C}$ | 28 TSSOP-EP* | U28ME-1 |

+ Denotes a lead-free package.

* EP = Exposed paddle.

Typical Operating Circuits



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ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|-----------------------------------|---|-----------------|
| V _{CC} to AGND..... | -0.3V to +30V | OUT0–OUT7 Sink Current..... | 60mA |
| Current into V _{CC} (V _{CC} > 24V)..... | ±30mA | Total PGND Current..... | 480mA |
| V+ to PGND..... | -0.3V to +6V | Continuous Power Dissipation (T _A = +70°C) | |
| OUT to AGND..... | -0.3V to (V _{CC} + 0.3V) | 28-Pin TSSOP (derate 27mW/°C* above +70°C)..... | 2162mW |
| OUT Current (10μs duration)..... | ±1A | Operating Temperature Range..... | -40°C to +125°C |
| FB, COMP, CS, RTCT, REF to AGND..... | -0.3V to +6V | Junction Temperature..... | +150°C |
| COMP Sink Current..... | 10mA | Storage Temperature Range..... | -65°C to +150°C |
| OUT0–OUT7 to PGND..... | -0.3V to +40V | Lead Temperature (soldering, 10s)..... | +300°C |
| DIN, CLK, LE, OE, SET to PGND..... | -0.3V to (V+ + 0.3V) | | |
| DOUT Current..... | ±10mA | | |

*Per JEDEC51 Standard (Multilayer Board).

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (PWM CONTROLLER)

(V_{CC} = +15V, V+ = +3V to +5.5V referenced to PGND, R_T = 10kΩ, C_T = 3.3nF, REF = open, COMP = open, C_{REF} = 0.1μF, V_{FB} = 2V, CS = AGND, AGND = PGND = 0V; all voltages are measured with respect to AGND, unless otherwise noted. T_J = T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|---------------------|--|-------|-------|-------|-------|
| REFERENCE | | | | | | |
| Output Voltage | V _{REF} | I _{REF} = 1mA, T _J = +25°C | 4.95 | 5 | 5.05 | V |
| Line Regulation | ΔV _{LINE} | 12V < V _{CC} < 25V, I _{REF} = 1mA | | 0.4 | 4 | mV |
| Load Regulation | ΔV _{LOAD} | 1mA < I _{REF} < 20mA | | 6 | 50 | mV |
| Total Output-Voltage Variation | V _{REFT} | (Note 2) | 4.875 | | 5.125 | V |
| Output Noise Voltage | V _{NOISE} | 10Hz < f < 10kHz | | 50 | | μV |
| Output Short-Circuit Current | I _{SHORT} | V _{REF} = 0V | 30 | | 180 | mA |
| OSCILLATOR | | | | | | |
| Initial Accuracy | | T _J = +25°C | 51 | 54 | 57 | kHz |
| Voltage Stability | | 12V < V _{CC} < 25V | | 0.2 | 0.5 | % |
| Temperature Stability | | | | 1 | | % |
| RTCT Ramp Peak-to-Peak | | | | 1.7 | | V |
| RTCT Ramp Valley | | | | 1.1 | | V |
| Discharge Current | I _{DIS} | V _{RTCT} = 2V, T _J = +25°C | 7.9 | 8.3 | 8.7 | mA |
| | | V _{RTCT} = 2V, -40°C ≤ T _J ≤ +125°C | 7.5 | 8.3 | 9.0 | |
| Frequency Range | f _{OSC} | | 20 | | 1000 | kHz |
| ERROR AMPLIFIER | | | | | | |
| FB Input Voltage | V _{FB} | FB shorted to COMP | 2.45 | 2.50 | 2.55 | V |
| Input Bias Current | I _{B(FB)} | | | -0.01 | -0.1 | μA |
| Open-Loop Gain | A _{VOL} | 2V ≤ V _{COMP} ≤ 4V | | 100 | | dB |
| Unity-Gain Bandwidth | f _{GBW} | | | 1 | | MHz |
| Power-Supply Rejection Ratio | PSRR | 12V ≤ V _{CC} ≤ 25V | 60 | 80 | | dB |
| COMP Sink Current | I _{SINK} | V _{FB} = 2.7V, V _{COMP} = 1.1V | 2 | 6 | | mA |
| COMP Source Current | I _{SOURCE} | V _{FB} = 2.3V, V _{COMP} = 5V | 0.5 | 1.2 | 1.8 | mA |
| COMP Output-Voltage High | V _{OH} | V _{FB} = 2.3V, R _{COMP} = 15kΩ to AGND | 5 | 5.8 | | V |
| COMP Output-Voltage Low | V _{OL} | V _{FB} = 2.7V, R _{COMP} = 15kΩ to V _{REF} | | 0.1 | 1.1 | V |

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ELECTRICAL CHARACTERISTICS (PWM CONTROLLER) (continued)

($V_{CC} = +15V$, $V_+ = +3V$ to $+5.5V$ referenced to PGND, $R_T = 10k\Omega$, $C_T = 3.3nF$, REF = open, COMP = open, $C_{REF} = 0.1\mu F$, $V_{FB} = 2V$, CS = AGND, AGND = PGND = 0V; all voltages are measured with respect to AGND, unless otherwise noted. $T_J = T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|-----------------------|--|--|-------|-------|---------|----------|
| CURRENT-SENSE AMPLIFIER | | | | | | | |
| Current-Sense Gain | ACS | (Notes 3, 4) | 2.85 | 3.00 | 3.40 | V/V | |
| Maximum Current-Sense Signal | VCS_MAX | (Note 3) | 0.275 | 0.300 | 0.325 | V | |
| Power-Supply Rejection Ratio | PSRR | $12V \leq V_{CC} \leq 25V$ | | 70 | | dB | |
| Current-Sense Input Bias Current | I _{CS} | $V_{COMP} = 0V$ | | -1 | -2.5 | μA | |
| Current Sense to OUT Delay | t _{PWM} | 50mV overdrive | | 60 | | ns | |
| MOSFET DRIVER | | | | | | | |
| OUT Low-Side On-Resistance | V _{RDS_ONL} | I _{SINK} = 200mA | T _J = -40°C to +85°C (Note 2) | | 4.5 | 10 | Ω |
| | | | T _J = -40°C to +125°C | | 4.5 | 12 | |
| OUT High-Side On-Resistance | V _{RDS_ONH} | I _{SOURCE} = 100mA | T _J = -40°C to +85°C (Note 2) | | 3.5 | 7.5 | Ω |
| | | | T _J = -40°C to +125°C | | 3.5 | 10 | |
| Source Current (Peak) | I _{SOURCE} | C _{LOAD} = 10nF | | 2 | | A | |
| Sink Current (Peak) | I _{SINK} | C _{LOAD} = 10nF | | 1 | | A | |
| Rise Time | t _R | C _{LOAD} = 1nF | | 15 | | ns | |
| Fall Time | t _F | C _{LOAD} = 1nF | | 22 | | ns | |
| UNDERVOLTAGE LOCKOUT/STARTUP | | | | | | | |
| Startup Voltage Threshold | V _{CC_START} | | 7.98 | 8.4 | 8.82 | V | |
| Minimum Operating Voltage After Turn-On | V _{CC_MIN} | | 7.1 | 7.6 | 8.0 | V | |
| Undervoltage-Lockout Hysteresis | UVLO _{HYST} | | | 0.8 | | V | |
| PULSE-WIDTH MODULATION (PWM) | | | | | | | |
| Maximum Duty Cycle | D _{MAX} | | 94.5 | 96 | 97.5 | % | |
| Minimum Duty Cycle | D _{MIN} | | | | 0 | % | |
| SUPPLY CURRENT | | | | | | | |
| Startup Supply Current | I _{START} | V _{CC} = 7.5V | | 32 | 65 | μA | |
| Operating Supply Current | I _{CC} | V _{FB} = V _{CS} = 0V | | 3 | 5 | mA | |
| V _{CC} Zener Voltage | V _Z | I _{CC} = 25mA | 24 | 26.5 | | V | |

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ELECTRICAL CHARACTERISTICS (LED DRIVER)

(V+ = +3V to +5.5V, AGND = PGND = 0V; all voltages are measured with respect to PGND, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|-------------|-----|--------------|-------|
| Operating Supply Voltage | V+ | | 3.0 | | 5.5 | V |
| Output Voltage | V _{OUT_} | | | | 36 | V |
| Standby Current (Interface Idle, All Output Ports High Impedance) | | R _{SET} = 360Ω, DIN, LE, CLK = PGND or V+, \overline{OE} = V+, DOUT unconnected | | 3.6 | 4.5 | mA |
| Standby Current (Interface Active, All Output Ports High Impedance) | | R _{SET} = 360Ω, f _{CLK} = 5MHz, \overline{OE} = V+, DIN, LE = PGND or V+, DOUT unconnected | | 3.8 | 4.8 | mA |
| Supply Current (Interface Idle, All Output Ports Active Low) | I+ | R _{SET} = 360Ω, \overline{OE} = PGND, DIN, LE = V+, DOUT unconnected | | 17 | 30 | mA |
| INTERFACE (DIN, CLK, DOUT, LE, \overline{OE}) | | | | | | |
| Input-Voltage High (DIN, CLK, LE, \overline{OE}) | V _{IH} | | 0.7 x V+ | | | V |
| Input-Voltage Low (DIN, CLK, LE, \overline{OE}) | V _{IL} | | | | 0.3 x V+ | V |
| Hysteresis Voltage (DIN, CLK, LE, \overline{OE}) | V _{HYST} | | | 0.8 | | V |
| Input Leakage Current (DIN, CLK) | I _{LEAK} | | -1 | | +1 | μA |
| \overline{OE} Pullup Current to V+ | I _{\overline{OE}} | V+ = 5.5V, \overline{OE} = PGND | 0.25 | 1.5 | 25.0 | μA |
| LE Pulldown Current to PGND | I _{LE} | V+ = 5.5V, LE = V+ | 0.25 | 1.5 | 25.0 | μA |
| Output-Voltage High (DOUT) | V _{OH} | I _{SOURCE} = 4mA | | | V+ - 0.5V | V |
| Output-Voltage Low (DOUT) | V _{OL} | I _{SINK} = 4mA | | | 0.5 | V |
| OUT_ Output Current | I _{OUT_} | 0°C ≤ T _A ≤ +125°C, V _{OUT} = 1V to 2.5V, R _{SET} = 360Ω | 46.5 | 50 | 53.5 | mA |
| | | T _A = -40°C, V _{OUT} = 1V to 2.5V, R _{SET} = 360Ω | 43 | | 57 | |
| OUT_ Leakage Current | | \overline{OE} = V+ | | | 1 | μA |
| OUT_ Fault Detection Threshold (MAX16808) | V _{OUTH} | V+ = 5.5V, \overline{OE} = V+ | | 0.8 | | V |

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5V TIMING CHARACTERISTICS

(V+ = +4.5V to +5.5V, AGND = PGND = 0V; all voltages are measured with respect to PGND, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 5)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--|-----------------------------|--------------------------------------|-----|-----|-----|-------|
| INTERFACE TIMING CHARACTERISTICS | | | | | | |
| CLK Clock Period | t _{CP} | | 40 | | | ns |
| CLK Pulse-Width High | t _{CH} | | 19 | | | ns |
| CLK Pulse-Width Low | t _{CL} | | 19 | | | ns |
| DIN Setup Time | t _{DS} | | 4 | | | ns |
| DIN Hold Time | t _{DH} | | 8 | | | ns |
| DOUT Propagation Delay | t _{DO} | | 12 | | 50 | ns |
| DOUT Rise Time | t _{DR} | C _{DOUT} = 10pF, 20% to 80% | | | 10 | ns |
| DOUT Fall Time | t _{DF} | C _{DOUT} = 10pF, 80% to 20% | | | 10 | ns |
| LE Pulse-Width High | t _{LW} | | 20 | | | ns |
| LE Setup Time | t _{LS} | | 15 | | | ns |
| LE Rising to OUT_ Rising Delay | t _{LRR} | (Note 6) | | | 110 | ns |
| LE Rising to OUT_ Falling Delay | t _{LRF} | (Note 6) | | | 325 | ns |
| CLK Rising to OUT_ Rising Delay | t _{CRR} | (Note 6) | | | 110 | ns |
| CLK Rising to OUT_ Falling Delay | t _{CRF} | (Note 6) | | | 325 | ns |
| $\overline{\text{OE}}$ Rising to OUT_ Rising Delay | t _{OE_R} | (Note 6) | | | 110 | ns |
| $\overline{\text{OE}}$ Falling to OUT_ Falling Delay | t _{OE_F} | (Note 6) | | | 325 | ns |
| OUT_ Turn-On Fall Time | t _F | 80% to 20% (Note 6) | | | 210 | ns |
| OUT_ Turn-Off Rise Time | t _R | 20% to 80% (Note 6) | | | 130 | ns |

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3.3V TIMING CHARACTERISTICS

(V+ = +3V to < +4.5V, AGND = PGND = 0V; all voltages are measured with respect to PGND, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 5)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|--------------------------------------|-----|-----|-----|-------|
| INTERFACE TIMING CHARACTERISTICS | | | | | | |
| CLK Clock Period | t _{CP} | | 52 | | | ns |
| CLK Pulse-Width High | t _{CH} | | 24 | | | ns |
| CLK Pulse-Width Low | t _{CL} | | 24 | | | ns |
| DIN Setup Time | t _{DS} | | 4 | | | ns |
| DIN Hold Time | t _{DH} | | 8 | | | ns |
| DOUT Propagation Delay | t _{DO} | | 12 | | 70 | ns |
| DOUT Rise Time | t _{DR} | C _{DOUT} = 10pF, 20% to 80% | | | 12 | ns |
| DOUT Fall Time | t _{DF} | C _{DOUT} = 10pF, 80% to 20% | | | 12 | ns |
| LE Pulse-Width High | t _{LW} | | 20 | | | ns |
| LE Setup Time | t _{LS} | | 15 | | | ns |
| LE Rising to OUT_ Rising Delay | t _{LRR} | (Note 6) | | | 140 | ns |
| LE Rising to OUT_ Falling Delay | t _{LRF} | (Note 6) | | | 350 | ns |
| CLK Rising to OUT_ Rising Delay | t _{CRR} | (Note 6) | | | 140 | ns |
| CLK Rising to OUT_ Falling Delay | t _{CRF} | (Note 6) | | | 350 | ns |
| OE Rising to OUT_ Rising Delay | t _{OER} | (Note 6) | | | 140 | ns |
| OE Falling to OUT_ Falling Delay | t _{OEF} | (Note 6) | | | 350 | ns |
| OUT_ Turn-On Fall Time | t _F | 80% to 20% (Note 6) | | | 275 | ns |
| OUT_ Turn-Off Rise Time | t _R | 20% to 80% (Note 6) | | | 150 | ns |

Note 1: All devices are 100% production tested at T_J = +25°C and +125°C. Limits to -40°C are guaranteed by design.

Note 2: Guaranteed by design, not production tested.

Note 3: Parameter is measured at trip point of latch with V_{FB} = 0V.

Note 4: Gain is defined as $A = \Delta V_{COMP} / \Delta V_{CS}$, $0.05V \leq V_{CS} \leq 0.25V$.

Note 5: See Figures 3 and 4.

Note 6: A 65Ω pullup resistor is connected from OUT_ to 5.5V. Rising refers to V_{OUT_} when current through OUT_ is turned off and falling refers to V_{OUT_} when current through OUT_ is turned on.

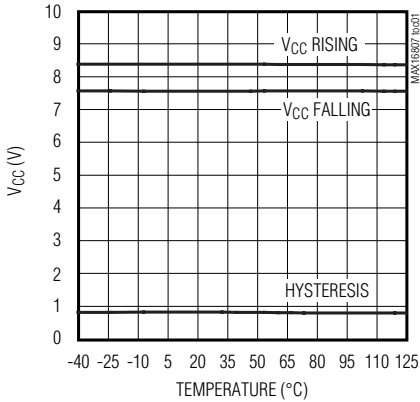
Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

Typical Operating Characteristics

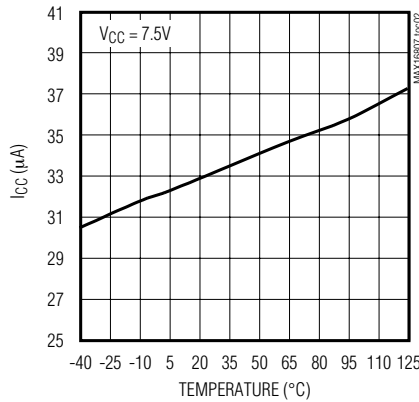
($V_{CC} = +15V$, $V_+ = 3V$ to $5.5V$, $R_T = 10k\Omega$, $C_T = 3.3nF$, $V_{REF} = COMP = open$, $C_{REF} = 0.1\mu F$, $V_{FB} = 2V$, $CS = AGND = PGND = 0V$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

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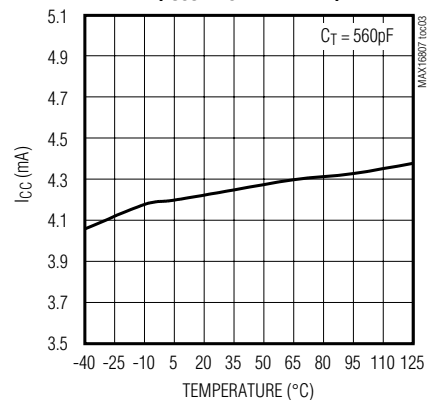
BOOTSTRAP UVLO vs. TEMPERATURE



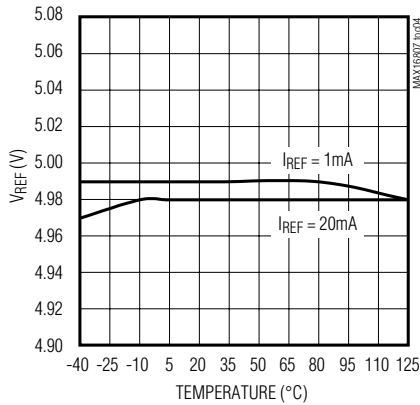
STARTUP CURRENT vs. TEMPERATURE



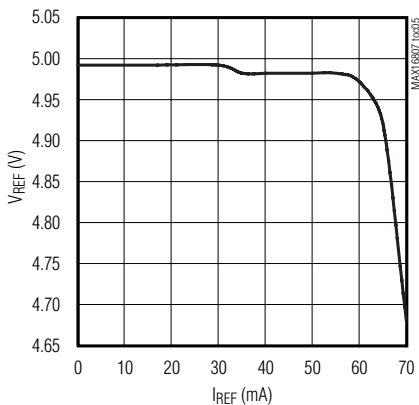
OPERATING SUPPLY CURRENT vs. TEMPERATURE AFTER STARTUP
($f_{osc} = f_{sw} = 300kHz$)



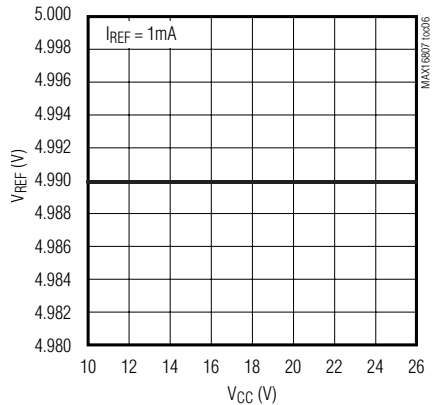
REFERENCE VOLTAGE vs. TEMPERATURE



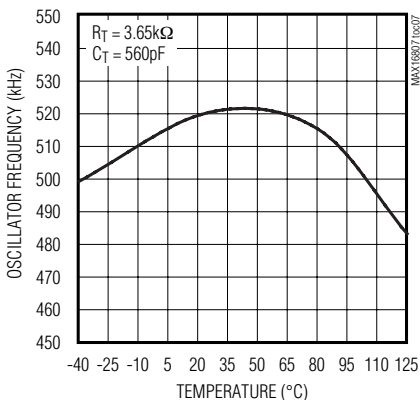
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



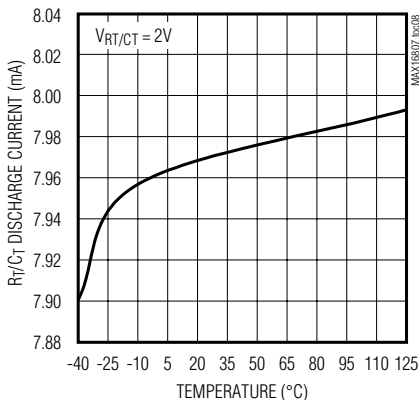
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



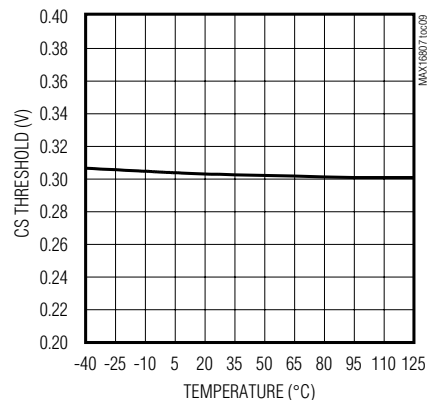
OSCILLATOR FREQUENCY (f_{osc}) vs. TEMPERATURE



OSCILLATOR R_T/C_T DISCHARGE CURRENT vs. TEMPERATURE



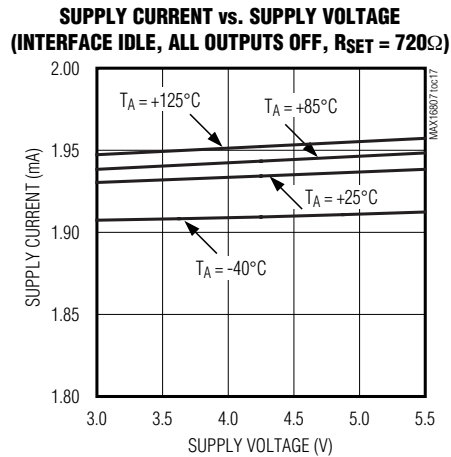
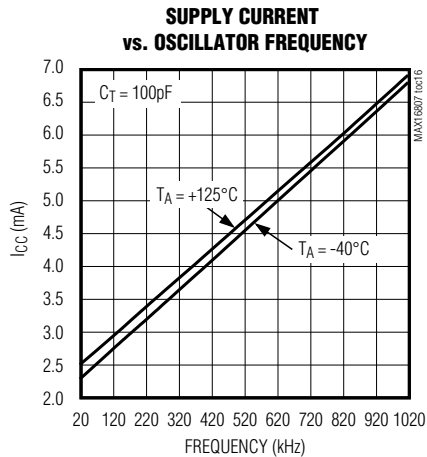
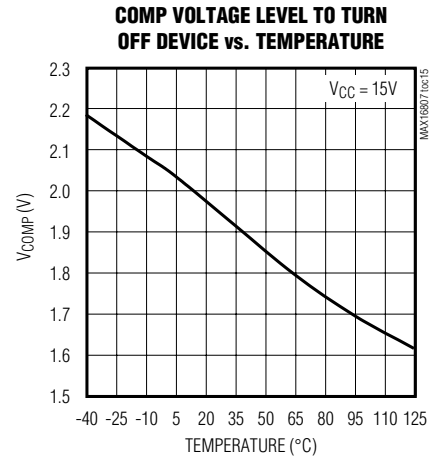
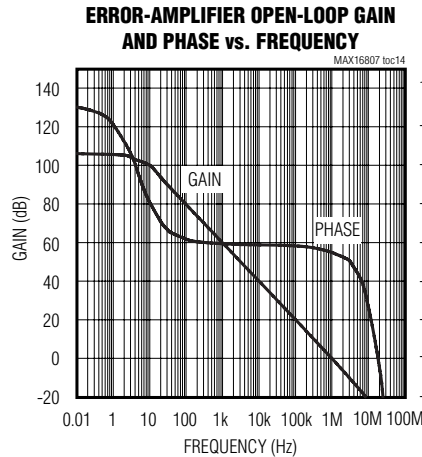
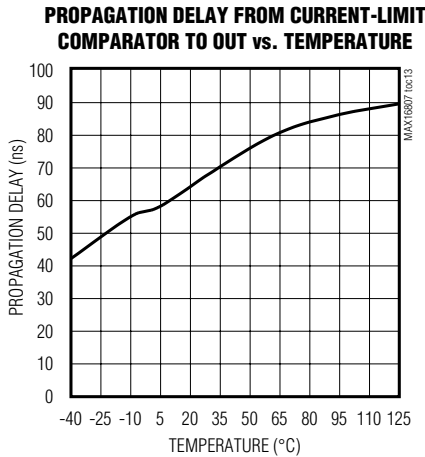
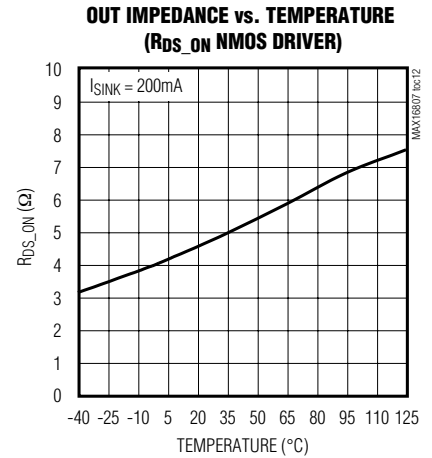
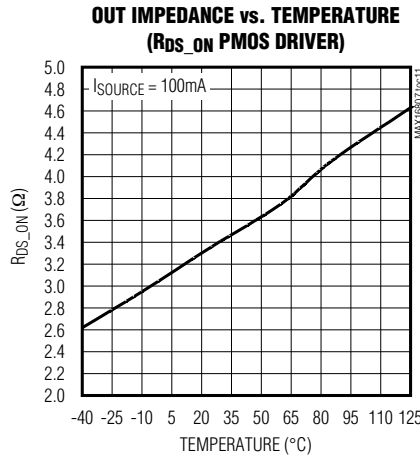
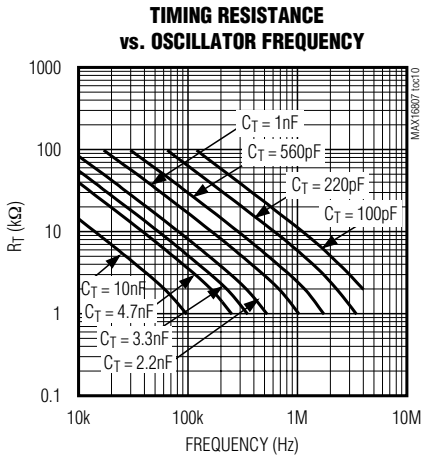
CURRENT-SENSE TRIP THRESHOLD vs. TEMPERATURE



Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

Typical Operating Characteristics (continued)

($V_{CC} = +15V$, $V_+ = 3V$ to $5.5V$, $R_T = 10k\Omega$, $C_T = 3.3nF$, $V_{REF} = COMP = open$, $C_{REF} = 0.1\mu F$, $V_{FB} = 2V$, $CS = AGND = PGND = 0V$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

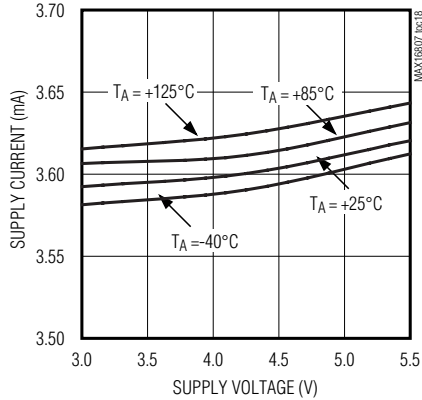


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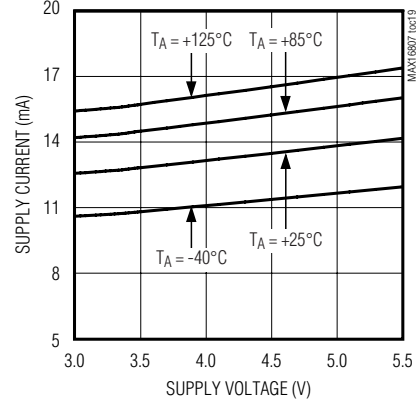
Typical Operating Characteristics (continued)

($V_{CC} = +15V$, $V_+ = 3V$ to $5.5V$, $R_T = 10k\Omega$, $C_T = 3.3nF$, $V_{REF} = COMP = open$, $C_{REF} = 0.1\mu F$, $V_{FB} = 2V$, $CS = AGND = PGND = 0V$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

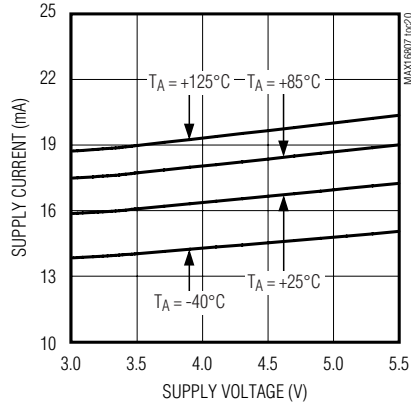
SUPPLY CURRENT vs. SUPPLY VOLTAGE
(INTERFACE IDLE, ALL OUTPUTS OFF, $R_{SET} = 360\Omega$)



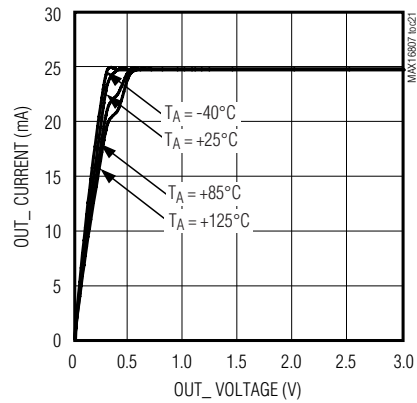
SUPPLY CURRENT vs. SUPPLY VOLTAGE
(INTERFACE IDLE, ALL OUTPUTS ON, $R_{SET} = 720\Omega$)



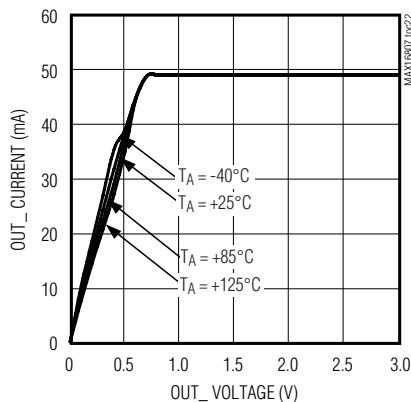
SUPPLY CURRENT vs. SUPPLY VOLTAGE
(INTERFACE IDLE, ALL OUTPUTS ON, $R_{SET} = 360\Omega$)



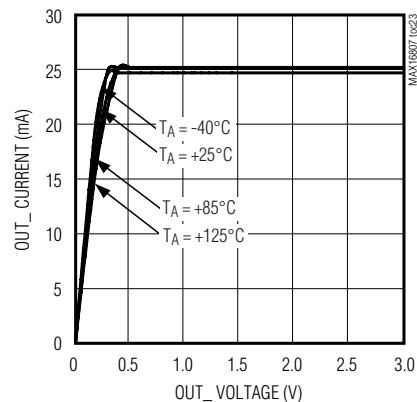
OUT_CURRENT vs. OUT_VOLTAGE
($R_{SET} = 720\Omega$, $V_+ = 3.3V$)



OUT_CURRENT vs. OUT_VOLTAGE
($R_{SET} = 360\Omega$, $V_+ = 3.3V$)



OUT_CURRENT vs. OUT_VOLTAGE
($R_{SET} = 720\Omega$, $V_+ = 5.0V$)

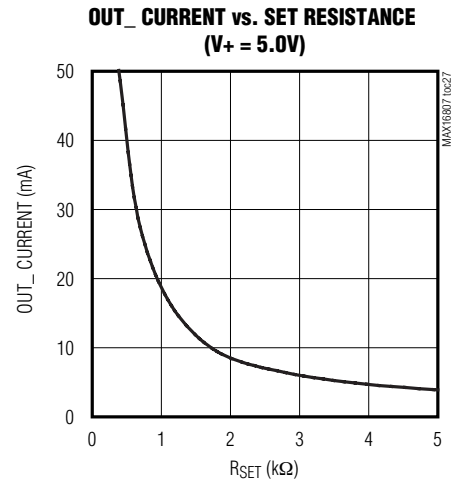
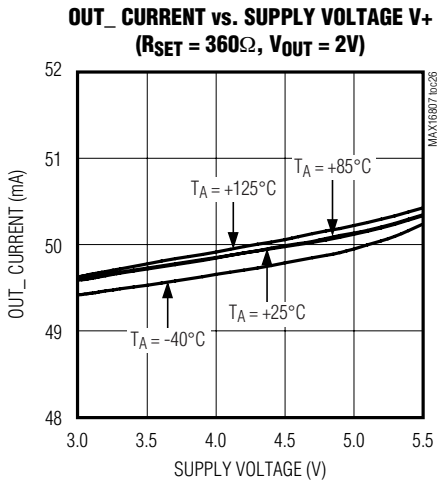
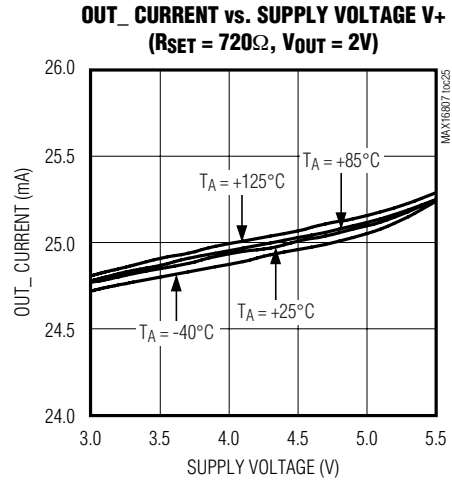
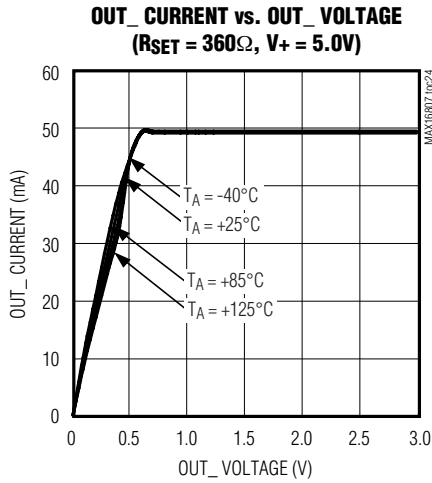


MAX16807/MAX16808

Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

Typical Operating Characteristics (continued)

($V_{CC} = +15V$, $V_+ = 3V$ to $5.5V$, $R_T = 10k\Omega$, $C_T = 3.3nF$, $V_{REF} = COMP = open$, $C_{REF} = 0.1\mu F$, $V_{FB} = 2V$, $CS = AGND = PGND = 0V$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)



Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

Pin Description

| PIN | NAME | FUNCTION |
|-----------|-----------------|--|
| 1, 13, 28 | N.C. | No Connection. Not internally connected. Leave unconnected. |
| 2 | AGND | Analog Ground |
| 3 | OUT | MOSFET Driver Output OUT. Connects to the gate of the external n-channel MOSFET. |
| 4 | V _{CC} | Power-Supply Input. Bypass V _{CC} to AGND with a 0.1μF ceramic capacitor or a parallel combination of a 0.1μF and a higher value ceramic capacitor. |
| 5 | REF | 5V Reference Output. Bypass REF to AGND with a 0.1μF ceramic capacitor. |
| 6–9 | OUT4–OUT7 | LED Driver Outputs. OUT4–OUT7 are open-drain, constant-current-sinking outputs rated for 36V. |
| 10 | \overline{OE} | Active-Low Output Enable Input. Drive \overline{OE} low to PGND to enable the OUT0–OUT7. Drive \overline{OE} high to disable OUT0–OUT7. |
| 11 | DOUT | Serial-Data Output. Data is clocked out of the 8-bit internal shift register to DOUT on CLK's rising edge. |
| 12 | SET | LED Current Setting. Connect R _{SET} from SET to PGND to set the LED current. |
| 14 | V+ | LED Driver Positive Supply Voltage. Bypass V+ to PGND with a 0.1μF ceramic capacitor. |
| 15, 16 | PGND | Power Ground |
| 17 | DIN | Serial-Data Input |
| 18 | CLK | Serial-Clock Input |
| 19 | LE | Latch-Enable Input. Data is loaded transparently from the internal shift register(s) to the output latch(es) while LE is high. Data is latched into the output latch(es) on LE's falling edge, and retained while LE is low. |
| 20–23 | OUT0–OUT3 | LED Driver Outputs. OUT0–OUT3 are open-drain, constant-current-sinking outputs rated for 36V. |
| 24 | COMP | Error-Amplifier Output |
| 25 | FB | Error-Amplifier Inverting Input |
| 26 | CS | PWM Controller Current-Sense Input |
| 27 | RTCT | PWM Controller Timing Resistor/Capacitor Connection. A resistor R _T from RTCT to REF and a capacitor C _T from RTCT to AGND set the oscillator frequency. |
| — | EP | Exposed Paddle. Connect to the ground plane for improved power dissipation. Do not use as the only ground connection for the part. |

Detailed Description

The MAX16807/MAX16808 LED drivers include an internal switch-mode controller that can be used as boost or buck-boost (SEPIC) converters to generate the voltage necessary to drive the multiple strings of LEDs. These devices incorporate an integrated low-side driver, a programmable oscillator (20kHz to 1MHz), an error amplifier, a low-voltage (300mV) current sense for higher efficiency, and a 5V reference to power up external circuitry (see Figures 1a, 1b, and 1c).

The MAX16807/MAX16808 LED drivers include a 4-wire serial interface and a current-mode PWM controller to generate the necessary voltage for driving eight open-drain, constant-current-sinking output ports. The drivers

use current-sensing feedback circuitry (not simple current mirrors) to ensure very small current variations over the full allowed range of output voltage (see the *Typical Operating Characteristics*). The 4-wire serial interface comprises an 8-bit shift register and an 8-bit transparent latch. The shift register is written through a clock input, CLK, and a data input, DIN, and the data propagates to a data output, DOUT. The data output allows multiple drivers to be cascaded and operated together. The contents of the 8-bit shift register are loaded into the transparent latch through a latch-enable input, LE. The latch is transparent to the shift register outputs when high and latches the current state on the falling edge of LE. Each driver output is an open-drain, constant-current sink that should be connected to the cath-

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ode of a string of LEDs connected in series. The constant-current capability is up to 55mA per output, set for all 8 outputs by an external resistor, R_{SET} . The devices can operate in a stand-alone mode (see the *Typical Operating Circuits*.)

The MAX16808 includes circuitry that automatically detects open-circuit LEDs. Fault status is loaded into the serial-interface shift register when LE goes high and is automatically shifted out on DOUT when the next data transmission is shifted in. The number of channels can be expanded by using the MAX6970 and MAX6971 family in conjunction with the MAX16807 and MAX16808.

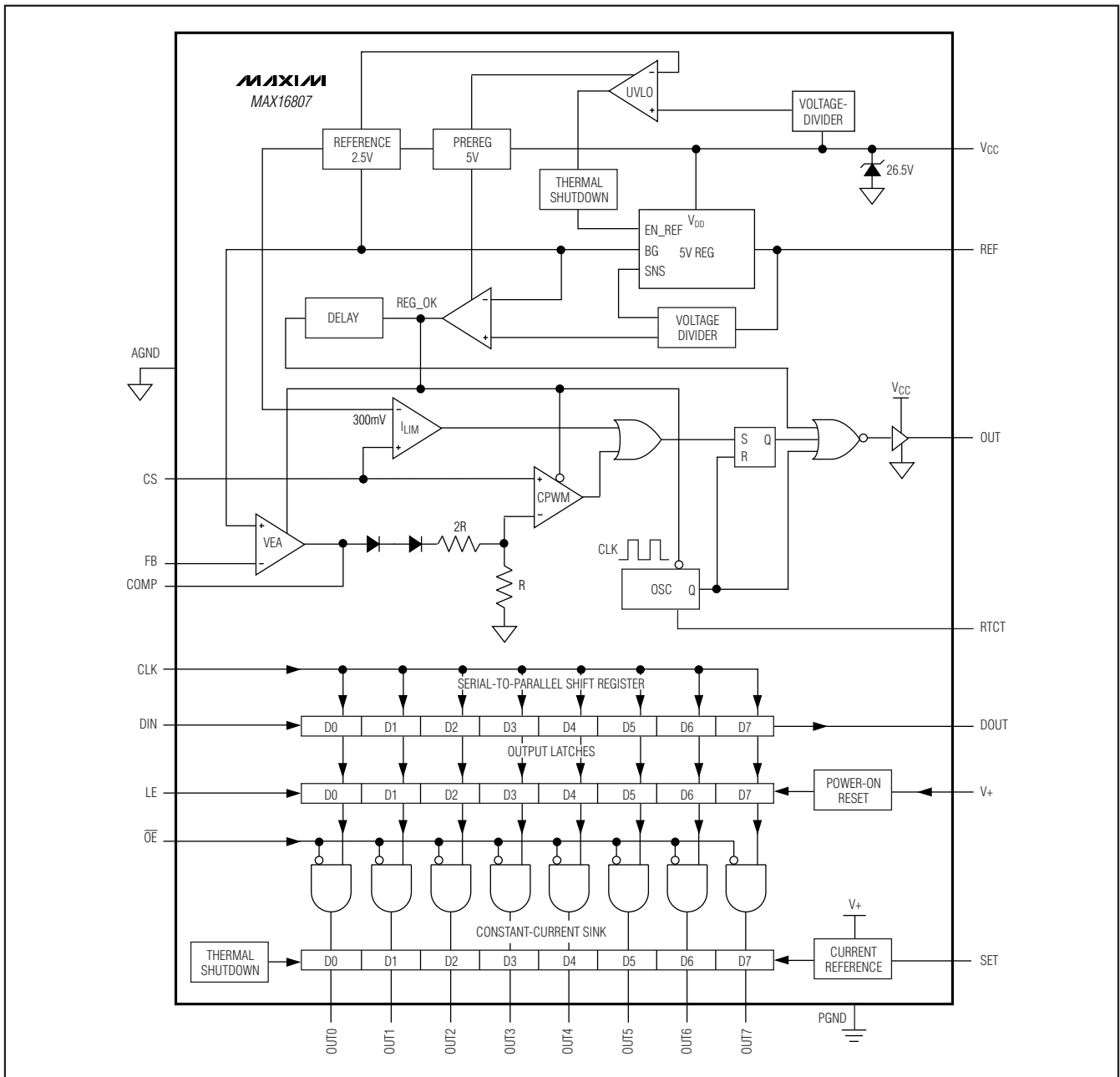


Figure 1a. Internal Block Diagram (MAX16807)

Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

MAX16807/MAX16808

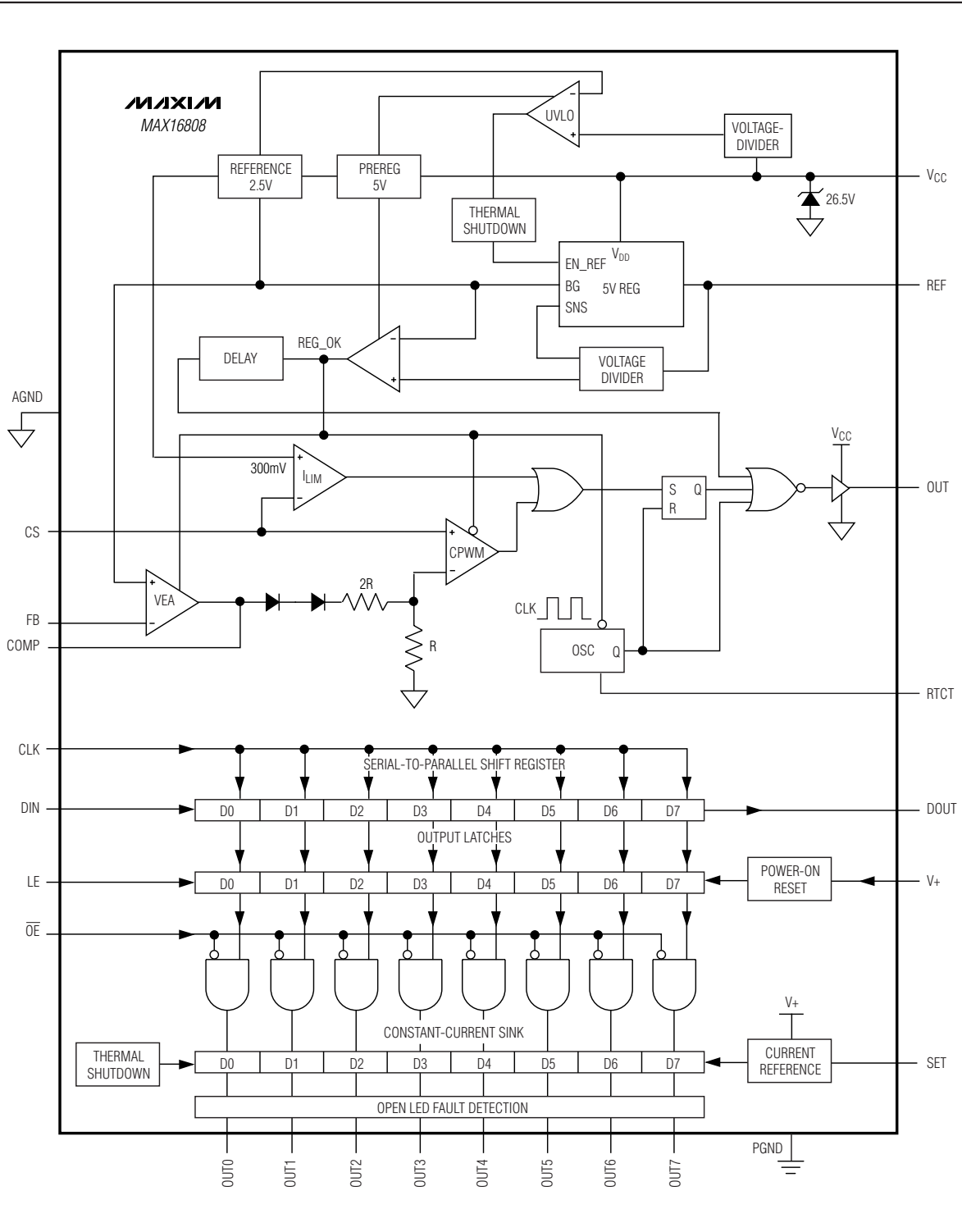


Figure 1b. Internal Block Diagram (MAX16808)

Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

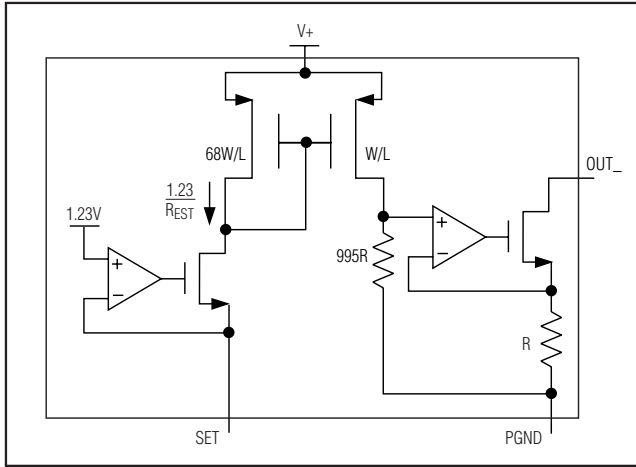


Figure 1c. OUT_ Driver Internal Diagram

Switch-Mode Controller

Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Second, the stability requirements of the current-mode controller are reduced to that of a single pole system unlike the double pole in the voltage-mode control scheme. The MAX16807/MAX16808 use a current-mode control loop where the output of the error amplifier is compared to the current-sense voltage (V_{CS}). When the current-sense signal is lower than the inverting input of the CPWM comparator, the output of the comparator is low and the switch is turned on at each clock pulse. When the current-sense signal is higher than the inverting input of the CPWM comparator, the output is high and the switch is turned off.

Undervoltage Lockout (UVLO)

The turn-on supply voltage for the MAX16807/MAX16808 is 8.4V (typ). Once V_{CC} reaches 8.4V, the reference powers up. There is a 0.8V of hysteresis from the turn-on voltage to the UVLO threshold. Once V_{CC} reaches 8.4V, the MAX16807/MAX16808 operate with V_{CC} down to 7.6V (typ). Once V_{CC} goes below 7.6V, the device is in UVLO. When in UVLO, the quiescent supply current into V_{CC} falls back to 32 μ A (typ), and OUT and REF are pulled low.

MOSFET Driver

OUT drives an external n-channel MOSFET and swings from AGND to V_{CC} . Ensure that V_{CC} remains below the absolute maximum V_{GS} rating of the external MOSFET.

OUT is a push-pull output with the on-resistance of the pMOS typically 3.5 Ω and the on-resistance of the nMOS typically 4.5 Ω . The driver can source 2A and sink 1A typically. This allows for the MAX16807/MAX16808 to quickly turn on and off high gate-charge MOSFETs. Bypass V_{CC} with one or more 0.1 μ F ceramic capacitors to AGND, placed close to the V_{CC} pin. The average current sourced to drive the external MOSFET depends on the total gate charge (Q_G) and operating frequency of the converter. The power dissipation in the MAX16807/MAX16808 is a function of the average output drive current (I_{DRIVE}). Use the following equation to calculate the power dissipation in the device due to I_{DRIVE} :

$$I_{DRIVE} = (Q_G \times f_{sw})$$

$$PD = (I_{DRIVE} + I_{CC}) \times V_{CC}$$

where I_{CC} is the operating supply current. See the *Typical Operating Characteristics* for the operating supply current at a given frequency.

Error Amplifier

The MAX16807/MAX16808 include an internal error amplifier. The inverting input is at FB and the noninverting input is internally connected to a 2.5V reference. Set the output voltage using a resistive divider between output of the converter V_{OUT} , FB, and AGND. Use the following formula to set the output voltage:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$$

where $V_{FB} = 2.5V$.

Oscillator

The oscillator frequency is programmable using an external capacitor and a resistor at RTCT (see R_T and C_T in the *Typical Operating Circuits*). R_T is connected from RTCT to the 5V reference (REF), and C_T is connected from RTCT to AGND. REF charges C_T through R_T until its voltage reaches 2.8V. C_T then discharges through an 8.3mA internal current sink until C_T 's voltage reaches 1.1V, at which time C_T is allowed to charge through R_T again. The oscillator's period is the sum of the charge and discharge times of C_T . Calculate the charge time as follows:

$$t_C = 0.57 \times R_T \times C_T$$

where t_C is in seconds, R_T in ohms (Ω), and C_T in Farads (F).

The discharge time is then:

$$t_D = (R_T \times C_T \times 1000) / [(4.88 \times R_T) - (1.8 \times 1000)]$$

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where t_D is in seconds, R_T in ohms (Ω), and C_T in Farads (F).

The oscillator frequency is then:

$$f_{OSC} = \frac{1}{(t_C + t_D)}$$

Reference Output

REF is a 5V reference output that can source 20mA. Bypass REF to AGND with a 0.1 μ F capacitor.

Current Limit

The MAX16807/MAX16808 include a fast current-limit comparator to terminate the on cycle during an overload or a fault condition. The current-sense resistor, R_{CS} , connected between the source of the external MOSFET and AGND, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 0.3V. Use the following equation to calculate R_{CS} :

$$R_{CS} = \frac{V_{CS}}{I_{P-P}}$$

I_{P-P} is the peak current that flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (OUT) turns the switch off within 60ns. In most cases, a small RC filter is required to filter out the leading-edge spike on the sense waveform. Set the time constant of the RC filter at 50ns.

Buck-Boost (SEPIC) Operation

Figure 2 shows a buck-boost application circuit using the MAX16807/MAX16808 in a stand-alone mode of operation. SEPIC topology is necessary when the total forward voltage of the LEDs in a string is such that V_{OUT} can be below or above V_{IN} .

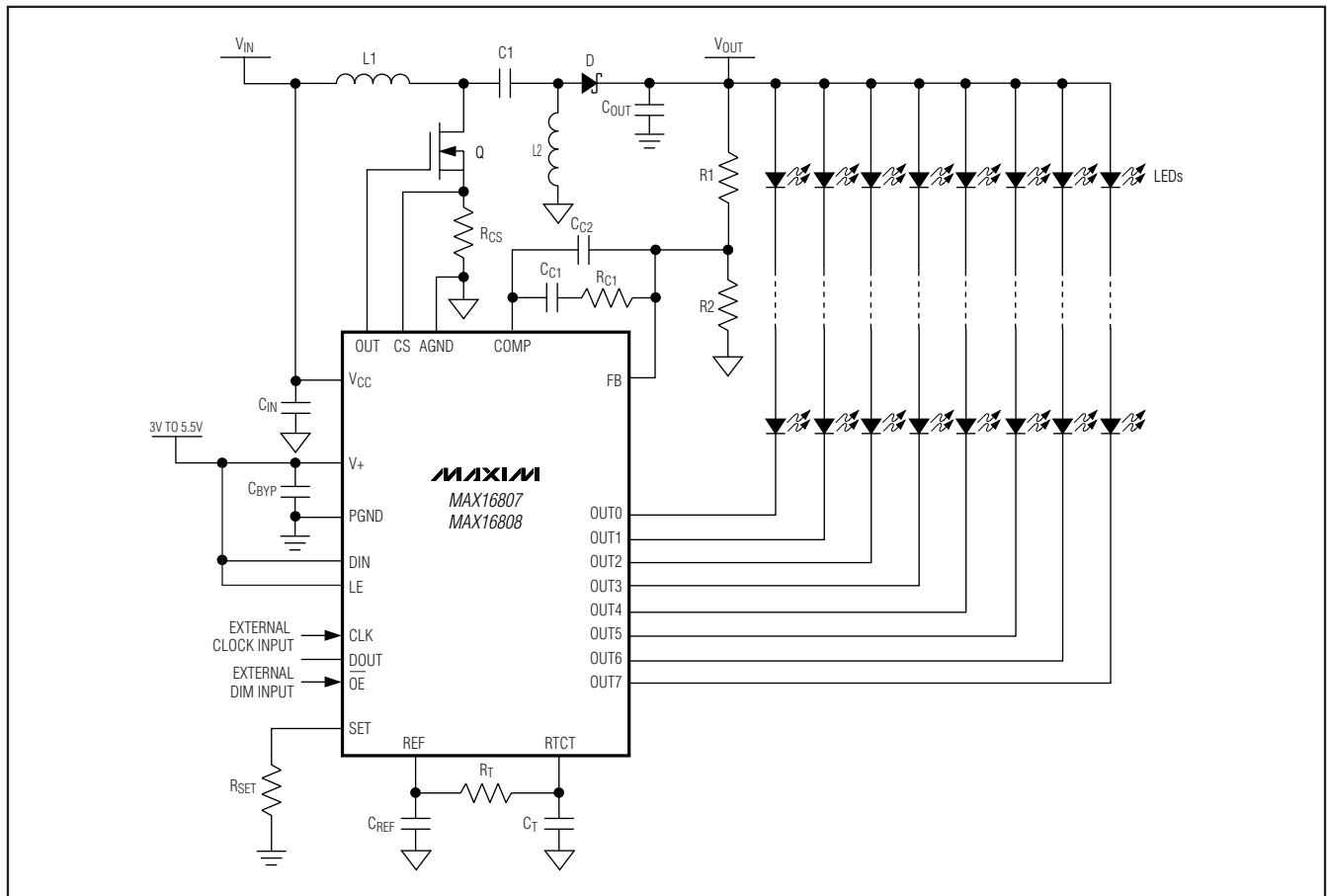


Figure 2. Buck-Boost (SEPIC) Configuration

Integrated 8-Channel LED Drivers with Switch-Mode Boost and SEPIC Controller

LED Driver

4-Wire Interface

The MAX16807/MAX16808 also operate in a stand-alone mode (see the *Typical Operating Circuits*). For use with a microcontroller, the MAX16807/MAX16808 feature a 4-wire serial interface using DIN, CLK, LE, \overline{OE} inputs and DOUT as a data output. This interface is used to write the LED channels' data to the MAX16807/MAX16808. The serial-interface data word length is 8 bits, D0–D7. See [Figure 3](#).

The functions of the five interface pins are as follows:

DIN is the serial-data input, and must be stable when it is sampled on the rising edge of CLK. Data is shifted in MSB first. This means that data bit D7 is clocked in first, followed by 7 more data bits, finishing with the LSB, D0.

CLK is the serial-clock input that shifts data at DIN into the MAX16807/MAX16808's 8-bit shift register on its rising edge.

LE is the latch enable input of the MAX16807/MAX16808 that transfers data from the 8-bit shift register to its 8-bit output latch (transparent latch). The data is latched on the falling edge of LE ([Figure 4](#)). The fourth input (\overline{OE}) provides output-enable control of the output drivers. When \overline{OE} is driven high, the outputs (OUT0–OUT7) are forced to high impedance without altering the contents of the output latches. Driving \overline{OE} low enables the outputs to follow the state of the output latches. \overline{OE} is independent of the operation of the serial interface operation. Data can be shifted into the serial-interface shift register and latched, regardless of the state of \overline{OE} . DOUT is the serial-data output that shifts data out from the MAX16807/MAX16808's 8-bit shift register on the rising edge of CLK. Data at DIN propagates through the shift register and appears at DOUT eight clock cycles later. [Table 1](#) shows the 4-wire serial-interface truth table.

Table 1. 4-Wire Serial-Interface Truth Table

| SERIAL DATA INPUT DIN | CLOCK INPUT CLK | SHIFT REGISTER CONTENTS | | | | | | LOAD INPUT | LATCH CONTENTS | | | | | | BLANKING INPUT | OUTPUT CONTENTS CURRENT AT OUT _n | | | | | | |
|--------------------------|--------------------|-------------------------|----|----|-----|------|------|------------|----------------|----|----|-----|------|----|-----------------|---|----|----|-----|------|----|--|
| | | D0 | D1 | D2 | ... | Dn-1 | Dn | LE | D0 | D1 | D2 | ... | Dn-1 | Dn | \overline{OE} | D0 | D1 | D2 | ... | Dn-1 | Dn | |
| H | | H | R0 | R1 | ... | Rn-2 | Rn-1 | | | | | | | | | | | | | | | |
| L | | L | R0 | R1 | ... | Rn-2 | Rn-1 | | | | | | | | | | | | | | | |
| X | | R0 | R1 | R2 | ... | Rn-1 | Rn | | | | | | | | | | | | | | | |
| | | X | X | X | ... | X | X | L | R0 | R1 | R2 | ... | Rn-1 | Rn | | | | | | | | |
| | | P0 | P1 | P2 | ... | Pn-1 | Pn | H | P0 | P1 | P2 | ... | Pn-1 | Pn | L | P0 | P1 | P2 | ... | Pn-1 | Pn | |
| | | | | | | | | | X | X | X | ... | X | X | H | L | L | L | ... | L | L | |

L = Low Logic Level
H = High Logic Level
X = Don't Care
P = Present State (Shift Register)
R = Previous State (Latched)

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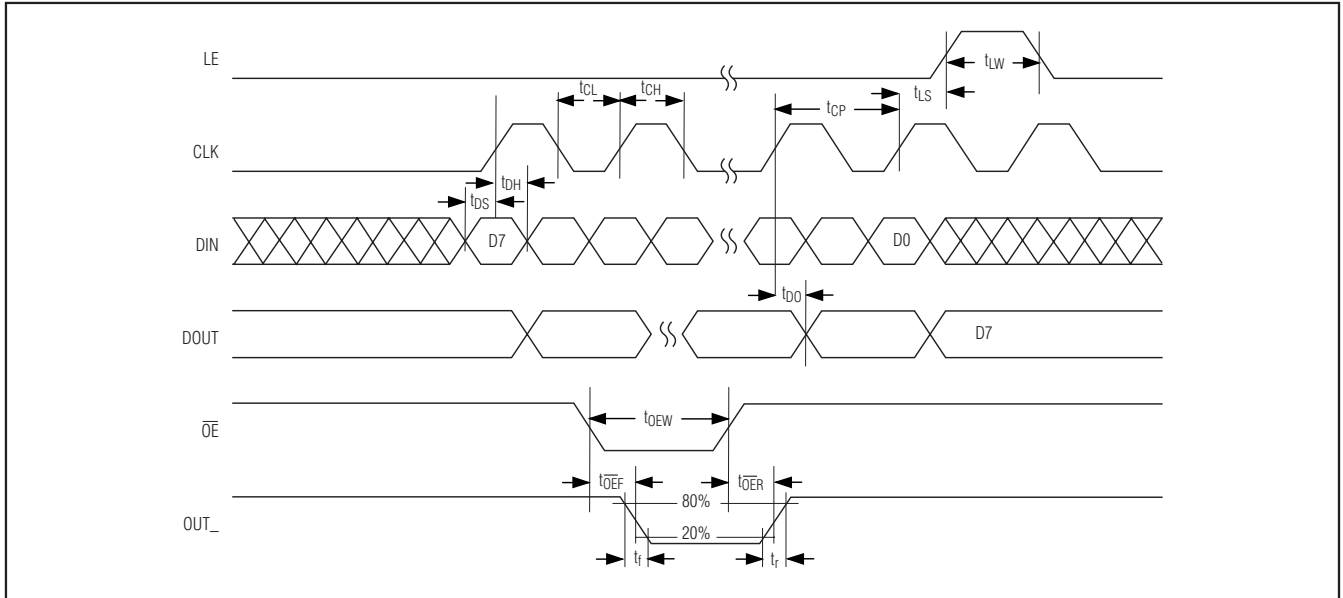


Figure 3. 4-Wire Serial-Interface Timing Diagram

LED Fault Detection (MAX16808)

The MAX16808 includes circuitry that detects open-circuit LEDs automatically. An open-circuit fault occurs when an output is sinking current less than approximately 50% of the programmed current flows. Open circuits are checked just after the falling edge of OE. The fault data is latched on the rising edge of LE and is shifted out when new LED data is loaded into the output latches from the shift register. If one or more output ports are detected with an open-circuit fault, the D6 and D5 bits of DOUT go high. If no open-circuit faults are detected, D6 and D5 are set to low. The data in the other 6 bit positions in DOUT are not altered. Fault status is shifted out on DOUT for the first two rising edges of the clock after the falling edge of LE (see Figure 5). LE is normally taken high after all 8 bits of new LED

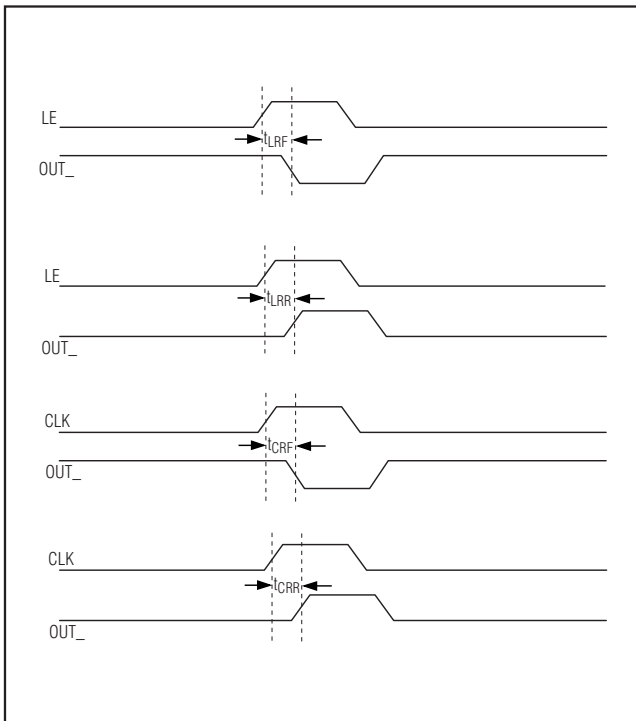


Figure 4. LE and CLK to OUT_ Timing

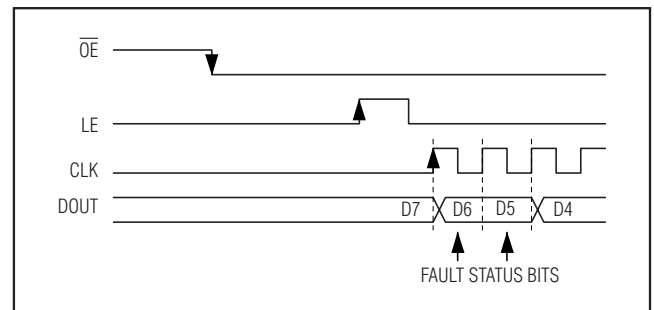


Figure 5. Fault Timing

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data have been clocked into the shift register(s), and then DOUT outputs data bit D7. A typical fault-detecting application tests all the shifted out data. Bits D0–D4 and D7 are checked against the originally transmitted data to check data-link integrity. Bits D5 and D6 are checked first to see that they contain the same data (validating the status), and second, whether faults are reported or not by the actual logic level.

Selecting External Component R_{SET} to Set LED Output Current

The MAX16807/MAX16808 use an external resistor, R_{SET} , to set the LED current for outputs OUT0–OUT7. The minimum allowed value of R_{SET} is 330 Ω , which sets the output currents to 55mA. The maximum allowed value of R_{SET} is 5k Ω ($I_{OUT_} = 3.6mA$) and maximum allowed capacitance at SET is 100pF.

Use the following formula to set the output current:

$$R_{SET} = \frac{18,000}{I_{OUT_}}$$

where $I_{OUT_}$ is the desired output current in milliamps and the value for R_{SET} is in ohms.

Overtemperature Cutoff

The MAX16807/MAX16808 contain an internal temperature sensor that turns off all outputs when the die temperature exceeds +165°C. The outputs are enabled again when the die temperature drops below +140°C. Register contents are not affected, so when a driver is overdissipating, the external symptom is the load LEDs cycling on and off as the driver repeatedly overheats and cools, alternately turning itself off and then back on again.

Stand-Alone Operation

In stand-alone operation, the MAX16807/MAX16808 does not use the 4-wire interface (see the *Typical Operating Circuits*). Connect DIN and LE to V+ provide at least 8 external clock pulses to CLK to enable 8 outputs. This startup pulse sequence can be provided either using an external clock or the PWM signal. The external clock can also be generated using the signal at RTCT and an external comparator.

LED Dimming

PWM Dimming

All the output channels can be dimmed simultaneously by applying a PWM signal (50Hz to 30kHz) to \overline{OE} . This allows for a wide range of dimming up to a 5000:1 ratio. Each channel can be independently turned on and off using a 4-wire serial interface. The dimming is proportional to the PWM duty cycle.

LED Current Amplitude Adjustment

Using an analog or digital potentiometer as R_{SET} allows for LED current amplitude adjustment and linear dimming.

Computing Power Dissipation

Use the following equation to estimate the upper limit power dissipation (PD) for the MAX16807/MAX16808:

$$PD = DUTY \times \left[(V+ \times I+) + \sum_{i=0}^7 V_{OUTi} \times I_{OUTi} \right] + (V_{CC} \times I_{CC})$$

where:

V+ = supply voltage

I+ = operating supply current

DUTY = PWM duty cycle applied to \overline{OE}

V_{OUTi} = MAX16807/MAX16808 port output voltage when driving load LED(s)

I_{OUTi} = LED drive current programmed by R_{SET}

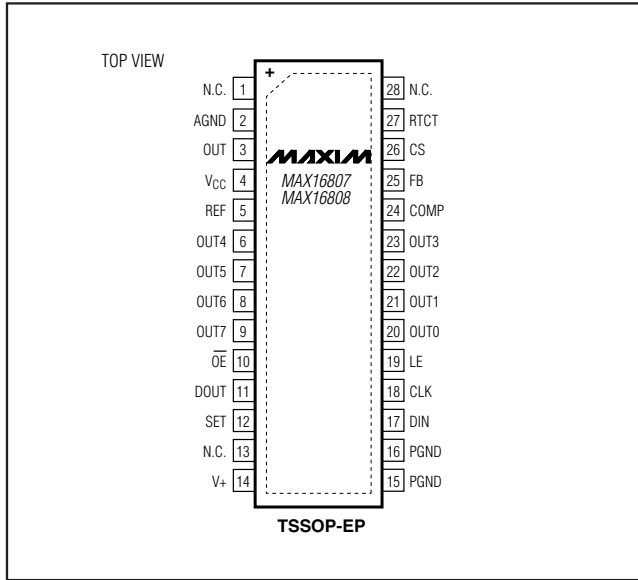
PD = power dissipation.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting AGND, PGND, the input bypass-capacitor ground lead, and the output-filter ground lead to a single point (star ground configuration). Also, minimize trace lengths to reduce stray capacitance, trace resistance, and radiated noise. The trace between the output voltage-divider and the FB pin must be kept short, as well as the trace between AGND and PGND.

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Pin Configuration



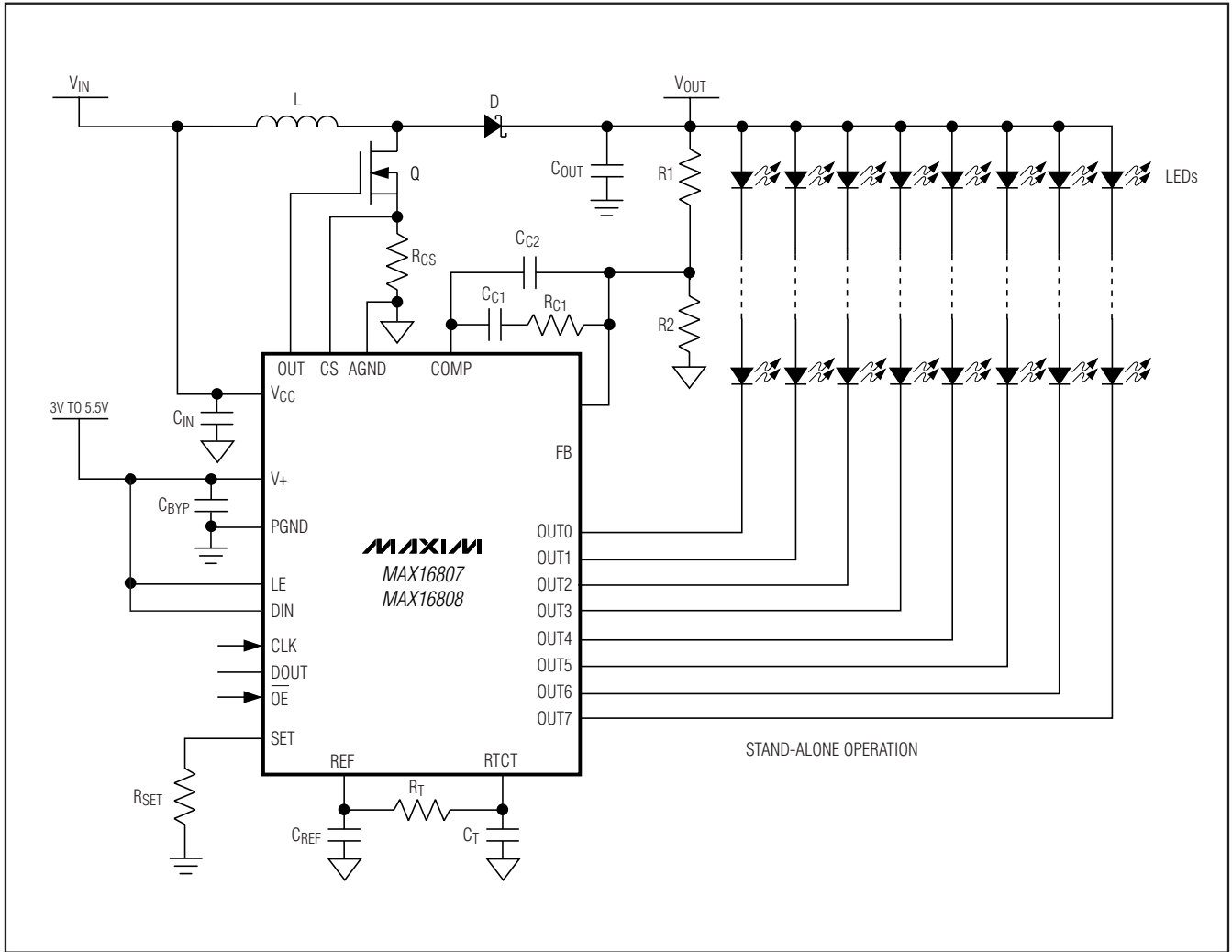
Chip Information

PROCESS: BiCMOS

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Typical Operating Circuits (continued)



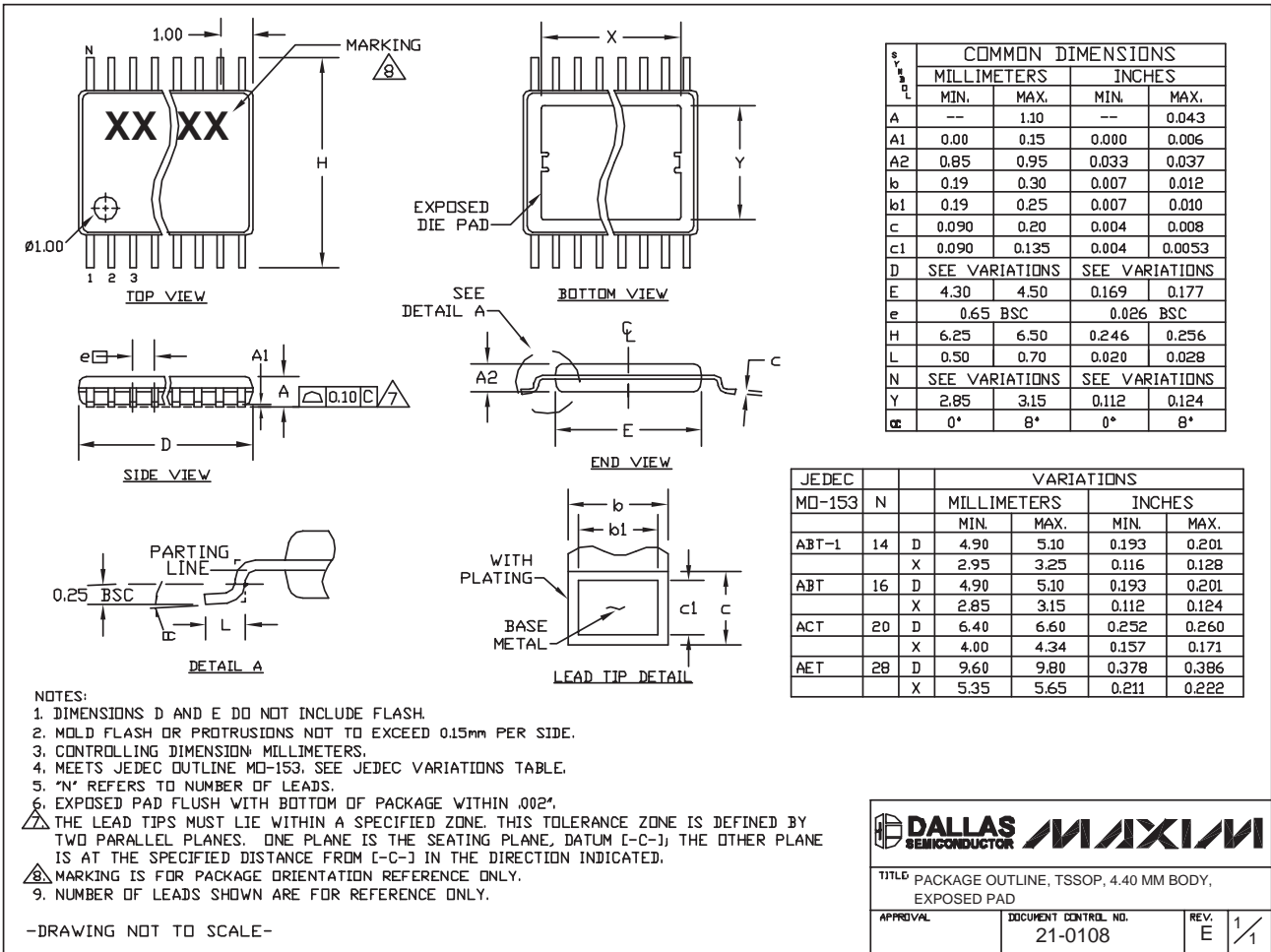
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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

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TSSOP 4.4mm BODY, EPS



Revision History

Pages changed at Rev 1: 1, 21

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