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MDOT064128AY-WP	64 x 128	White	OLED Module
Specification			
Version: 1		Date: 18/11/2015	
Revision			
1	18/11/2015	First Release.	

Display Features			
Resolution	64 x 128	RoHS compliant	
Appearance	White on Black		
Logic Voltage	3V		
Interface	Parallel / SPI / I²C		
Module Size	14.00 x 43.80 x 1.20mm		
Operating Temperature	-40°C ~ +80°C	Box Quantity	Weight / Display
Construction	COT	---	---

* - For full design functionality, please use this specification in conjunction with the SSD1305Z specification.(Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearance	**Voltage**

1. Basic Specifications

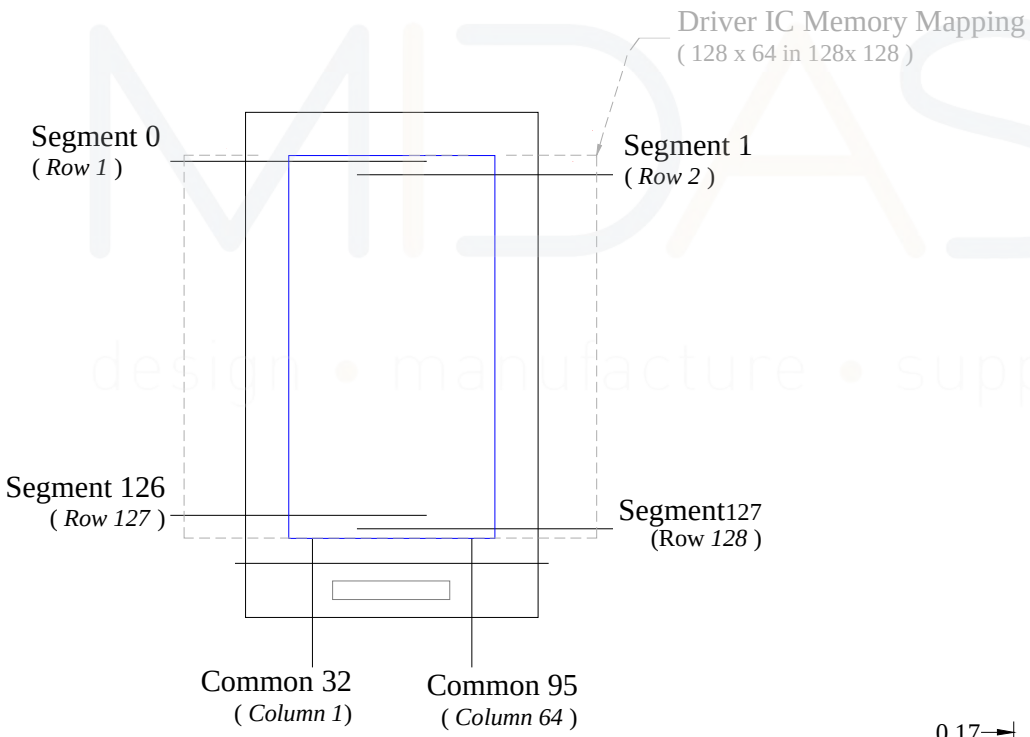
1.1 Display Specifications

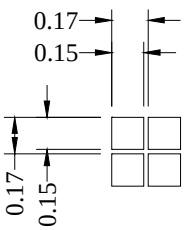
1) Display Mode : Passive Matrix
2) Display Color : Monochrome (White)
3) Drive Duty : 1/64 Duty

1.2 Mechanical Specifications

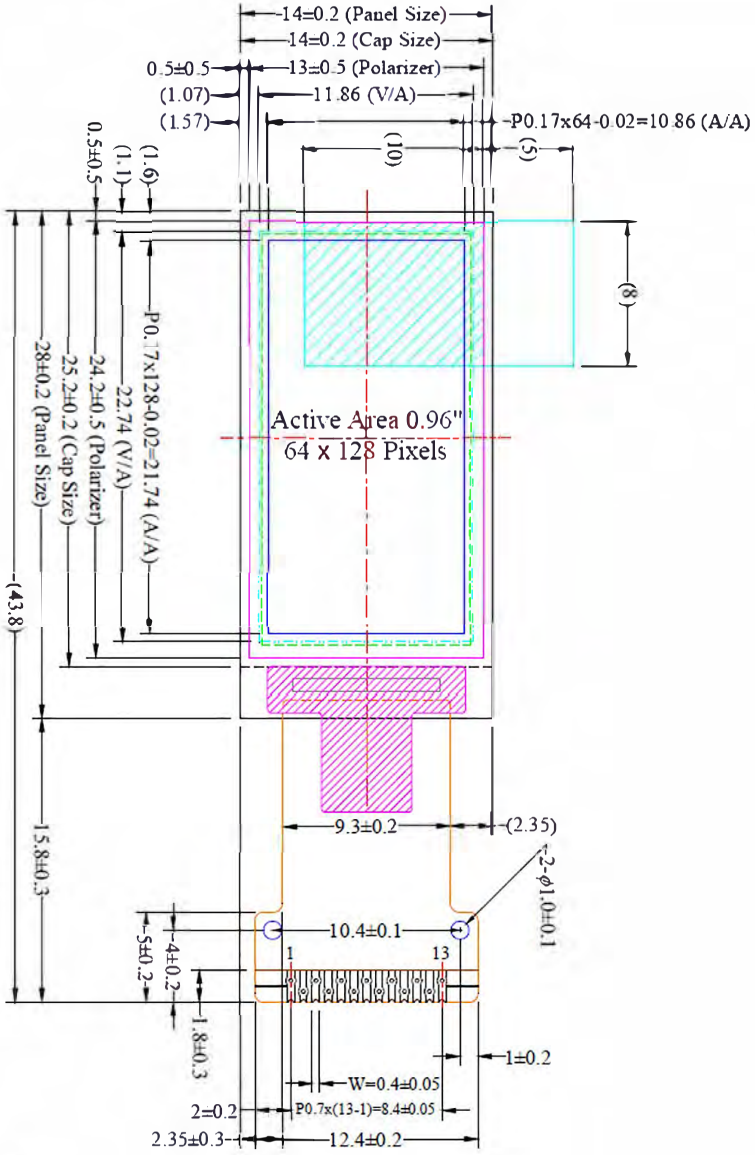
1) Outline Drawing : According to the annexed outline drawing
2) Number of Pixels : 64 x 128
3) Module Size : 14.00 × 43.80 × 1.20 (mm)
4) Panel Size : 14.00 × 28.00 × 1.20 (mm) including "Anti-Glare Polarizer"
5) Active Area : 10.86 × 21.74 (mm)
6) Pixel Pitch : 0.17 × 0.17 (mm)
7) Pixel Size : 0.15 × 0.15 (mm)
8) Weight : T.B.D. (g) ± 10%

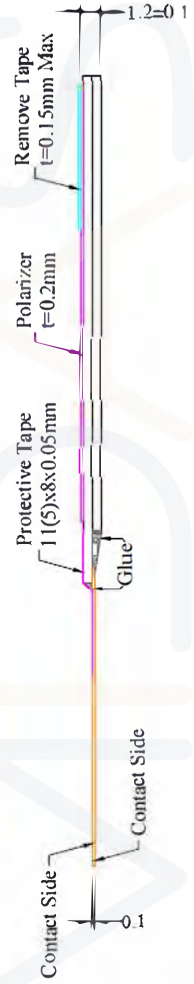
1.3 Memory Mapping & Pixel Construction

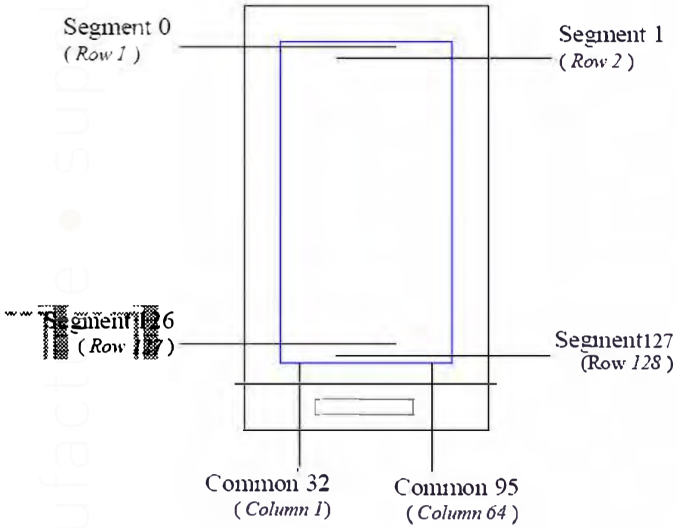


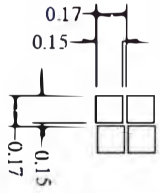


Pixel Detail
Scale (10:1)









Pixel Detail
Scale (10:1)

Pin	Symbol
1	NC
2	VPP
3	VCOM
4	VDD
5	IM1
6	IREF
7	CS
8	RES
9	A0
10	D0
11	D1
12	VSS
13	NC

Notes:

1. Color: White
2. Driver IC: SH1107
3. FPC Number:
4. Interface:4-wire SPI , I2C
5. General Tolerance: ±0.30
6. The total thickness (1.3 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 1.55 Max.

1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
2	VPP	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be supplied externally.
4	VDD	P	**Power Supply for Logic** This is a voltage supply pin. It must be connected to external source.
12	VSS	P	**Ground of OEL System** This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
Driver			
3	VCOMH	O	**Voltage Output High Level for COM Signal** This pin is for the voltage output high level for COM signals. A capacitor should be connected between this pin and GND.
6	IREF	O	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and GND. Set the current at 15.625μA maximum.
Interface			
5	IM1	I	**Communicating Protocol Select** These pins are MCU interface selection input. See the following table: 4-wire SPI: IM1 = 0 I^2C: IM1 = 1
7	CS	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CSB is pulled low.
8	RES	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed.
9	A0	I	**Data/Command Control** This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SI will be interpreted as data. When it is pulled low, the data at SI will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
10, 11	D0, D1	I/O	**Serial Data Input/Output and clock** When serial mode is selected, D1 will be the serial data input SI and D0 will be the serial clock input SCL. When I^2C mode is selected, D1 be the serial data input SDA and D0 is the serial clock input, SCL.
Reserve			
1, 13	N.C.	-	**Reserved Pin** The N.C. pins between function pins are reserved for compatible and flexible design.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	3.6	V	1, 2
Supply Voltage for Display	V_{PP}	0	10	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
LIFE TIME 80nits (Typ)	30K			hour	

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: End of lifetime is specified as 50% of initial brightness reached. The reference average operation life time at room temperature is estimated by the accelerated at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 4		150	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 3.0V, V_{PP} = 9.0V.
Software configuration follows Section 4.5 Initialization.

3.2 DC Characteristics

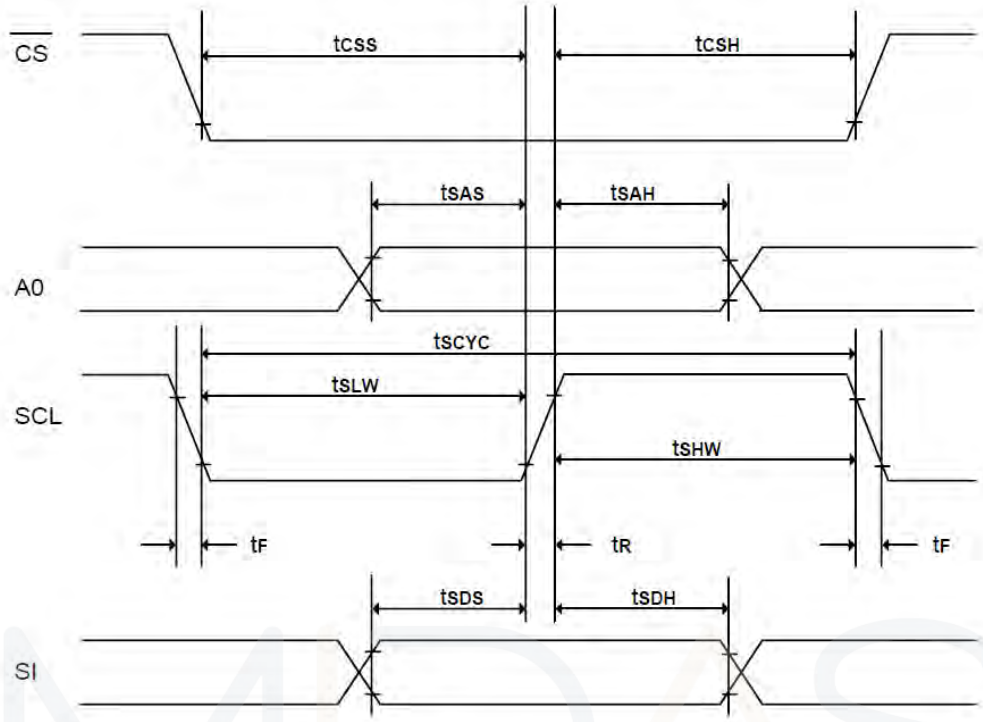
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	3.0	3.5	V
Supply Voltage for Display	V_{PP}	Note 5	8.5	9.0	9.5	V
High Level Input	V_{IHC}		$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{ILC}		0	-	$0.2\times V_{DD}$	V
High Level Output	V_{OHC}	I_{OH} = -500µA	$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OLC}	I_{OL} = 500µA	0	-	$0.2\times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}		-	110	160	µA
Operating Current for V_{PP}	I_{PP}	Note 6	-	5.3	6.6	mA
		Note 7	-	8.7	10.9	mA
		Note 8	-	16.9	21.1	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	0.1	5	µA
Sleep Mode Current for V_{PP}	$I_{PP, SLEEP}$		-	0.5	5	µA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{PP}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DD} = 3.0V, V_{PP} = 9.0V, 30% Display Area Turn on.
Note 7: V_{DD} = 3.0V, V_{PP} = 9.0V, 50% Display Area Turn on.
Note 8: V_{DD} = 3.0V, V_{PP} = 9.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.5 Initialization.

3.3 AC Characteristics

3.3.1 4-wire SPI interface Timing Characteristics:



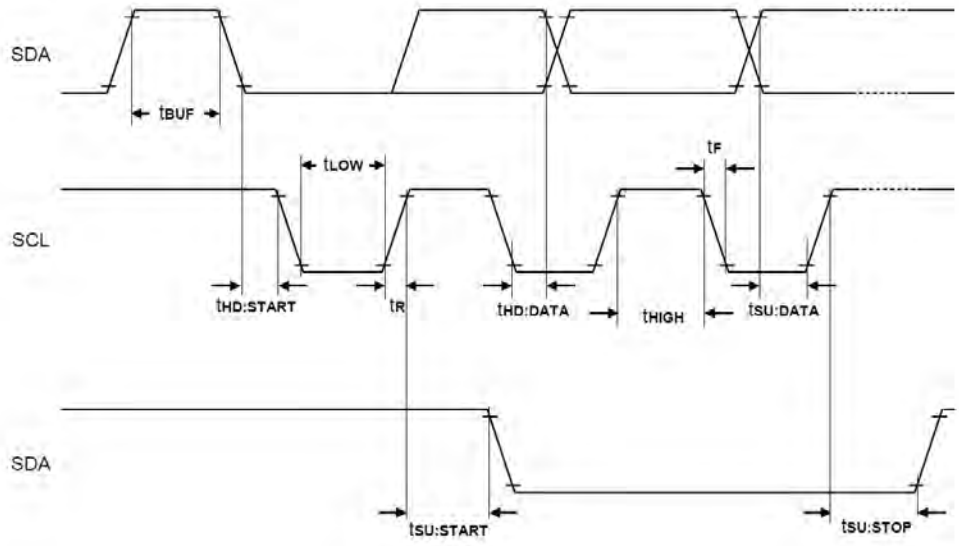
(V_{DD} - GND = 1.65V to 2.4V, T_a = 25°C)

Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	500	-	ns
t_{SAS}	Address Setup Time	300	-	ns
t_{SAH}	Address Hold Time	300	-	ns
t_{SDS}	Data Setup Time	200	-	ns
t_{SDH}	Data Hold Time	200	-	ns
t_{CSS}	Chip Select Setup Time	240	-	ns
t_{CSH}	Chip Select Hold Time	120	-	ns
t_{SHW}	Serial Clock H Pulse Width	200	-	ns
t_{SLW}	Serial Clock L Pulse Width	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

(V_{DD} - GND = 2.4V to 3.5V, T_a = 25°C)

Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	250	-	ns
t_{SAS}	Address Setup Time	150	-	ns
t_{SAH}	Address Hold Time	150	-	ns
t_{SDS}	Data Setup Time	100	-	ns
t_{SDH}	Data Hold Time	100	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{SHW}	Serial Clock H Pulse Width	100	-	ns
t_{SLW}	Serial Clock L Pulse Width	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

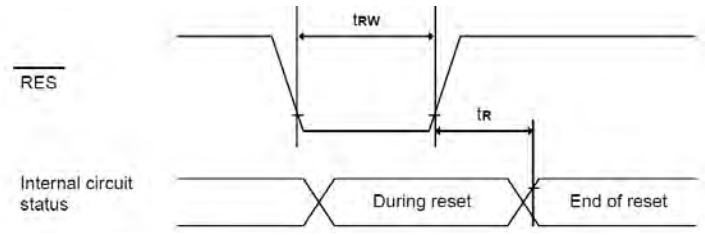
3.3.2 I2C interface Timing Characteristics:



(V_{DD} - GND = 1.65V to 3.5V, T_a = 25°C)

Symbol	Description	Min	Max	Unit
f_{SCL}	SCL Clock frequency	DC	400	KHz
t_{LOW}	SCL clock Low pulse width	1.3	-	μs
t_{HIGH}	SCL clock High pulse width	0.6	-	μs
$t_{SU:DATA}$	Data Setup Time	100	-	ns
$t_{HD:DATA}$	Data Hold Time	0	0.9	μs
t_R	SCL, SDA Rise Time	20+0.1Cb	300	ns
t_F	SCL, SDA Fall Time	20+0.1Cb	300	ns
Cb	Capacity load on each bus line		400	pF
$t_{SU:START}$	Setup Time for re-START	0.6	-	μs
$t_{HD:START}$	START Hold Time	0.6	-	μs
$t_{HD:STOP}$	Setup Time for STOP	0.6	-	μs
t_{BUF}	Bus free times between STOP and START condition	1.3	-	μs

3.3.3 Reset Timing Characteristics:



(V_{DD} - GND = 1.65V to 3.5V, T_a = 25°C)

Symbol	Description	Min	Max	Unit
t_R	Reset time	-	2.0	µs
t_{RW}	Reset Low pulse width	10.0	-	µs

4. Functional Specification

4.1 Commands

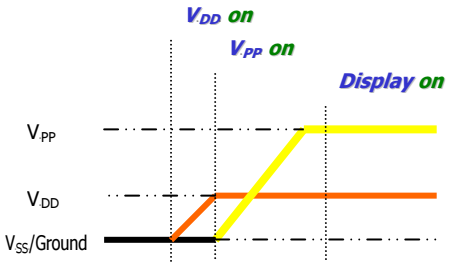
Refer to the Technical Manual for the SH1107

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

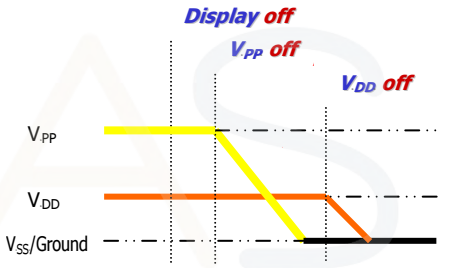
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{PP}
6. Delay 100ms
   (When V_{PP} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{PP}
3. Delay 100ms
   (When V_{PP} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD} and V_{PP} inside the driver IC, V_{PP} becomes lower than V_{DD} whenever V_{DD} is ON and V_{PP} is OFF.
2) V_{PP} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{PP}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{PP} power down.

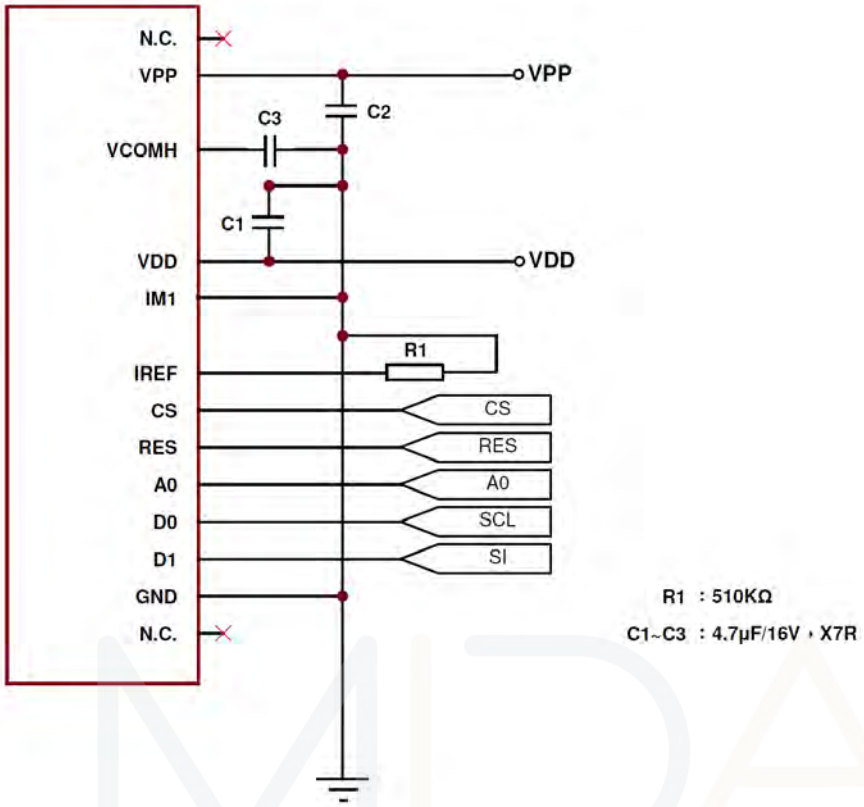
4.3 Reset Circuit

When RESB input is low, the chip is initialized with the following status:

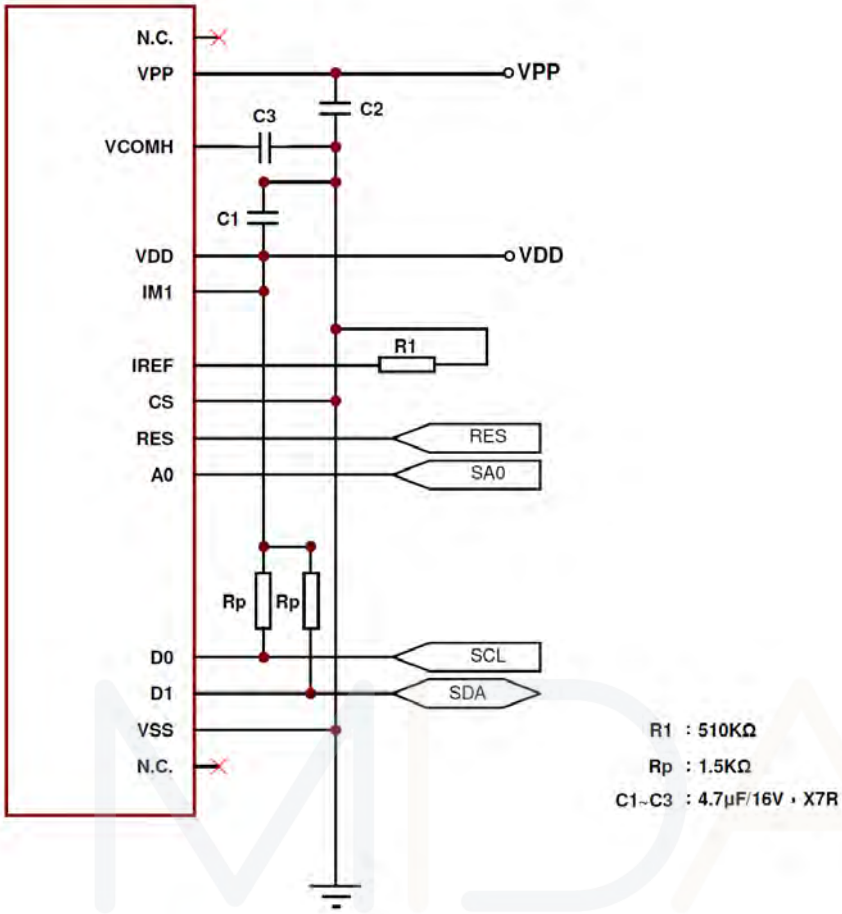
1. Display is OFF. Common and Segment are in high impedance state.
2. 128×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 is mapped to the top line of the display).
4. Shift register data clear in serial interface
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 80h
8. Internal DC-DC is selected

4.4 Application Circuit

4.4.1 4-wire SPI interface



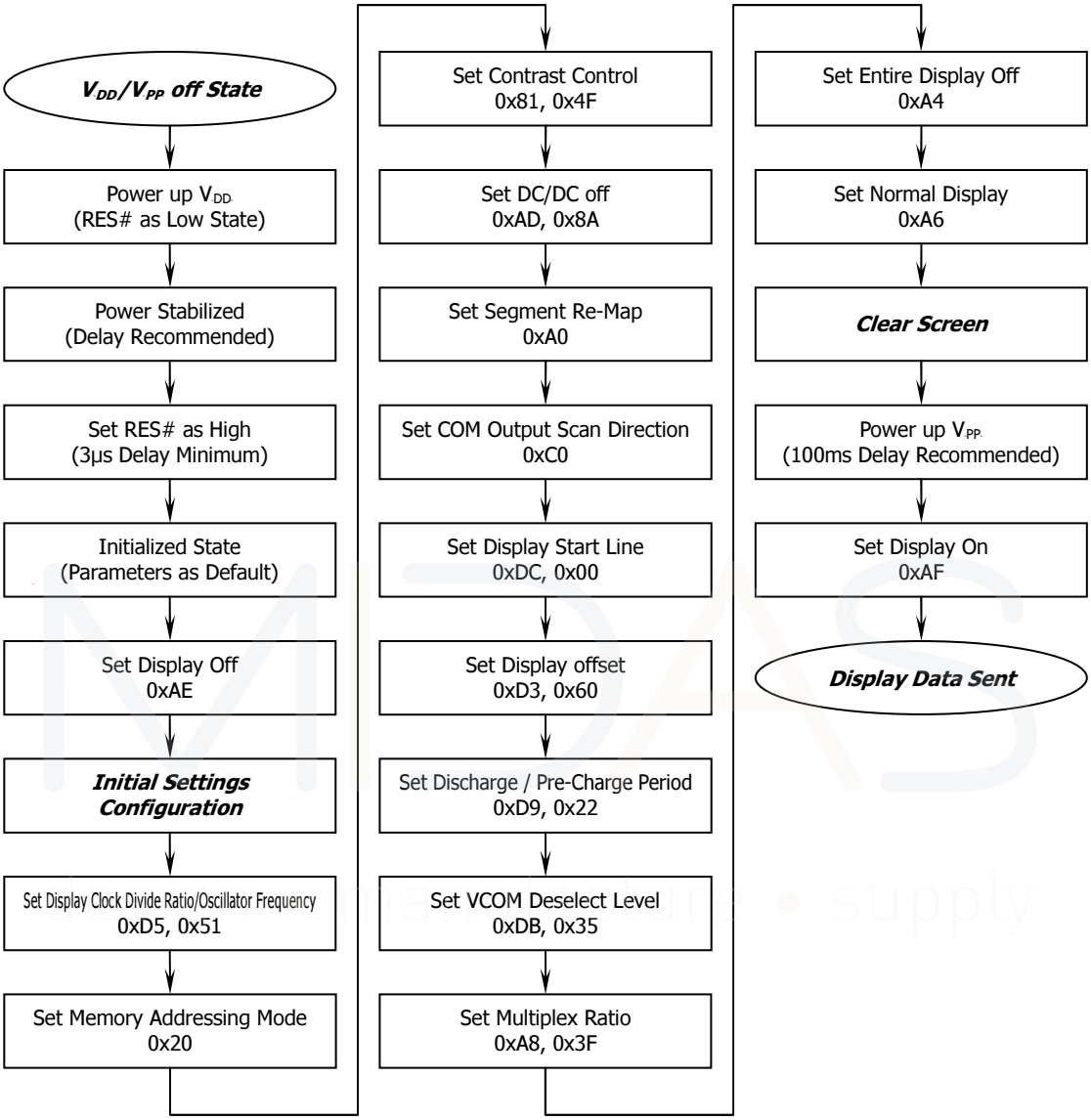
4.4.2 I^2C interface



4.5 Actual Application Example

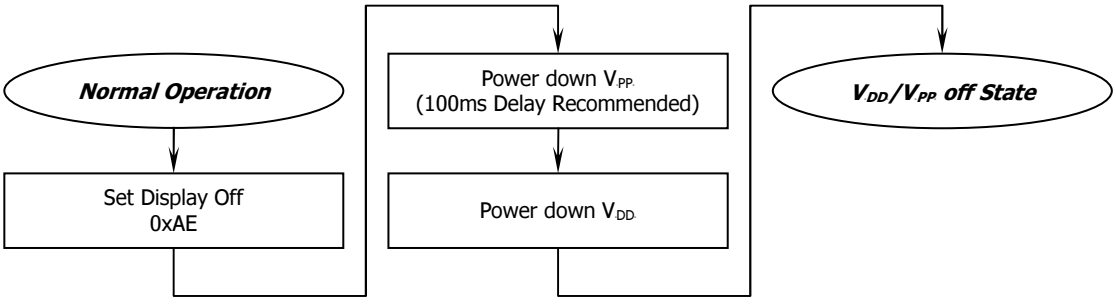
Command usage and explanation of an actual example

<Power up Sequence>

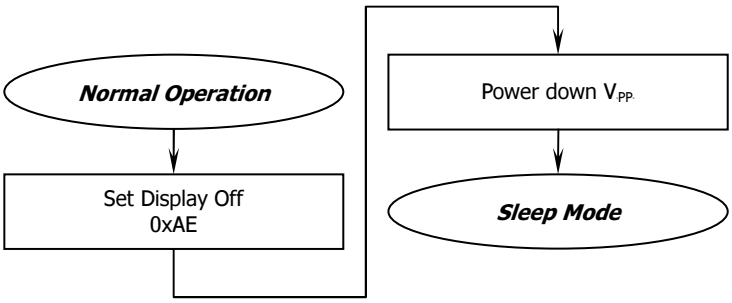


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>