M16C/62A Group, M16C/62P Group

Replacement Guide for M16C/62A (Discontinued Model)

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Abstract

This application note is a reference material for replacing the M16C/62A Group, which is discontinued model and upward compatible, with the M16C/62P Group. The document describes the changes required when replacing the M16C/62A Group with the M16C/62P Group using the existing usage conditions for the M16C/62A Group.

Please have a careful evaluation after replacing the product. Then the detailed specifications for each function must be confirmed with the User's Manual: Hardware.

Products

- M16C/62A Group
- M16C/62P Group

Contents

1. Why the M16C/62P Group is Suitable for Replacing the M16C/62A Group

The M16C/62P Group includes enhanced peripheral functions while it maintains compatibility of pin allocations and peripheral functions with the M16C/62A. Also the M16C/62P Group has fewer differences with the M16C/62A compared with other groups. Thus the replacement can be done easily. Furthermore the M16C/62P Group is the Product Longevity Program (PLP) product. Visit our website to see the detailed information of the PLP products.

Figure 1.1 Successor Products of the M16C/62A Group.

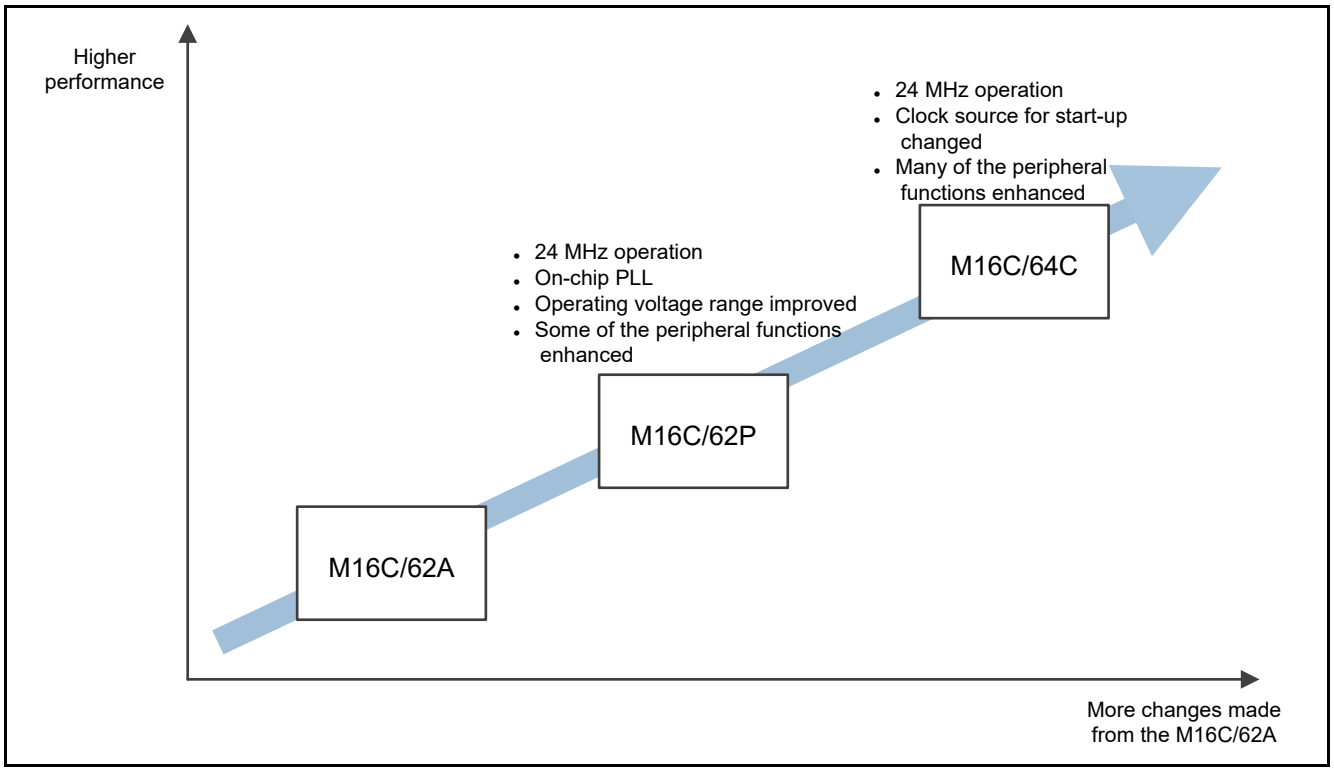

Figure 1.1 Successor Products of the M16C/62A Group

2. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- M16C/62P, M16C/62A Group Differences between M16C/62P and M16C/62A Rev.2.02 (REJ05B0186)
- M16C/62P Group Flash Memory Version CPU Rewrite Mode (EW0 Mode) Sample Rev.1.00 (REJ05B0600)

For reference application notes, the latest versions are always recommended. Visit the Renesas Electronics Corporation website to check and download the latest version.

3. Replacing the Software

Table 3.1 lists the peripheral functions that need changes in the software. For differences in functions (overview only), pin functions, and development tools, refer to the application notes listed in 2.Reference Application Notes. The descriptions in this section assume that the value after reset is used for the SFR registers newly added in the M16C/62P and the new functions are not used. This document provides the information for replacement between 100-pin products.

When using the peripheral functions listed in Table 3.1, the software needs to be changed. Also careful evaluation must be performed since the operation timings may differ.

3.1 Changes Required in the Software When Replacing M16C/62A with M16C/62P

3.1.1 Peripheral Functions that Need Changes in the Software

Table 3.1 Peripheral Functions that Need Changes in the Software

Peripheral Function	Mode	Item to be Changed in the Software
Processor mode	Single-chip mode	Common for all modes • The value in the PM13 bit after a reset is different. M16C/62A: 0 M16C/62P: 1 Memory expansion mode and microprocessor mode • The following addresses are reserved areas in M16C/62P. Do not access these areas in M16C/62P. • 08000h to 10000h • 27000h to 28000h
	Memory expansion mode	
	Microprocessor mode	
Watchdog timer (monitoring timer)	—	Write a program to refresh the counter in the watchdog timer interrupt.
Three-phase motor control timer	—	Set 1 to the PRC1 bit in the Protect (PRCR) register to write registers INVC0 and INVC1.
Serial interface (1)	Clock synchronous serial I/O mode	Setting values of the SFRs in the M16C/62A can be used in M16C/62P without any change.
	Clock asynchronous serial I/O (UART) mode	UART0, UART1 • Sleep mode cannot be used.
	Simple I^2C mode (special mode 1)	UART2 • The LSYN bit has been removed from the products except M3062LFGFP and M3062LFGPGP. • The SDDS bit has been removed. • The SHTC bit has been removed.
	SIM mode	UART0, UART1 • Sleep mode cannot be used.
Flash memory	EW0 mode	The SFRs and control commands are different between M16C/62A and M16C/62P.
External bus	—	The address bus width and external bus are different between M16C/62A and M16C/62P.

Note:
1. The following operation timings are different between M16C/62A and M16C/62P:
RTS assertion, overrun error occurrence, and transmission start (UART2 only).

3.1.2 Replacing the Software for Processor Mode

This section describes the changes required when replacing the software for processor mode.

- Value of the PM13 bit after a reset

  The value of the PM13 bit after a reset is different between M16C/62A and M16C/62P. Change the setting value according to the value set in M16C/62A.

- Memory space

  Addresses 08000h to 10000h and 27000h and 28000h are reserved areas in M16C/62P. If these areas are used in M16C/62A, relocate the contents in the areas to other areas.

3.1.3 Replacing the Software for the Watchdog Timer (Monitoring Timer)

This section describes the changes required when replacing the software for the watchdog timer.

- Refreshing the watchdog timer start register after an underflow

  In M16C/62P, the counter must be refreshed when the watchdog timer underflows. Add a program to the watchdog timer interrupt handler to refresh the counter by writing a given value to the watchdog timer start register.

3.1.4 Replacing the Software for the Three-Phase Motor Control Timer

This section describes the changes required when replacing the software for the three-phase motor control timer.

- Protection for registers INVC0 and INVC1

  The write protection function is available for registers INVC0 and INVC1 in the M16C/62P. Set the PRC1 bit in the PRCR register to 1 (write enabled) before writing to registers INVC0 and INVC1.

3.1.5 Replacing the Software for the Serial Interface

This section describes the changes required when replacing the software for the serial interface. The following operation timings are different between M16C/62A and M16C/62P.

- Timing of RTS assertion
- Timing when an overrun error occurs
- Timing to start transmission (UART2 only)

A. When using clock synchronous serial I/O mode

Setting values of the SFRs in the M16C/62A can be used in M16C/62P without any change.

B. When using UART mode

(1) UART2

Setting values of the SFRs in the M16C/62A can be used in M16C/62P without any change.

(2) UART0 and UART1

- SLEP bit in the UiMR register (i = 0 and 1)

The SLEP bit has been removed in M16C/62P. Therefore sleep mode cannot be used. Bit 7 which is the corresponding bit to the SLEP bit currently has the function to switch the I/O polarity for TXD and RXD in M16C/62P. Set an appropriate value to bit 7 according to the communication format used.

C. Simple I^2C mode (UART2 only)

- LSYN bit in the U2SMR register

The LSYN bit has been removed in the M16C/62P products except M3062LFGFP and M3062LFGPGP. The bit corresponding to the LSYN bit becomes a reserved bit in the product without the LSYN bit. Set 0 to the bit.

- SDDS bit in the U2SMR register

The SDDS bit has been removed in M16C/62P and bit 7 which is the corresponding bit to the SDDS bit currently becomes a reserved bit. Set 0 to bit 7 in the U2SMR register.

The digital delay setup value must be set to 300 ns or greater by bits DL2 to DL0 in the U2SMR3 register.

- SHTC bit in the U2SMR2 register

The SHTC bit has been removed in M16C/62P and bit 7 which is the corresponding bit to the SHTC bit currently becomes a reserved bit. Set 0 to bit 7 in the U2SMR2 register.

The equivalent function of the SHTC bit can be achieved by setting the IICM bit in the U2SMR register to 1.

D. SIM mode

1. UART2

   Setting values of the SFRs in the M16C/62A can be used in M16C/62P without any change.

2. UART0 and UART1

   - SLEP bit in the UiMR register (i = 0 and 1)

   The SLEP bit has been removed in M16C/62P. Therefore sleep mode cannot be used. Bit 7 which is the corresponding bit to the SLEP bit currently has the function to switch the I/O polarity for TXD and RXD in M16C/62P. Set an appropriate value to bit 7 according to the communication format used.

3.1.6 Replacing the Software for the Flash Memory

The software commands that controls programming operation for the flash memory differ between M16C/62A and M16C/62P. Thus the program has to be redesigned. Please replace the program in reference to the application notes listed in 2. Reference Application Notes.

3.1.7 Replacing the Software for the External Bus

This section describes the changes required when replacing the software for the external bus.

A. **Address bus width**

PM06 bit in PM0 register and PM11 bit in PM1 register have the function address output in M16C/62P. Set an appropriate value to for each register according to the address bus width used.

B. **Separate bus**

1. External bus timing of a separate bus (no wait)

   M16C/62A and M16C/62P have a different external bus timing for the separate bus (no wait) write cycle.

   Table 3.2 list differences of the external bus timing at a separate bus (no wait) write cycle.

   Figure 3.1 and Figure 3.2 show the external bus timing of a separate bus (no wait) for M16C/62A and M16C/62P respectively.

Table 3.2 Separate bus (no wait) external bus timing differences at write cycle

Item	M16C/62A	M16C/62P
Bus cycle	1 BCLK cycle	2 BCLK cycle
Write signal output timing	Falling of the first bus cycle	Rise of the second bus cycle
Data bus output width	1/2 BCLK cycle	1 BCLK cycle
Data bus output timing	Falling of the first bus cycle	Rise of the second bus cycle
Address bus output width	1 BCLK cycle	2 BCLK cycle
Chip select output timing	1 BCLK cycle	2 BCLK cycle

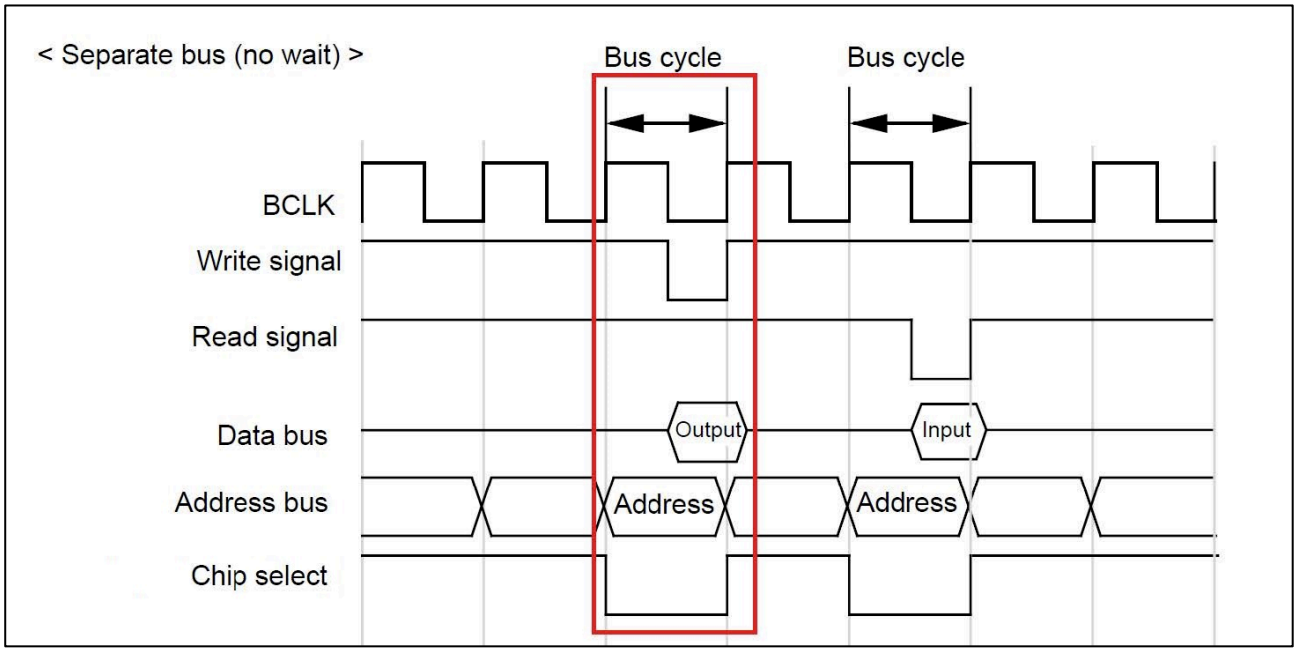

Figure 3.1 External bus timing of separate bus(no wait) for M16C/62A

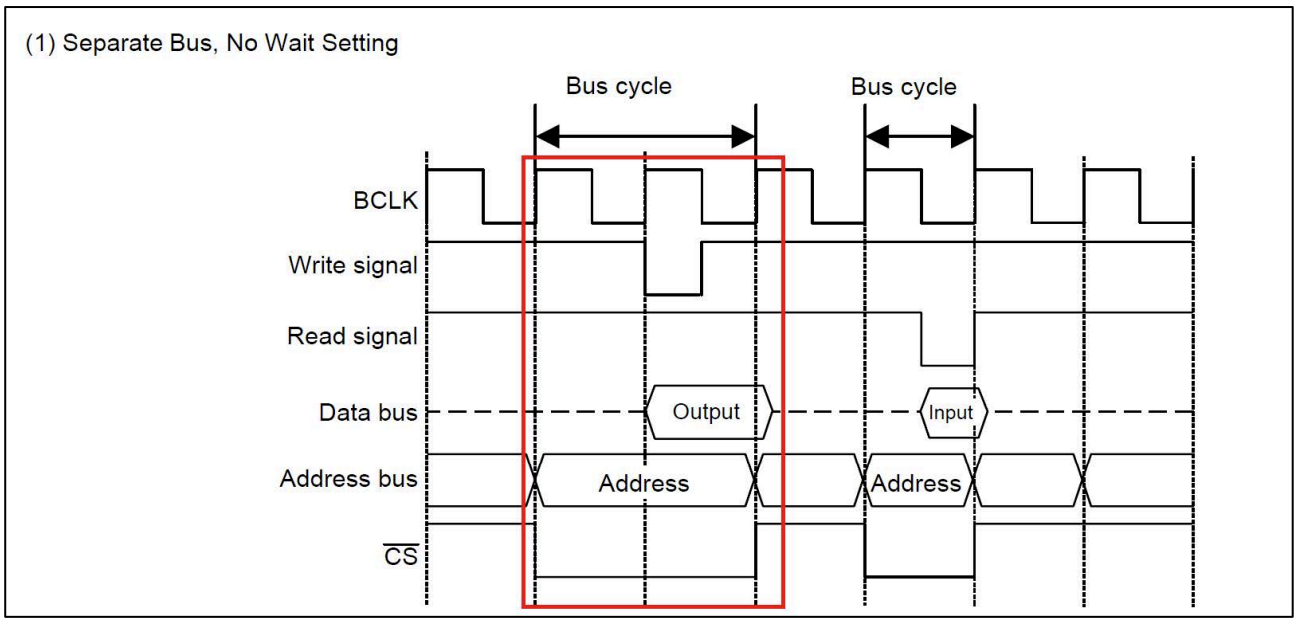

Figure 3.2 External bus timing of separate bus(no wait) for M16C/62P

2. External bus timing of separate bus (1wait)
M16C/62A and M16C/62P have a different write signal output width at the separate bus write cycle (1 wait setting) . Figure 3.3 and Figure 3.4 show examples of the external bus timing of the separate bus(with wait) for M16C/62A and separate bus(1 wait) for M16C/62P respectively.

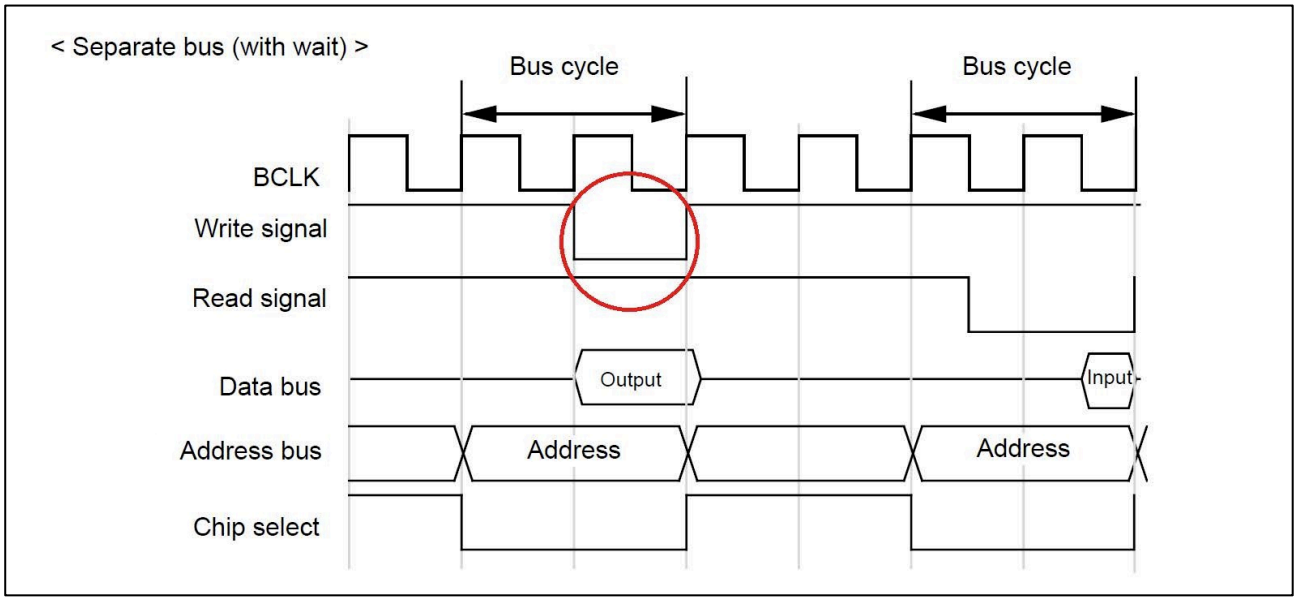

Figure 3.3 External bus timing of separate bus(with wait) for M16C/62A

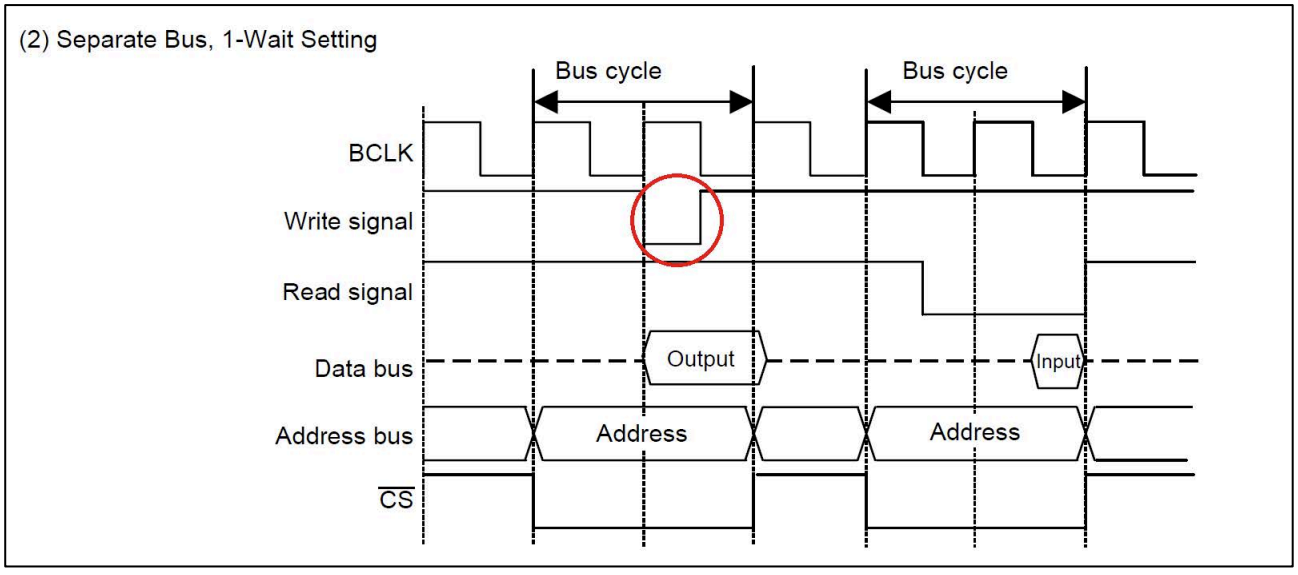

Figure 3.4 External bus timing of separate bus(1 wait) for M16C/62P

3. The number of separate bus wait cycles available in M16C/62P

The number of separate bus wait cycles are selectable from 1 wait to 2-3 waits .
Figure 3.5 and Figure 3.6 show example of the external bus timing for a separate bus(2 wait) for M16C/62P , and the external bus timing of a separate bus (3 wait) for M16C/62P respectively.

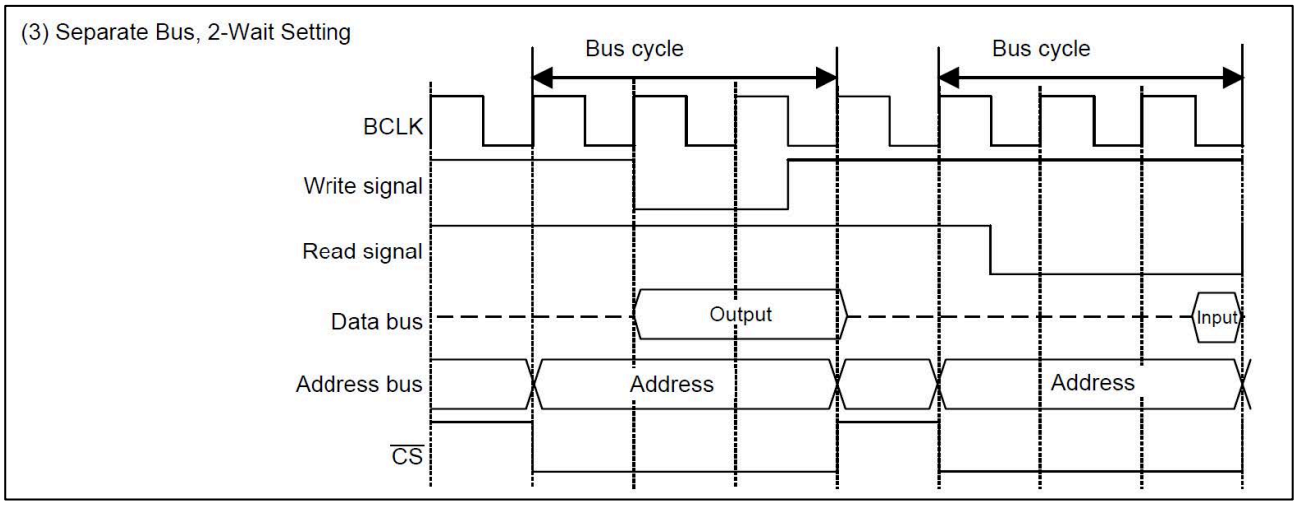

Figure 3.5 External bus timing of separate bus (2 waits) for M16C/62P

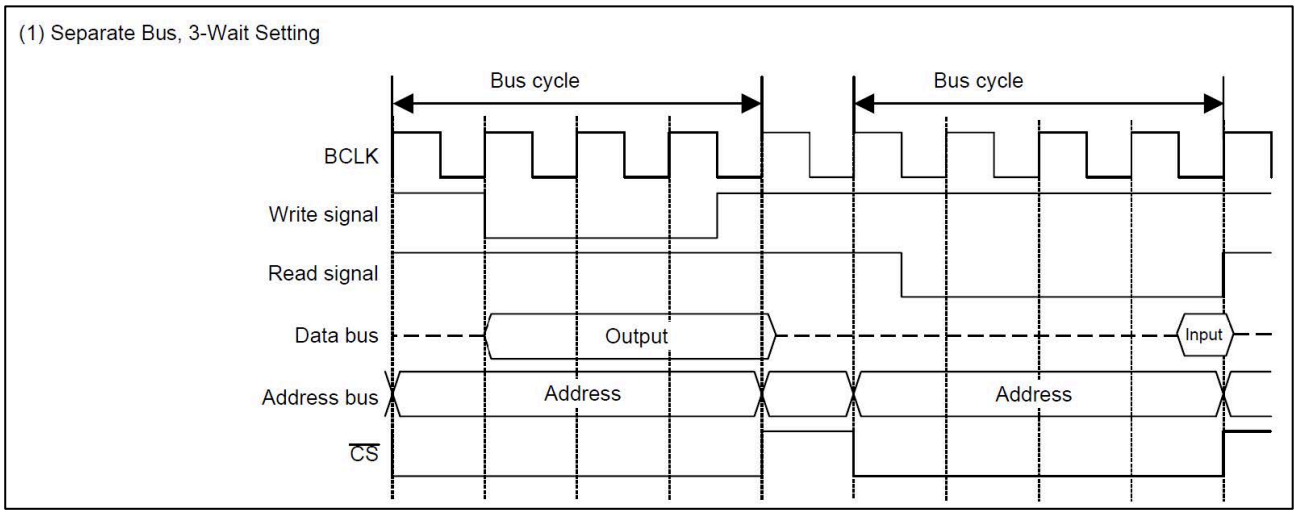

Figure 3.6 External bus timing of separate bus(3 waits) for M16C/62P

C. **Multiplexed Bus**

The external bus timing is the same for M16C/62A and M16C/ 62P in the multiplexed bus (1 wait). The number of the multiplexed bus wait cycles are selectable from 1 wait to 2- 3 waits for M16C/62P. Figure 3.7 and Figure 3.8 shows the external bus timing of the multiplexed bus(1 or 2 wait(s)) for M16C/62P and multiplexed bus(3 waits) for M16C/62P respectively.

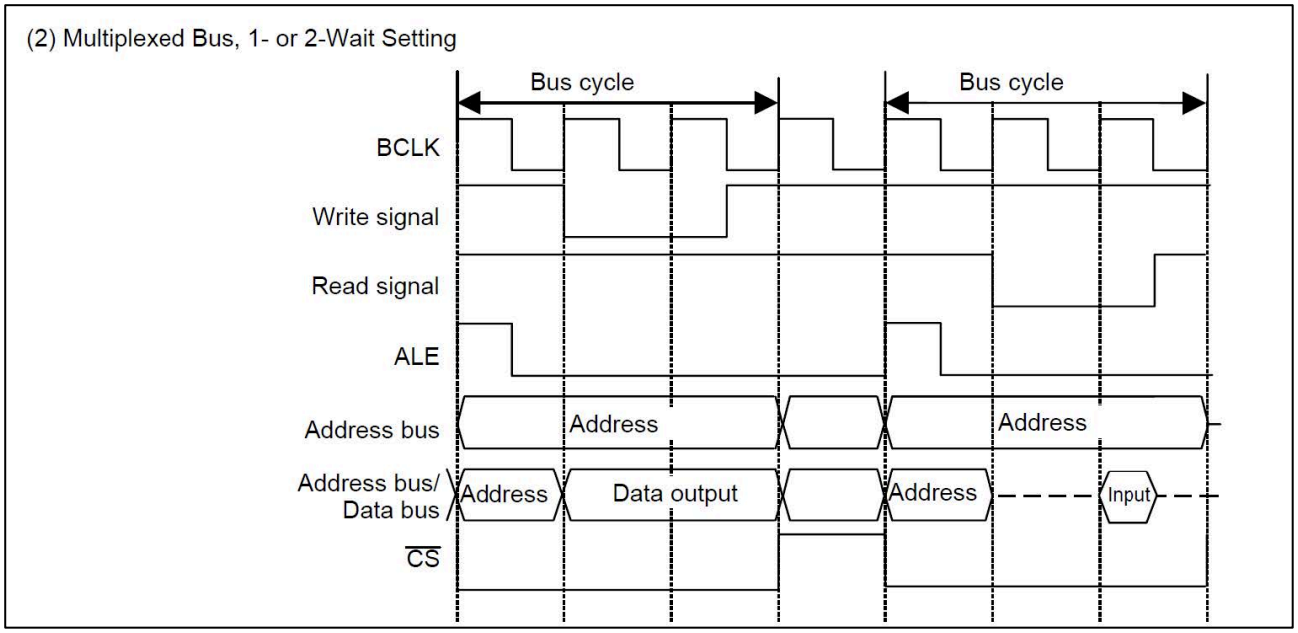

Figure 3.7 External bus timing of Multiplexed bus(1 or 2 wait) for M16C/62P

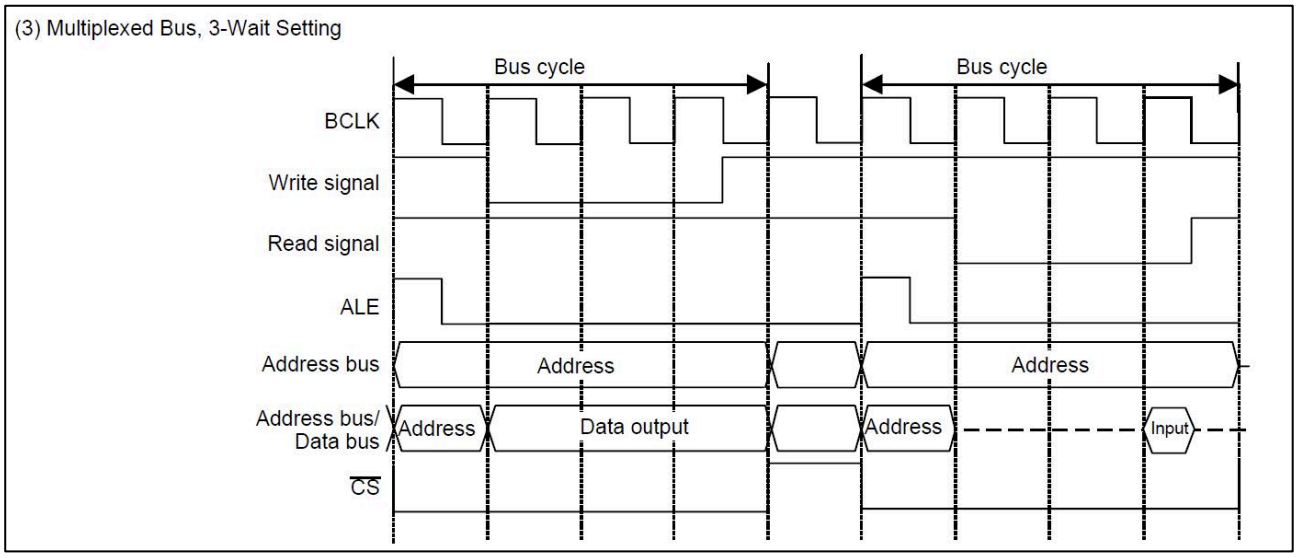

Figure 3.8 External bus timing of multiplexed bus (3 wait) for M16C/62P

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4. FAQs Relating to the M16C/62A Replacement

The following tables list frequently asked questions relating to the M16C/62A replacement with the M16C/62P.

Q-1	When replacing M16C/62A with M16C/62P, if additional functions are not used, can the current hardware be used without any change?
A-1	The hardware can be basically used as it is since pin functions and pin allocations are compatible between the Groups. However the electrical characteristics or noise tolerance may possibly be different between the Groups. Please have a careful evaluation with the user system. Also contact the crystal/ceramic resonator manufacturer and decide the optimum oscillator parameter on the user system.

Q-2	Do M16C/62A and M16C/62P use the same access cycle for SFR registers/ internal RAM/internal ROM ?
A-2	Yes, the access cycle is the same for M16C/62A and M16C/62P. However, when using M16C/62P with the PLL clock at the clock frequency higher than 16 MHz, set the PM20 bit in the PM2 register to 0 (2 wait) so that the SFR register access cycle is set to 2 waits.

Q-3	M16C/62A is upward compatible with M16C/62P. What is actually compatible - e.g. development environment or development language?
A-3	Please refer to the following application note for the differences of development tool between the Groups. • Differences between M16C/62P and M16C/62A (REJ05B0186) http://www.renesas.com/products/mpumcu/m16c/m16c60/m16c62p/app_notes.jsp

Q-4	We use the three-phase motor control timer function. There is a note regarding the INV16 bit in the M16C/62P Group User's Manual: Hardware. According to the note, when the following conditions are met, the INV16 bit must be set to 1. • INV15 bit is 0 (enables dead time) • INV03 bit is 1 (enables three-phase control timer output) Currently the bit corresponding to the INV16 bit is set to 0 while the conditions above are met since bits INV14, INV15, and INV16 do not exist in M16C/62A. If the INV16 bit is 0 when the conditions above are met, what sort of risk will we have?
A-4	The INV16 bit is newly added function in the M16C/62P for the case the dead time becomes short. If bits INV14, INV15, and INV16 are set to 0, the operation will be the same as the M16C/62A. If the operation has been confirmed with that particular condition in the M16C/62A, the INV16 bit does not need to be set. However we recommend complying with the User's Manual: Hardware for the product used. Please have a careful evaluation with the setting and determine what setting to be used.

5. Appendix

5.1 SFRs that Have Bits Changed in M16C/62P from M16C/62A

Table 5.1 to Table 5.5 list the SFRs that have bits changed in M16C/62P from M16C/62A.

Table 5.1 SFRs that Have Bits Changed in M16C/62P from M16C/62A (1/5)

* Processor mode register (PM1)

M16C/62A		M16C/62P		Remarks
PM10	Reserved	Set to 0.	CS2 area switch bit	0: 08000h to 26FFFh (Block A disable)	
PM11	Reserved	Set to 0.	Port P3_7 to P3_4 function select bit	0: Address output	
PM12	Reserved	Set to 0.	Watchdog timer function select bit	0: Watchdog timer interrupt 1: Watchdog timer reset	
PM13	Internal reserved area expansion bit	0 : The internal RAM area is 15 kbytes or less and the internal ROM area is 192 kbytes or less 1: Expands the internal RAM area and internal ROM area to over 15 kbytes and to over 192 kbytes respectively.	Internal reserved area expansion bit	0: Internal RAM area: 15 Kbytes, internal ROM area: 192 Kbytes 1: Entire internal RAM area can be used and entire ROM area can be used.	The value after a reset is different depending on the MCU Group as listed below. M16C/62A: 0 M16C/62P: 1
PM14 PM15	Reserved	Set to 0.	Memory area expansion bit	00: 1-Mbyte mode (no expansion) 11: 4-Mbyte mode	

* System clock control register 0 (CM0)

M16C/62A		M16C/62P		Remarks
CM07	System clock select bit	0: XIN_XOUT 1: XCIN_XCOUT	System clock select bit	0: Main clock, PLL clock, or on-chip oscillator clock 1: Sub clock	

* System clock control register 1 (CM1)

M16C/62A		M16C/62P		Remarks
CM11	Reserved	Set to 0.	System Clock Select Bit 1	0: Main clock 1: PLL clock	

* Protect register (PRCR)

M16C/62A		M16C/62P		Remarks
PRC0	Enables writing to system clock control registers 0 and 1 (addresses 0006_{16} and 0007_{16})	0: Write-inhibited 1: Write-enabled	Enable write to CM0, CM1, CM2, PLC0 and PCLKR registers	0: Write protected 1: Write enabled	
PRC1	Enables writing to processor mode registers 0 and 1 (addresses 0004_{16} and 0005_{16})	0: Write-inhibited 1: Write-enabled	Enable write to PM0, PM1, PM2, TB2SC, INVC0 and INVC1 registers	0: Write protected 1: Write enabled	
PRC3	Reserved	Set to 0.	Enable write to VCR2 and D4INT registers	0: Write protected 1: Write enabled	

* Watchdog timer control register (WDC)

M16C/62A		M16C/62P		Remarks
WDC5	Reserved	Set to 0.	Cold start/warm start discrimination flag	0: Cold start 1: Warm start	

Table 5.2 SFRs that Have Bits Changed in M16C/62P from M16C/62A (2/5)

* Three-phase PWM control register 1 (62A)/Three-phase control register 1 (62P) (INVC1)

	M16C/62A		M16C/62P		Remarks
INV10	Timer Ai start trigger signal select bit	0: Timer B2 overflow signal 1: Timer B2 overflow signal, signal for writing to timer B2	Timer A1, A2 and A4 start trigger select bit	0: Timer B2 underflow 1: Timer B2 underflow and write to Timer B2	
INV12	Short circuit timer count source select bit	0: Do not set. 1: f1/2	Dead time timer count source select bit	0: f1 or f2 1: f1 divided-by-2 or f2 divided-by-2	
INV13	Reserved	Set to 0.	Carrier wave detect bit	0: Timer A1 reload control signal is 0 1: Timer A1 reload control signal is 1	
INV14	Reserved	Set to 0.	Output polarity control bit	0: Active Low of an output waveform 1: Active High of an output waveform	
INV15	Reserved	Set to 0.	Dead time disable bit	0: Enables dead time 1: Disables dead time	
INV16	Reserved	Set to 0.	Dead time timer trigger select bit	0: Falling edge of a one-shot pulse of Timer A1, A2, A4 1: Rising edge of the three-phase output shift register (U-, V-, W-phase)	

* SI/O3 control register (S3C)

	M16C/62A		M16C/62P		Remarks
SM34	Reserved	Set to 0.	CLK polarity select bit	0: Transmit data is output at falling edge of transfer clock and receive data is input at rising edge. 1: Transmit data is output at rising edge of transfer clock and receive data is input at falling edge.	

* SI/O4 control register (S4C)

	M16C/62A		M16C/62P		Remarks
SM44	Reserved	Set to 0.	CLK polarity select bit	0: Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1: Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	

Table 5.3 SFRs that Have Bits Changed in M16C/62P from M16C/62A (3/5)

* UART2 special mode register 3 (U2SMR3)

M16C/62A			M16C/62P		Remarks
CKPH	Reserved	Set to 0.	Clock phase set bit	0: Without clock delay 1: With clock delay	
NODC	Reserved	Set to 0.	Clock output select bit	0: CLKi is CMOS output 1: CLKi is N-channel open drain output	
DL2 to DL0	SDA digital delay setup bit	000: Analog delay is selected 001:1 to 2 cycle(s) of 1/f(XIN) 010: 2 to 3 cycles of 1/f(XIN) 011: 3 to 4 cycles of 1/f(XIN) 100: 4 to 5 cycles of 1/f(XIN) 101: 5 to 6 cycles of 1/f(XIN) 110: 6 to 7 cycles of 1/f(XIN) 111: 7 to 8 cycles of 1/f(XIN)	SDA2 digital delay setup bit	000: Without delay 001: 1 to 2 cycle(s) of UiBRG count source 010: 2 to 3 cycles of UiBRG count source 011: 3 to 4 cycles of UiBRG count source 100: 4 to 5 cycles of UiBRG count source 101: 5 to 6 cycles of UiBRG count source 110: 6 to 7 cycles of UiBRG count source 111: 7 to 8 cycles of UiBRG count source	Set 300 ns or greater value for digital delay value.

* UART2 special mode register 2 (U2SMR2)

M16C/62A			M16C/62P		Remarks
SHTC	Start/stop condition control bit	0: Set up time/hold time is not set. 1: Set up time/hold time is set.	Reserved	Set to 0.	

* UART2 special mode register (U2SMR)

M16C/62A			M16C/62P		Remarks
LSYN	SCLL sync output enable bit	0: Disabled 1: Enabled	M3062LFGPFP and M3062LFGPGP: SCLL sync output enable bit Products other than above: Reseved bit	M3062LFGPFP and M3062LFGPGP: 0: Disable, 1: Enable Products other than above: Set to 0.	
SDDS	SDA digital delay select bit	0: Analog delay output is selected 1: Digital delay output is selected	Reserved	Set to 0.	

* One-shot start flag (ONSF)

M16C/62A			M16C/62P		Remarks
TAZIE	Reserved	Set to 0.	Z-phase input enable bit	0: Z-phase input disabled 1: Z-phase input enabled	

* UART0 transmit/receive mode register (U0MR)

M16C/62A			M16C/62P		Remarks
SMD2 to SMD0	Serial I/O mode select bit	Clock synchronous serial I/O mode: Set to 001. UART mode: 100: Transfer data 7 bits long 101: Transfer data 8 bits long 110: Transfer data 9 bits long	Serial I/O mode select bit	000: Serial interface disabled 001: Clock synchronous serial I/O mode 010: I2C mode 100: UART mode transfer data 7 bits long 101: UART mode transfer data 8 bits long 110: UART mode transfer data 9 bits long Do not set except above	
SLEP (62A), IOPOL (62P)	Sleep select bit	0: Sleep mode deselected 1: Sleep mode selected	TXD, RXD I/O polarity reverse bit	0: No reverse 1: Reverse	

Table 5.4 SFRs that Have Bits Changed in M16C/62P from M16C/62A (4/5)

* UART0 transmit/receive control register 0 (U0C0)

M16C/62A			M16C/62P		Remarks
NCH	Data output select bit	0: TXDi pin is CMOS output 1: TXDi pin is N-channel open-drain output	Data output select bit	0: TXDi/SDAi and SCLi pins are CMOS output 1: TXDi/SDAi and SCLi pins are N-channel open-drain output	

* UART0 transmit/receive control register 1 (U0C1)

M16C/62A			M16C/62P		Remarks
U0LCH	Reserved	Set to 0.	Data logic select bit	0: No reverse 1: Reverse	
U0ERE	Reserved	Set to 0.	Error signal output enable bit	0: Output disabled 1: Output enabled	

* UART1 transmit/receive mode register (U1MR)

M16C/62A			M16C/62P		Remarks
SMD2 to SMD0	Serial I/O mode select bit	Clock synchronous serial I/O mode: Set to 001. UART mode: 100: Transfer data 7 bits long 101: Transfer data 8 bits long 110: Transfer data 9 bits long	Serial I/O mode select bit	000: Serial interface disabled 001: Clock synchronous serial I/O mode 010: I2C mode 100: UART mode transfer data 7 bits long 101: UART mode transfer data 8 bits long 110: UART mode transfer data 9 bits long Do not set except above	
SLEP (62A), IOPOL	Sleep select bit	UART mode: 0: Sleep mode deselected 1: Sleep mode selected	TXD, RXD I/O polarity reverse bit	0: No reverse 1: Reverse	

* UART1 transmit/receive control register 1 (U1C1)

M16C/62A			M16C/62P		Remarks
U1LCH	Reserved	Set to 0.	Data logic select bit	0: No reverse 1: Reverse	
U1ERE	Reserved	Set to 0.	Error signal output enable bit	0: Output disabled 1: Output enabled	

* UART transmit/receive control register 2 (UCON)

M16C/62A			M16C/62P		Remarks
RCSP	Reserved	Set to 0.	Separate UART0 CTS/RTS bit	0: CTS/RTS shared pin 1: CTS/RTS separated (CTS0 supplied from the P6_4 pin)	

Table 5.5 SFRs that Have Bits Changed in M16C/62P from M16C/62A (5/5)

* Flash memory control register 1 (FMR1)

M16C/62A			M16C/62P		Remarks
FMR11	Reserved	Set to 0.	EW1 mode select bit	0: EW0 mode 1: EW1 mode	
FMR13	Flash memory power supply-OFF bit	0: Flash memory power supply is connected. 1: Flash memory power supply-off	Reserved	Set to 0.	
FMR16	Reserved	Set to 0.	Lock bit status flag	0: Lock 1: Unlock	

* Flash memory control register 0 (FMR0)

M16C/62A			M16C/62P		Remarks
FMR03 (62A), FMSTP (62P)	Flash memory reset bit	0: Normal operation 1: Reset	Flash memory stop bit	0: Enables flash memory operation 1: Stops flash memory operation (placed in low power mode, flash memory initialized)	
FMR07	Reserved	Set to 0.	Erase status flag	0: Terminated normally 1: Terminated in error	

* A-D control register 2 (ADCON2)

M16C/62A			M16C/62P		Remarks
ADGSEL1-ADGSEL0	Reserved	Set to 0.	A/D input group select bit	00: Port P10 group is selected 01: Do not set 10: Port P0 group is selected 11: Port P2 group is selected	
CKS2	Reserved	Set to 0.	Frequency select bit 2	0: Selects fAD, fAD divided by 2, or fAD divided by 4. 1: Selects fAD divided by 3, fAD divided by 6, or fAD divided by 12.	

6. Reference Documents

User's Manual: Hardware

M16C/62A Group User's Manual: Hardware Rev.1.00 (MEJ06B0006-0100Z)

M16C/62P Group User's Manual: Hardware Rev.2.41 (REJ09B0185-0241)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	M16C/62A Group, M16C/62P Group Application Note Replacement Guide for M16C/62A (Discontinued Model)

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 15, 2014	—	First edition issued
1.10	Dec. 15, 2017	2	Added item in Contents “Replacing the Software for the External bus”
		4	Added item in Table 3.1 “External bus”
		7	Added section “3.1.7 Replacing the Software for the External bus”
		12	Revised the description in Q2 from "RAM, and ROM" to "internal RAM, and internal ROM"

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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