2ED21091S06F

650 V half bridge gate driver with integrated bootstrap diode

Features

- Unique Infineon Thin-Film-Silicon On Insulator (SOI)-technology
- Negative VS transient immunity of 100 V
- Floating channel designed for bootstrap operation
- Operating voltages (VS node) upto + 650 V
- Maximum bootstrap voltage (VB node) of + 675 V
- Integrated ultra-fast, low resistance bootstrap diode
- Logic operational up to –11 V on VS Pin
- Negative voltage tolerance on inputs of –5 V
- Independent under voltage lockout for both channels
- Schmitt trigger inputs with hysteresis
- 3.3 V, 5 V and 15 V input logic compatible
- Maximum supply voltage of 25 V
- Internal 540 ns dead time and programmable up to 2.7 us with external resistor
- The dual function DT/SD input turns off both channels
- RoHS compliant

Product summary

V_{S_OFFSET} = 650 V max.
I_{o+pk} / I_{o-pk} (typ.) = + 0.29 A/ - 0.7 A
V_{CC} = 10 V to 20 V
Internal deadtime = 540 ns typ.
t_{ON} / t_{OFF} (typ.) = 740 ns/ 200 ns

Packages

DSO-8

Potential applications

Driving IGBTs, enhancement mode N-Channel MOSFETs in various power electronic applications.
Typical Infineon recommendations are as below:

- Motor drives, general purpose inverters having TRENCHSTOP™ IGBT6 or 600 V EasyPACK™ modules or its equivalent power stages
- Refrigeration compressors, induction cookers, other major home appliances having RCD series IGBTs or TRENCHSTOP™ family IGBTs or their equivalent power stages
- Battery operated small home appliances such as power tools, vaccum cleaners using low voltage OptiMOS™ MOSFETs or their equivalent power stages
- Totem pole, half-bridge and full-bridge converters in offline AC-DC power supplies for industrial SMPS having high voltage CoolMOS™ super junction MOSFETs or TRENCHSTOP™ H3 and WR5 IGBT series or their equivalent
- High power LED and HID lighting having CoolMOS™ super junction MOSFETs
- Electric vehicle (EV) charging stations and battery management systems
- Driving 650 V SiC MOSFETs in above applications

Product validation

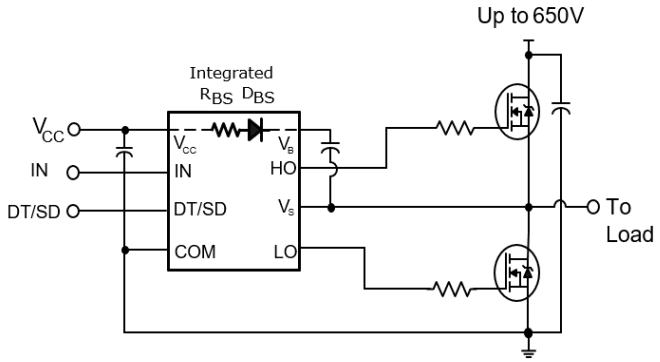
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Ordering information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
2ED21091S06F	DSO - 8	Tape and Reel	2500	2ED21091S06FXUMA1

Description

The 2ED21091S06F is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Based on Infineon's SOI-technology there is an excellent ruggedness and noise immunity with capability to maintain operational logic at negative voltages of up to - 11 V on VS pin (V_{CC} = 15 V) on transient voltages. There are not any parasitic thyristor structures present in the device, hence no parasitic latch up may occur at all temperature and voltage conditions. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET, SiC MOSFET or IGBT in the high side configuration, which operate up to 650 V.



Refer to lead assignments for correct pin configuration. This diagram shows electrical connections only. Please refer to our application notes and design tips for proper circuit board layout.

*Bootstrap diode is monolithically integrated

Figure 1 Typical application block diagram

Summary of feature comparison of the 2ED210x family:

Table 1

Part No.	Input logic	Cross conduction prevention logic	Deadtime	Ground pins	t_{ON} / t_{OFF}	Package
2ED2106S06F	HIN, LIN	No	None	COM	200 ns / 200 ns	DSO - 8
2ED21064S06J				VSS / COM		DSO - 14
2ED2108S06F	HIN, $\overline{\text{LIN}}$	Yes	Internal 540 ns	COM		DSO - 8
2ED21084S06J			Programmable 540 ns - 5000 ns	VSS / COM		DSO - 14
2ED2109S06F	IN, $\overline{\text{SD}}$	Yes	Internal 540 ns	COM	740 ns / 200 ns	DSO - 8
2ED21094S06J			Programmable 540 ns - 5000 ns	VSS / COM		DSO - 14
2ED21091S06F	IN, DT/SD	Yes	Programmable 540 ns - 2700 ns	COM		DSO – 8

1 Table of contents

2 Block diagram

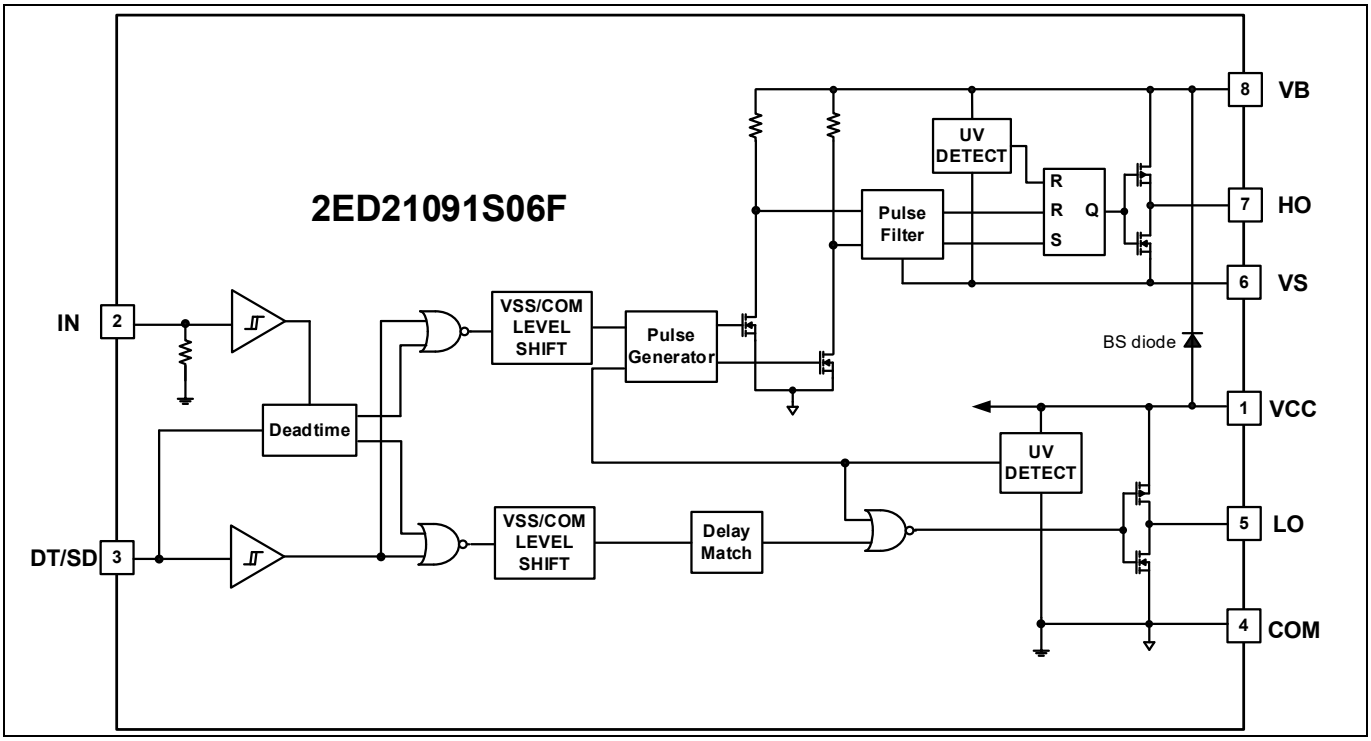
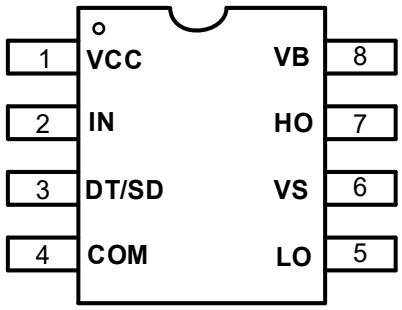


Figure 2 Block diagrams

3 Pin configuration and functionality

3.1 Pin configuration



8 - Lead DSO - 8 (150 mil)

2ED21091S06F

Figure 3 2ED2109S06F pin assignments (top view)

3.2 Pin functionality

Table 2

Symbol	Description
VCC	Low-side and logic supply voltage
IN	Logic input for high-side and low-side gate driver output (HO and LO), in phase with HO. Schmitt trigger input with hysteresis and pull down
DT/SD	Logic input for shut down (out of phase) and programmable dead time pin
COM	Low-side gate drive return
LO	Low-side driver output
VS	High voltage floating supply return
HO	High-side driver output
VB	High-side gate drive floating supply

4 Electrical parameters

4.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 3 Absolute maximum ratings

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating well supply voltage Note 1		V_{CC} – 5	675	V
V_S	High-side floating well supply return voltage		V_{CC} – V_{BS} – 5	650	
V_{HO}	Floating gate drive output voltage		V_S – 0.5	V_B + 0.5	
V_{BS}	Floating gate drive voltage supply voltage		-1	25	
V_{CC}	Low side supply voltage		-1	25	
V_{LO}	Low-side output voltage		- 0.5	V_{CC} + 0.5	
V_{IN}	Logic input voltage		- 5	V_{CC} + 0.5	
$V_{DT/SD}$	Programmable dead time pin voltage		- 0.5	4	
dV_S/dt	Allowable V_S offset supply transient relative to COM		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8 - Lead DSO - 8	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	8 - Lead DSO - 8	—	200	°C/W
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		- 55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins V_{CC} and V_B in case of activated bootstrap diode.

4.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} – COM) = (V_B – V_S) = 15 V.

Table 4 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_B	Bootstrap voltage	V_S + 10	V_S + 20	V
V_{BS}	High-side floating well supply voltage	10	20	
V_S	High-side floating well supply offset voltage Note 2	V_{CC} – V_{BS} – 1	650	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{CC}	Low-side supply voltage	10	20	
V_{LO}	Low-side output voltage	COM	V_{CC}	
V_{IN}	Logic input voltage	- 4	5	
$V_{DT/SD}$	Programmable dead time pin voltage	-0.5	4	
R_{DT}	Programmable dead time resistor	12	150	kΩ
T_A	Ambient temperature	- 40	125	°C

Note 2: Logic operation for V_S of – 11 V to +650 V.

4.3 Static electrical characteristics

(V_{CC} – COM) = (V_B – V_S) = 15 V, and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to Vss / COM and are applicable to the respective input leads: IN and DT/SD. The V_O and I_O parameters are referenced to V_S / COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Table 5 Static electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.6	8.2	8.9	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	6.7	7.2	8.1		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	—	1.0	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.4	9.1	9.8		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.5	8.2	8.9		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	—	0.9	—		
I_{LK}	High-side floating well offset supply leakage	—	1	12.5	uA	V_B = V_S = 650 V
I_{QBS}	Quiescent V_{BS} supply current	—	170	—		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	—	600	—		V_{IN} = 0 V or 5 V
V_{OH}	High level output voltage drop, V_{cc} - V_{LO}, V_B - V_{HO}	—	0.05	0.2	V	I_O = 2 mA
V_{OL}	Low level output voltage drop, V_O	—	0.02	0.1		
I_{o+mean}	Mean output current from 3 V to 6 V	180	230	—	mA	C_L = 22 nF
I_{o+}	Peak output current turn-on[1]	—	290	—		V_O = 0 V
I_{o-mean}	Mean output current from 12 V to 9 V	450	650	—		C_L = 22 nF
I_{o-}	Peak output current turn-off[1]	—	700	—		V_O = 15 V
V_{IH}	Logic “1” input voltage	1.7	2.1	2.4	V	Vcc = 10 V to 20 V
V_{IL}	Logic “0” input voltage	0.7	0.9	1.1		
$V_{SD,TH}$	/SD input threshold	0.7	0.9	1.1		
I_{IN+}	Input bias current (Output = High)	—	25	50	µA	IN = 5 V
I_{IN-}	Input bias current (Output = Low)	—	—	10		IN = 0 V
I_{SD+}	/SD input bias current	—	—	- 400		$V_{DT/SD}$ = 0 V
V_{FBSD}	Bootstrap diode forward voltage between Vcc and VB	—	1	1.2	V	I_F = 0.3 mA
I_{FBSD}	Bootstrap diode forward current between Vcc and VB	45	85	125	mA	V_{CC} - V_B = 4 V
R_{BSD}	Bootstrap diode resistance	20	30	45	Ω	V_{F1} = 4 V,V_{F2} = 5 V
V_S	Allowable Negative VS pin voltage for IN Signal propagation to HO	—	-11	-10	V	Vcc = 15 V

[1] Not subjected to production test, verified by characterization.

4.4 Dynamic electrical characteristics

V_{CC} = V_{BS} = 15 V, T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

Table 6 Dynamic electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	—	740	1030	ns	V_{IN} = 0 V or 5 V V_S = 0 V
t_{OFF}	Turn-off propagation delay	—	200	300		
tsd	Shut-down propagation delay	—	200	300		
t_R	Turn-on rise time	—	100	150		
t_F	Turn-off fall time	—	35	80		
MT	Delay matching time (HS & LS turn-on/off)	—	—	70		
DT	Dead time	350	540	730		RDT = 12 Ω
		1.9	2.7	3.5	us	RDT = 150 kΩ
MDT	Matching Dead time	—	0	70	ns	RDT = 12 Ω
		—	0	600		RDT = 150 kΩ

5 Application information and additional details

5.1 IGBT / MOSFET gate drive

The 2ED21091S06F HVIC is designed to drive MOSFET or IGBT power devices. Figure 4 and Figure 5 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

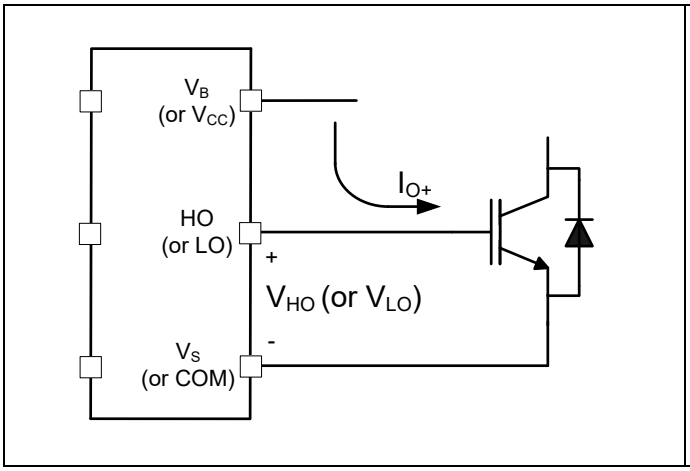


Figure 4 HVIC Sourcing current

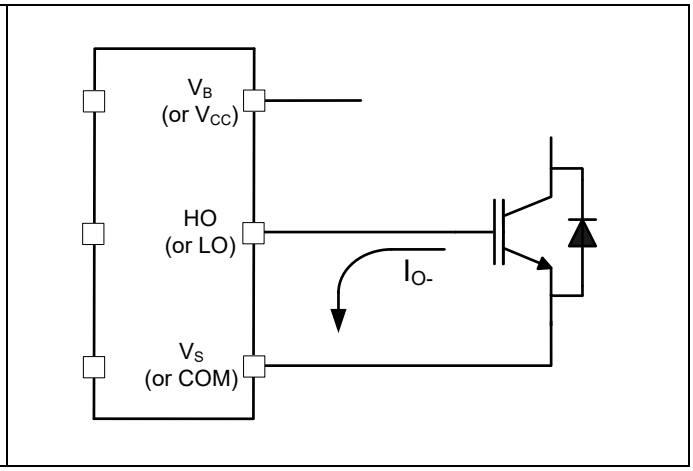


Figure 5 HVIC Sinking current

5.2 Switching and timing relationships

The relationships between the input and output signals of the 2ED21091S06F are illustrated below in Figure 6 and Figure 7. From these figures, we can see the definitions of several timing parameters (i.e. t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

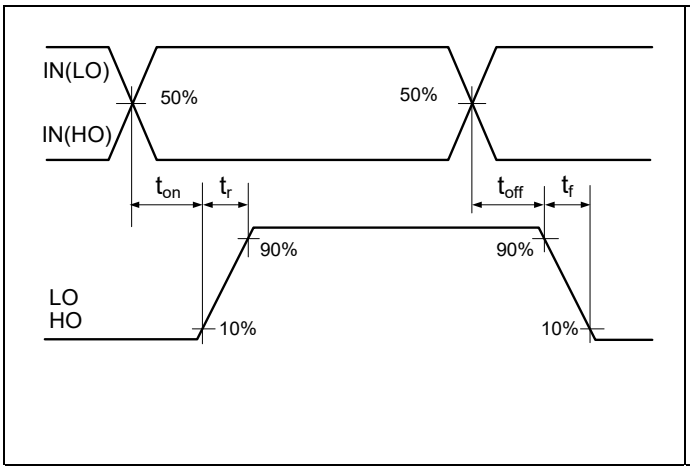


Figure 6 Switching timing diagram

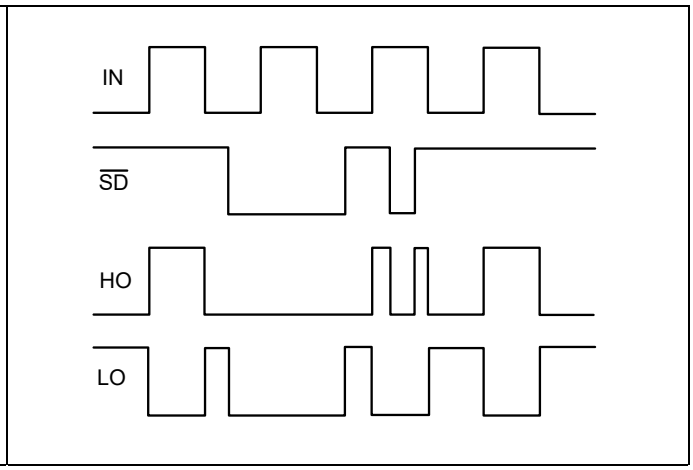


Figure 7 Input/output logic diagram

5.3 Deadtime

This family of HVICs features integrated deadtime protection circuitry. The deadtime is programmable for 2ED21091S06F, it is greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than interal deadtime; external deadtimes larger than internal deadtime are not modified by the gate driver. Figure 8 illustrates the deadtime period and the relationship between the output gate signals.
The deadtime circuitry of 2ED21091S06F is matched with respect to the high- and low-side outputs. Figure 8 defines the two deadtime parameters (i.e., DT_{LO-HO} and DT_{HO-LO}); the deadtime matching parameter (MDT) associated with the 2ED21091S06F specifies the maximum difference between DT_{LO-HO} and DT_{HO-LO}.

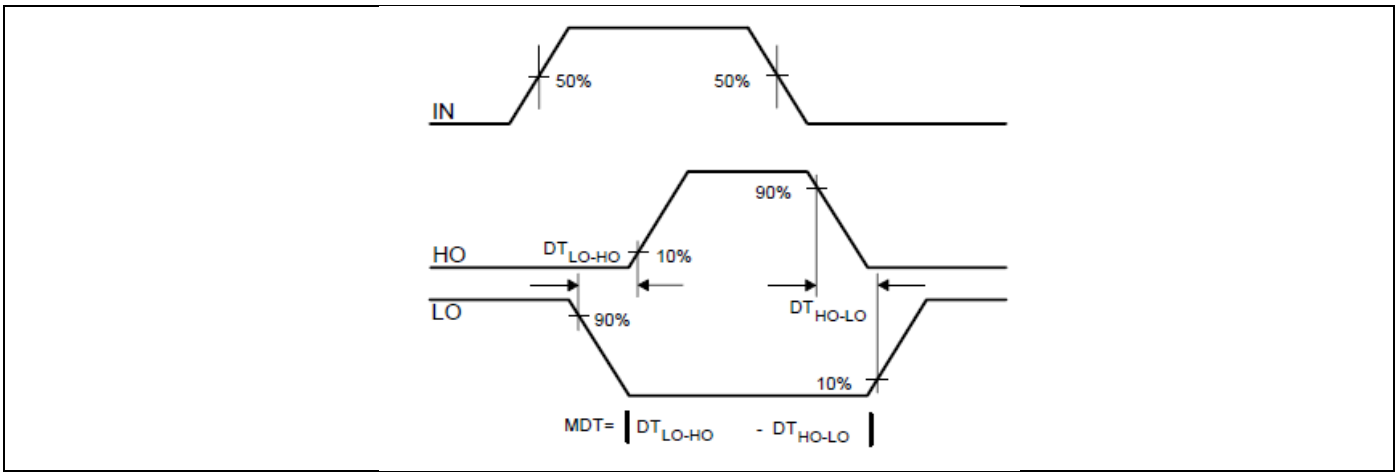


Figure 8 Deadtime matching waveform definition

5.4 Matched propagation delays

The 2ED21091S06F is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the 2ED21091S06F is matched to the propagation turn-off delay (t_{OFF}).

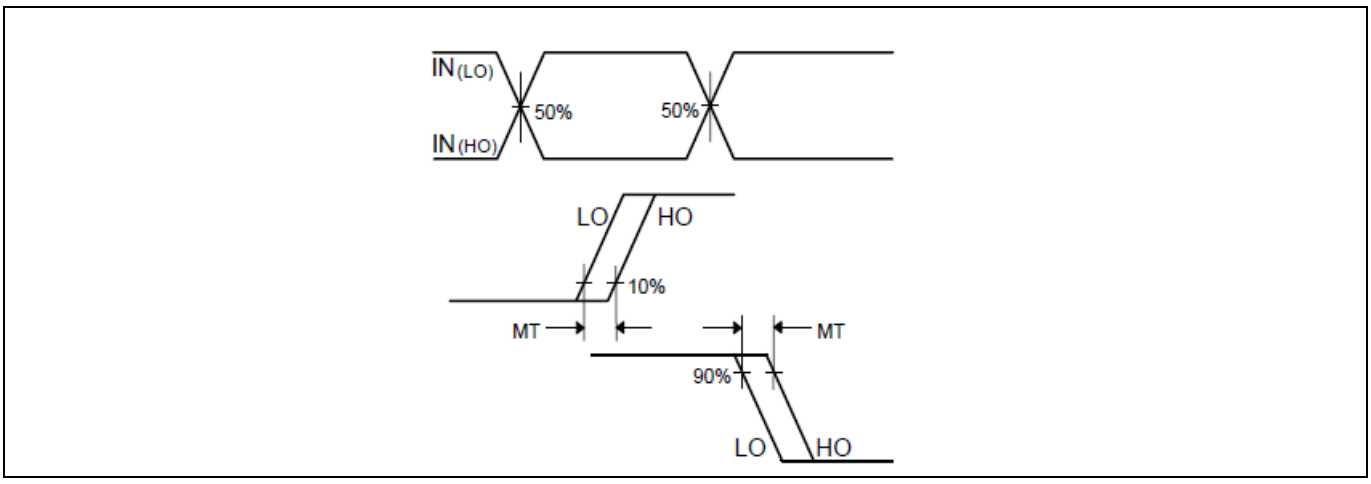


Figure 9 Delay matching waveform definition

5.5 Shutdown input

2ED21091S06F provides a shutdown functionality that allows to disable the output. When /SD in pulled down (the disable voltage is lower than $V_{SD,TH}$) the output is disable. Once the external pull down is released, the output is active. The relationships between the input, output and enable signals of the 2ED21091S06F are illustrated below in Figure 7 / 10. From these figures, we can see the definition of the parameter (i.e. t_{SD}) associated with this device.
Note: If the DT/SD is floating, the output is aslo disable.

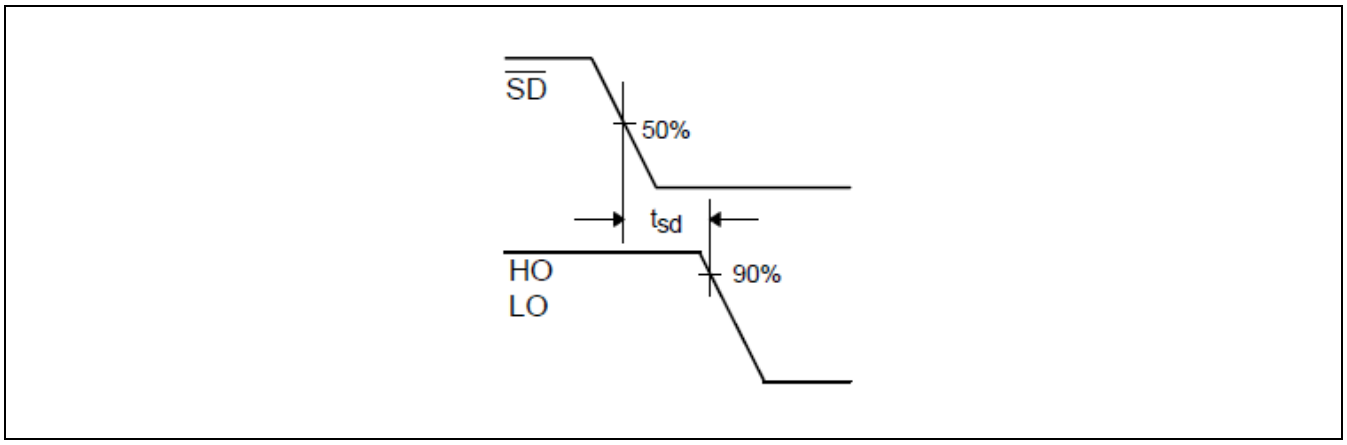


Figure 10 Shutdown waveform definitions

5.6 Input logic compatibility

The input pins are based on a TTL and CMOS compatible input-threshold logic that is independent of the Vcc supply voltage. Figure 11 illustrates an input signal to the 2ED21091S06F, its input threshold values, and the logic state of the IC as a result of the input signal. The typical high threshold (V_{IH}) of 2.1 V and typical low threshold (V_{IL}) of 0.9 V. The input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 0.9 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 2ED21091S06F also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 2ED21091S06F has input pins that are capable of sustaining voltages higher than the bias voltage applied on the Vcc pin of the device.

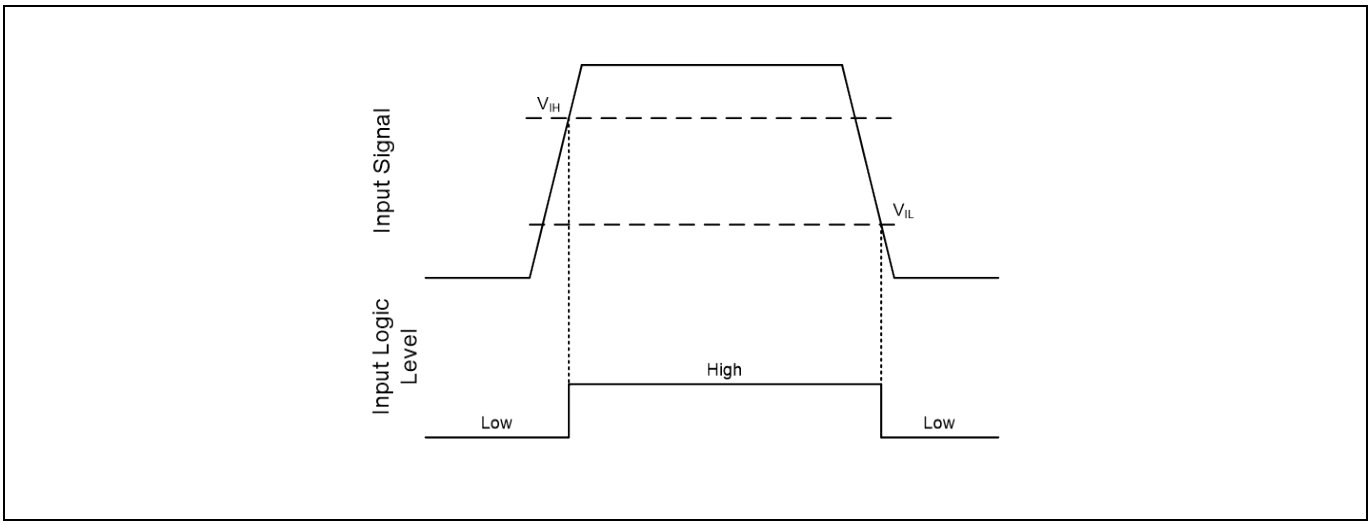


Figure 11 IN input thresholds

5.7 Undervoltage lockout

This IC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 12 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC won't turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV+} threshold, the IC won't turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

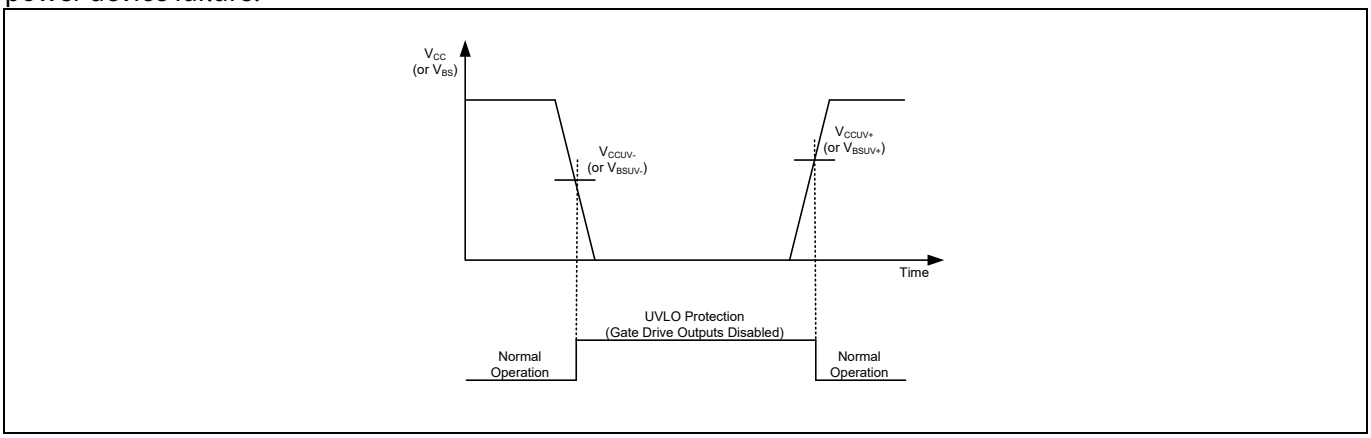


Figure 12 UVLO protection

5.8 Bootstrap diode

An ultra-fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The integrated diode with its resistrance helps save cost and improve reliability by reducing external components as shown below Figure 13 and Figure 14.

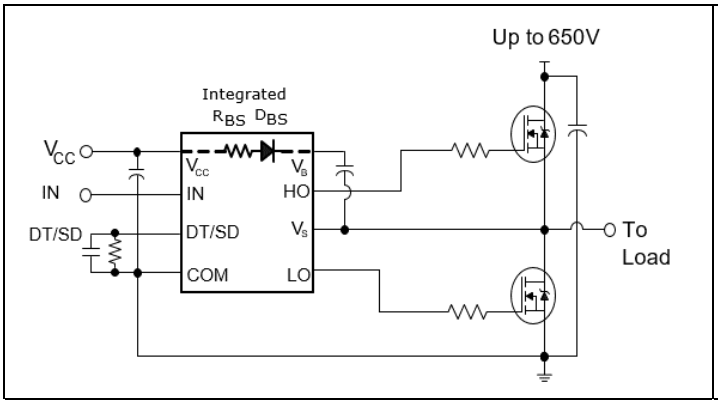


Figure 13 2ED210x with integrated components

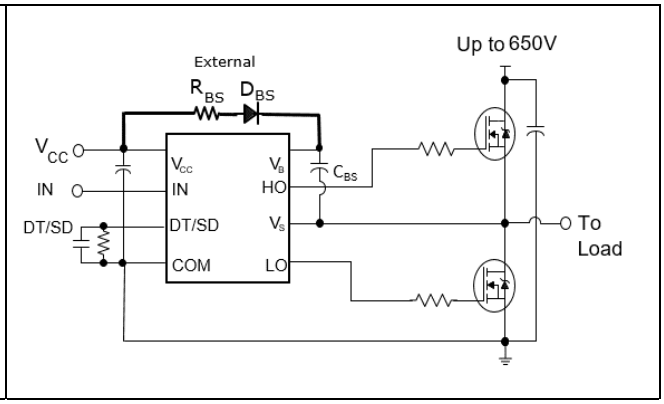


Figure 14 Standard bootstrap gate driver

The low ohmic current limiting resistor provides essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 2ED210x family allows faster recharging of the bootstrap capacitor during periods of small duty cycles on the low side transistor. The bootstrap diode is a real pn-diode which works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal motor drives control.

5.9 Calculating the bootstrap capacitance C_{BS}

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to Figure 15. This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.

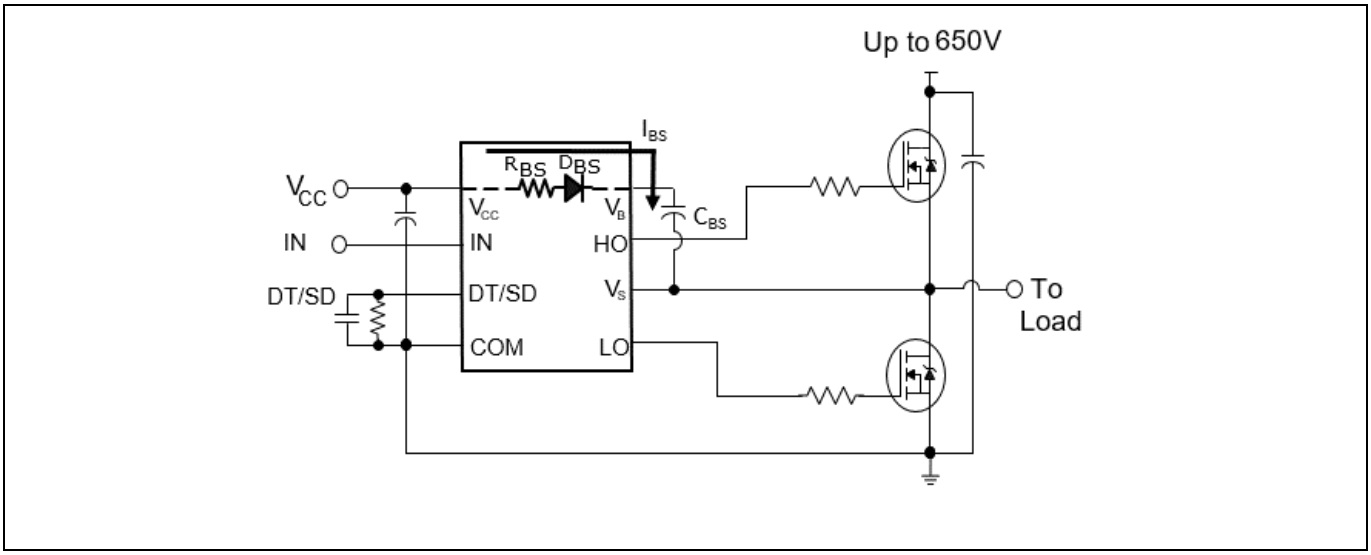


Figure 15 Half bridge bootstrap circuit in 2ED210x

When the low side MOSFET turns on, it will force the potential of pin V_S to GND. The existing difference between the voltage of the bootstrap capacitor V_{CBS} and V_{CC} results in a charging current I_{BS} into the capacitor C_{BS}. The current I_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor. This pin is on high potential again after low side is turned off and high side is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VCC}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin V_B and V_{CC}. The voltage of the bootstrap capacitor can now supply the high side gate drive sections. It is a general design rule for the location of bootstrap capacitors C_{BS}, that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual high side driver section. However, all parts of the 2ED210x family, which have the UVLO also contain a filter at each supply section in order to actively avoid such undesired UVLO triggers.

The current limiting resistor R_{BS} according to Figure 15 reduces the peak of the pulse current during the low side MOSFET turn-on. The pulse current will occur at each turn-on of the low side MOSFET, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: The high side quiescent current and the gate charge of the high side MOSFET to be turned on.

The minimum size of the bootstrap capacitor is given by

$$C_{BS} = \frac{Q_{GTOT}}{\Delta V_{BS}}$$

ΔV_{BS} is the maximum allowable voltage drop at the bootstrap capacitor within a switching period, typically 1 V. It is recommended to keep the voltage drop below the undervoltage lockout (UVLO) of the high side and limit

$$\Delta V_{BS} \leq (V_{CC} - V_F - V_{GSmin} - V_{DSon})$$

$V_{GSmin} > V_{BSUV-}$, V_{GSmin} is the minimum gate source voltage we want to maintain and V_{BSUV-} is the high-side supply undervoltage negative threshold.

V_{CC} is the IC voltage supply, V_F is bootstrapdiode forward voltage and V_{DSon} is drain-source voltage of low side MOSFET.

Please note, that the value Q_{GTOT} may vary to a maximum value based on different factors as explained below and the capacitor shows voltage dependent derating behavior of its capacitance.

The influencing factors contributing V_{BS} to decrease are:

- MOSFET turn on required Gate charge (Q_G)
- MOSFET gate-source leakage current (I_{LK_GS})
- Floating section quiescent current (I_{QBS})
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE})
- Charge required by the internal level shifters (Q_{LS}): typical 1nC
- Bootstrap capacitor leakage current (I_{LK_CAP})
- High side on time (T_{HON})

Considering the above,

$$Q_{GTOT} = Q_G + Q_{LS} + \left(I_{QBS} + I_{LK_{GS}} + I_{LK} + I_{LK_{DIODE}} + I_{LK_{CAP}}\right) * T_{HON}$$

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic capacitor and low ESR ceramic capacitor may result in an efficient solution).

The above C_{BS} equation is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of low side. The recommended bootstrap capacitance is therefore in the range up to 4.7 µF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances.

5.10 Tolerant to negative tranisents on input pins

Typically the driver's ground pin is connected close to the source pin of the MOSFET or IGBT. The microcontroller which sends the IN PWM signal refers to the same ground and in most cases there will be an offset voltage between the microcontroller ground pin and driver ground because of ground bounce. The 2ED210x family can handle negative voltage spikes up to 5 V. The recommended operating level is at negative 4 V with absolute maximum of negative 5 V. Standard half bridge or high-side/low-side gate drivers only allow negative voltage levels down to -0.3 V. The 2ED210x family has much better noise immunity capability on the input pins.

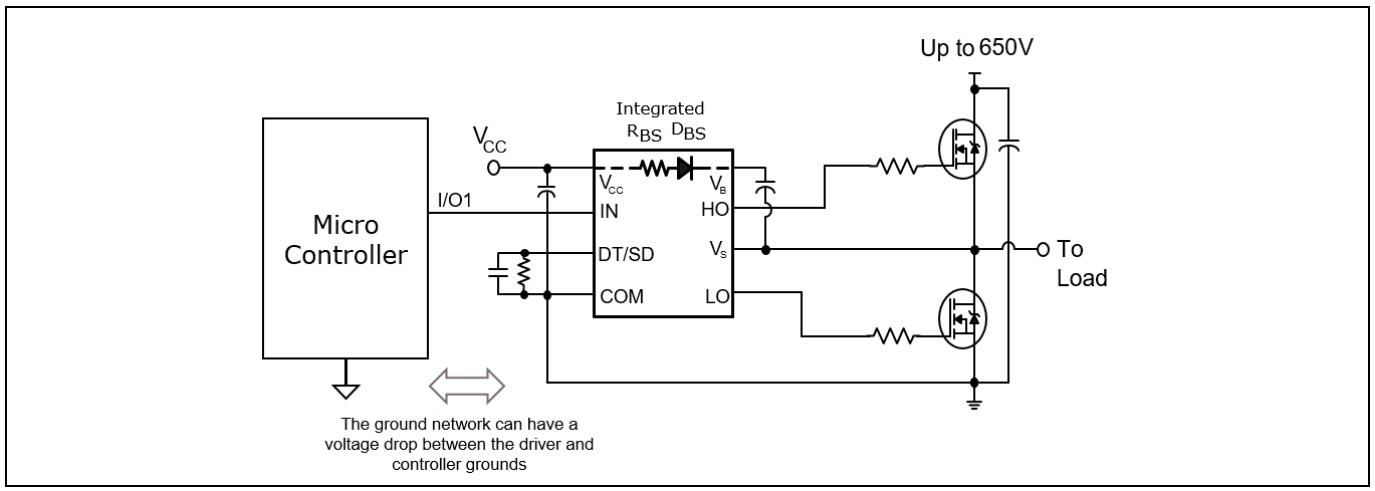


Figure 16 Negative voltage tolerance on inputs of upto –5 V

5.11 Negative voltage transient tolerance of VS pin

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 17, here we define the power switches and diodes of the inverter.
If the high-side switch (e.g., the IGBT Q1 in Figure 18) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

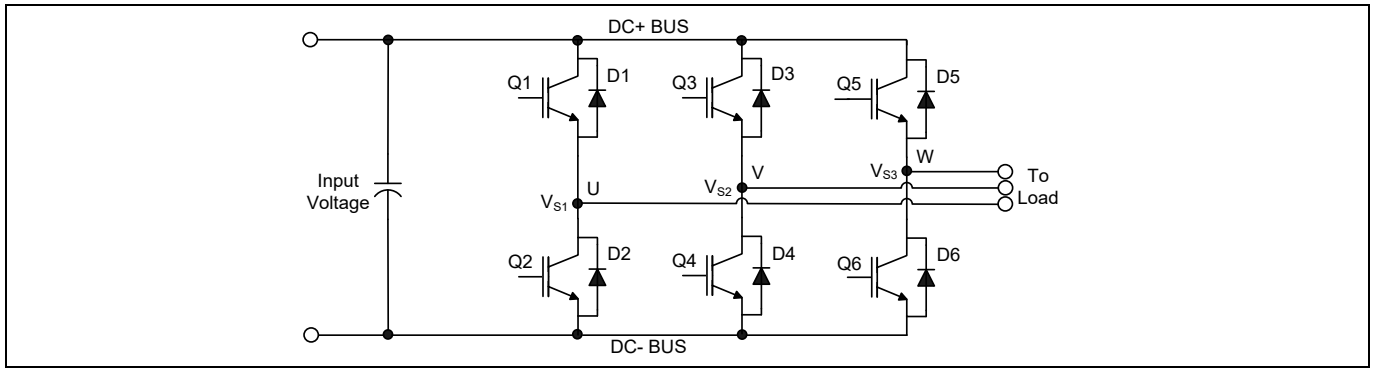


Figure 17 Three phase inverter

Also when the V phase current flows from the inductive load back to the inverter (see Figure 18 C) and D)), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient"

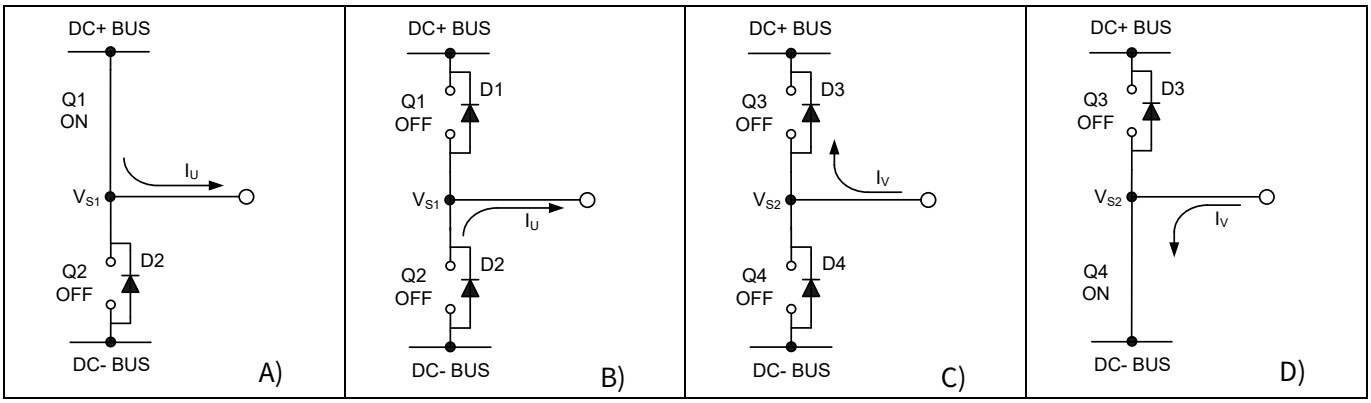


Figure 18 A) Q1 conducting B) D2 conducting C) D3 conducting D) Q4 conducting

The circuit shown in Figure 19-A depicts one leg of the three phase inverter; Figure 19-B and 19-C show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- BUS (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- BUS is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

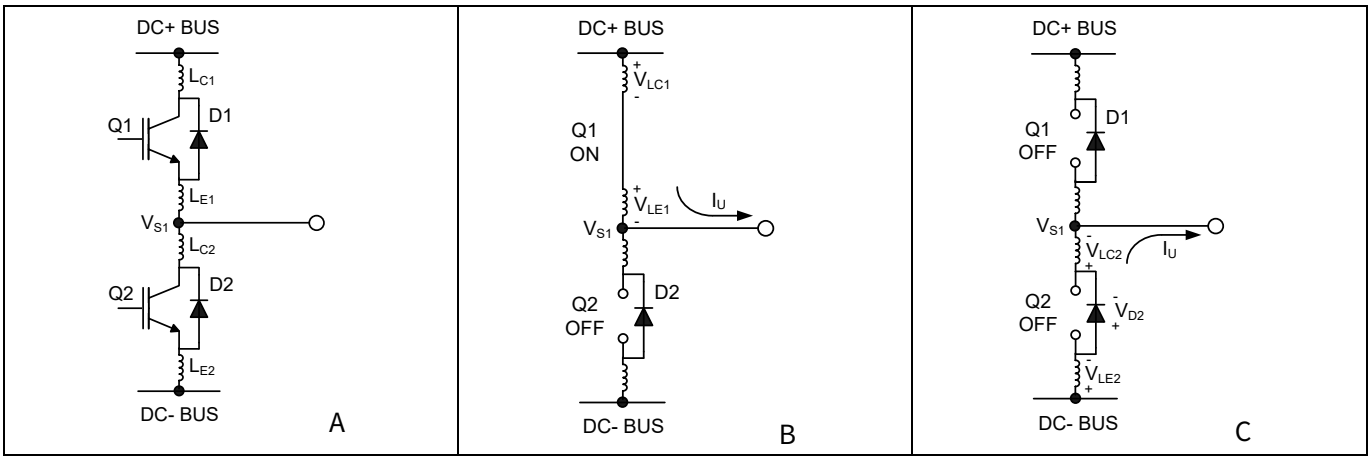


Figure 19 Figure A shows the parasitic elements. Figure B shows the generation of VS positive. Figure C shows the generation of VS negative

5.12 NTSOA – Negative Transient Safe Operating Area

In a typical motor drive system, dV/dt is typically designed to be in the range of 3 – 5 V / ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 2ED21091S06F's robustness can be seen in Figure 20, where the 2ED21091S06F's Safe Operating Area is shown at V_{BS}=15 V based on repetitive negative VS spikes. A negative VS transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

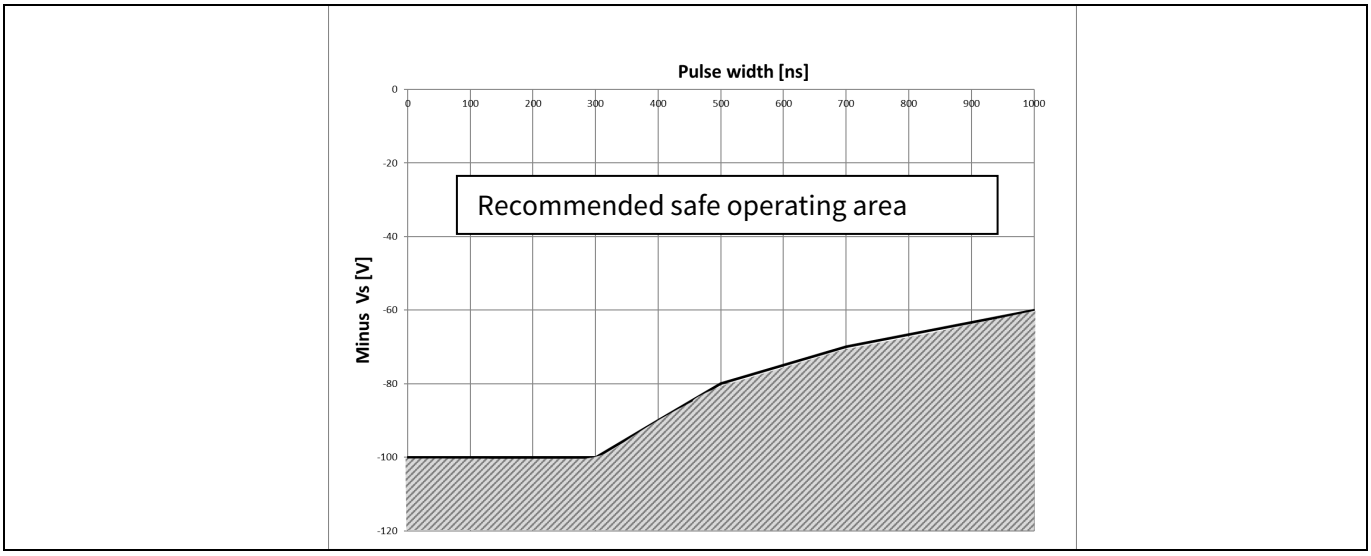


Figure 20 Negative VS transient SOA for 2ED21091S06F @ VBS=15 V

Even though the 2ED21091S06F has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative VS transients as much as possible by careful PCB layout and component use.

5.13 Higher headroom for input to output signal transmission with logic operation upto -11 V

If there is not enough voltage for the level shifter to transmit a valid signal to the high side. High side driver doesn't turn on. The level shifter circuit is with respect to COM (refer to Block Diagram on page 4), the voltage from V_B to COM is the supply voltage of level shifter. Under the condition of VS is negative voltage with respect to COM, the voltage of VS - COM is decreased, as shown in Figure 21. There is a minimum operational supply voltage of level shifter, if the supply voltage of level shifter is too low, the level shifter cannot pass through IN signal to HO. The specification of VS is –11 V as the internal structure allows a voltage difference of 15 V between Vcc and COM pins. If $V_B - V_S$ voltage is different, the minimum VS voltage changes accordingly.

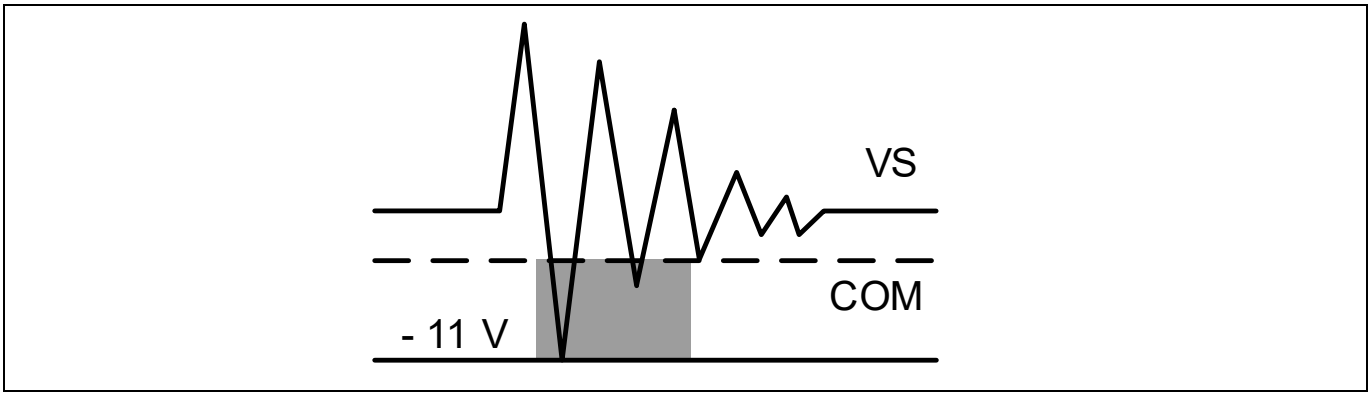


Figure 21 Headroom for HV level shifter data transmission

5.14 Maximum switching frequency

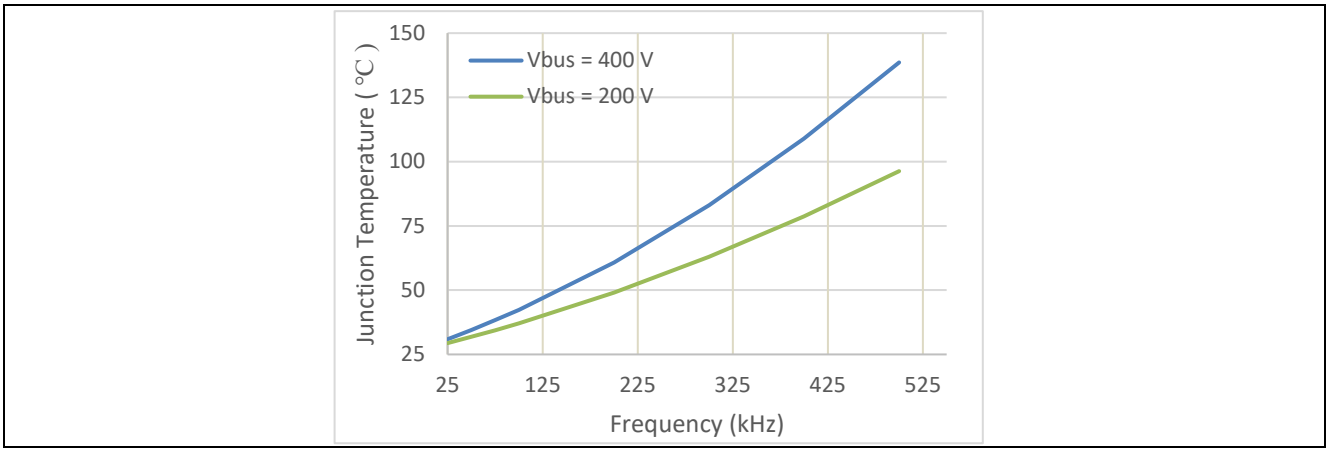
The 2ED21091S06F is capable of switching at higher frequencies as compared to standard half-bridge or high side / low side gate drivers. It is essential to ensure that the component is not thermally overloaded when operating at higher frequencies. This can be checked by means of the thermal resistance junction to ambient and the calculation or measurement of the dissipated power. The thermal resistance is given in the datasheet (section 4) and refers to a specific layout. Changes of this layout may lead to an increased thermal resistance, which will reduce the total dissipated power of the driver IC. One should therefore do temperature measurements in order to avoid thermal overload under application relevant conditions of ambient temperature and housing.

The maximum chip temperature T_J can be calculated with

$$T_J = \mathrm{Pd} \cdot Rth_{JA} + T_{A\_max}$$, where T_{A_max} is the maximum ambient temperature.

The dissipated power Pd by the driver IC is a combination of several sources. These are explained in detail in the application note “Advantages of Infineon’s Silicon on Insulator (SOI) technology based High Voltage Gate Driver ICs (HVICs)”

Here is the example of the figures which estimates the gate driver IC junction temperature when switching a given MOSFET at different switching frequencies.



*Assumptions for above curves: LLC topology, Power switch = IPP60R600P6, T_a = 25 °C, V_{BUS} = 400 V, V_{CC} = 12 V, R_{gon} = 3.9 Ω, R_{goff} = 1 Ω

Figure 22 Estimated T_J vs. Frequencies

5.15 PCB layout tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coulping, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 23). In order to reduce the EM coulping and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

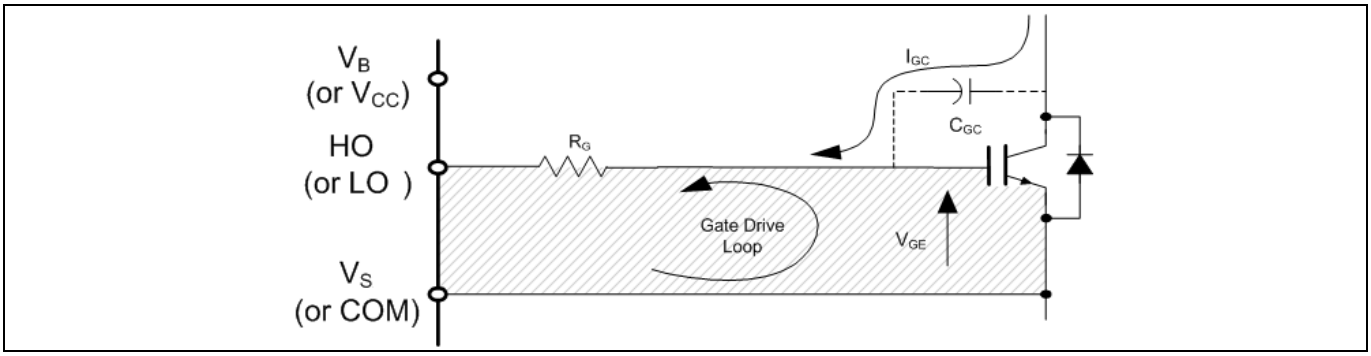


Figure 23 Avoid antenna loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative VS spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the VS pin and the switch node (see Figure 24 - A), and in some cases using a clamping diode between COM and V_S (see Figure 24 - B). See DT04-4 at www.infineon.com for more detailed explanations.

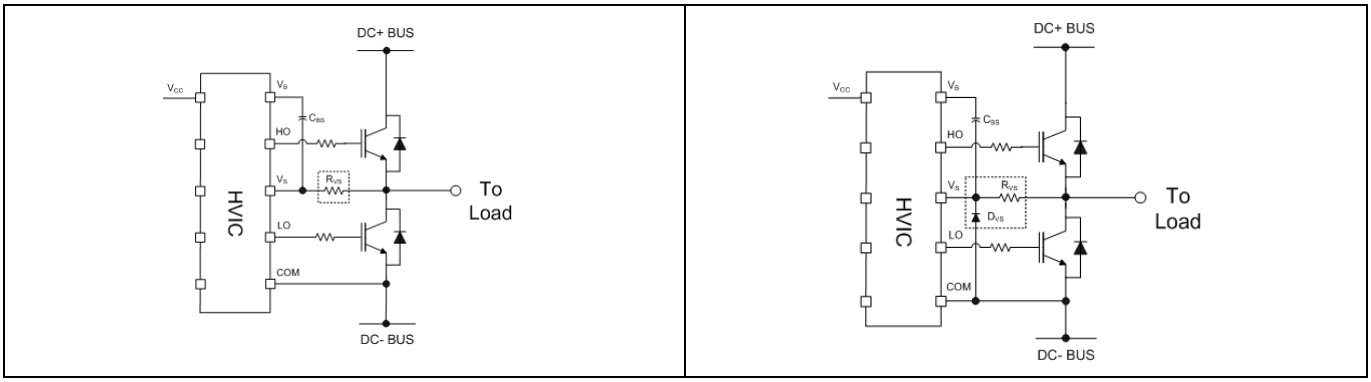


Figure 24 Resistor between the VS pin and the switch node and clamping diode between COM and VS

6 Qualification information[1]

Table 7 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		DSO-8	MSL3[3], 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (1.0 kV) (per JEDEC standard JS-002)	
	Human body model	Class 2 (1.5 kV) (per JEDEC standard JS-001)	
IC latch-up test		Class II Level A (per JESD85)	
RoHS compliant		Yes	

7 Related products

Table 8

Product	Description
Gate Driver ICs	
6EDL04I06 / 6EDL04N06	600 V, 3 phase level shift thin-film SOI gate driver with integrated high speed, low R_{BSD} bootstrap diodes with over-current protection (OCP), 240/420 mA source/sink current drive, Fault reporting, and Enable for MOSFET or IGBT switches.
2EDL23I06 / 2EDL23N06	600 V, Half-bridge thin-film SOI level shift gate driver with integrated high speed, low R_{BSD} bootstrap diode, with over-current protection (OCP), 2.3/2.8 A source/sink current driver, and one pin Enable/Fault function for MOSFET or IGBT switches.
Power Switches	
IKD04N60R / RF	600 V TRENCHSTOP™ IGBT with integrated diode in PG-TO252-3 package
IKD06N65ET6	650 V TRENCHSTOP™ IGBT with integrated diode in DPAK
IPD65R950CFD	650 V CoolMOS CFD2 with integrated fast body diode in DPAK
IPN50R950CE	500 V CoolMOS CE Superjunction MOSFET in PG-SOT223 package
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
[3] Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

8 Package details

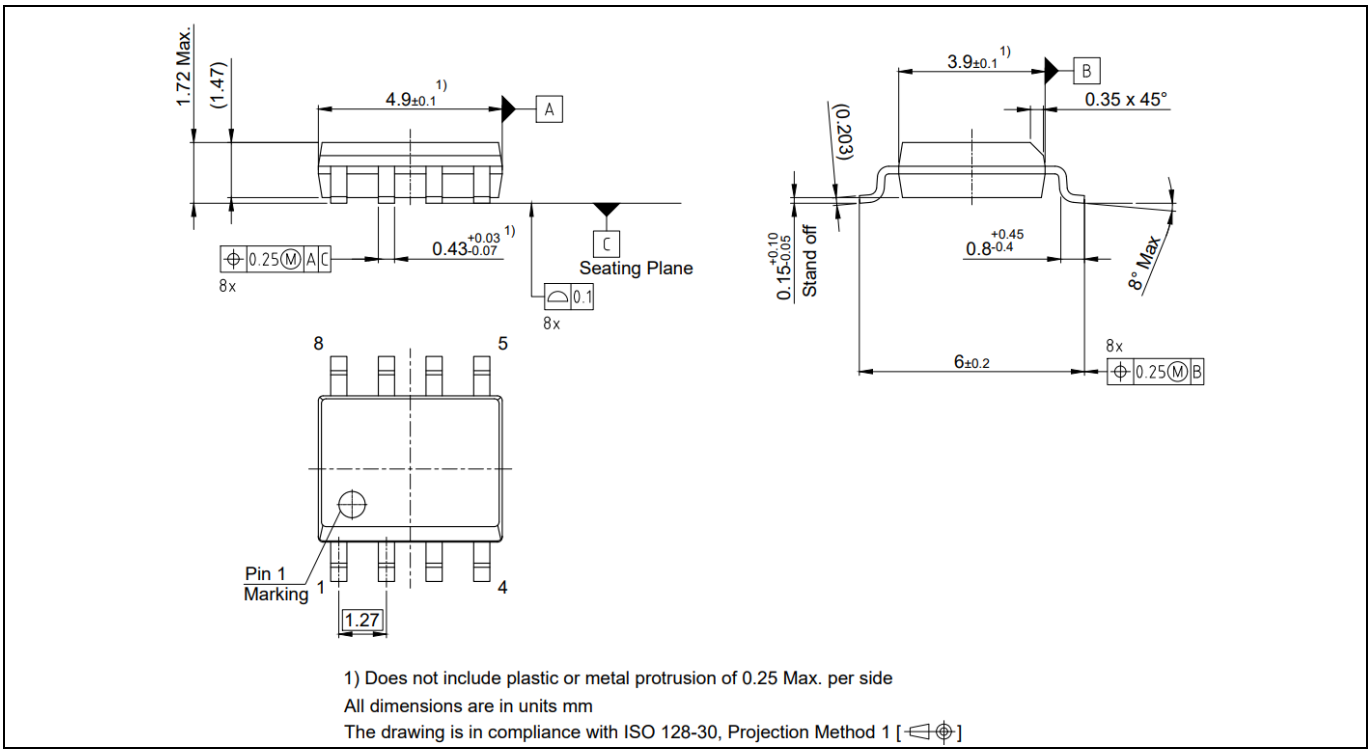


Figure 25 8 - Lead DSO

9 Part marking information

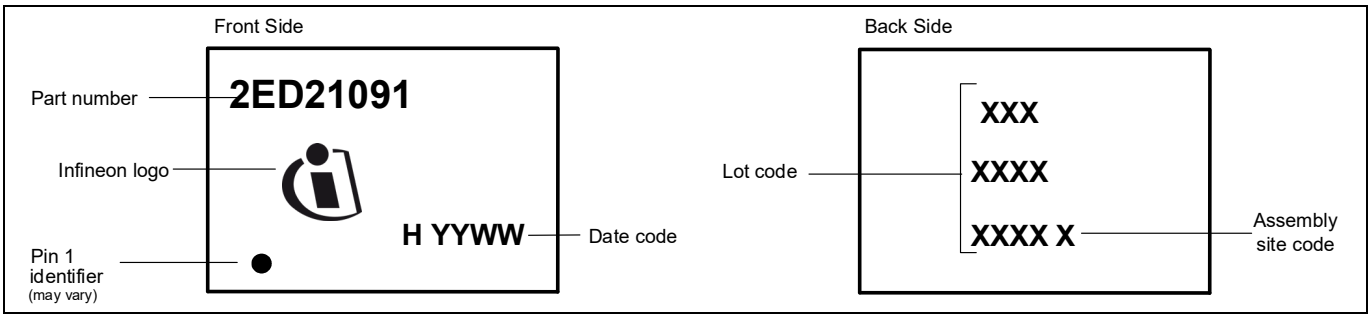


Figure 26 Marking information PG-DSO-8

10 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

10.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

11 Revision history

Document version	Date of release	Description of changes
2.00	Aug 12, 2019	Final Datasheet
2.10	Sep. 12, 2019	Revised parameter values in Table 6, 7 to match the test conditions.

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