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*M68HC08*  
*Microcontrollers*

MC68HC908QY4  
MC68HC908QT4  
MC68HC908QY2  
MC68HC908QT2  
MC68HC908QY1  
MC68HC908QT1

*Advance Information*

MC68HC908QY4/D  
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**MC68HC908QY4**  
**MC68HC908QT4**  
**MC68HC908QY2**  
**MC68HC908QT2**  
**MC68HC908QY1**  
**MC68HC908QT1**  
**Advance Information**

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

## Revision History

### Revision History

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## Section 1. General Description

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### 1.2 Introduction

The MC68HC908QY4 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is a Complex Instruction Set Computer (CISC) with a Von Neumann architecture. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

**Table 1-1. Summary of Device Variations**

Device	FLASH Memory Size	Analog-to-Digital Converter	Pin Count
MC68HC908QT1	1536 bytes	—	8 pins
MC68HC908QT2	1536 bytes	4 ch, 8 bit	8 pins
MC68HC908QT4	4096 bytes	4 ch, 8 bit	8 pins
MC68HC908QY1	1536 bytes	—	16 pins
MC68HC908QY2	1536 bytes	4 ch, 8 bit	16 pins
MC68HC908QY4	4096 bytes	4 ch, 8 bit	16 pins

## 1.3 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- 5-V and 3-V operating voltages ( $V_{DD}$ )
- 8-MHz internal bus operation at 5 V, 4-MHz at 3 V
- Trimmable internal oscillator
  - 3.2 MHz internal bus operation
  - 8-bit trim capability
  - $\pm 25\%$  untrimmed
  - $\pm 5\%$  trimmed
- Auto wake-up from STOP capability
- Configuration (CONFIG) register for MCU configuration options, including:
  - Low-voltage inhibit (LVI) trip point
- In-system FLASH programming
- FLASH security<sup>(1)</sup>
- On-chip in-application programmable FLASH memory (with internal program/erase voltage generation)
  - MC68HC908QY4 and MC68HC908QT4 — 4096 bytes
  - MC68HC908QY2, MC68HC908QY1, MC68HC908QT2, and MC68HC908QT1 — 1536 bytes
- 128 bytes of on-chip random-access memory (RAM)
- 2-channel, 16-bit timer interface module (TIM)
- 4-channel, 8-bit analog-to-digital converter (ADC) on MC68HC908QY2, MC68HC908QY4, MC68HC908QT2, and MC68HC908QT4

---

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

- 5 or 13 bidirectional input/output (I/O) lines and one input only:
  - Six shared with keyboard interrupt function and ADC
  - Two shared with timer channels
  - One shared with external interrupt (IRQ)
  - Eight extra I/O lines on 16-pin package only
  - High current sink/source capability on all port pins
  - Selectable pullups on all ports, selectable on an individual bit basis
  - Three-state ability on all port pins
- 6-bit keyboard interrupt with wakeup feature (KBI)
- Low-voltage inhibit (LVI) module features:
  - Software selectable trip point in CONFIG register
- System protection features:
  - Computer operating properly (COP) watchdog
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- External asynchronous interrupt pin with internal pullup ( $\overline{\text{IRQ}}$ ) shared with general-purpose input pin
- Master asynchronous reset pin ( $\overline{\text{RST}}$ ) shared with general-purpose input pin
- Power-on reset
- Internal pullups on  $\overline{\text{IRQ}}$  and  $\overline{\text{RST}}$  to reduce external components
- Memory mapped I/O registers
- Power saving stop and wait modes
- MC68HC908QY4, MC68HC908QY2, and MC68HC908QY1 are available in these packages:
  - 16-pin plastic dual in-line package (PDIP)
  - 16-pin small outline integrated circuit (SOIC) package
  - 16-pin thin shrink small outline package (TSSOP)

- MC68HC908QT4, MC68HC908QT2, and MC68HC908QT1 are available in these packages:
  - 8-pin PDIP
  - 8-pin SOIC

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast  $8 \times 8$  multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

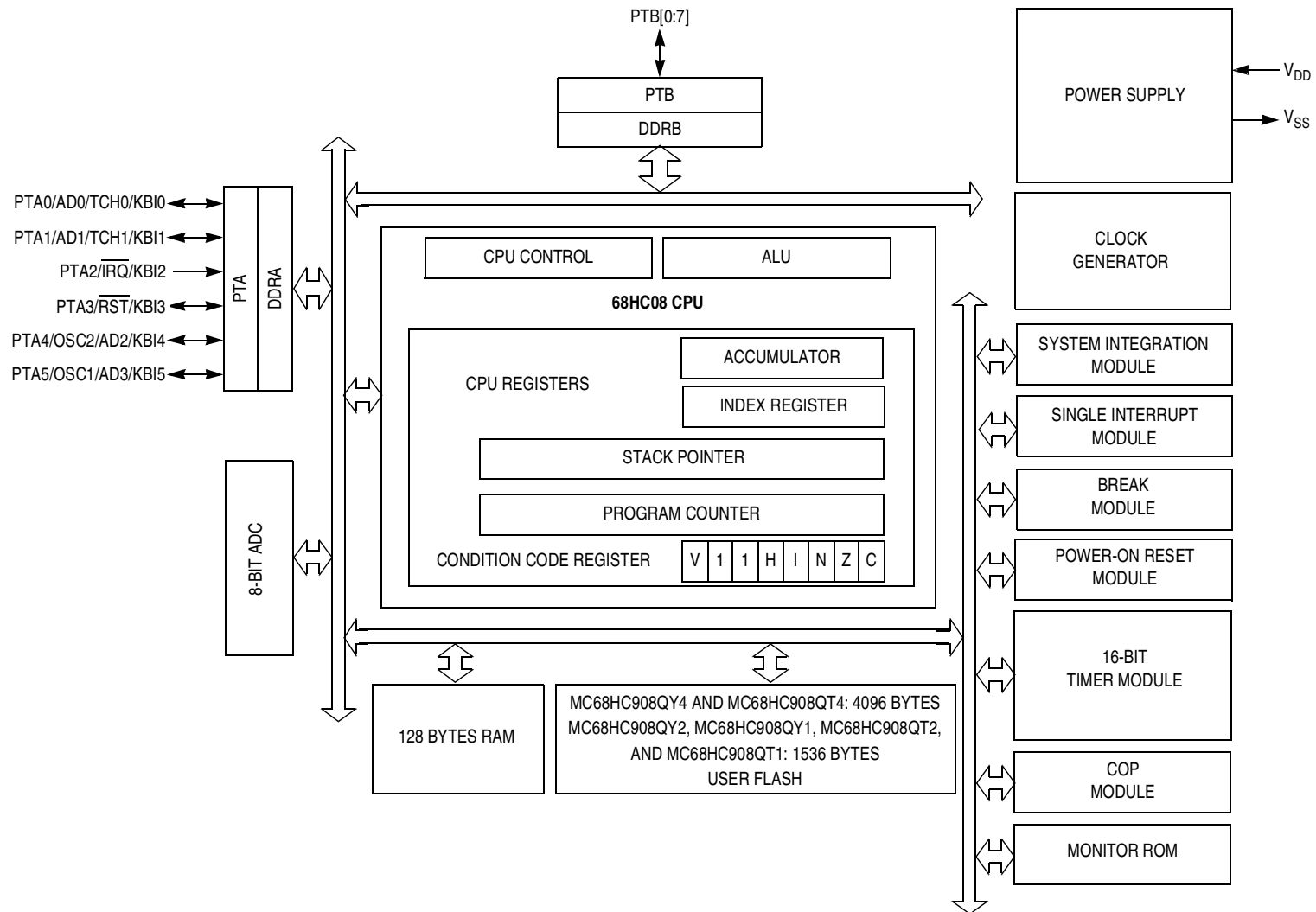
### 1.4 MCU Block Diagram

**Figure 1-1** shows the structure of the MC68HC908QY4.

### 1.5 Pin Assignments

The MC68HC908QT4, MC68HC908QT2, and MC68HC908QT1 are available in 8-pin packages and the MC68HC908QY4, MC68HC908QY2, and MC68HC908QY1 in 16-pin packages.

**Figure 1-2** shows the pin assignment for these packages.

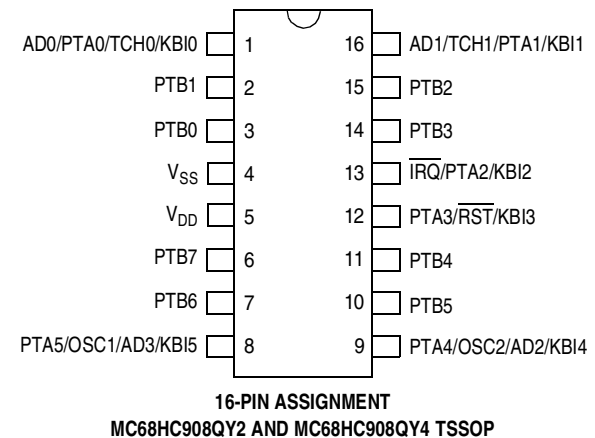
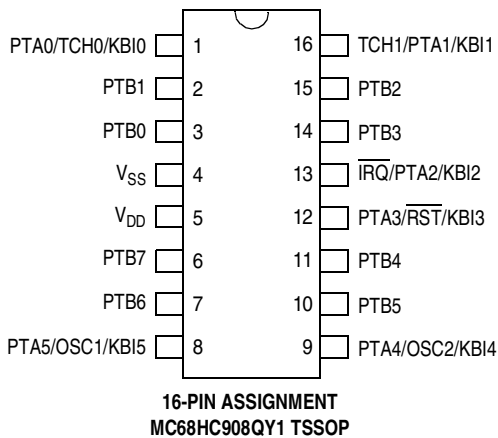
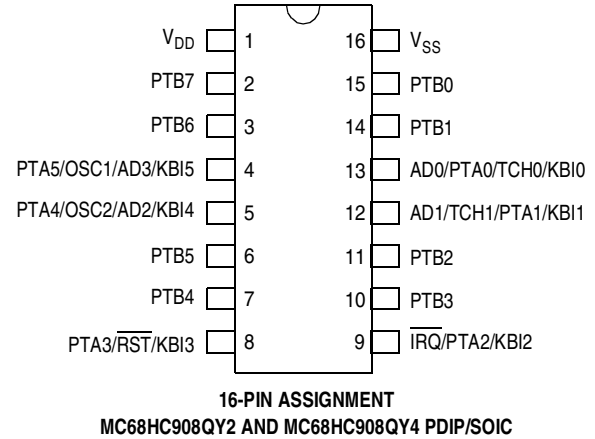
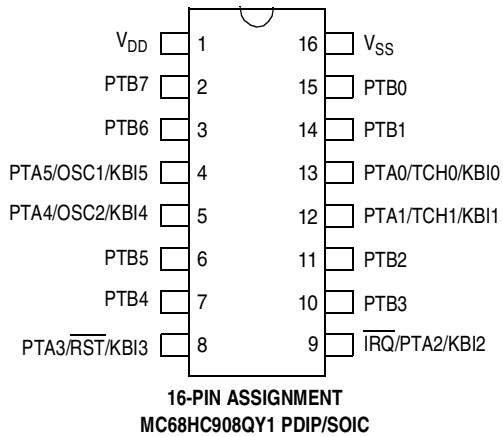
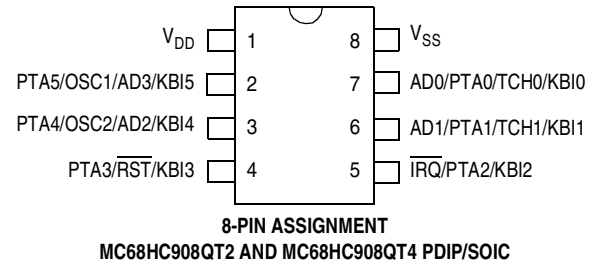
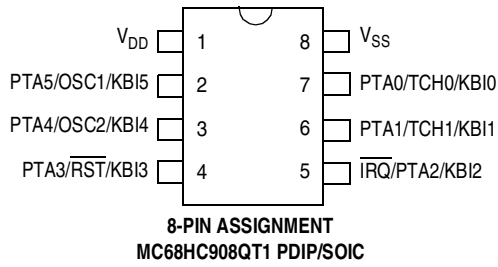


$\overline{RST}$ ,  $\overline{IRQ}$ : Pins have internal 30K pull up  
 PTA[0:5]: High current sink source capability  
 PTA[0:5]: Pins have programmable keyboard interrupt and pull up  
 PTB[0:7]: Not available on 8-pin devices – MC68HC908QT1, MC68HC908QT2, and MC68HC908QT4

Figure 1-1. Block Diagram

MC68HC908QY4 • MC68HC908QT4 • MC68HC908QY2 • MC68HC908QT2 • MC68HC908QY1 • MC68HC908QT1

# General Description



**Figure 1-2. MCU Pin Assignments**

## 1.6 Pin Functions

**Table 1-2** provides a description of the pin functions.

**Table 1-2. Pin Functions**

Pin Name	Description	Input/Output	Voltage Level
$V_{DD}$	Power supply	Power	5 V or 3 V
$V_{SS}$	Power supply ground	Power	0 V
$\overline{RST}$	Reset input, active high with Internal pullup and schmitt trigger input	Input	$V_{DD}$
$\overline{IRQ}$	External IRQ pin with software programmable internal pullup and schmitt trigger input. This pin is also used for mode entry selection.	Input	$V_{DD}$ to $V_{DD} + V_{HI}$
OSC1	XTAL, RC oscillator, or external oscillator input.	Input	Analog
	Internal oscillator — shared with PTA5/AD3/KBI5	Input/Output	Digital/Analog
OSC2	For XTAL oscillator option: XTAL oscillator output, this is the inverting OSC1 signal	Output	Analog
	<b>For other oscillator option:</b> OSC2 disabled — PTA4/AD2/KBI4, with programmable pullup OSC2 enabled — RC or internal oscillator output signal	Input/Output	$V_{DD}$
PTA[0:5]	5 general-purpose I/O ports and 1 input only	Input/Output	$V_{DD}$
	Shared with 6 keyboard interrupts KBI[0:5]	Input	$V_{DD}$
	Each pin has programmable internal pullup device	Input	$V_{DD}$
PTB[0:7] <sup>(1)</sup>	8 general-purpose I/O ports.	Input/Output	$V_{DD}$

1. The PTB pins are not available on the 8-pin packages.

## 1.7 Pin Function Priority

**Table 1-3** is meant to resolve the priority if multiple functions are enabled on a single pin.

**NOTE:** Upon reset all pins come up as input ports regardless of the priority table.

**Table 1-3. Function Priority in Shared Pins**

Pin Name	Highest-to-Lowest Priority Sequence
PTA[0]	AD0 → TCH0 → KBI[0] → PTA[0]
PTA[1]	AD1 → TCH1 → KBI[1] → PTA[1]
PTA[2]	$\overline{\text{IRQ}}$ → KBI[2] → PTA[2]
PTA[3]	$\overline{\text{RST}}$ → KBI[3] → PTA[3]
PTA[4]	OSC2 → AD2 → KBI[4] → PTA[4]
PTA[5]	OSC1 → AD3 → KBI[5] → PTA[5]



## Section 2. Memory

### 2.1 Contents

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2.4	Reserved Memory Locations . . . . .	35
2.5	Input/Output (I/O) Section. . . . .	35

### 2.2 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in [Figure 2-1](#), includes:

- 4096 bytes of user FLASH for MC68HC908QT4 and MC68HC908QY4
- 1536 bytes of user FLASH for MC68HC908QT2, MC68HC908QT1, MC68HC908QY2, and MC68HC908QY1
- 128 bytes of random access memory (RAM)
- 48 bytes of user-defined vectors, located in FLASH
- 416 bytes of monitor read-only memory (ROM)
- 1536 bytes of FLASH program and erase routines, located in ROM

### 2.3 Unimplemented Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In [Figure 2-1](#) and in register figures in this document, unimplemented locations are shaded.

# Memory

\$0000 ↓ \$003F	I/O REGISTERS 64 BYTES
\$0040 ↓ \$007F	RESERVED 64 BYTES
\$0080 ↓ \$00FF	RAM 128 BYTES
\$0100 ↓ \$27FF	UNIMPLEMENTED 9984 BYTES
\$2800 ↓ \$2DFF	AUXILIARY ROM 1536 BYTES
\$2E00 ↓ \$EDFF	UNIMPLEMENTED 49152 BYTES
\$EE00 ↓ \$FDFE	FLASH MEMORY MC68HC908QT4 AND MC68HC908QY4 4096 BYTES
\$FE00	BREAK STATUS REGISTER (BSR)
\$FE01	RESET STATUS REGISTER (SRSR)
\$FE02	BREAK AUXILIARY REGISTER (BRKAR)
\$FE03	BREAK FLAG CONTROL REGISTER (BFCR)
\$FE04	INTERRUPT STATUS REGISTER 1 (INT1)
\$FE05	INTERRUPT STATUS REGISTER 2 (INT2)
\$FE06	INTERRUPT STATUS REGISTER 3 (INT3)
\$FE07	RESERVED FOR FLASH TEST CONTROL REGISTER (FLTCR)
\$FE08	FLASH CONTROL REGISTER (FLCR)
\$FE09	BREAK ADDRESS HIGH REGISTER (BRKH)
\$FE0A	BREAK ADDRESS LOW REGISTER (BRKL)
\$FE0B	BREAK STATUS AND CONTROL REGISTER (BRKSCR)
\$FE0C	LVISR
\$FE0D ↓ \$FE0F	RESERVED FOR FLASH TEST 3 BYTES
\$FE10 ↓ \$FFAF	MONITOR ROM 416 BYTES
\$FFB0 ↓ \$FFBD	UNIMPLEMENTED 14 BYTES
\$FFBE	FLASH BLOCK PROTECT REGISTER (FLBPR)
\$FFBF	UNIMPLEMENTED
\$FFC0	INTERNAL OSCILLATOR TRIM VALUE
\$FFC1	RESERVED
\$FFC2 ↓ \$FFCF	UNIMPLEMENTED 14 BYTES
\$FFD0 ↓ \$FFFF	USER VECTORS 48 BYTES

UNIMPLEMENTED 9984 BYTES	\$0100 ↓ \$27FF
AUXILIARY ROM MC68HC908QT1 AND MC68HC908QY1 1536 BYTES	\$2800 ↓ \$2DFF
UNIMPLEMENTED 51712 BYTES	\$2E00 ↓ \$F7FF
FLASH MEMORY MC68HC908QT1 AND MC68HC908QY1 1536 BYTES	\$F800 ↓ \$FDFE

**MC68HC908QT1, MC68HC908QT2,  
MC68HC908QY1, and MC68HC908QY2  
Memory Map**

**Figure 2-1. Memory Map**

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## 2.4 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In [Figure 2-1](#) and in register figures in this document, reserved locations are marked with the word Reserved or with the letter R.

## 2.5 Input/Output (I/O) Section

Addresses \$0000–\$003F, shown in [Figure 2-2](#), contain most of the control, status, and data registers. Additional I/O registers have these addresses:

- \$FE00 — Break status register, BSR
- \$FE01 — Reset status register, SRSR
- \$FE02 — Break auxiliary register, BRKAR
- \$FE03 — Break flag control register, BFCR
- \$FE04 — Interrupt status register 1, INT1
- \$FE05 — Interrupt status register 2, INT2
- \$FE06 — Interrupt status register 3, INT3
- \$FE07 — Reserved
- \$FE08 — FLASH control register, FLCR
- \$FE09 — Break address register high, BRKH
- \$FE0A — Break address register low, BRKL
- \$FE0B — Break status and control register, BRKSCR
- \$FE0C — LVI status register, LVISR
- \$FE0D — Reserved
- \$FFBE — FLASH block protect register, FLBPR
- \$FFC0 — Internal OSC trim value — Optional
- \$FFFF — COP control register, COPCTL

# Memory

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$0000	Port A Data Register (PTA) <a href="#">See page 165.</a>	Read:	0	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	U	0	U	U	U	U	U	U
\$0001	Port B Data Register (PTB) <a href="#">See page 169.</a>	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
\$0002	Unimplemented									
\$0003	Unimplemented									
\$0004	Data Direction Register A (DDRA) <a href="#">See page 166.</a>	Read:	0	0	DDRA5	DDRA4	DDRA3	0	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0005	Data Direction Register B (DDRB) <a href="#">See page 170.</a>	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0006	Unimplemented									
\$000A	Unimplemented									
\$000B	Port A Input Pullup Enable Register (PTAPUE) <a href="#">See page 168.</a>	Read:	OSC2EN	0	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000C	Port B Input Pullup Enable Register (PTBPUE) <a href="#">See page 171.</a>	Read:	PTBPUE7	PTBPUE6	PTBPUE5	PTBPUE4	PTBPUE3	PTBPUE2	PTBPUE1	PTBPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000D	Unimplemented									
\$0019	Unimplemented									

= Unimplemented    
 R = Reserved    
U = Unaffected

**Figure 2-2. Control, Status, and Data Registers (Sheet 1 of 6)**

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$001A	Keyboard Status and Control Register (KBSCR) <a href="#">See page 185.</a>	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$001B	Keyboard Interrupt Enable Register (KBIER) <a href="#">See page 186.</a>	Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$001C	Unimplemented									
\$001D	IRQ Status and Control Register (INTSCR) <a href="#">See page 178.</a>	Read:	0	0	0	0	IRQF1	0	IMASK1	MODE1
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$001E	Configuration Register 2 (CONFIG2) <sup>(1)</sup> <a href="#">See page 56.</a>	Read:	IRQPUD	IRQEN	R	OSCOPT1	OSCOPT0	R	R	RSTEN
		Write:								
		Reset:	0	0	0	0	0	0	0	0
1. One-time writable register after each reset. 2. RSTEN reset to logic 0 by a power-on reset (POR) only.										
\$001F	Configuration Register 1 (CONFIG1) <sup>(1)</sup> <a href="#">See page 57.</a>	Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVI5OR3	SSREC	STOP	COPD
		Write:								
		Reset:	0	0	0	0	0 <sup>(2)</sup>	0	0	0
1. One-time writable register after each reset. 2. LVI5OR3 reset to logic 0 by a power-on reset (POR) only.										
\$0020	TIM Status and Control Register (TSC) <a href="#">See page 143.</a>	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
\$0021	TIM Counter Register High (TCNTH) <a href="#">See page 146.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0022	TIM Counter Register Low (TCNTL) <a href="#">See page 146.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
<span style="display: inline-block; width: 20px; height: 10px; background-color: #cccccc; border: 1px solid black;"></span> = Unimplemented <span style="display: inline-block; width: 20px; height: 10px; border: 1px solid black; text-align: center; margin-left: 10px;">R</span> = Reserved             U = Unaffected										

**Figure 2-2. Control, Status, and Data Registers (Sheet 2 of 6)**

# Memory

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$0023	TIM Counter Modulo Register High (TMODH) <a href="#">See page 146.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0024	TIM Counter Modulo Register Low (TMODL) <a href="#">See page 146.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0025	TIM Channel 0 Status and Control Register (TSC0) <a href="#">See page 147.</a>	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0026	TIM Channel 0 Register High (TCH0H) <a href="#">See page 151.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
\$0027	TIM Channel 0 Register Low (TCH0L) <a href="#">See page 151.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
\$0028	TIM Channel 1 Status and Control Register (TSC1) <a href="#">See page 147.</a>	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0029	TIM Channel 1 Register High (TCH1H) <a href="#">See page 151.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
\$002A	TIM Channel 1 Register Low (TCH1L) <a href="#">See page 151.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
\$002B	Unimplemented									
\$0035	Unimplemented									

= Unimplemented    
 R = Reserved    
 U = Unaffected

**Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 6)**

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0		
\$0036	Oscillator Status Register (OSCSTAT) <a href="#">See page 111.</a>	Read:	R	R	R	R	R	ECGON	ECGST		
		Write:									
		Reset:	0	0	0	0	0	0	0		
\$0037	Unimplemented										
\$0038	Oscillator Trim Register (OSCTRIM) <a href="#">See page 112.</a>	Read:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0	
		Write:									
		Reset:	1	0	0	0	0	0	0	0	
\$0039	Unimplemented										
\$003B	Unimplemented										
\$003C	ADC Status and Control Register (ADSCR) <a href="#">See page 159.</a>	Read:	COCO	AIEN	ADCO	CH4	CH3	CH2	CH1	CH0	
		Write:									
		Reset:	0	0	0	1	1	1	1	1	
\$003D	Unimplemented										
\$003E	ADC Data Register (ADR) <a href="#">See page 161.</a>	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
		Write:									
		Reset:	Indeterminate after reset								
\$003F	ADC Input Clock Register (ADICLK) <a href="#">See page 161.</a>	Read:				0	0	0	0	0	
		Write:	ADIV2	ADIV1	ADIV0						
		Reset:	0	0	0	0	0	0	0	0	
\$FE00	Break Status Register (BSR) <a href="#">See page 210.</a>	Read:	R	R	R	R	R	R	SBSW	R	
		Write:								See note 1	
		Reset:	0								
1. Writing a logic 0 clears SBSW.											
\$FE01	SIM Reset Status Register (SRSR) <a href="#">See page 98.</a>	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0	
		Write:									
		POR:	1	0	0	0	0	0	0	0	
<span style="border: 1px solid black; display: inline-block; width: 20px; height: 10px; background-color: #cccccc; vertical-align: middle;"></span> = Unimplemented <span style="border: 1px solid black; display: inline-block; width: 20px; height: 10px; background-color: #ffffff; vertical-align: middle;"></span> R = Reserved              U = Unaffected											

**Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 6)**

# Memory

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0	
\$FE02	Break Auxiliary Register (BRKAR) <a href="#">See page 209.</a>	Read:	0	0	0	0	0	0	0	BDCOP	
		Write:									
		Reset:	0	0	0	0	0	0	0	0	
\$FE03	Break Flag Control Register (BFCR) <a href="#">See page 211.</a>	Read:	BCFE	R	R	R	R	R	R	R	
		Write:									
		Reset:	0								
\$FE04	Interrupt Status Register 1 (INT1) <a href="#">See page 178.</a>	Read:	0	IF5	IF4	IF3	0	IF1	0	0	
		Write:	R	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0	0
\$FE05	Interrupt Status Register 2 (INT2) <a href="#">See page 178.</a>	Read:	IF14	0	0	0	0	0	0	0	
		Write:	R	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0	0
\$FE06	Interrupt Status Register 3 (INT3) <a href="#">See page 178.</a>	Read:	0	0	0	0	0	0	0	IF15	
		Write:	R	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0	0
\$FE07	Reserved		R	R	R	R	R	R	R	R	
\$FE08	FLASH Control Register (FLCR) <a href="#">See page 47.</a>	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM	
		Write:									
		Reset:	0	0	0	0	0	0	0	0	0
\$FE09	Break Address High Register (BRKH) <a href="#">See page 208.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
		Write:									
		Reset:	0	0	0	0	0	0	0	0	0
\$FE0A	Break Address low Register (BRKL) <a href="#">See page 208.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
		Write:									
		Reset:	0	0	0	0	0	0	0	0	0
\$FE0B	Break Status and Control Register (BRKSCR) <a href="#">See page 207.</a>	Read:	BRKE	BRKA	0	0	0	0	0	0	
		Write:									
		Reset:	0	0	0	0	0	0	0	0	0

= Unimplemented    
 = Reserved    
U = Unaffected


**Figure 2-2. Control, Status, and Data Registers (Sheet 5 of 6)**



Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$FE0C	LVI Status Register (LVISR) <a href="#">See page 201.</a>	Read:	LVIOUT	0	0	0	0	0	R	
		Write:								
		Reset:	0	0	0	0	0	0	0	
\$FE0D	Reserved for FLASH Test	R	R	R	R	R	R	R	R	
\$FE0F	Reserved for FLASH Test	R	R	R	R	R	R	R	R	
\$FFB0	Unimplemented									
\$FFBD	Unimplemented									
\$FFBE	FLASH Block Protect Register (FLBPR) <a href="#">See page 53.</a>	Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FFBF	Unimplemented									
\$FFC0	Internal Oscillator Trim Value (Optional)	Read:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
		Write:								
		Reset:	1	0	0	0	0	0	0	0
\$FFC1	Reserved	R	R	R	R	R	R	R	R	
\$FFC2	Unimplemented									
\$FFCF	Unimplemented									
\$FFFF	COP Control Register (COPCTL) <a href="#">See page 194.</a>	Read:	LOW BYTE OF RESET VECTOR							
		Write:	WRITING CLEARS COP COUNTER (ANY VALUE)							
		Reset:	Unaffected by reset							
			= Unimplemented		R = Reserved		U = Unaffected			

**Figure 2-2. Control, Status, and Data Registers (Sheet 6 of 6)**

**Table 2-1. Vector Addresses**

Vector Priority	Vector	Address	Vector
Lowest  Highest	IF15	\$FFDE	ADC conversion complete vector (high)
		\$FFDF	ADC conversion complete vector (low)
	IF14	\$FFE0	Keyboard vector (high)
		\$FFE1	Keyboard vector (low)
	IF13 ↓ IF6	—	Not used
	IF5	\$FFF2	TIM overflow vector (high)
		\$FFF3	TIM overflow vector (low)
	IF4	\$FFF4	TIM Channel 1 vector (high)
		\$FFF5	TIM Channel 1 vector (low)
	IF3	\$FFF6	TIM Channel 0 vector (high)
		\$FFF7	TIM Channel 0 vector (low)
	IF2	—	Not used
	IF1	\$FFFA	$\overline{\text{IRQ}}$ vector (high)
		\$FFFB	$\overline{\text{IRQ}}$ vector (low)
	—	\$FFFC	SWI vector (high)
		\$FFFD	SWI vector (low)
	—	\$FFFE	Reset vector (high)
		\$FFFF	Reset vector (low)

## Section 3. Random-Access Memory (RAM)

### 3.1 Contents

3.2	Introduction . . . . .	43
3.3	Functional Description . . . . .	43

### 3.2 Introduction

This section describes the 128 bytes of random-access memory (RAM).

### 3.3 Functional Description

Addresses \$0080–\$00FF are RAM locations. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64-Kbyte memory space.

**NOTE:** *For correct operation, the stack pointer must point only to RAM locations.*

Before processing an interrupt, the central processor unit (CPU) uses five bytes of the stack to save the contents of the CPU registers.

**NOTE:** *For M6805, M146805, and M68HC05 compatibility, the H register is not stacked.*

During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

**NOTE:** *Be careful when using nested subroutines. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.*

# Random-Access Memory (RAM)

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## Section 4. FLASH Memory (FLASH)

### 4.1 Contents

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4.3	Functional Description . . . . .	46
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4.5	FLASH Page Erase Operation . . . . .	48
4.6	FLASH Mass Erase Operation . . . . .	49
4.7	FLASH Program Operation. . . . .	49
4.8	FLASH Protection. . . . .	51
4.9	FLASH Block Protect Register . . . . .	53
4.10	Wait Mode. . . . .	54
4.11	Stop Mode . . . . .	54

### 4.2 Introduction

This section describes the operation of the embedded FLASH memory. The FLASH memory can be read, programmed, and erased from a single external supply. The program and erase operations are enabled through the use of an internal charge pump.

- MC68HC908QY4 and MC68HC908QT4: 4096 bytes user FLASH from \$EE00–\$FDFF
- MC68HC908QY2, MC68HC908QT2, MC68HC908QY1 and MC68HC908QT1: 1536 bytes user FLASH from \$F600–\$FBFF

### 4.3 Functional Description

The FLASH memory consists of an array of 4096 or 1536 bytes with an additional 48 bytes for user vectors. The minimum size of FLASH memory that can be erased is 64 bytes; and the maximum size of FLASH memory that can be programmed in a program cycle is 32 bytes (a row). Program and erase operations are facilitated through control bits in the FLASH control register (FLCR). Details for these operations appear later in this section. The address ranges for the user memory and vectors are:

- \$EE00 – \$FDFF; user memory, 4096 bytes: MC68HC908QY4 and MC68HC908QT4
- \$F600 – \$FBFF; user memory, 1536 bytes: MC68HC908QY2, MC68HC908QT2, MC68HC908QY1 and MC68HC908QT1
- \$FFD0 – \$FFFF; user interrupt vectors, 48 bytes.

**NOTE:** *An erased bit reads as logic 1 and a programmed bit reads as logic 0. A security feature prevents viewing of the FLASH contents.<sup>(1)</sup>*

---

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

## 4.4 FLASH Control Register

The FLASH control register (FLCR) controls FLASH program and erase operations.

Address: \$FE08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
Write:								
Reset:	0	0	0	0	0	0	0	0

**Figure 4-1. FLASH Control Register (FLCR)**

### HVEN — High Voltage Enable Bit

This read/write bit enables high voltage from the charge pump to the memory for either program or erase operation. It can only be set if either PGM = 1 or ERASE = 1 and the proper sequence for program or erase is followed.

- 1 = High voltage enabled to array and charge pump on
- 0 = High voltage disabled to array and charge pump off

### MASS — Mass Erase Control Bit

This read/write bit configures the memory for mass erase operation.

- 1 = Mass Erase operation selected
- 0 = Mass Erase operation unselected

### ERASE — Erase Control Bit

This read/write bit configures the memory for erase operation.

ERASE is interlocked with the PGM bit such that both bits cannot be equal to 1 or set to 1 at the same time.

- 1 = Erase operation selected
- 0 = Erase operation unselected

### PGM — Program Control Bit

This read/write bit configures the memory for program operation.

PGM is interlocked with the ERASE bit such that both bits cannot be equal to 1 or set to 1 at the same time.

- 1 = Program operation selected
- 0 = Program operation unselected

### 4.5 FLASH Page Erase Operation

Use the following procedure to erase a page of FLASH memory. A page consists of 64 consecutive bytes starting from addresses \$XX00, \$XX40, \$XX80, or \$XXC0. The 48-byte user interrupt vectors area also forms a page. Any FLASH memory page can be erased alone.

1. Set the ERASE bit and clear the MASS bit in the FLASH control register.
2. Read the FLASH block protect register.
3. Write any data to any FLASH location within the address range of the block to be erased.
4. Wait for a time,  $t_{nvs}$  (minimum 10  $\mu$ s).
5. Set the HVEN bit.
6. Wait for a time,  $t_{Erase}$  (minimum 4 ms).
7. Clear the ERASE bit.
8. Wait for a time,  $t_{nvh}$  (minimum 5  $\mu$ s).
9. Clear the HVEN bit.
10. After time,  $t_{rcv}$  (typical 1  $\mu$ s), the memory can be accessed in read mode again.

**NOTE:** Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.



## 4.6 FLASH Mass Erase Operation

Use the following procedure to erase the entire FLASH memory to read as logic 1:

1. Set both the ERASE bit and the MASS bit in the FLASH control register.
2. Read from the FLASH block protect register.
3. Write any data to any FLASH address<sup>(1)</sup> within the FLASH memory address range.
4. Wait for a time,  $t_{nvs}$  (minimum 10  $\mu$ s).
5. Set the HVEN bit.
6. Wait for a time,  $t_{Erase}$  (minimum 4 ms).
7. Clear the ERASE bit.
8. Wait for a time,  $t_{nvh1}$  (minimum 100  $\mu$ s).
9. Clear the HVEN bit.
10. After time,  $t_{rcv}$  (typical 1  $\mu$ s), the memory can be accessed in read mode again.

**NOTE:** Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.

## 4.7 FLASH Program Operation

Programming of the FLASH memory is done on a row basis. A row consists of 32 consecutive bytes starting from addresses \$XX00, \$XX20, \$XX40, \$XX60, \$XX80, \$XXA0, \$XXC0, or \$XXE0. Use the following step-by-step procedure to program a row of FLASH memory

**Figure 4-2** shows a flowchart of the programming algorithm.

**NOTE:** *In order to avoid program disturbs, the row must be erased before any byte on that row is programmed.*

1. When in monitor mode, with security sequence failed (see [9.5 Security](#)), write to the FLASH block protect register instead of any FLASH address.

1. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
2. Read from the FLASH block protect register.
3. Write any data to any FLASH location within the address range desired.
4. Wait for a time,  $t_{nvs}$  (minimum 10  $\mu$ s).
5. Set the HVEN bit.
6. Wait for a time,  $t_{pgs}$  (minimum 5  $\mu$ s).
7. Write data to the FLASH address being programmed<sup>(1)</sup>.
8. Wait for time,  $t_{PROG}$  (minimum 30  $\mu$ s).
9. Repeat step 6 and 7 until all the bytes within the row are programmed.
10. Clear the PGM bit<sup>(1)</sup>.
11. Wait for time,  $t_{nvh}$  (minimum 5  $\mu$ s).
12. Clear the HVEN bit.
13. After time,  $t_{rcv}$  (typical 1  $\mu$ s), the memory can be accessed in read mode again.

**NOTE:** *The COP register at location \$FFFF should not be written between steps 5-12, when the HVEN bit is set. Since this register is located at a valid FLASH address, unpredictable behavior may occur if this location is written while HVEN is set.*

This program sequence is repeated throughout the memory until all data is programmed.

**NOTE:** *Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order shown, other unrelated operations may occur between the steps. Do not exceed  $t_{PROG}$  maximum, see [18.14 Memory Characteristics](#).*

---

1. The time between each FLASH address change, or the time between the last FLASH address programmed to clearing PGM bit, must not exceed the maximum programming time,  $t_{PROG}$  maximum.

## 4.8 FLASH Protection

Due to the ability of the on-board charge pump to erase and program the FLASH memory in the target application, provision is made to protect blocks of memory from unintentional erase or program operations due to system malfunction. This protection is done by use of a FLASH block protect register (FLBPR). The FLBPR determines the range of the FLASH memory which is to be protected. The range of the protected area starts from a location defined by FLBPR and ends to the bottom of the FLASH memory (\$FFFF). When the memory is protected, the HVEN bit cannot be set in either ERASE or PROGRAM operations.

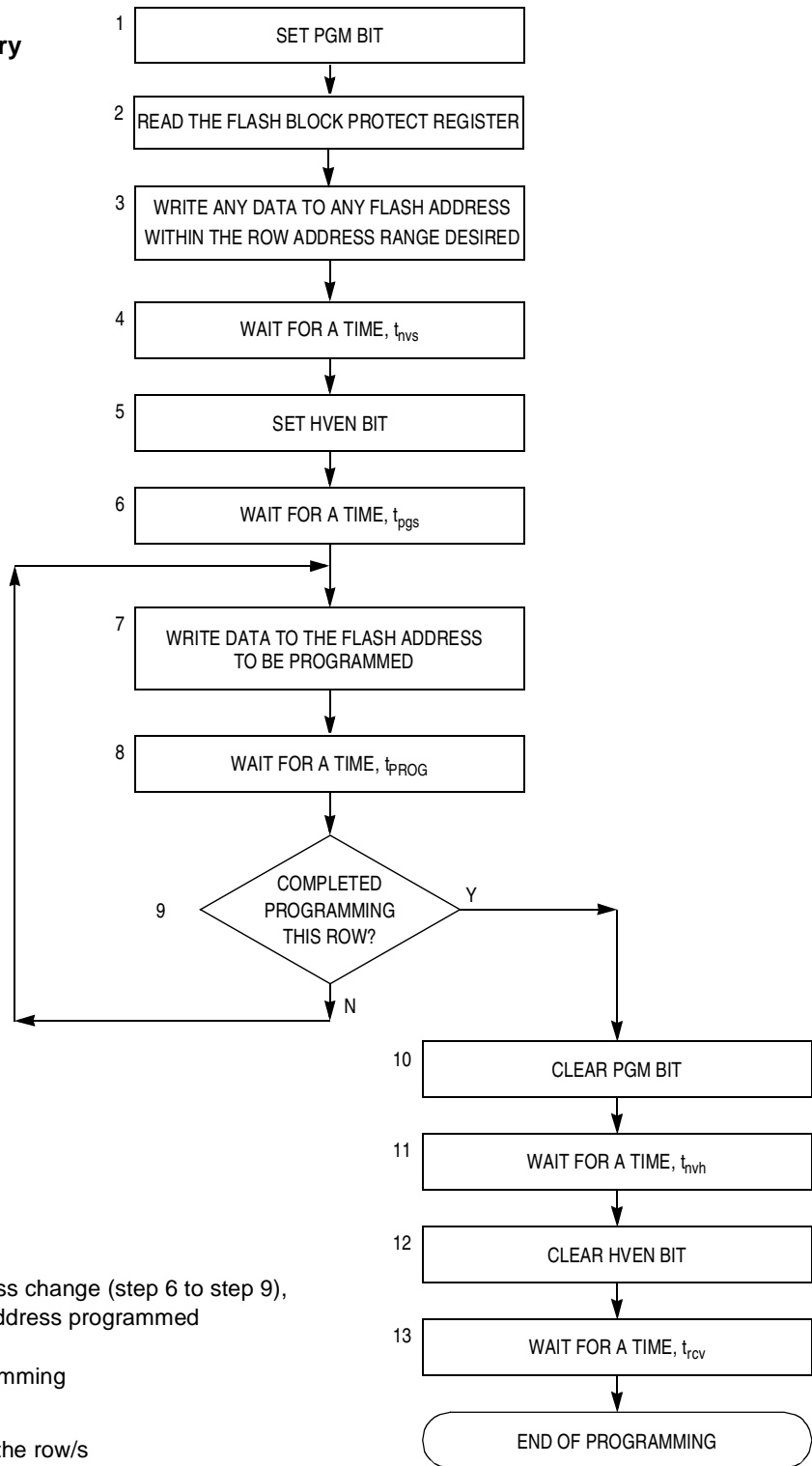
**NOTE:** *In performing a program or erase operation, the FLASH block protect register must be read after setting the PGM or ERASE bit and before asserting the HVEN bit.*

When the FLBPR is programmed with all 0 s, the entire memory is protected from being programmed and erased. When all the bits are erased (all 1's), the entire memory is accessible for program and erase.

When bits within the FLBPR are programmed, they lock a block of memory. The address ranges are shown in [4.9 FLASH Block Protect Register](#). Once the FLBPR is programmed with a value other than \$FF, any erase or program of the FLBPR or the protected block of FLASH memory is prohibited. The FLBPR itself can be erased or programmed only with an external voltage,  $V_{TST}$ , present on the  $\overline{IRQ}$  pin. This voltage also allows entry from reset into the monitor mode.

# FLASH Memory (FLASH)

## Algorithm for Programming a Row (32 Bytes) of FLASH Memory



**NOTES:**

The time between each FLASH address change (step 6 to step 9), or the time between the last FLASH address programmed to clearing PGM bit (step 6 to step 9) must not exceed the maximum programming time,  $t_{PROG\ max}$ .

This row program algorithm assumes the row/s to be programmed are initially erased.

**Figure 4-2. FLASH Programming Flowchart**

## 4.9 FLASH Block Protect Register

The FLASH block protect register is implemented as a byte within the FLASH memory, and therefore can only be written during a programming sequence of the FLASH memory. The value in this register determines the starting address of the protected range within the FLASH memory.

Address: \$FFBE

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
Write:								
Reset:	U	U	U	U	U	U	U	U

U = Unaffected by reset. Initial value from factory is 1.

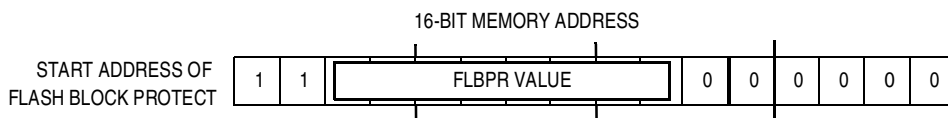
Write to this register is by a programming sequence to the FLASH memory.

**Figure 4-3. FLASH Block Protect Register (FLBPR)**

### BPR[7:0] — FLASH Protection Register Bits [7:0]

These eight bits in FLBPR represent bits [13:6] of a 16-bit memory address. Bits [15:14] are logic 1s and bits [5:0] are logic 0s.

The resultant 16-bit address is used for specifying the start address of the FLASH memory for block protection. The FLASH is protected from this start address to the end of FLASH memory, at \$FFFF. With this mechanism, the protect start address can be XX00, XX40, XX80, or XXC0 within the FLASH memory. See [Figure 4-4](#) and [Table 4-1](#).



**Figure 4-4. FLASH Block Protect Start Address**

**Table 4-1. Examples of Protect Start Address**

BPR[7:0]	Start of Address of Protect Range
\$00–\$B8	The entire FLASH memory is protected.
\$B9 (1011 1001)	\$EE40 (1110 1110 0100 0000)
\$BA (1011 1010)	\$EE80 (1110 1110 1000 0000)
\$BB (1011 1011)	\$EEC0 (1110 1110 1100 0000)
\$BC (1011 1100)	\$EF00 (1110 1111 0000 0000)
and so on...	
\$DE (1101 1110)	\$F780 (1111 0111 1000 0000)
\$DF (1101 1111)	\$F7C0 (1111 0111 1100 0000)
\$FE (1111 1110)	\$FF80 (1111 1111 1000 0000) FLBPR, OSCTRIM, and vectors are protected
\$FF	The entire FLASH memory is not protected.

## 4.10 Wait Mode

Putting the MCU into wait mode while the FLASH is in read mode does not affect the operation of the FLASH memory directly, but there will not be any memory activity since the CPU is inactive.

The WAIT instruction should not be executed while performing a program or erase operation on the FLASH, or the operation will discontinue and the FLASH will be on standby mode.

## 4.11 Stop Mode

Putting the MCU into stop mode while the FLASH is in read mode does not affect the operation of the FLASH memory directly, but there will not be any memory activity since the CPU is inactive.

The STOP instruction should not be executed while performing a program or erase operation on the FLASH, or the operation will discontinue and the FLASH will be on standby mode

**NOTE:** *Standby mode is the power-saving mode of the FLASH module in which all internal control signals to the FLASH are inactive and the current consumption of the FLASH is at a minimum.*

## Section 5. Configuration Register (CONFIG)

### 5.1 Contents

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5.3	Functional Description . . . . .	55

### 5.2 Introduction

This section describes the configuration registers (CONFIG1 and CONFIG2). The configuration registers enable or disable the following options:

- Stop mode recovery time ( $32 \times 2\text{OSCOU}$  cycles or  $4096 \times 2\text{OSCOU}$  cycles)
- STOP instruction
- Computer operating properly module (COP)
- COP reset period (COPRS):  $(2^{13}-2^4) \times 2\text{OSCOU}$  or  $(2^{18}-2^4) \times 2\text{OSCOU}$
- Low-voltage inhibit (LVI) enable and trip voltage selection
- OSC option selection
- $\overline{\text{IRQ}}$  pin
- $\overline{\text{RST}}$  pin
- Auto wake-up timeout period

### 5.3 Functional Description

The configuration registers are used in the initialization of various options. The configuration registers can be written once after each reset.

## Configuration Register (CONFIG)

Most of the configuration register bits are cleared during reset. Since the various options affect the operation of the microcontroller unit (MCU) it is recommended that this register be written immediately after reset. The configuration register is located at \$001E and \$001F, and may be read at anytime.

**NOTE:** *The CONFIG registers are one-time writable by the user after each reset. Upon a reset, the CONFIG registers default to predetermined settings as shown in [Figure 5-1](#) and [Figure 5-2](#).*

Address: \$001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQPUD	IRQEN	R	OSCOPT1	OSCOPT0	R	R	RSTEN
Write:								
Reset:	0	0	0	0	0	0	0	U
POR:	0	0	0	0	0	0	0	0

R = Reserved                      U = Unaffected

**Figure 5-1 Configuration Register 2 (CONFIG2)**

IRQPUD —  $\overline{\text{IRQ}}$  Pin Pullup Control Bit

1 = Internal pullup is disconnected

0 = Internal pullup is connected between  $\overline{\text{IRQ}}$  pin and  $V_{DD}$

IRQEN —  $\overline{\text{IRQ}}$  Pin Function Selection Bit

1 = Interrupt request function active in pin

0 = Interrupt request function inactive in pin

OSCOPT1 and OSCOPT0 — Selection Bits for Oscillator Option

(0, 0) Internal oscillator

(0, 1) External oscillator

(1, 0) External RC oscillator

(1, 1) External XTAL oscillator

RSTEN —  $\overline{\text{RST}}$  Pin Function Selection

1 = Reset function active in pin

0 = Reset function inactive in pin

**NOTE:** *The RSTEN bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.*



Address: \$001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVI5OR3	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0	U	0	0	0
POR:	0	0	0	0	0	0	0	0

R = Reserved      U = Unaffected

**Figure 5-2 Configuration Register 1 (CONFIG1)**

**COPRS (Out of STOP Mode) — COP Reset Period Selection Bit**

1 = COP reset short cycle =  $(2^{13} - 2^4) \times 2\text{OSCOU}$

0 = COP reset long cycle =  $(2^{18} - 2^4) \times 2\text{OSCOU}$

**COPRS (In STOP Mode) — Auto Wake-up Period Selection Bit**

1 = Auto wake-up short cycle =  $(2^9) \times \text{INTRCOSC}$

0 = Auto wake-up long cycle =  $(2^{14}) \times \text{INTRCOSC}$

**LVISTOP — LVI Enable in Stop Mode Bit**

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP.

1 = LVI enabled during stop mode

0 = LVI disabled during stop mode

**LVIRSTD — LVI Reset Disable Bit**

LVIRSTD disables the reset signal from the LVI module.

1 = LVI module resets disabled

0 = LVI module resets enabled

**LVIPWRD — LVI Power Disable Bit**

LVIPWRD disables the LVI module.

1 = LVI module power disabled

0 = LVI module power enabled

### LVI5OR3 — LVI 5-V or 3-V Operating Mode Bit

LVI5OR3 selects the voltage operating mode of the LVI module. The voltage mode selected for the LVI should match the operating  $V_{DD}$  for the LVI's voltage trip points for each of the modes.

1 = LVI operates in 5-V mode

0 = LVI operates in 3-V mode

**NOTE:** *The LVI5OR3 bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.*

### SSREC — Short Stop Recovery Bit

SSREC enables the CPU to exit stop mode with a delay of 32 2OSCOU cycles instead of a 4096-2OSCOU cycle delay.

1 = Stop mode recovery after 32 2OSCOU cycles

0 = Stop mode recovery after 4096 2OSCOU cycles

**NOTE:** *Exiting stop mode by an LVI reset will result in the long stop recovery.*

When using the LVI during normal operation but disabling during stop mode, the LVI will have an enable time of  $t_{EN}$ . The system stabilization time for power-on reset and long stop recovery (both 4096 2OSCOU cycles) gives a delay longer than the LVI enable time for these startup scenarios. There is no period where the MCU is not protected from a low-power condition. However, when using the short stop recovery configuration option, the 32-2OSCOU delay must be greater than the LVI's turn on time to avoid a period in startup where the LVI is not protecting the MCU.

### STOP — STOP Instruction Enable Bit

STOP enables the STOP instruction.

1 = STOP instruction enabled

0 = STOP instruction treated as illegal opcode

### COPD — COP Disable Bit

COPD disables the COP module.

1 = COP module disabled

0 = COP module enabled

## Section 6. Central Processor Unit (CPU)

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### 6.2 Introduction

The M68HC08 CPU (central processor unit) is an enhanced and fully object-code-compatible version of the M68HC05 CPU. The *CPU08 Reference Manual* (Motorola document order number CPU08RM/AD) contains a description of the CPU instruction set, addressing modes, and architecture.

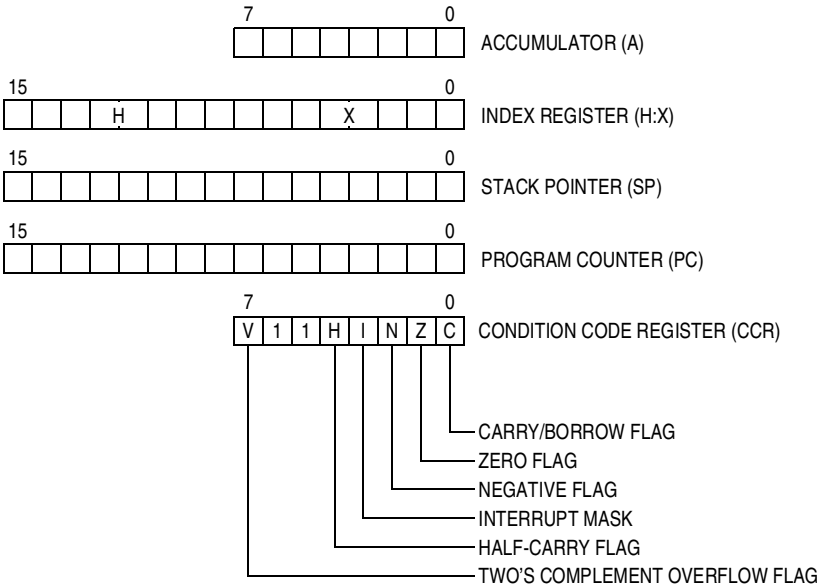
## 6.3 Features

Features of the CPU include:

- Object code fully upward-compatible with M68HC05 Family
- 16-bit stack pointer with stack manipulation instructions
- 16-bit index register with x-register manipulation instructions
- 8-MHz CPU internal bus frequency
- 64-Kbyte program/data memory space
- 16 addressing modes
- Memory-to-memory data moves without using accumulator
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- Enhanced binary-coded decimal (BCD) data handling
- Modular architecture with expandable internal bus definition for extension of addressing range beyond 64 Kbytes
- Low-power stop and wait modes

## 6.4 CPU Registers

**Figure 6-1** shows the five CPU registers. CPU registers are not part of the memory map.



**Figure 6-1. CPU Registers**

**6.4.1 Accumulator**

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.



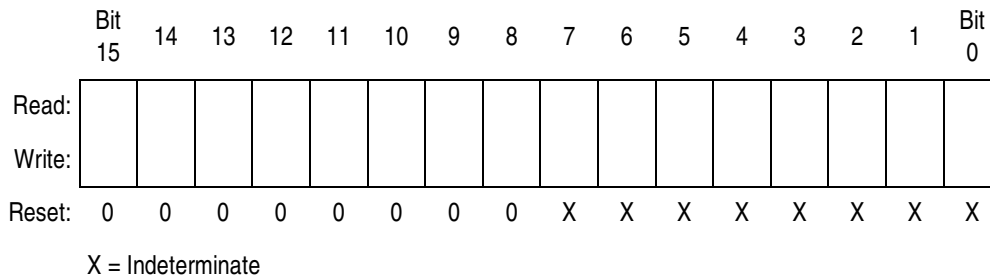
**Figure 6-2. Accumulator (A)**

**6.4.2 Index Register**

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.

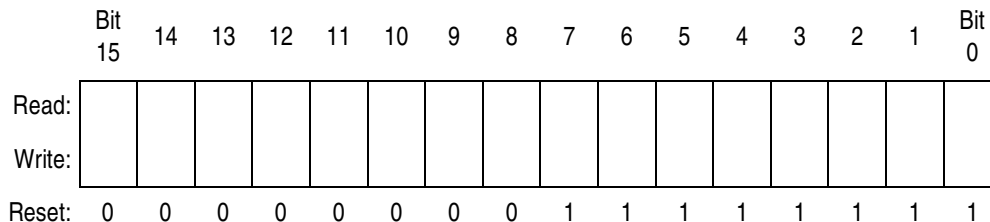


**Figure 6-3. Index Register (H:X)**

### 6.4.3 Stack Pointer

The stack pointer is a 16-bit register that contains the address of the next location on the stack. During a reset, the stack pointer is preset to \$00FF. The reset stack pointer (RSP) instruction sets the least significant byte to \$FF and does not affect the most significant byte. The stack pointer decrements as data is pushed onto the stack and increments as data is pulled from the stack.

In the stack pointer 8-bit offset and 16-bit offset addressing modes, the stack pointer can function as an index register to access data on the stack. The CPU uses the contents of the stack pointer to determine the conditional address of the operand.



**Figure 6-4. Stack Pointer (SP)**

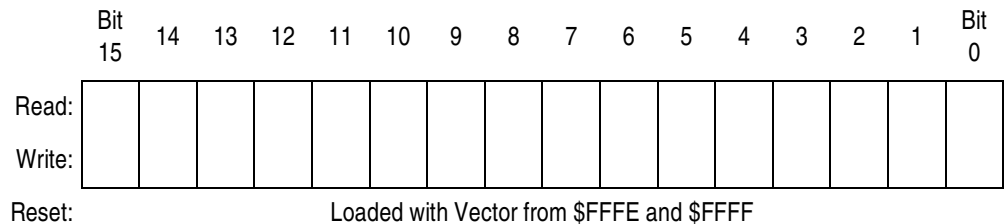
**NOTE:** *The location of the stack is arbitrary and may be relocated anywhere in RAM. Moving the SP out of page 0 (\$0000 to \$00FF) frees direct address (page 0) space. For correct operation, the stack pointer must point only to RAM locations.*

### 6.4.4 Program Counter

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

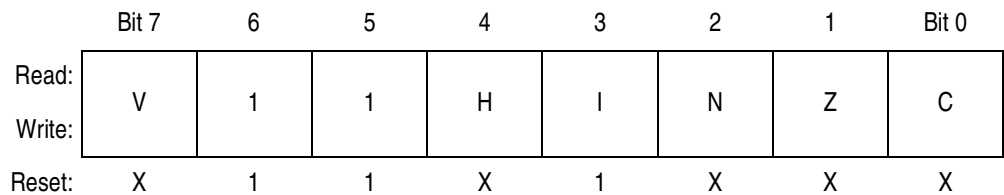
During reset, the program counter is loaded with the reset vector address located at \$FFFE and \$FFFF. The vector address is the address of the first instruction to be executed after exiting the reset state.



**Figure 6-5. Program Counter (PC)**

### 6.4.5 Condition Code Register

The 8-bit condition code register contains the interrupt mask and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to logic 1. The following paragraphs describe the functions of the condition code register.



X = Indeterminate

**Figure 6-6. Condition Code Register (CCR)**

### V — Overflow Flag

The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag.

1 = Overflow

0 = No overflow

### H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C flags to determine the appropriate correction factor.

1 = Carry between bits 3 and 4

0 = No carry between bits 3 and 4

### I — Interrupt Mask

When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the interrupt vector is fetched.

1 = Interrupts disabled

0 = Interrupts enabled

**NOTE:** *To maintain M6805 Family compatibility, the upper byte of the index register (H) is not stacked automatically. If the interrupt service routine modifies H, then the user must stack and unstack H using the PSHH and PULH instructions.*

After the I bit is cleared, the highest-priority interrupt request is serviced first.

A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack and restores the interrupt mask from the stack. After any reset, the interrupt mask is set and can be cleared only by the clear interrupt mask software instruction (CLI).



#### N — Negative flag

The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result.

- 1 = Negative result
- 0 = Non-negative result

#### Z — Zero flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of \$00.

- 1 = Zero result
- 0 = Non-zero result

#### C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.

- 1 = Carry out of bit 7
- 0 = No carry out of bit 7

## 6.5 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations defined by the instruction set.

Refer to the *CPU08 Reference Manual* (Motorola document order number CPU08RM/AD) for a description of the instructions and addressing modes and more detail about the architecture of the CPU.

## 6.6 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

### 6.6.1 Wait Mode

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

### 6.6.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

## 6.7 CPU During Break Interrupts

If a break module is present on the MCU, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with \$FFFC:\$FFFD or with \$FEFC:\$FEFD in monitor mode

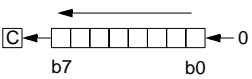
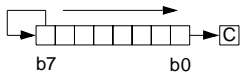
The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.

## 6.8 Instruction Set Summary

Table 6-1 provides a summary of the M68HC08 instruction set.

Table 6-1. Instruction Set Summary (Sheet 1 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #opr ADC opr ADC opr,X ADC opr,X ADC ,X ADC opr,SP ADC opr,SP	Add with Carry	$A \leftarrow (A) + (M) + (C)$	↑	↑	-	↑	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #opr ADD opr ADD opr ADD opr,X ADD opr,X ADD ,X ADD opr,SP ADD opr,SP	Add without Carry	$A \leftarrow (A) + (M)$	↑	↑	-	↑	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #opr	Add Immediate Value (Signed) to SP	$SP \leftarrow (SP) + (16 \ll M)$	-	-	-	-	-	-	IMM	A7	ii	2
AIX #opr	Add Immediate Value (Signed) to H:X	$H:X \leftarrow (H:X) + (16 \ll M)$	-	-	-	-	-	-	IMM	AF	ii	2
AND #opr AND opr AND opr AND opr,X AND opr,X AND ,X AND opr,SP AND opr,SP	Logical AND	$A \leftarrow (A) \& (M)$	0	-	-	↑	↑	-	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL opr ASLA ASLX ASL opr,X ASL ,X ASL opr,SP	Arithmetic Shift Left (Same as LSL)		↑	-	-	↑	↑	↑	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
ASR opr ASRA ASRX ASR opr,X ASR opr,X ASR opr,SP	Arithmetic Shift Right		↑	-	-	↑	↑	↑	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff	4 1 1 4 3 5
BCC rel	Branch if Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel ? (C) = 0$	-	-	-	-	-	-	REL	24	rr	3
BCLR n, opr	Clear Bit n in M	$M_n \leftarrow 0$	-	-	-	-	-	-	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BCS rel	Branch if Carry Bit Set (Same as BLO)	$PC \leftarrow (PC) + 2 + rel ? (C) = 1$	-	-	-	-	-	-	REL	25	rr	3
BEQ rel	Branch if Equal	$PC \leftarrow (PC) + 2 + rel ? (Z) = 1$	-	-	-	-	-	-	REL	27	rr	3

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## Table 6-1. Instruction Set Summary (Sheet 2 of 7)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles	
			V	H	I	N	Z					C
BGE <i>opr</i>	Branch if Greater Than or Equal To (Signed Operands)	$PC \leftarrow (PC) + 2 + rel ? (N \oplus V) = 0$	-	-	-	-	-	REL	90	rr	3	
BGT <i>opr</i>	Branch if Greater Than (Signed Operands)	$PC \leftarrow (PC) + 2 + rel ? (Z)   (N \oplus V) = 0$	-	-	-	-	-	REL	92	rr	3	
BHCC <i>rel</i>	Branch if Half Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel ? (H) = 0$	-	-	-	-	-	REL	28	rr	3	
BHCS <i>rel</i>	Branch if Half Carry Bit Set	$PC \leftarrow (PC) + 2 + rel ? (H) = 1$	-	-	-	-	-	REL	29	rr	3	
BHI <i>rel</i>	Branch if Higher	$PC \leftarrow (PC) + 2 + rel ? (C)   (Z) = 0$	-	-	-	-	-	REL	22	rr	3	
BHS <i>rel</i>	Branch if Higher or Same (Same as BCC)	$PC \leftarrow (PC) + 2 + rel ? (C) = 0$	-	-	-	-	-	REL	24	rr	3	
BIH <i>rel</i>	Branch if $\overline{IRQ}$ Pin High	$PC \leftarrow (PC) + 2 + rel ? \overline{IRQ} = 1$	-	-	-	-	-	REL	2F	rr	3	
BIL <i>rel</i>	Branch if $\overline{IRQ}$ Pin Low	$PC \leftarrow (PC) + 2 + rel ? \overline{IRQ} = 0$	-	-	-	-	-	REL	2E	rr	3	
BIT # <i>opr</i> BIT <i>opr</i> BIT <i>opr</i> BIT <i>opr</i> ,X BIT <i>opr</i> ,X BIT ,X BIT <i>opr</i> ,SP BIT <i>opr</i> ,SP	Bit Test	(A) & (M)	0	-	-	†	†	-	IMM DIR EXT IX2 IX1 IX SP1 SP2	A5 B5 C5 D5 E5 F5 9EE5 9ED5	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
BLE <i>opr</i>	Branch if Less Than or Equal To (Signed Operands)	$PC \leftarrow (PC) + 2 + rel ? (Z)   (N \oplus V) = 1$	-	-	-	-	-	REL	93	rr	3	
BLO <i>rel</i>	Branch if Lower (Same as BCS)	$PC \leftarrow (PC) + 2 + rel ? (C) = 1$	-	-	-	-	-	REL	25	rr	3	
BLS <i>rel</i>	Branch if Lower or Same	$PC \leftarrow (PC) + 2 + rel ? (C)   (Z) = 1$	-	-	-	-	-	REL	23	rr	3	
BLT <i>opr</i>	Branch if Less Than (Signed Operands)	$PC \leftarrow (PC) + 2 + rel ? (N \oplus V) = 1$	-	-	-	-	-	REL	91	rr	3	
BMC <i>rel</i>	Branch if Interrupt Mask Clear	$PC \leftarrow (PC) + 2 + rel ? (I) = 0$	-	-	-	-	-	REL	2C	rr	3	
BMI <i>rel</i>	Branch if Minus	$PC \leftarrow (PC) + 2 + rel ? (N) = 1$	-	-	-	-	-	REL	2B	rr	3	
BMS <i>rel</i>	Branch if Interrupt Mask Set	$PC \leftarrow (PC) + 2 + rel ? (I) = 1$	-	-	-	-	-	REL	2D	rr	3	
BNE <i>rel</i>	Branch if Not Equal	$PC \leftarrow (PC) + 2 + rel ? (Z) = 0$	-	-	-	-	-	REL	26	rr	3	
BPL <i>rel</i>	Branch if Plus	$PC \leftarrow (PC) + 2 + rel ? (N) = 0$	-	-	-	-	-	REL	2A	rr	3	
BRA <i>rel</i>	Branch Always	$PC \leftarrow (PC) + 2 + rel$	-	-	-	-	-	REL	20	rr	3	
BRCLR <i>n,opr,rel</i>	Branch if Bit <i>n</i> in M Clear	$PC \leftarrow (PC) + 3 + rel ? (Mn) = 0$	-	-	-	-	†	-	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN <i>rel</i>	Branch Never	$PC \leftarrow (PC) + 2$	-	-	-	-	-	REL	21	rr	3	

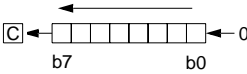
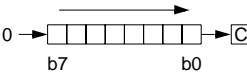
Table 6-1. Instruction Set Summary (Sheet 3 of 7)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles	
			V	H	I	N	Z					C
BRSET <i>n,opr,rel</i>	Branch if Bit <i>n</i> in M Set	$PC \leftarrow (PC) + 3 + rel ? (Mn) = 1$	-	-	-	-	-	†	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET <i>n,opr</i>	Set Bit <i>n</i> in M	$Mn \leftarrow 1$	-	-	-	-	-	-	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BSR <i>rel</i>	Branch to Subroutine	$PC \leftarrow (PC) + 2$ ; push (PCL) $SP \leftarrow (SP) - 1$ ; push (PCH) $SP \leftarrow (SP) - 1$ $PC \leftarrow (PC) + rel$	-	-	-	-	-	-	REL	AD	rr	4
CBEQ <i>opr,rel</i> CBEQA # <i>opr,rel</i> CBEQX # <i>opr,rel</i> CBEQ <i>opr,X+,rel</i> CBEQ <i>X+,rel</i> CBEQ <i>opr,SP,rel</i>	Compare and Branch if Equal	$PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \$00$ $PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \$00$ $PC \leftarrow (PC) + 3 + rel ? (X) - (M) = \$00$ $PC \leftarrow (PC) + 3 + rel ? (A) - (M) = \$00$ $PC \leftarrow (PC) + 2 + rel ? (A) - (M) = \$00$ $PC \leftarrow (PC) + 4 + rel ? (A) - (M) = \$00$	-	-	-	-	-	-	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	$C \leftarrow 0$	-	-	-	-	-	0	INH	98		1
CLI	Clear Interrupt Mask	$I \leftarrow 0$	-	-	0	-	-	-	INH	9A		2
CLR <i>opr</i> CLRA CLR X CLR H CLR <i>opr,X</i> CLR ,X CLR <i>opr,SP</i>	Clear	$M \leftarrow \$00$ $A \leftarrow \$00$ $X \leftarrow \$00$ $H \leftarrow \$00$ $M \leftarrow \$00$ $M \leftarrow \$00$ $M \leftarrow \$00$	0	-	-	0	1	-	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd ff ff ff	3 1 1 1 3 2 4
CMP # <i>opr</i> CMP <i>opr</i> CMP <i>opr</i> CMP <i>opr,X</i> CMP <i>opr,X</i> CMP ,X CMP <i>opr,SP</i> CMP <i>opr,SP</i>	Compare A with M	$(A) - (M)$	†	-	-	†	†	†	IMM DIR EXT IX2 IX1 IX SP1 SP2	A1 B1 C1 D1 E1 F1 9EE1 9ED1	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
COM <i>opr</i> COMA COM X COM <i>opr,X</i> COM ,X COM <i>opr,SP</i>	Complement (One's Complement)	$M \leftarrow (\overline{M}) = \$FF - (M)$ $A \leftarrow (\overline{A}) = \$FF - (M)$ $X \leftarrow (\overline{X}) = \$FF - (M)$ $M \leftarrow (\overline{M}) = \$FF - (M)$ $M \leftarrow (\overline{M}) = \$FF - (M)$ $M \leftarrow (\overline{M}) = \$FF - (M)$	0	-	-	†	†	1	DIR INH INH IX1 IX SP1	33 43 53 63 73 9E63	dd ff ff ff	4 1 1 4 3 5
CPHX # <i>opr</i> CPHX <i>opr</i>	Compare H:X with M	$(H:X) - (M:M + 1)$	†	-	-	†	†	†	IMM DIR	65 75	ii ii+1 dd	3 4

## Table 6-1. Instruction Set Summary (Sheet 4 of 7)

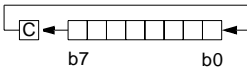
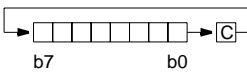
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles	
			V	H	I	N	Z					C
CPX #opr CPX opr CPX opr CPX ,X CPX opr,X CPX opr,X CPX opr,SP CPX opr,SP	Compare X with M	(X) - (M)	†	-	-	†	†	†	IMM DIR EXT IX2 IX1 IX SP1 SP2	A3 B3 C3 D3 E3 F3 9EE3 9ED3	ii dd hh ll ee ff ff ff ff	2 3 4 4 3 2 4 5
DAA	Decimal Adjust A	(A) <sub>10</sub>	U	-	-	†	†	†	INH	72		2
DBNZ opr,rel DBNZA rel DBNZX rel DBNZ opr,X,rel DBNZ X,rel DBNZ opr,SP,rel	Decrement and Branch if Not Zero	A ← (A) - 1 or M ← (M) - 1 or X ← (X) - 1 PC ← (PC) + 3 + rel? (result) ≠ 0 PC ← (PC) + 2 + rel? (result) ≠ 0 PC ← (PC) + 2 + rel? (result) ≠ 0 PC ← (PC) + 3 + rel? (result) ≠ 0 PC ← (PC) + 2 + rel? (result) ≠ 0 PC ← (PC) + 4 + rel? (result) ≠ 0	-	-	-	-	-	-	DIR INH INH IX1 IX SP1	3B 4B 5B 6B 7B 9E6B	dd rr rr rr ff rr rr ff rr	5 3 3 5 4 6
DEC opr DECA DECX DEC opr,X DEC ,X DEC opr,SP	Decrement	M ← (M) - 1 A ← (A) - 1 X ← (X) - 1 M ← (M) - 1 M ← (M) - 1 M ← (M) - 1	†	-	-	†	†	-	DIR INH INH IX1 IX SP1	3A 4A 5A 6A 7A 9E6A	dd  ff ff	4 1 1 4 3 5
DIV	Divide	A ← (H:A)/(X) H ← Remainder	-	-	-	-	†	†	INH	52		7
EOR #opr EOR opr EOR opr EOR opr,X EOR opr,X EOR ,X EOR opr,SP EOR opr,SP	Exclusive OR M with A	A ← (A ⊕ M)	0	-	-	†	†	-	IMM DIR EXT IX2 IX1 IX SP1 SP2	A8 B8 C8 D8 E8 F8 9EE8 9ED8	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
INC opr INCA INCX INC opr,X INC ,X INC opr,SP	Increment	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1 M ← (M) + 1	†	-	-	†	†	-	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd  ff ff	4 1 1 4 3 5
JMP opr JMP opr JMP opr,X JMP opr,X JMP ,X	Jump	PC ← Jump Address	-	-	-	-	-	-	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2
JSR opr JSR opr JSR opr,X JSR opr,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) - 1 Push (PCH); SP ← (SP) - 1 PC ← Unconditional Address	-	-	-	-	-	-	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	4 5 6 5 4
LDA #opr LDA opr LDA opr LDA opr,X LDA opr,X LDA ,X LDA opr,SP LDA opr,SP	Load A from M	A ← (M)	0	-	-	†	†	-	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5

**Table 6-1. Instruction Set Summary (Sheet 5 of 7)**

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles	
			V	H	I	N	Z					C
LDHX #opr LDHX opr	Load H:X from M	$H:X \leftarrow (M:M + 1)$	0	-	-	†	†	-	IMM DIR	45 55	ii jj dd	3 4
LDX #opr LDX opr LDX opr LDX opr,X LDX opr,X LDX ,X LDX opr,SP LDX opr,SP	Load X from M	$X \leftarrow (M)$	0	-	-	†	†	-	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh ll ee ff ff ff ff ff ff	2 3 4 4 3 2 4 5
LSL opr LSLA LSLX LSL opr,X LSL ,X LSL opr,SP	Logical Shift Left (Same as ASL)		†	-	-	†	†	†	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
LSR opr LSRA LSRX LSR opr,X LSR ,X LSR opr,SP	Logical Shift Right		†	-	-	0	†	†	DIR INH INH IX1 IX SP1	34 44 54 64 74 9E64	dd ff ff	4 1 1 4 3 5
MOV opr,opr MOV opr,X+ MOV #opr,opr MOV X+,opr	Move	$(M)_{\text{Destination}} \leftarrow (M)_{\text{Source}}$ $H:X \leftarrow (H:X) + 1$ (IX+D, DIX+)	0	-	-	†	†	-	DD DIX+ IMD IX+D	4E 5E 6E 7E	dd dd dd ii dd dd	5 4 4 4
MUL	Unsigned multiply	$X:A \leftarrow (X) \times (A)$	-	0	-	-	-	0	INH	42		5
NEG opr NEGA NEGX NEG opr,X NEG ,X NEG opr,SP	Negate (Two's Complement)	$M \leftarrow -(M) = \$00 - (M)$ $A \leftarrow -(A) = \$00 - (A)$ $X \leftarrow -(X) = \$00 - (X)$ $M \leftarrow -(M) = \$00 - (M)$ $M \leftarrow -(M) = \$00 - (M)$	†	-	-	†	†	†	DIR INH INH IX1 IX SP1	30 40 50 60 70 9E60	dd ff ff	4 1 1 4 3 5
NOP	No Operation	None	-	-	-	-	-	-	INH	9D		1
NSA	Nibble Swap A	$A \leftarrow (A[3:0]:A[7:4])$	-	-	-	-	-	-	INH	62		3
ORA #opr ORA opr ORA opr ORA opr,X ORA opr,X ORA ,X ORA opr,SP ORA opr,SP	Inclusive OR A and M	$A \leftarrow (A)   (M)$	0	-	-	†	†	-	IMM DIR DIR EXT IX2 IX1 IX SP1 SP2	AA BA CA DA EA FA 9EEA 9EDA	ii dd hh ll ee ff ff ff ff ff	2 3 4 4 3 2 4 5
PSHA	Push A onto Stack	Push (A); $SP \leftarrow (SP) - 1$	-	-	-	-	-	-	INH	87		2
PSHH	Push H onto Stack	Push (H); $SP \leftarrow (SP) - 1$	-	-	-	-	-	-	INH	8B		2
PSHX	Push X onto Stack	Push (X); $SP \leftarrow (SP) - 1$	-	-	-	-	-	-	INH	89		2
PULA	Pull A from Stack	$SP \leftarrow (SP + 1)$ ; Pull (A)	-	-	-	-	-	-	INH	86		2
PULH	Pull H from Stack	$SP \leftarrow (SP + 1)$ ; Pull (H)	-	-	-	-	-	-	INH	8A		2
PULX	Pull X from Stack	$SP \leftarrow (SP + 1)$ ; Pull (X)	-	-	-	-	-	-	INH	88		2

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## Table 6-1. Instruction Set Summary (Sheet 6 of 7)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles					
			V	H	I	N	Z					C				
ROL <i>opr</i> ROLA ROLX ROL <i>opr</i> ,X ROL ,X ROL <i>opr</i> ,SP	Rotate Left through Carry		†	-	-	†	†	†	DIR INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5				
ROR <i>opr</i> RORA RORX ROR <i>opr</i> ,X ROR ,X ROR <i>opr</i> ,SP			Rotate Right through Carry		†	-	-	†	†	†	DIR INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5		
RSP					Reset Stack Pointer	$SP \leftarrow \$FF$	-	-	-	-	-	INH	9C		1	
RTI					Return from Interrupt	$SP \leftarrow (SP) + 1$ ; Pull (CCR) $SP \leftarrow (SP) + 1$ ; Pull (A) $SP \leftarrow (SP) + 1$ ; Pull (X) $SP \leftarrow (SP) + 1$ ; Pull (PCH) $SP \leftarrow (SP) + 1$ ; Pull (PCL)	†	†	†	†	†	†	INH	80		7
RTS					Return from Subroutine	$SP \leftarrow SP + 1$ ; Pull (PCH) $SP \leftarrow SP + 1$ ; Pull (PCL)	-	-	-	-	-	-	INH	81		4
SBC # <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> ,X SBC <i>opr</i> ,X SBC ,X SBC <i>opr</i> ,SP SBC <i>opr</i> ,SP	Subtract with Carry	$A \leftarrow (A) - (M) - (C)$			†	-	-	†	†	†	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5		
SEC			Set Carry Bit	$C \leftarrow 1$	-	-	-	-	1	INH	99		1			
SEI			Set Interrupt Mask	$I \leftarrow 1$	-	-	1	-	-	INH	9B		2			
STA <i>opr</i> STA <i>opr</i> STA <i>opr</i> ,X STA <i>opr</i> ,X STA ,X STA <i>opr</i> ,SP STA <i>opr</i> ,SP			Store A in M	$M \leftarrow (A)$	0	-	-	†	†	-	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ff ee ff	3 4 4 3 2 4 5		
STHX <i>opr</i>					Store H:X in M	$(M:M + 1) \leftarrow (H:X)$	0	-	-	†	†	-	DIR	35	dd	4
STOP	Enable $\overline{IRQ}$ Pin; Stop Oscillator	$I \leftarrow 0$ ; Stop Oscillator			-	-	0	-	-	-	INH	8E		1		
STX <i>opr</i> STX <i>opr</i> STX <i>opr</i> ,X STX <i>opr</i> ,X STX ,X STX <i>opr</i> ,SP STX <i>opr</i> ,SP	Store X in M	$M \leftarrow (X)$			0	-	-	†	†	-	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ff ee ff	3 4 4 3 2 4 5		
SUB # <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> ,X SUB <i>opr</i> ,X SUB ,X SUB <i>opr</i> ,SP SUB <i>opr</i> ,SP					Subtract	$A \leftarrow (A) - (M)$	†	-	-	†	†	†	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5



**Table 6-1. Instruction Set Summary (Sheet 7 of 7)**

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles	
			V	H	I	N	Z					C
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) - 1; Push (PCH) SP ← (SP) - 1; Push (X) SP ← (SP) - 1; Push (A) SP ← (SP) - 1; Push (CCR) SP ← (SP) - 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	-	-	1	-	-	-	INH	83		9
TAP	Transfer A to CCR	CCR ← (A)	↑	↑	↑	↑	↑	↑	INH	84		2
TAX	Transfer A to X	X ← (A)	-	-	-	-	-	-	INH	97		1
TPA	Transfer CCR to A	A ← (CCR)	-	-	-	-	-	-	INH	85		1
TST <i>opr</i> TSTA TSTX TST <i>opr,X</i> TST ,X TST <i>opr,SP</i>	Test for Negative or Zero	(A) - \$00 or (X) - \$00 or (M) - \$00	0	-	-	↑	↑	-	DIR INH INH IX1 IX SP1	3D 4D 5D 6D 7D 9E6D	dd ff ff	3 1 1 3 2 4
TSX	Transfer SP to H:X	H:X ← (SP) + 1	-	-	-	-	-	-	INH	95		2
TXA	Transfer X to A	A ← (X)	-	-	-	-	-	-	INH	9F		1
TXS	Transfer H:X to SP	(SP) ← (H:X) - 1	-	-	-	-	-	-	INH	94		2

- |       |   |            |   |
|-------|---|------------|---|
| A     | Accumulator   | <i>n</i>   | Any bit                                     |
| C     | Carry/borrow bit  | <i>opr</i> | Operand (one or two bytes)                  |
| CCR   | Condition code register   | PC         | Program counter                             |
| dd    | Direct address of operand   | PCH        | Program counter high byte                   |
| dd rr | Direct address of operand and relative offset of branch instruction | PCL        | Program counter low byte                    |
| DD    | Direct to direct addressing mode                                    | REL        | Relative addressing mode                    |
| DIR   | Direct addressing mode  | <i>rel</i> | Relative program counter offset byte        |
| DIX+  | Direct to indexed with post increment addressing mode               | rr         | Relative program counter offset byte        |
| ee ff | High and low bytes of offset in indexed, 16-bit offset addressing   | SP1        | Stack pointer, 8-bit offset addressing mode |
| EXT   | Extended addressing mode  | SP2        | Stack pointer 16-bit offset addressing mode |
| ff    | Offset byte in indexed, 8-bit offset addressing                     | SP         | Stack pointer                               |
| H     | Half-carry bit  | U          | Undefined                                   |
| H     | Index register high byte  | V          | Overflow bit                                |
| hh ll | High and low bytes of operand address in extended addressing        | X          | Index register low byte                     |
| I     | Interrupt mask  | Z          | Zero bit                                    |
| ii    | Immediate operand byte  | &          | Logical AND                                 |
| IMD   | Immediate source to direct destination addressing mode              |            | Logical OR                                  |
| IMM   | Immediate addressing mode   | ⊕          | Logical EXCLUSIVE OR                        |
| INH   | Inherent addressing mode  | ()         | Contents of                                 |
| IX    | Indexed, no offset addressing mode                                  | -( )       | Negation (two's complement)                 |
| IX+   | Indexed, no offset, post increment addressing mode                  | #          | Immediate value                             |
| IX+D  | Indexed with post increment to direct addressing mode               | «          | Sign extend                                 |
| IX1   | Indexed, 8-bit offset addressing mode                               | ←          | Loaded with                                 |
| IX1+  | Indexed, 8-bit offset, post increment addressing mode               | ?          | If  |
| IX2   | Indexed, 16-bit offset addressing mode                              | :          | Concatenated with                           |
| M     | Memory location   | ↑          | Set or cleared                              |
| N     | Negative bit  | —          | Not affected                                |

## 6.9 Opcode Map

The opcode map is provided in [Table 6-2](#).

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

**Table 6-2. Opcode Map**

MSB LSB	Bit Manipulation		Branch	Read-Modify-Write						Control		Register/Memory							
	DIR	DIR	REL	DIR	INH	INH	IX1	SP1	IX	INH	INH	IMM	DIR	EXT	IX2	SP2	IX1	SP1	IX
	0	1	2	3	4	5	6	9E6	7	8	9	A	B	C	D	9ED	E	9EE	F
0	BRSET0 3 DIR	BSET0 2 DIR	BRA 2 REL	NEG 2 DIR	NEGA 1 INH	NEGX 1 INH	NEG 2 IX1	NEG 3 SP1	NEG 1 IX	RTI 1 INH	BGE 2 REL	SUB 2 IMM	SUB 2 DIR	SUB 3 EXT	SUB 3 IX2	SUB 4 SP2	SUB 2 IX1	SUB 3 SP1	SUB 1 IX
1	BRCLR0 3 DIR	BCLR0 2 DIR	BRN 2 REL	CBEQ 3 DIR	CBEQA 3 IMM	CBEQX 3 IMM	CBEQ 3 IX1+	CBEQ 4 SP1	CBEQ 2 IX+	RTS 1 INH	BLT 2 REL	CMP 2 IMM	CMP 2 DIR	CMP 3 EXT	CMP 3 IX2	CMP 4 SP2	CMP 2 IX1	CMP 3 SP1	CMP 1 IX
2	BRSET1 3 DIR	BSET1 2 DIR	BHI 2 REL		MUL 1 INH	DIV 1 INH	NSA 1 INH		DAA 1 INH		BGT 2 REL	SBC 2 IMM	SBC 2 DIR	SBC 3 EXT	SBC 3 IX2	SBC 4 SP2	SBC 2 IX1	SBC 3 SP1	SBC 1 IX
3	BRCLR1 3 DIR	BCLR1 2 DIR	BLS 2 REL	COM 2 DIR	COMA 1 INH	COMX 1 INH	COM 2 IX1	COM 3 SP1	COM 1 IX	SWI 1 INH	BLE 2 REL	CPX 2 IMM	CPX 2 DIR	CPX 3 EXT	CPX 3 IX2	CPX 4 SP2	CPX 2 IX1	CPX 3 SP1	CPX 1 IX
4	BRSET2 3 DIR	BSET2 2 DIR	BCC 2 REL	LSR 2 DIR	LSRA 1 INH	LSRX 1 INH	LSR 2 IX1	LSR 3 SP1	LSR 1 IX	TAP 1 INH	TXS 1 INH	AND 2 IMM	AND 2 DIR	AND 3 EXT	AND 3 IX2	AND 4 SP2	AND 2 IX1	AND 3 SP1	AND 1 IX
5	BRCLR2 3 DIR	BCLR2 2 DIR	BCS 2 REL	STHX 2 DIR	LDHX 3 IMM	LDHX 2 DIR	CPHX 3 IMM		CPHX 2 DIR	TPA 1 INH	TSX 2 INH	BIT 2 IMM	BIT 2 DIR	BIT 3 EXT	BIT 3 IX2	BIT 4 SP2	BIT 2 IX1	BIT 3 SP1	BIT 1 IX
6	BRSET3 3 DIR	BSET3 2 DIR	BNE 2 REL	ROR 2 DIR	RORA 1 INH	RORX 1 INH	ROR 2 IX1	ROR 3 SP1	ROR 1 IX	PULA 1 INH		LDA 2 IMM	LDA 2 DIR	LDA 3 EXT	LDA 3 IX2	LDA 4 SP2	LDA 2 IX1	LDA 3 SP1	LDA 1 IX
7	BRCLR3 3 DIR	BCLR3 2 DIR	BEQ 2 REL	ASR 2 DIR	ASRA 1 INH	ASRX 1 INH	ASR 2 IX1	ASR 3 SP1	ASR 1 IX	PSHA 1 INH	TAX 1 INH	AIS 2 IMM	STA 2 DIR	STA 3 EXT	STA 3 IX2	STA 4 SP2	STA 2 IX1	STA 3 SP1	STA 1 IX
8	BRSET4 3 DIR	BSET4 2 DIR	BHCC 2 REL	LSL 2 DIR	LSLA 1 INH	LSLX 1 INH	LSL 2 IX1	LSL 3 SP1	LSL 1 IX	PULX 1 INH	CLC 1 INH	EOR 2 IMM	EOR 2 DIR	EOR 3 EXT	EOR 3 IX2	EOR 4 SP2	EOR 2 IX1	EOR 3 SP1	EOR 1 IX
9	BRCLR4 3 DIR	BCLR4 2 DIR	BHCS 2 REL	ROL 2 DIR	ROLA 1 INH	ROLX 1 INH	ROL 2 IX1	ROL 3 SP1	ROL 1 IX	PSHX 1 INH	SEC 1 INH	ADC 2 IMM	ADC 2 DIR	ADC 3 EXT	ADC 3 IX2	ADC 4 SP2	ADC 2 IX1	ADC 3 SP1	ADC 1 IX
A	BRSET5 3 DIR	BSET5 2 DIR	BPL 2 REL	DEC 2 DIR	DECA 1 INH	DECX 1 INH	DEC 2 IX1	DEC 3 SP1	DEC 1 IX	PULH 1 INH	CLI 1 INH	ORA 2 IMM	ORA 2 DIR	ORA 3 EXT	ORA 3 IX2	ORA 4 SP2	ORA 2 IX1	ORA 3 SP1	ORA 1 IX
B	BRCLR5 3 DIR	BCLR5 2 DIR	BMI 2 REL	DBNZ 3 DIR	DBNZA 2 INH	DBNZX 2 INH	DBNZ 3 IX1	DBNZ 4 SP1	DBNZ 2 IX	PSHH 1 INH	SEI 1 INH	ADD 2 IMM	ADD 2 DIR	ADD 3 EXT	ADD 3 IX2	ADD 4 SP2	ADD 2 IX1	ADD 3 SP1	ADD 1 IX
C	BRSET6 3 DIR	BSET6 2 DIR	BMC 2 REL	INC 2 DIR	INCA 1 INH	INCX 1 INH	INC 2 IX1	INC 3 SP1	INC 1 IX	CLRH 1 INH	RSP 1 INH		JMP 2 DIR	JMP 3 EXT	JMP 3 IX2		JMP 2 IX1		JMP 1 IX
D	BRCLR6 3 DIR	BCLR6 2 DIR	BMS 2 REL	TST 2 DIR	TSTA 1 INH	TSTX 1 INH	TST 2 IX1	TST 3 SP1	TST 1 IX		NOP 1 INH	BSR 2 REL	JSR 2 DIR	JSR 3 EXT	JSR 3 IX2		JSR 2 IX1		JSR 1 IX
E	BRSET7 3 DIR	BSET7 2 DIR	BIL 2 REL		MOV 3 DD	MOV 2 DIX+	MOV 3 IMD		MOV 2 IX+D	STOP 1 INH	*	LDX 2 IMM	LDX 2 DIR	LDX 3 EXT	LDX 3 IX2	LDX 4 SP2	LDX 2 IX1	LDX 3 SP1	LDX 1 IX
F	BRCLR7 3 DIR	BCLR7 2 DIR	BIH 2 REL	CLR 2 DIR	CLRA 1 INH	CLRX 1 INH	CLR 2 IX1	CLR 3 SP1	CLR 1 IX	WAIT 1 INH	TXA 1 INH	AIX 2 IMM	STX 2 DIR	STX 3 EXT	STX 3 IX2	STX 4 SP2	STX 2 IX1	STX 3 SP1	STX 1 IX

INH Inherent  
 IMM Immediate  
 DIR Direct  
 EXT Extended  
 DD Direct-Direct  
 IX+D Indexed-Direct  
 REL Relative  
 IX Indexed, No Offset  
 IX1 Indexed, 8-Bit Offset  
 IX2 Indexed, 16-Bit Offset  
 IMM Immediate-Direct  
 DIX+ Direct-Indexed  
 SP1 Stack Pointer, 8-Bit Offset  
 SP2 Stack Pointer, 16-Bit Offset  
 IX+ Indexed, No Offset with Post Increment  
 IX1+ Indexed, 1-Byte Offset with Post Increment

Low Byte of Opcode in Hexadecimal

MSB	0	High Byte of Opcode in Hexadecimal
LSB	5 BRSET0 3 DIR	Cycles Opcode Mnemonic Number of Bytes / Addressing Mode
0		

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## Section 7. System Integration Module (SIM)

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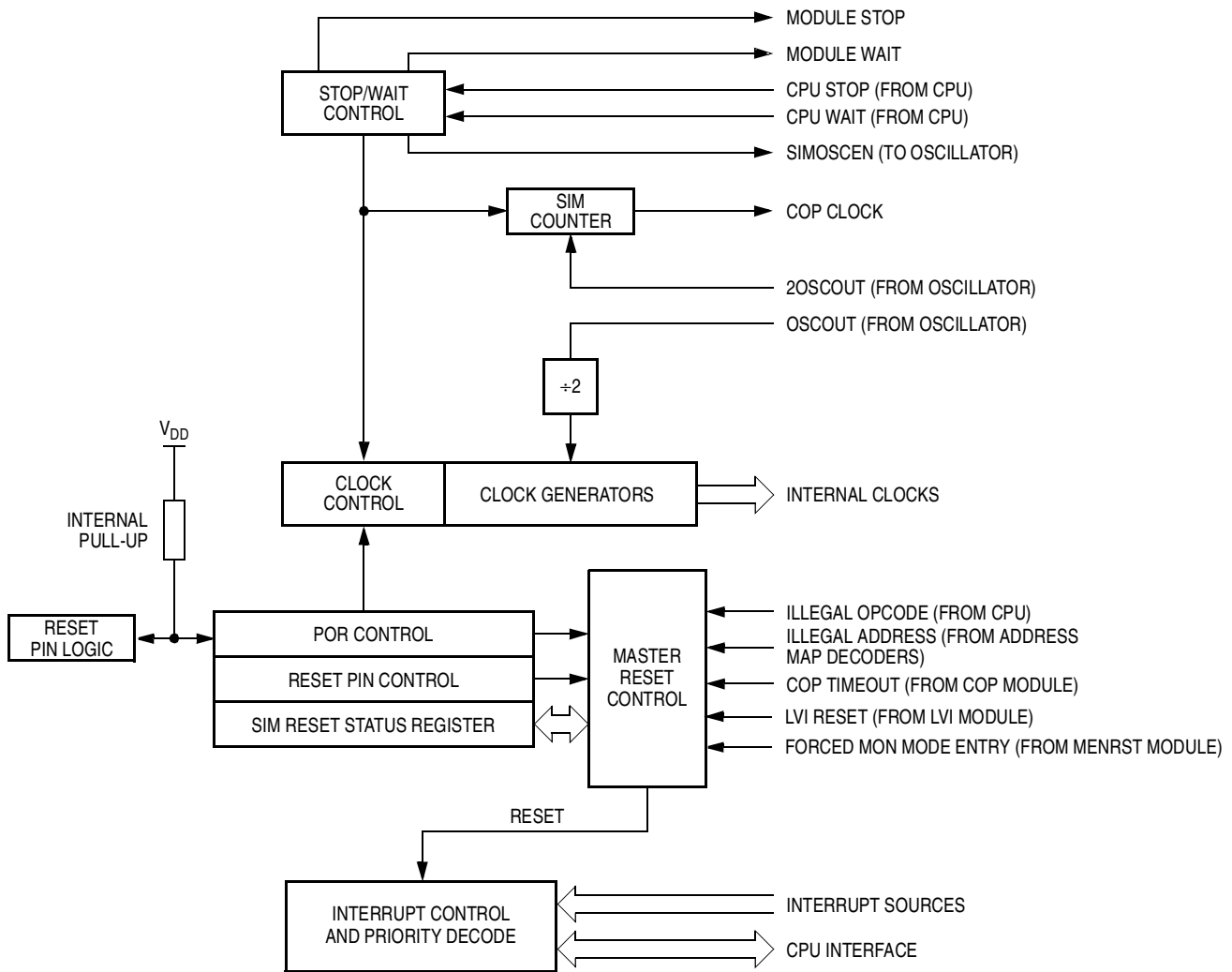
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## 7.2 Introduction

This section describes the system integration module (SIM), which supports up to 24 external and/or internal interrupts. Together with the central processor unit (CPU), the SIM controls all microcontroller unit (MCU) activities. A block diagram of the SIM is shown in **Figure 7-1**. **Figure 7-2** is a summary of the SIM I/O registers. The SIM is a system state controller that coordinates CPU and exception timing.

The SIM is responsible for:

- Bus clock generation and control for CPU and peripherals
  - Stop/wait/reset/break entry and recovery
  - Internal clock control
- Master reset control, including power-on reset (POR) and computer operating properly (COP) timeout
- Interrupt control:
  - Acknowledge timing
  - Arbitration control timing
  - Vector address generation
- CPU enable/disable timing
- Modular architecture expandable to 128 interrupt sources




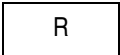
**Figure 7-1. SIM Block Diagram**

**Table 7-1. Signal Name Conventions**

Signal Name	Description
2OSCOU	Buffered clock from the internal, RC or XTAL oscillator circuit.
OSCOU	The 2OSCOU frequency divided by two. This signal is again divided by two in the SIM to generate the internal bus clocks (bus clock = 2OSCOU ÷ 4).
IAB	Internal address bus
IDB	Internal data bus
PORRST	Signal from the power-on reset module to the SIM
IRST	Internal reset signal
R/W	Read/write signal

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# System Integration Module (SIM)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0	
\$FE00	Break Status Register (BSR) <a href="#">See page 97.</a>	Read:	R	R	R	R	R	R	SBSW	R	
		Write:								Note 1	
		Reset:	0	0	0	0	0	0	0	0	0
1. Writing a logic 0 clears SBSW.											
\$FE01	SIM Reset Status Register (SRSR) <a href="#">See page 98.</a>	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0	
		Write:									
		POR:	1	0	0	0	0	0	0	0	0
\$FE02	Reserved		R	R	R	R	R	R	R	R	
\$FE03	Break Flag Control Register (BFCR) <a href="#">See page 99.</a>	Read:	BCFE	R	R	R	R	R	R	R	
		Write:									
		Reset:	0								
\$FE04	Interrupt Status Register 1 (INT1) <a href="#">See page 91.</a>	Read:	0	IF5	IF4	IF3	0	IF1	0	0	
		Write:	R	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0	0
\$FE05	Interrupt Status Register 2 (INT2) <a href="#">See page 91.</a>	Read:	IF14	0	0	0	0	0	0	0	
		Write:	R	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0	0
\$FE06	Interrupt Status Register 3 (INT3) <a href="#">See page 92.</a>	Read:	0	0	0	0	0	0	0	IF15	
		Write:	R	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0	0
				= Unimplemented				= Reserved			

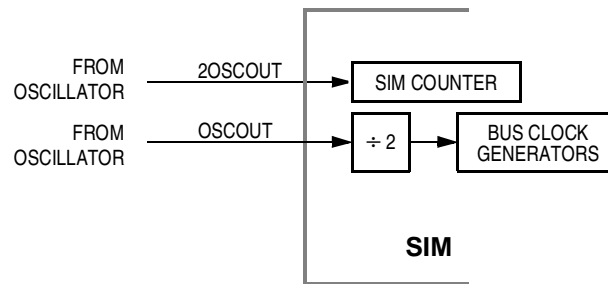
**Figure 7-2. SIM I/O Register Summary**

### 7.3 $\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ Pins initialization

$\overline{\text{RST}}$  and  $\overline{\text{IRQ}}$  pins come out of reset as PTA3 and PTA2 respectively.  $\overline{\text{RST}}$  and  $\overline{\text{IRQ}}$  functions can be activated by programming CONFIG2 accordingly. Refer to [Section 5. Configuration Register \(CONFIG\)](#).

### 7.4 SIM Bus Clock Control and Generation

The bus clock generator provides system clock signals for the CPU and peripherals on the MCU. The system clocks are generated from an incoming clock, OSCOUT, as shown in [Figure 7-3](#).



**Figure 7-3. SIM Clock Signals**

#### 7.4.1 Bus Timing

In user mode, the internal bus frequency is the oscillator frequency (20SCOUT) divided by four.

#### 7.4.2 Clock Start-Up from POR

When the power-on reset module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 20SCOUT cycle POR time out has completed. The  $\overline{\text{RST}}$  pin is driven low by the SIM during this entire period. The IBUS clocks start upon completion of the time out.

### 7.4.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt, break, or reset, the SIM allows 2OSCOU to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay time out. This time out is selectable as 4096 or 32 2OSCOU cycles. See [7.8.2 Stop Mode](#).

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

## 7.5 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ( $\overline{RST}$ )
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector \$FFFE–FFFF (\$FEFE–FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see [7.6 SIM Counter](#)), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). See [7.9 SIM Registers](#).

### 7.5.1 External Pin Reset

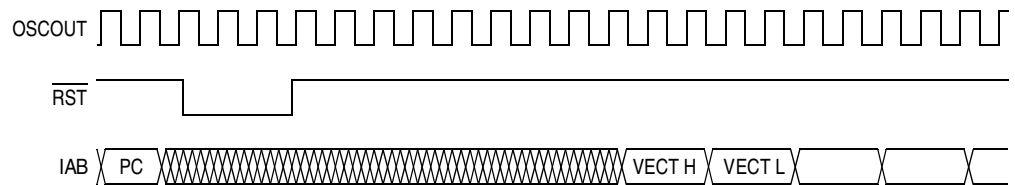
The  $\overline{RST}$  pin circuits include an internal pullup device. Pulling the asynchronous  $\overline{RST}$  pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as  $\overline{RST}$  is held low for a



minimum of 67 2OSCCLK cycles, assuming that the POR was not the source of the reset. See [Table 7-2](#) for details. [Figure 7-4](#) shows the relative timing.

**Table 7-2. PIN Bit Set Timing**

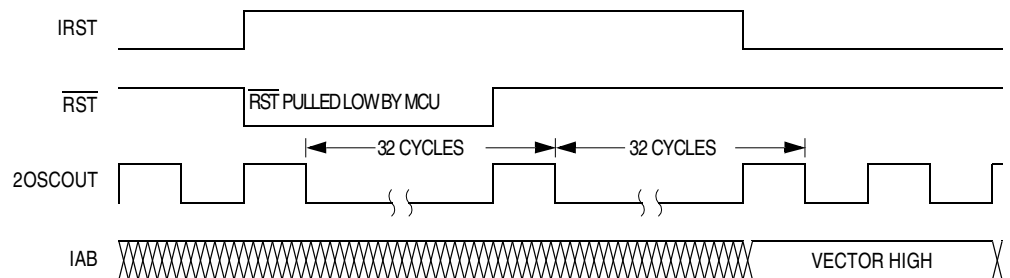
Reset Type	Number of Cycles Required to Set PIN
POR	4163 (4096 + 64 + 3)
All others	67 (64 + 3)



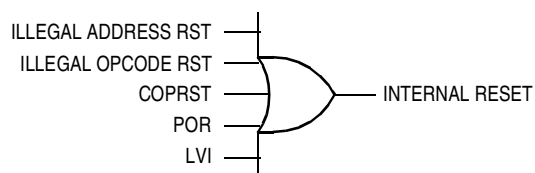
**Figure 7-4. External Reset Timing**

### 7.5.2 Active Resets from Internal Sources

All internal reset sources actively pull the  $\overline{\text{RST}}$  pin low for 32 2OSCCLK cycles to allow resetting of external peripherals. The internal reset signal IRST continues to be asserted for an additional 32 cycles (see [Figure 7-5](#)). An internal reset can be caused by an illegal address, illegal opcode, COP time out, LVI, or POR (see [Figure 7-6](#)).



**Figure 7-5. Internal Reset Timing**



**Figure 7-6. Sources of Internal Reset**

**NOTE:** For POR resets, the SIM cycles through 4096 2OSCOU $T$  cycles during which the SIM forces the  $\overline{RST}$  pin low. The internal reset signal then follows the sequence from the falling edge of  $\overline{RST}$  shown in [Figure 7-5](#).

The COP reset is asynchronous to the bus clock.

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

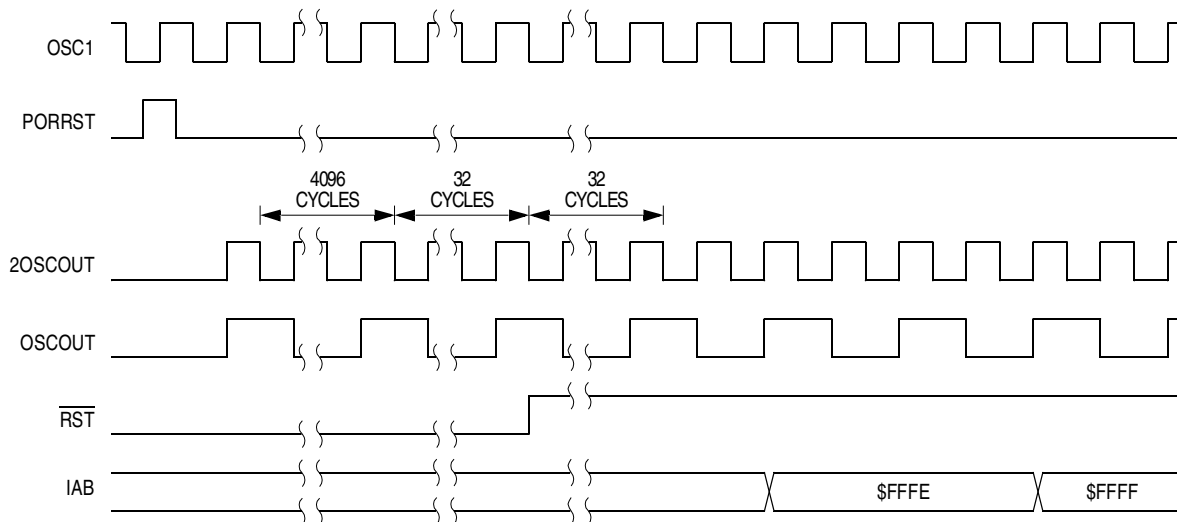
### 7.5.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power on has occurred. The external reset pin ( $\overline{RST}$ ) is held low while the SIM counter counts out 4096 2OSCOU $T$  cycles. Sixty-four 2OSCOU $T$  cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power on, the following events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables the oscillator to drive 2OSCOU $T$ .
- Internal clocks to the CPU and modules are held inactive for 4096 2OSCOU $T$  cycles to allow stabilization of the oscillator.
- The  $\overline{RST}$  pin is driven low during the oscillator stabilization time.
- The POR bit of the SIM reset status register (SRSR) is set and all other bits in the register are cleared.

See [Figure 7-7](#).



**Figure 7-7. POR Recovery**

### 7.5.2.2 Computer Operating Properly (COP) Reset

An input to the SIM is reserved for the COP reset signal. The overflow of the COP counter causes an internal reset and sets the COP bit in the SIM reset status register (SRSR). The SIM actively pulls down the  $\overline{\text{RST}}$  pin for all internal reset sources.

To prevent a COP module time out, write any value to location \$FFFF. Writing to location \$FFFF clears the COP counter and stages 12–5 of the SIM counter. The SIM counter output, which occurs at least every  $(2^{12} - 2^4)$  2OSCOU cycles, drives the COP counter. The COP should be serviced as soon as possible out of reset to guarantee the maximum amount of time before the first time out.

The COP module is disabled during a break interrupt with monitor mode when BDCOP bit is set in break auxiliary register (BRKAR).

### 7.5.2.3 Illegal Opcode Reset

The SIM decodes signals from the CPU to detect illegal instructions. An illegal instruction sets the ILOP bit in the SIM reset status register (SRSR) and causes a reset.

If the stop enable bit, STOP, in the mask option register is logic 0, the SIM treats the STOP instruction as an illegal opcode and causes an illegal opcode reset. The SIM actively pulls down the  $\overline{\text{RST}}$  pin for all internal reset sources.

### 7.5.2.4 Illegal Address Reset

An opcode fetch from an unmapped address generates an illegal address reset. The SIM verifies that the CPU is fetching an opcode prior to asserting the ILAD bit in the SIM reset status register (SRSR) and resetting the MCU. A data fetch from an unmapped address does not generate a reset. The SIM actively pulls down the  $\overline{\text{RST}}$  pin for all internal reset sources.

### 7.5.2.5 Low-Voltage Inhibit (LVI) Reset

The LVI asserts its output to the SIM when the  $V_{DD}$  voltage falls to the LVI trip voltage  $V_{\text{Trip}}$ . The LVI bit in the SIM reset status register (SRSR) is set, and the external reset pin ( $\overline{\text{RST}}$ ) is held low while the SIM counter counts out 4096 2OSCCLK cycles. Sixty-four 2OSCOOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur. The SIM actively pulls down the ( $\overline{\text{RST}}$ ) pin for all internal reset sources.

## 7.6 SIM Counter

The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter uses 12 stages for counting, followed by a 13th stage that triggers a reset of SIM counters and supplies the clock for the COP module. The SIM counter is clocked by the falling edge of 2OSCOU.

### 7.6.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the oscillator to drive the bus clock state machine.

### 7.6.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt, break, or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the configuration register 1 (CONFIG1). If the SSREC bit is a logic 1, then the stop recovery is reduced from the normal delay of 4096 2OSCOU cycles down to 32 2OSCOU cycles. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode. External crystal applications should use the full stop recovery time, that is, with SSREC cleared in the configuration register 1 (CONFIG1).

### 7.6.3 SIM Counter and Reset States

External reset has no effect on the SIM counter (see [7.8.2 Stop Mode](#) for details.) The SIM counter is free-running after all reset states. See [7.5.2 Active Resets from Internal Sources](#) for counter control and internal reset recovery sequences.

### 7.7 Exception Control

Normal sequential program execution can be changed in three different ways:

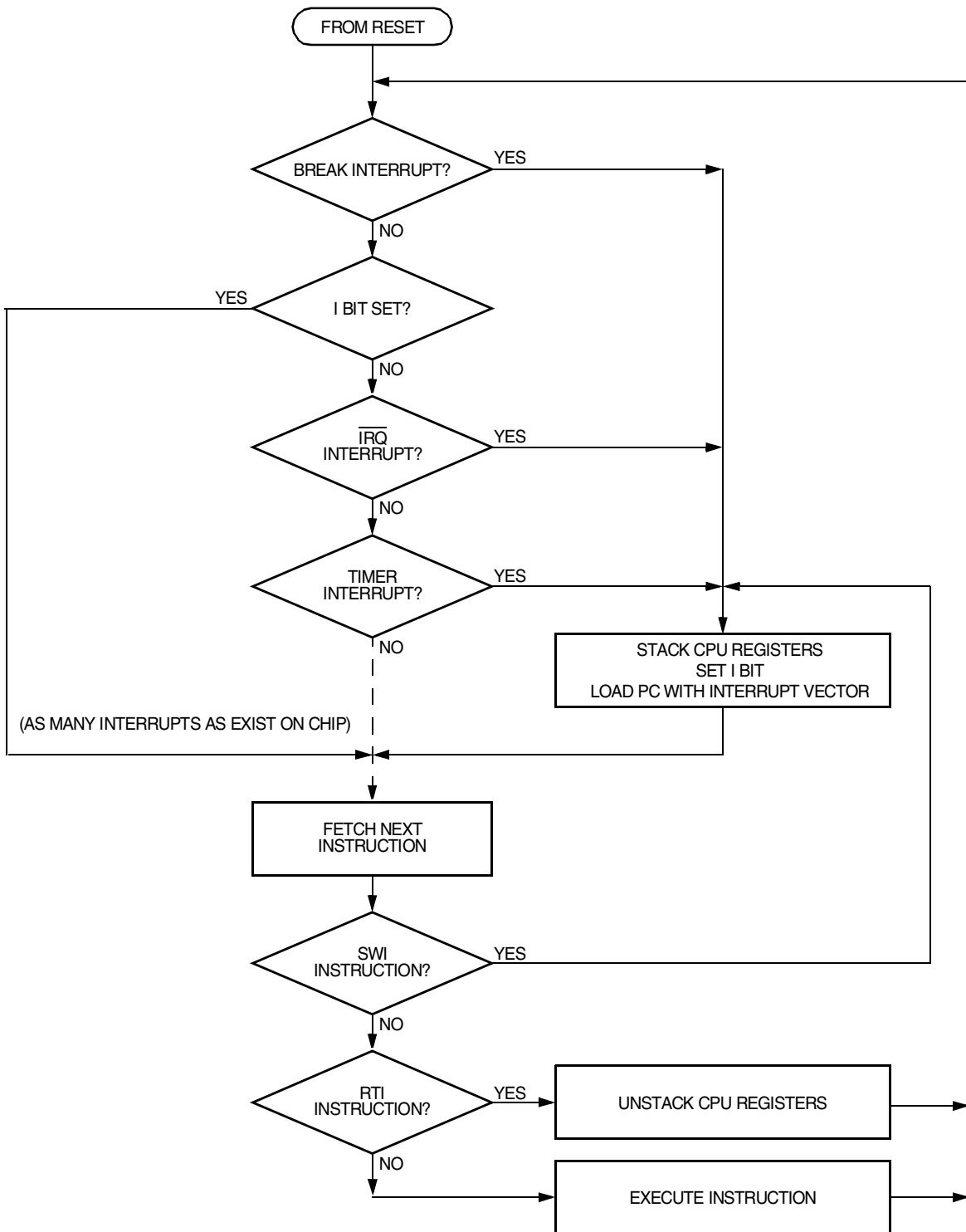
1. Interrupts
  - a. Maskable hardware CPU interrupts
  - b. Non-maskable software interrupt instruction (SWI)
2. Reset
3. Break interrupts

#### 7.7.1 Interrupts

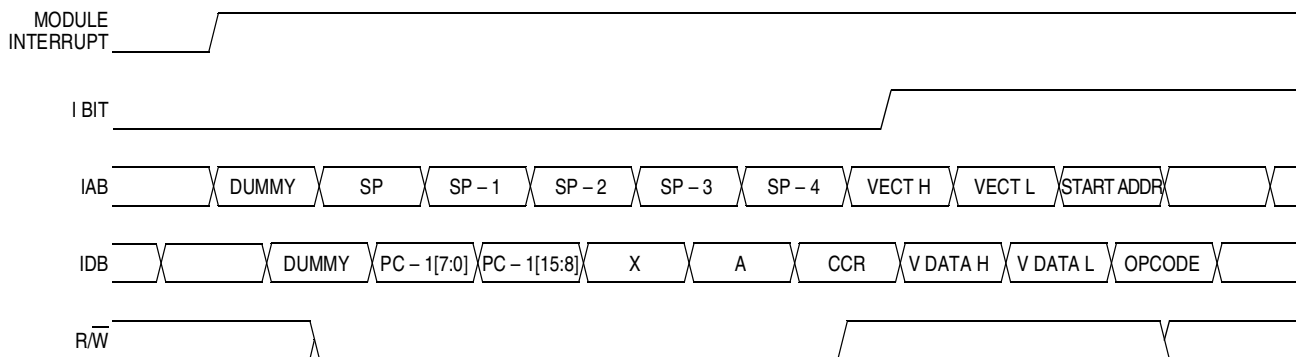
An interrupt temporarily changes the sequence of program execution to respond to a particular event. [Figure 7-8](#) flow charts the handling of system interrupts.

Interrupts are latched, and arbitration is performed in the SIM at the start of interrupt processing. The arbitration result is a constant that the CPU uses to determine which vector to fetch. Once an interrupt is latched by the SIM, no other interrupt can take precedence, regardless of priority, until the latched interrupt is serviced (or the I bit is cleared).

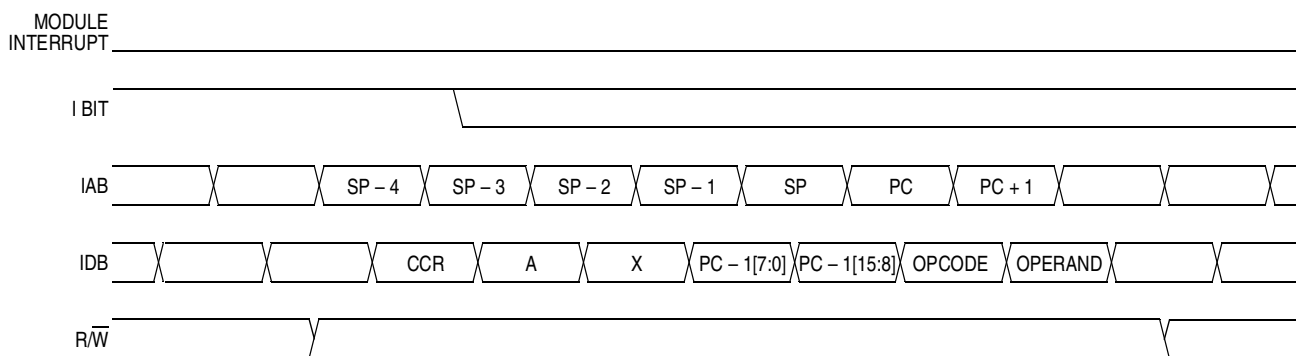
At the beginning of an interrupt, the CPU saves the CPU register contents on the stack and sets the interrupt mask (I bit) to prevent additional interrupts. At the end of an interrupt, the RTI instruction recovers the CPU register contents from the stack so that normal processing can resume. [Figure 7-9](#) shows interrupt entry timing. [Figure 7-10](#) shows interrupt recovery timing.



**Figure 7-8. Interrupt Processing**



**Figure 7-9. Interrupt Entry**



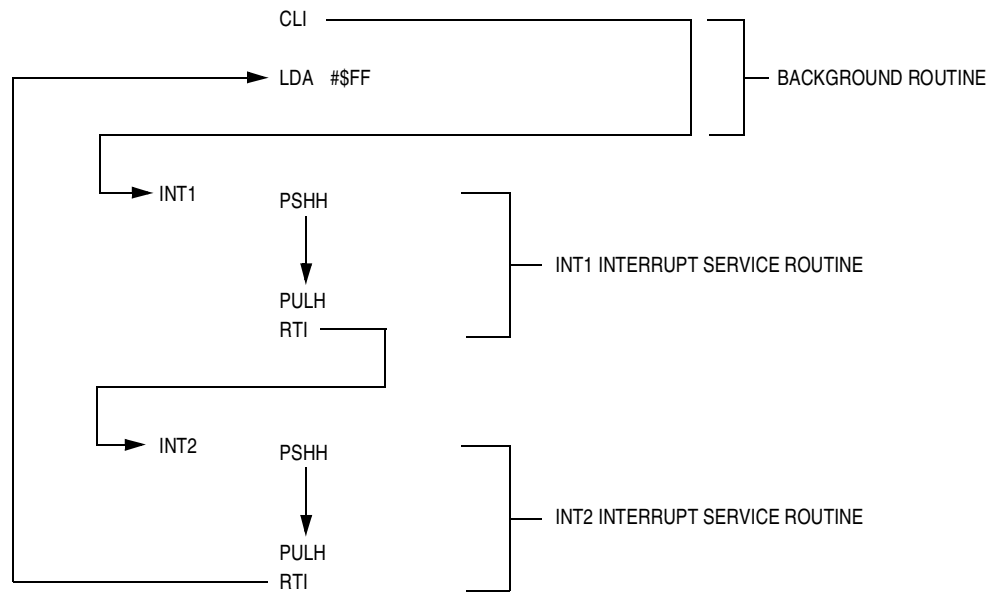
**Figure 7-10. Interrupt Recovery**

### 7.7.1.1 Hardware Interrupts

A hardware interrupt does not stop the current instruction. Processing of a hardware interrupt begins after completion of the current instruction. When the current instruction is complete, the SIM checks all pending hardware interrupts. If interrupts are not masked (I bit clear in the condition code register), and if the corresponding interrupt enable bit is set, the SIM proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

If more than one interrupt is pending at the end of an instruction execution, the highest priority interrupt is serviced first. [Figure 7-11](#) demonstrates what happens when two interrupts are pending. If an interrupt is pending upon exit from the original interrupt service routine, the pending interrupt is serviced before the LDA instruction is executed.





**Figure 7-11. Interrupt Recognition Example**

The LDA opcode is prefetched by both the INT1 and INT2 return-from-interrupt (RTI) instructions. However, in the case of the INT1 RTI prefetch, this is a redundant operation.

**NOTE:** *To maintain compatibility with the M6805 Family, the H register is not pushed on the stack during interrupt entry. If the interrupt service routine modifies the H register or uses the indexed addressing mode, software should save the H register and then restore it prior to exiting the routine.*

### 7.7.1.2 SWI Instruction


The SWI instruction is a non-maskable instruction that causes an interrupt regardless of the state of the interrupt mask (I bit) in the condition code register.

**NOTE:** *A software interrupt pushes PC onto the stack. A software interrupt does **not** push PC – 1, as a hardware interrupt does.*

## 7.7.2 Interrupt Status Registers

The flags in the interrupt status registers identify maskable interrupt sources. **Table 7-3** summarizes the interrupt sources and the interrupt status register flags that they set. The interrupt status registers can be useful for debugging.

**Table 7-3. Interrupt Sources**

Priority	Source	Flag	Mask <sup>(1)</sup>	INT Register Flag	Vector Address
Highest  Lowest	Reset	—	—	—	\$FFFE–\$FFFF
	SWI instruction	—	—	—	\$FFFC–\$FFFD
	$\overline{\text{IRQ}}$ pin	IRQF1	IMASK1	IF1	\$FFFA–\$FFFB
	Timer channel 0 interrupt	CH0F	CH0IE	IF3	\$FFF6–\$FFF7
	Timer channel 1 interrupt	CH1F	CH1IE	IF4	\$FFF4–\$FFF5
	Timer overflow interrupt	TOF	TOIE	IF5	\$FFF2–\$FFF3
	Keyboard interrupt	KEYF	IMASKK	IF14	\$FFDE–\$FFDF
	ADC conversion complete interrupt	COCO	AIEN	IF15	\$FFE0–\$FFE1

1. The I bit in the condition code register is a global mask for all interrupt sources except the SWI instruction.

### 7.7.2.1 Interrupt Status Register 1

Address: \$FE04

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	IF5	IF4	IF3	0	IF1	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 7-12. Interrupt Status Register 1 (INT1)**

#### IF1 and IF3–IF5 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 7-3](#).

1 = Interrupt request present

0 = No interrupt request present

Bit 0, 1, 3, and 7 — Always read 0

### 7.7.2.2 Interrupt Status Register 2

Address: \$FE05

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IF14	0	0	0	0	0	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 7-13. Interrupt Status Register 2 (INT2)**

#### IF14 — Interrupt Flags

This flag indicates the presence of interrupt requests from the sources shown in [Table 7-3](#).

1 = Interrupt request present

0 = No interrupt request present

Bit 0–6 — Always read 0

## 7.7.2.3 Interrupt Status Register 3

Address: \$FE06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	IF15
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

**Figure 7-14. Interrupt Status Register 3 (INT3)**

### IF15 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 7-3](#).

1 = Interrupt request present

0 = No interrupt request present

Bit 1–7 — Always read 0

## 7.7.3 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

## 7.7.4 Break Interrupts

The break module can stop normal program flow at a software programmable break point by asserting its break interrupt output. (See [Section 17. Break Module \(BREAK\)](#).) The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

### 7.7.5 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

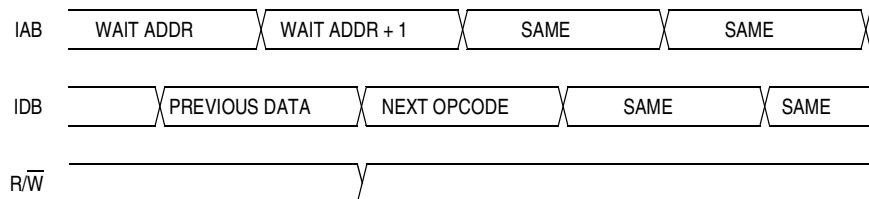
Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a two-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

## 7.8 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described below. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

### 7.8.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. [Figure 7-15](#) shows the timing for wait mode entry.



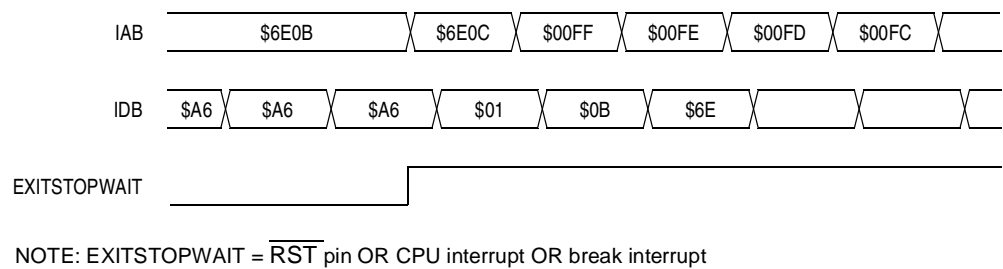
NOTE: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

**Figure 7-15. Wait Mode Entry Timing**

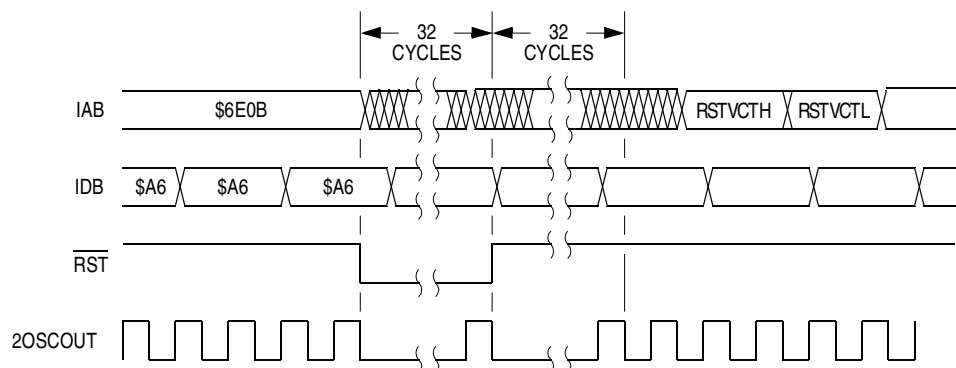
A module that is active during wait mode can wake up the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

Wait mode can also be exited by a reset or break. A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the break status register (BSR). If the COP disable bit, COPD, in the configuration register is logic 0, then the computer operating properly module (COP) is enabled and remains active in wait mode.

**Figure 7-16** and **Figure 7-17** show the timing for wait recovery.



**Figure 7-16. Wait Recovery from Interrupt or Break**



**Figure 7-17. Wait Recovery from Internal Reset**

## 7.8.2 Stop Mode

In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset or break also causes an exit from stop mode.

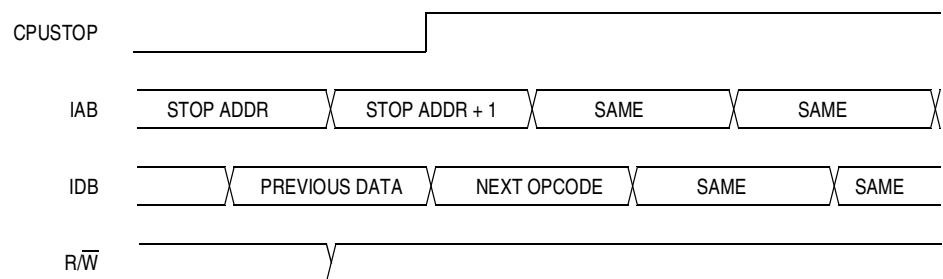
The SIM disables the oscillator signals (OSCOOUT and 2OSCOOUT) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the configuration register 1 (CONFIG1). If SSREC is set, stop recovery is reduced from the normal delay of 4096 2OSCOOUT cycles down to 32. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode.

**NOTE:** *External crystal applications should use the full stop recovery time by clearing the SSREC bit.*

A break interrupt during stop mode sets the SIM break stop/wait bit (SBSW) in the break status register (BSR).

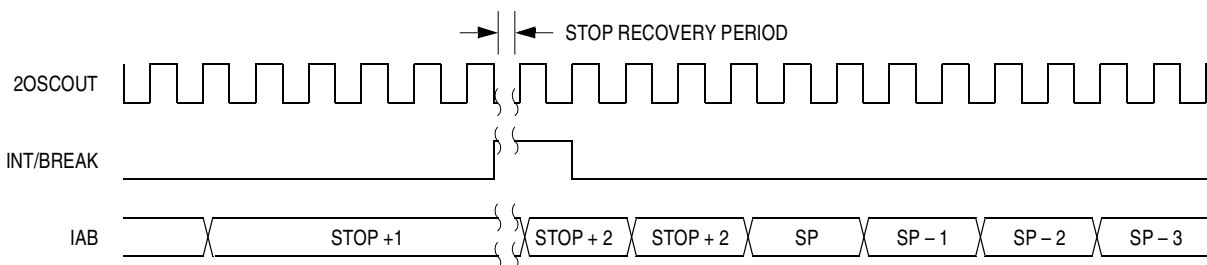
The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. [Figure 7-18](#) shows stop mode entry timing and [Figure 7-19](#) shows the stop mode recovery time from interrupt or break

**NOTE:** *To minimize stop current, all pins configured as inputs should be driven to a logic 1 or logic 0.*



NOTE: Previous data can be operand data or the STOP opcode, depending on the last instruction.

**Figure 7-18. Stop Mode Entry Timing**



**Figure 7-19. Stop Mode Recovery from Interrupt or Break**

## 7.9 SIM Registers

The SIM has three memory mapped registers. [Table 7-4](#) shows the mapping of these registers.

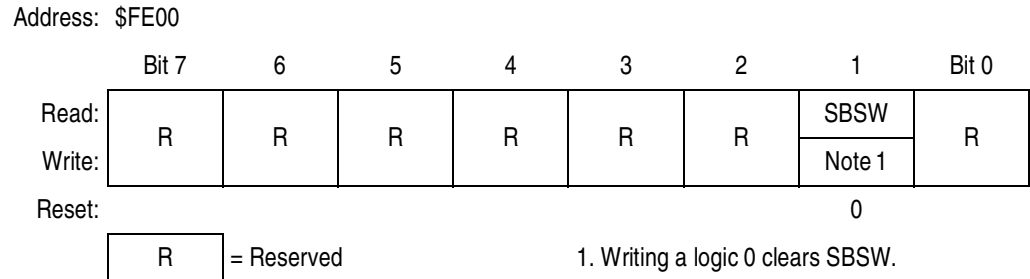
**Table 7-4. SIM Registers**

Address	Register	Access Mode
\$FE00	BSR	User
\$FE01	SRSR	User
\$FE03	BFCR	User



### 7.9.1 Break Status Register

The break status register (BSR) contains a flag to indicate that a break caused an exit from stop or wait mode.



**Figure 7-20. Break Status Register (BSR)**

#### SBSW — SIM Break Stop/Wait

This status bit is useful in applications requiring a return to wait or stop mode after exiting from a break interrupt. Clear SBSW by writing a logic 0 to it. Reset clears SBSW.

1 = Stop mode or wait mode was exited by break interrupt

0 = Stop mode or wait mode was not exited by break interrupt

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it. The following code is an example of this. Writing 0 to the SBSW bit clears it.

```

;This code works if the H register has been pushed onto the stack in the break
;service routine software. This code should be executed at the end of the break
;service routine software.
HIBYTE EQU 5
LOBYTE EQU 6
; If not SBSW, do RTI
BRCLR SBSW,BSR, RETURN ;See if wait mode or stop mode was exited by
;break.
TST LOBYTE,SP ;If RETURNLO is not zero,
BNE DOLO ;then just decrement low byte.
DEC HIBYTE,SP ;Else deal with high byte, too.
DOLO DEC LOBYTE,SP ;Point to WAIT/STOP opcode.
RETURN PULH ;Restore H register.
RTI


```

## 7.9.2 SIM Reset Status Register

This register contains seven flags that show the source of the last reset. Clear the SIM reset status register by reading it. A power-on reset sets the POR bit and clears all other bits in the register.

Address: \$FE01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
Write:								
POR:	1	0	0	0	0	0	0	0

 = Unimplemented

**Figure 7-21. SIM Reset Status Register (SRSR)**

**POR** — Power-On Reset Bit

- 1 = Last reset caused by POR circuit
- 0 = Read of SRSR

**PIN** — External Reset Bit

- 1 = Last reset caused by external reset pin ( $\overline{RST}$ )
- 0 = POR or read of SRSR

**COP** — Computer Operating Properly Reset Bit

- 1 = Last reset caused by COP counter
- 0 = POR or read of SRSR

**ILOP** — Illegal Opcode Reset Bit

- 1 = Last reset caused by an illegal opcode
- 0 = POR or read of SRSR

**ILAD** — Illegal Address Reset Bit (opcode fetches only)

- 1 = Last reset caused by an opcode fetch from an illegal address
- 0 = POR or read of SRSR

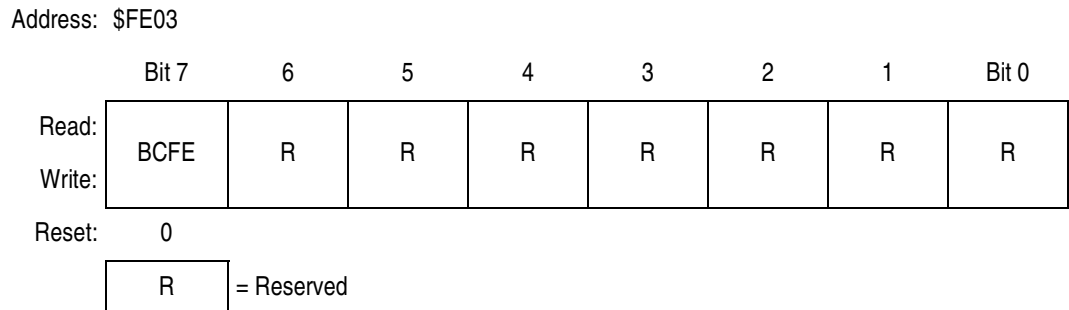
**MODRST** — Monitor Mode Entry Module Reset bit

- 1 = Last reset caused by monitor mode entry when vector locations \$FFFE and \$FFFF are \$FF after POR while  $IRQB = V_{DD}$
- 0 = POR or read of SRSR

LVI — Low Voltage Inhibit Reset bit  
 1 = Last reset caused by LVI circuit  
 0 = POR or read of SRSR

### 7.9.3 Break Flag Control Register

The break control register (BFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.



**Figure 7-22. Break Flag Control Register (BFCR)**

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

- 1 = Status bits clearable during break
- 0 = Status bits not clearable during break



## Section 8. Oscillator Module (OSC)

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### 8.2 Introduction

The oscillator module is used to provide a stable clock source for the microcontroller system and bus. The oscillator module generates two output clocks, OSCOUT and 2OSCOUT. The 2OSCOUT clock is used by the system integration module (SIM) and the computer operating properly module (COP). The OSCOUT clock is divided by two in the SIM to be used as the bus clock for the microcontroller. Therefore the bus frequency will be one fourth of the 2OSCOUT frequency.

### 8.3 Features

The oscillator has these four clock source options available:

1. Internal oscillator: An internally generated, fixed frequency clock, trimmable to  $\pm 5\%$ . This is the default option out of reset.
2. External oscillator: An external clock that can be driven directly into OSC1.
3. External RC: A built-in oscillator module (RC oscillator) that requires an external R connection only. The capacitor will be internal to the chip.
4. External crystal: A built-in oscillator module (XTAL oscillator) that requires an external crystal or ceramic-resonator.

### 8.4 Functional Description

The oscillator contains these major subsystems:

- Internal oscillator circuit
- Internal or external clock switch control
- External clock circuit
- External crystal circuit
- External RC clock circuit

## 8.4.1 Internal Oscillator

The internal oscillator circuit is designed for use with no external components to provide a clock source with tolerance less than  $\pm 25\%$  untrimmed. An 8-bit trimming register allows the adjust to a tolerance of less than  $\pm 5\%$ .

The internal oscillator will generate a clock of 12.8 MHz typical (INTCLK) resulting in a bus speed (internal clock  $\div$  4) of 3.2 MHz. 3.2 MHz came from the maximum bus speed guaranteed at 3 V which is 4 MHz. Since the internal oscillator will have a  $\pm 25\%$  tolerance (pre-trim), then the +25% case should not allow a frequency higher than 4 MHz:

$$3.2 \text{ MHz} + 25\% = 4 \text{ MHz}$$

**Figure 8-2** shows how 2OSCOUT is derived from INTCLK and, like the RC oscillator, OSC2 can output 2OSCOUT by setting OSC2EN in PTAPUE register. See **Section 12. Input/Output (I/O) Ports**.

### 8.4.1.1 Internal Oscillator Trimming

The 8-bit trimming register, OSCTRIM, allows a clock period adjust of +127 and -128 steps. Increasing OSCTRIM value increases the clock period. Trimming will allow the internal clock frequency value fit in a  $\pm 5\%$  range around 12.8 MHz.

There's an option to order a trimmed version of MC68HC908QY4. The trimming value will be provided in a known FLASH location, \$FFC0. So that the user would be able to copy this byte from the FLASH to the OSCTRIM register right at the beginning of assembly code.

Reset loads OSCTRIM with a default value of \$80.

### 8.4.1.2 Internal to External Clock Switching

When external clock source (external OSC, RC, or XTAL) is desired, the user must perform the following steps:

1. For External crystal circuits only, OSCOPT[1:0] = 1:1: To help precharge an external crystal oscillator, set PTA4 (OSC2) as an output and drive high for several cycles. This may help the crystal circuit start more robustly.
2. Set CONFIG2 bits OSCOPT[1:0] according to [Table 8-2](#). The oscillator module control logic will then set OSC1 as an external clock input and, if the external crystal option is selected, OSC2 will also be set as the clock output.
3. Create a software delay to wait the stabilization time needed for the selected clock source (crystal, resonator, RC) as recommended by the component manufacturer. A good rule of thumb for crystal oscillators is to wait 4096 cycles of the crystal frequency, i.e., for a 4-MHz crystal, wait approximately 1 msec.
4. After the manufacturer's recommended delay has elapsed, the ECGON bit in the OSC status register (OSCSTAT) needs to be set by the user software.
5. After ECGON set is detected, the OSC module checks for oscillator activity by waiting two external clock rising edges.
6. The OSC module then switches to the external clock. Logic provides a glitch free transition.
7. The OSC module first sets the ECGST bit in the OSCSTAT register and then stops the internal oscillator.

**NOTE:** *Once transition to the external clock is done, the internal oscillator will only be reactivated with reset. No post-switch clock monitor feature is implemented (clock does not switch back to internal if external clock dies).*



## 8.4.2 External Oscillator

The external clock option is designed for use when a clock signal is available in the application to provide a clock source to the microcontroller. The OSC1 pin is enabled as an input by the oscillator module. The clock signal is used directly to create 2OSCOUT and also divided by two to create OSCOUT.

In this configuration, the OSC2 pin cannot output 2OSCOUT. So the OSC2EN bit in the port A pullup enable register will be clear to enable PTA4 I/O functions on the pin.

## 8.4.3 XTAL Oscillator

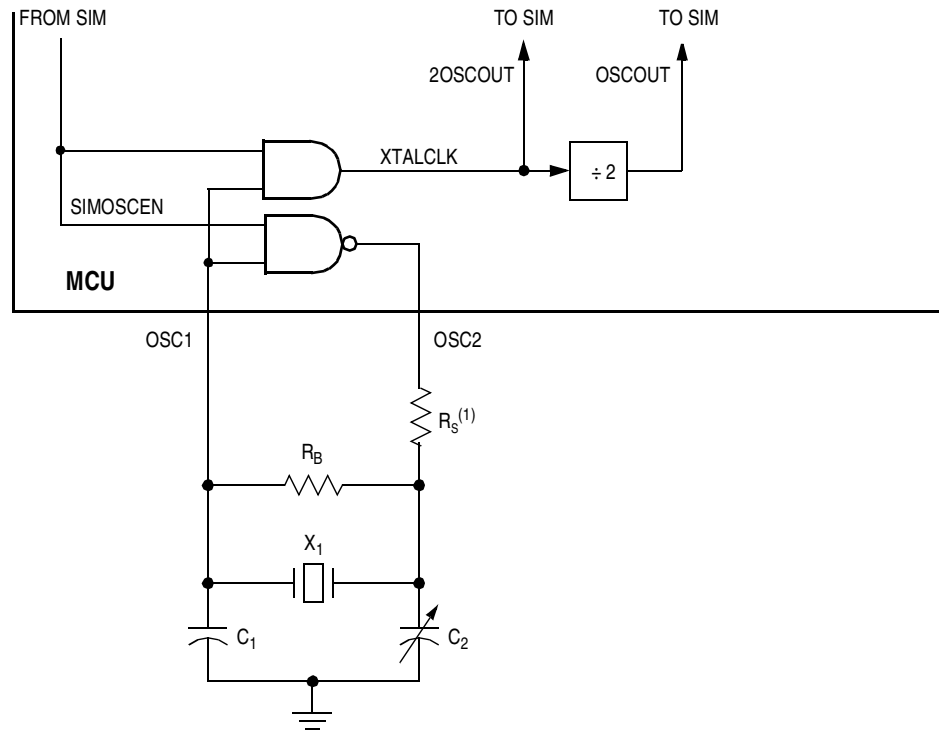
The XTAL oscillator circuit is designed for use with an external crystal or ceramic resonator to provide an accurate clock source. In this configuration, the OSC2 pin is dedicated to the external crystal circuit. The OSC2EN bit in the port A pullup enable register has no effect when this clock mode is selected.

In its typical configuration, the XTAL oscillator is connected in a Pierce oscillator configuration, as shown in [Figure 8-1](#). This figure shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal,  $X_1$
- Fixed capacitor,  $C_1$
- Tuning capacitor,  $C_2$  (can also be a fixed capacitor)
- Feedback resistor,  $R_B$
- Series resistor,  $R_S$  (optional)

**NOTE:** *The series resistor ( $R_S$ ) is included in the diagram to follow strict Pierce oscillator guidelines and may not be required for all ranges of operation, especially with high frequency crystals. Refer to the crystal manufacturer's data for more information.*

## Oscillator Module (OSC)



Note 1.

$R_S$  can be zero (shorted) when used with higher-frequency crystals. Refer to manufacturer's data. See [Section 18. Electrical Specifications](#) for component value requirements.

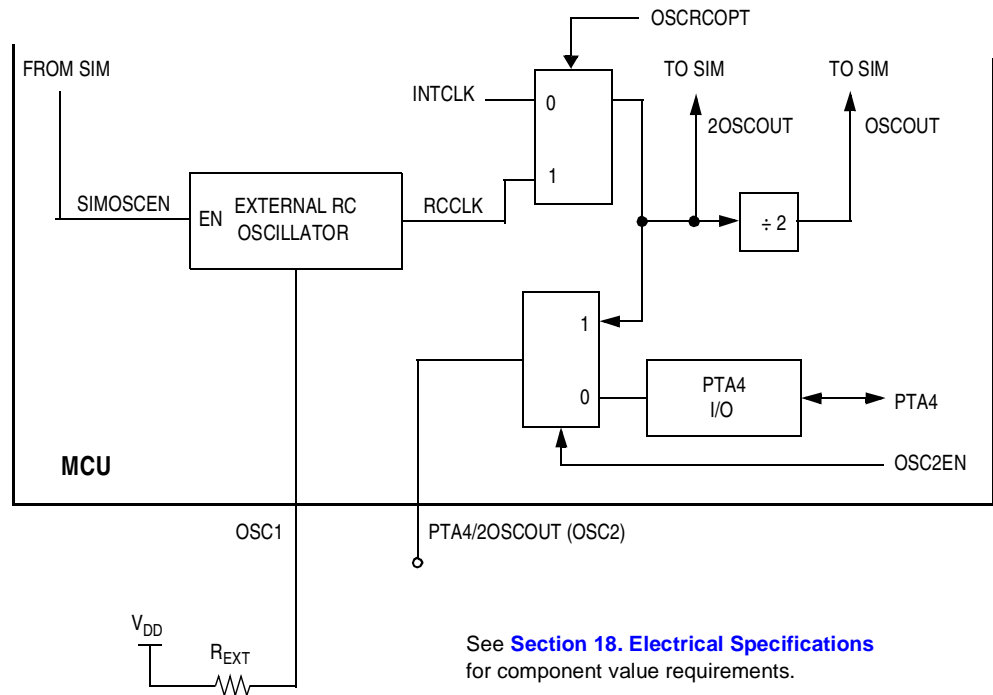
**Figure 8-1. XTAL Oscillator External Connections**

### 8.4.4 RC Oscillator

The RC oscillator circuit is designed for use with external R to provide a clock source with tolerance less than 25%.

In its typical configuration, the RC oscillator requires two external components, one R and one C. In the MC68HC908QY4, the capacitor is internal to the chip. The R value should have a tolerance of 1% or less, to obtain a clock source with less than 25% tolerance. The oscillator configuration uses one component,  $R_{EXT}$ .

In this configuration, the OSC2 pin can be left in the reset state as PTA4. Or, the OSC2EN bit in the port A pullup enable register can be set to enable the OSC2 function on the pin without affecting the clocks.



**Figure 8-2. RC Oscillator External Connections**

## 8.5 Oscillator Module Signals

The following paragraphs describe the signals that are inputs to and outputs from the oscillator module.

### 8.5.1 Crystal Amplifier Input Pin (OSC1)

The OSC1 pin is either an input to the crystal oscillator amplifier, an input to the RC oscillator circuit, or an external clock source.

For the internal oscillator configuration, the OSC1 pin can assume other functions according to [Table 1-3. Function Priority in Shared Pins.](#)

## 8.5.2 Crystal Amplifier Output Pin (OSC2/PTA4/2OSCOUT)

For the XTAL oscillator device, the OSC2 pin is the crystal oscillator inverting amplifier output.

For the external clock option, the OSC2 pin is dedicated to the PTA4 I/O function. The OSC2EN bit has no effect.

For the internal oscillator or RC oscillator options, the OSC2 pin can assume other functions according to [Table 1-3. Function Priority in Shared Pins](#), or the output of the oscillator clock (2OSCOUT).

**Table 8-1. OSC2 Pin Function**

Option	OSC2 Pin Function
XTAL oscillator	Inverting OSC1
External clock	PTA4 I/O
Internal oscillator or RC oscillator	Controlled by OSC2EN bit in PTAPUE register OSC2EN = 0: PTA4 I/O OSC2EN = 1: 2OSCOUT output

## 8.5.3 Oscillator Enable Signal (SIMOSCEN)

The SIMOSCEN signal comes from the system integration module (SIM) and enables/disables either the XTAL oscillator circuit, the RC oscillator, or the internal oscillator.

## 8.5.4 XTAL Oscillator Clock (XTALCLK)

XTALCLK is the XTAL oscillator output signal. It runs at the full speed of the crystal ( $f_{XCLK}$ ) and comes directly from the crystal oscillator circuit. [Figure 8-1](#) shows only the logical relation of XTALCLK to OSC1 and OSC2 and may not represent the actual circuitry. The duty cycle of XTALCLK is unknown and may depend on the crystal and other external factors. Also, the frequency and amplitude of XTALCLK can be unstable at start up.

### 8.5.5 RC Oscillator Clock (RCCLK)

RCCLK is the RC oscillator output signal. Its frequency is directly proportional to the time constant of external R and internal C. [Figure 8-2](#) shows only the logical relation of RCCLK to OSC1 and may not represent the actual circuitry.

### 8.5.6 Internal Oscillator Clock (INTCLK)

INTCLK is the internal oscillator output signal. Its nominal frequency is fixed to 12.8 MHz, but it can be also trimmed using the oscillator trimming feature of the OSCTRIM register (see [8.4.1.1 Internal Oscillator Trimming](#)).

### 8.5.7 Oscillator Out 2 (2OSCOUT)

2OSCOUT is the same as the input clock (XTALCLK, RCCLK, or INTCLK). This signal is driven to the SIM module and is used to determine the COP cycles.

### 8.5.8 Oscillator Out (OSCOUT)

The frequency of this signal is equal to half of the 2OSCOUT, this signal is driven to the SIM for generation of the bus clocks used by the CPU and other modules on the MCU. OSCOUT will be divided again in the SIM and results in the internal bus frequency being one fourth of either the XTALCLK, RCCLK, or INTCLK frequency.

## 8.6 Low Power Modes

The WAIT and STOP instructions put the MCU in low-power consumption standby modes.

## 8.6.1 Wait Mode

The WAIT instruction has no effect on the oscillator logic. OSCOUT and 2OSCOUT continue to drive to the SIM module.

## 8.6.2 Stop Mode

The STOP instruction disables either the XTALCLK, the RCCLK, or INTCLK output, hence OSCOUT and 2OSCOUT.

## 8.7 Oscillator During Break Mode

The oscillator continues to drive OSCOUT and 2OSCOUT when the device enters the break state.

## 8.8 CONFIG2 Options

Two CONFIG2 register options affect the operation of the oscillator module: OSCOPT1 and OSCOPT0. All CONFIG2 register bits will have a default configuration. Refer to [Section 5. Configuration Register \(CONFIG\)](#) for more information on how the CONFIG2 register is used.

[Table 8-2](#) shows how the OSCOPT bits are used to select the oscillator clock source.

**Table 8-2. Oscillator Modes**

OSCOPT1	OSCOPT0	Oscillator Modes
0	0	Internal Oscillator
0	1	External Oscillator
1	0	External RC
1	1	External Crystal

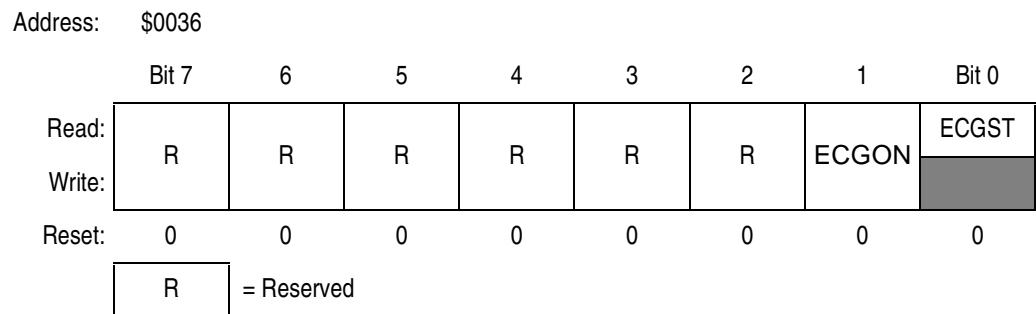
## 8.9 Input/Output (I/O) Registers

The oscillator module contains these two registers:

1. Oscillator status register (OSCSTAT)
2. Oscillator trim register (OSCTRIM)

### 8.9.1 Oscillator Status Register

The oscillator status register (OSCSTAT) contains the bits for switching from internal to external clock sources



**Figure 8-3. Oscillator Status Register (OSCSTAT)**

#### ECGON — External Clock Generator On Bit

This read/write bit enables external clock generator, so that the switching process can be initiated. This bit is forced low during reset. This bit is ignored in monitor mode with the internal oscillator bypassed, PTM or CTM mode.

- 1 = External clock generator enabled
- 0 = External clock generator disabled

#### ECGST — External Clock Status Bit

This read-only bit indicates whether or not an external clock source is engaged to drive the system clock.

- 1 = An external clock source engaged
- 0 = An external clock source disengaged

## 8.9.2 Oscillator Trim Register (OSCTRIM)

Address: \$0038

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM71	TRIM0
Write:								
Reset:	1	0	0	0	0	0	0	0

**Figure 8-4. Oscillator Trim Register (OSCTRIM)**

### TRIM7–TRIM0 — Internal Oscillator Trim Factor Bits

These read/write bits change the size of the internal capacitor used by the internal oscillator. By testing the frequency of the internal clock and incrementing or decrementing this factor accordingly, the accuracy of the internal clock can be improved to  $\pm 5\%$ . Incrementing this factor by one decreases the frequency by 0.195% of the unadjusted value. Decrementing this factor by one increases the frequency by 0.195%. The reset value is \$80, thereby centering the range of possible adjustments.



## Section 9. Monitor ROM (MON)

### 9.1 Contents

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### 9.2 Introduction

This section describes the monitor read-only memory (MON) and the monitor mode entry methods. The monitor ROM allows complete testing of the microcontroller unit (MCU) through a single-wire interface with a host computer. Monitor mode entry can be achieved without use of the higher test voltage,  $V_{TST}$ , as long as vector addresses \$FFFE and \$FFFF are blank, thus reducing the hardware requirements for in-circuit programming.

## 9.3 Features

Features of the monitor ROM include:

- Normal user-mode pin functionality on most pins
- One pin dedicated to serial communication between monitor read-only memory (ROM) and host computer
- Standard mark/space non-return-to-zero (NRZ) communication with host computer
- Execution of code in random-access memory (RAM) or FLASH
- FLASH memory security feature<sup>(1)</sup>
- FLASH memory programming interface
- Use of external 9.83 MHz crystal or clock to generate internal frequency of 2.4576 MHz
- Simple internal oscillator mode of operation (no external clock or high voltage)
- 574 bytes monitor ROM code size
- Monitor mode entry without high voltage,  $V_{TST}$ , if reset vector is blank (\$FFFE and \$FFFF contain \$FF)
- Standard monitor mode entry if high voltage is applied to  $\overline{IRQ}$

## 9.4 Functional Description

The monitor ROM receives and executes commands from a host computer. [Figure 9-1](#), [Figure 9-2](#), and [Figure 9-3](#) show example circuits used to enter monitor mode and communicate with a host computer via a standard RS-232 interface.

Simple monitor commands can access any memory address. In monitor mode, the MCU can execute code downloaded into RAM by a host computer while most MCU pins retain normal operating mode functions. All communication between the host computer and the MCU is through

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1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

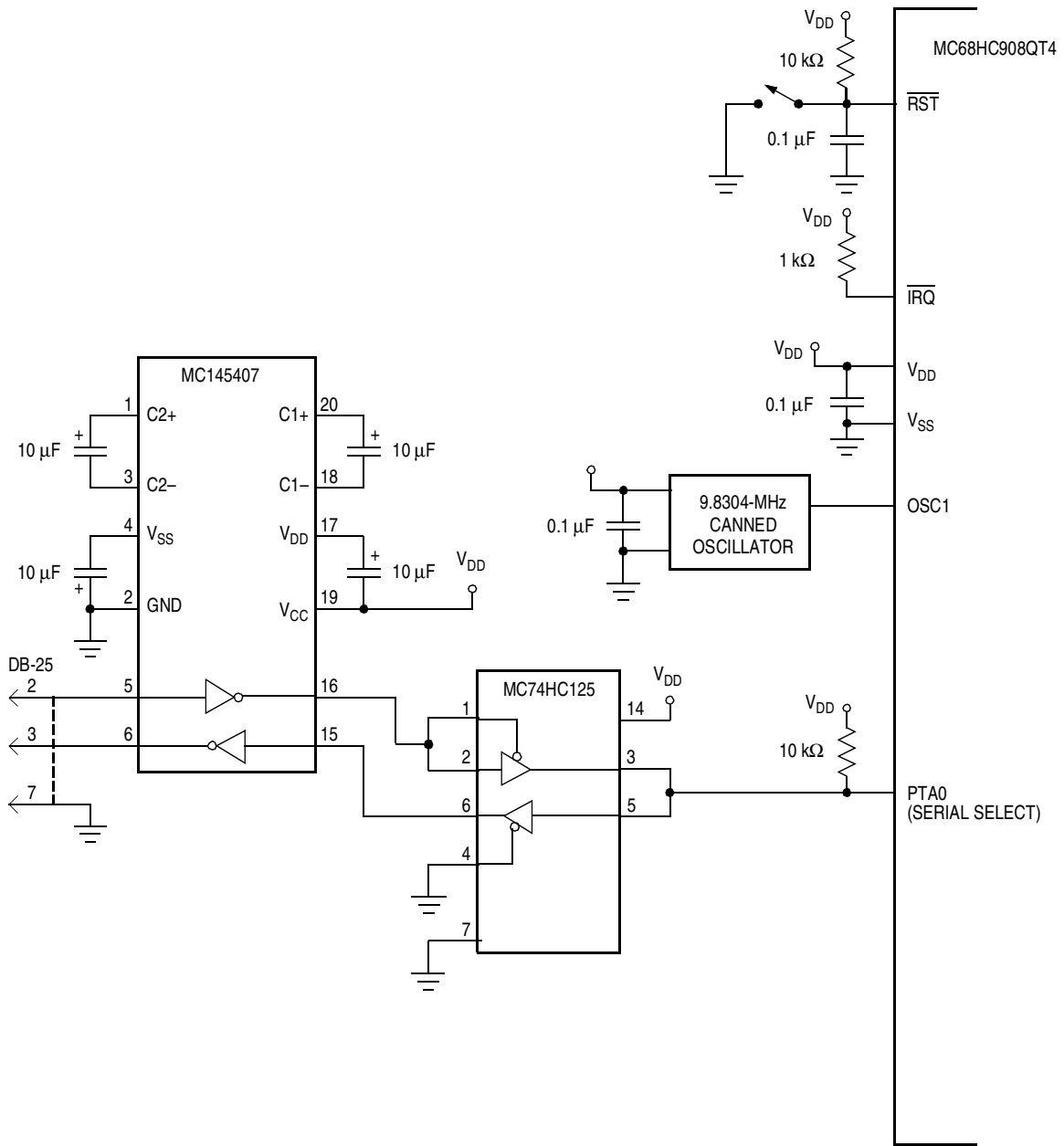
the PTA0 pin. A level-shifting and multiplexing interface is required between PTA0 and the host computer. PTA0 is used in a wired-OR configuration and requires a pullup resistor.

The monitor code has been updated from previous versions of the monitor code to allow enabling the internal oscillator to generate the internal clock. This addition, which is enabled when  $\overline{\text{IRQ}}$  is held low out of reset, is intended to support serial communication/programming at 9600 baud in monitor mode by using the internal oscillator, and the internal oscillator user trim value OSCTRIM (FLASH location \$FFC0, if programmed) to generate the desired internal frequency (3.2 MHz). Since this feature is enabled only when  $\overline{\text{IRQ}}$  is held low out of reset, it cannot be used when the reset vector is programmed (i.e., the value is not \$FFFF) because entry into monitor mode in this case requires  $V_{\text{TST}}$  on IRQ. The IRQ pin must remain low during this monitor session in order to maintain communication.

**Table 9-1** shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a power-on reset (POR) and will allow communication at 9600 baud provided one of the following sets of conditions is met:

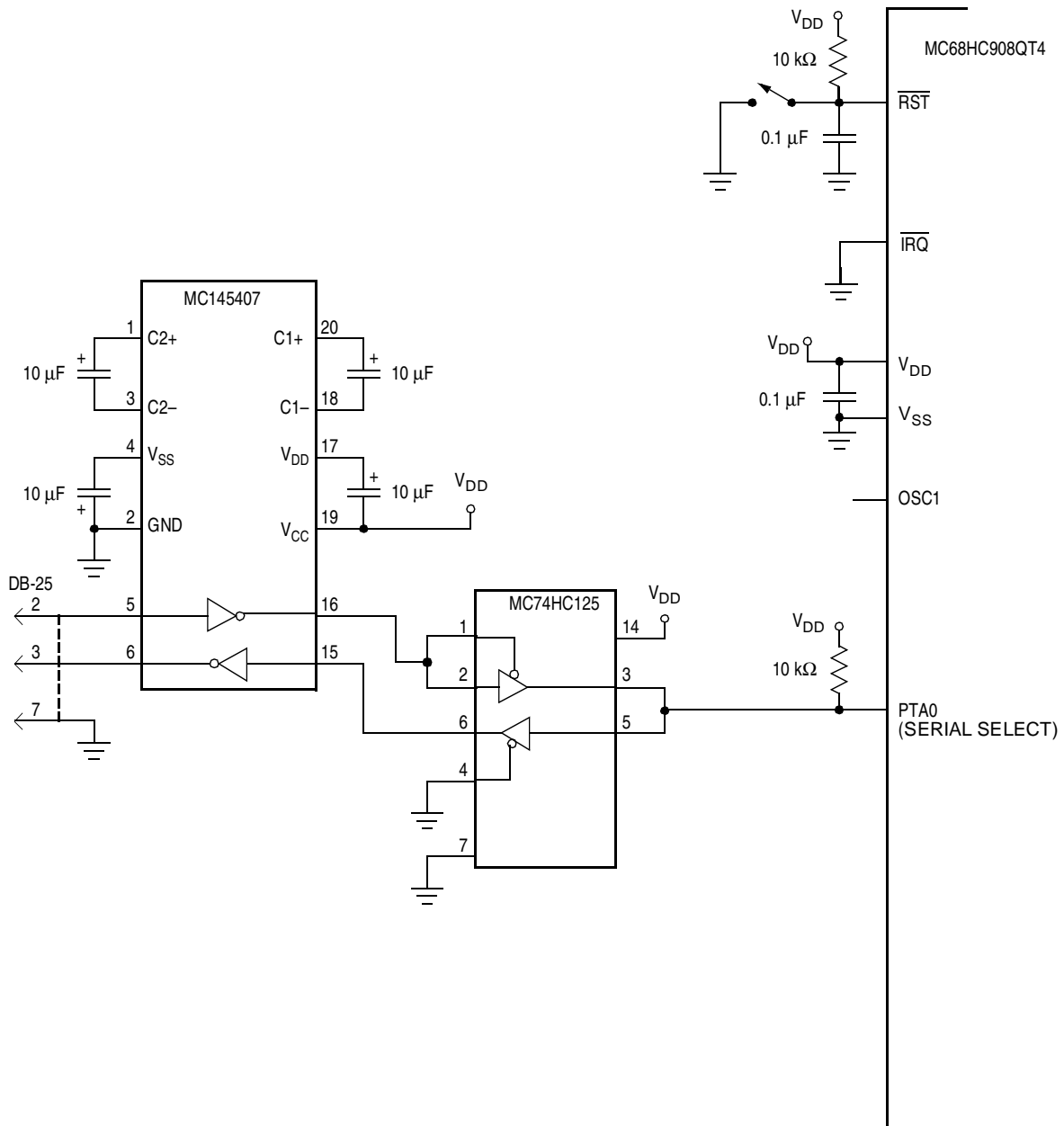
- If \$FFFE and \$FFFF does not contain \$FF (programmed state):
  - The external clock is 9.8304 MHz
  - $\overline{\text{IRQ}} = V_{\text{TST}}$
- If \$FFFE and \$FFFF contain \$FF (erased state):
  - The external clock is 9.8304 MHz
  - $\overline{\text{IRQ}} = V_{\text{DD}}$  (this can be implemented through the internal  $\overline{\text{IRQ}}$  pullup)
- If \$FFFE and \$FFFF contain \$FF (erased state):
  - $\overline{\text{IRQ}} = V_{\text{SS}}$  (internal oscillator is selected, no external clock required)

# Monitor ROM (MON)



**Figure 9-1. Monitor Mode Circuit  
(External Clock, No High Voltage)**

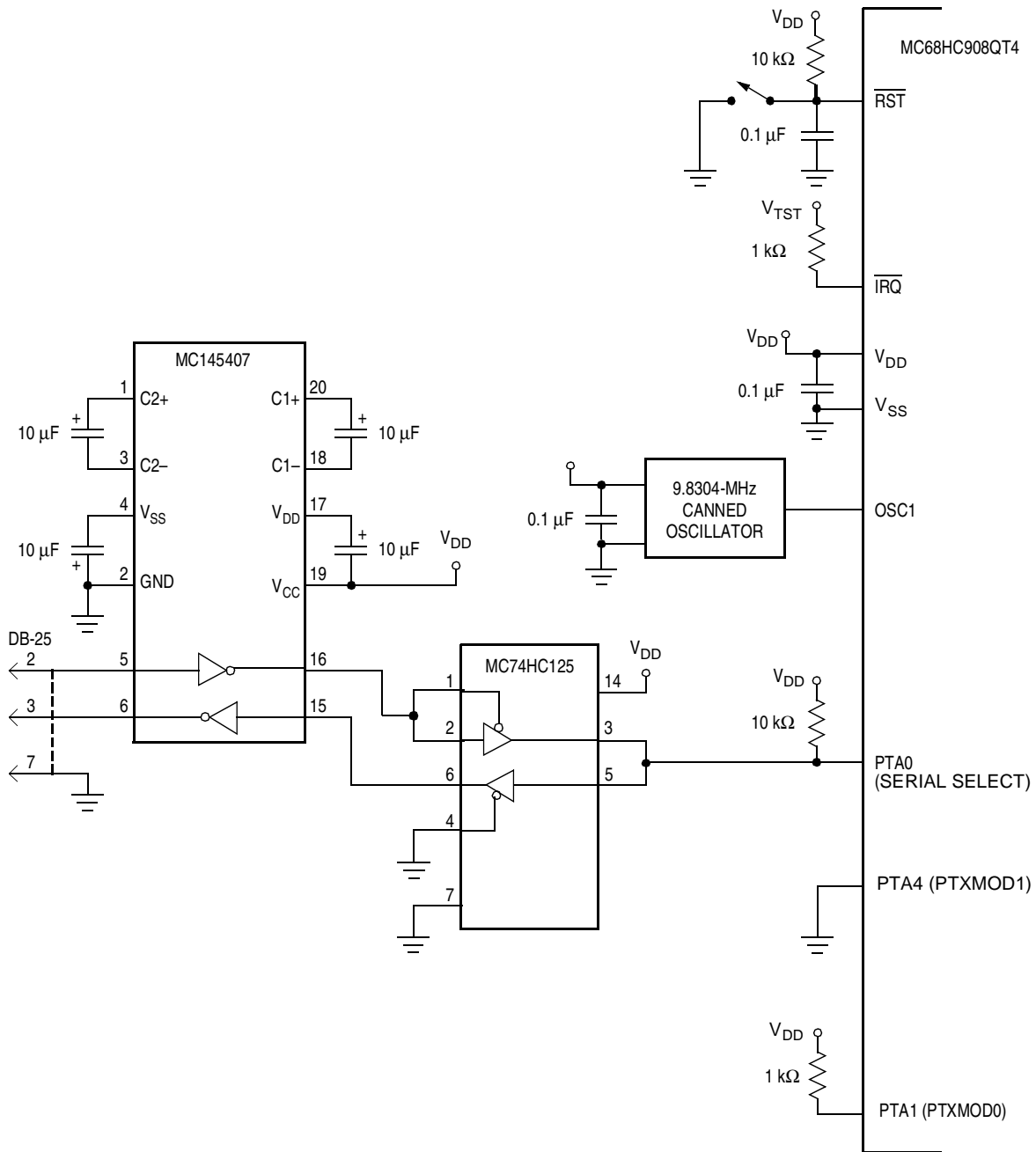
MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1



**Figure 9-2. Monitor Mode Circuit  
(Internal Clock, No High Voltage)**

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

# Monitor ROM (MON)



**Figure 9-3. Monitor Mode Circuit  
(External Clock, with High Voltage)**

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

**Table 9-1. Monitor Mode Signal Requirements and Options**

Mode	$\overline{\text{IRQ}}$	$\overline{\text{RST}}$	\$FFFE/ \$FFFF	PTA1	PTA4	External Clock (MHz)	Bus Frequency (MHz)	COP	Comment
$V_{\text{TST}}$ monitor mode	$V_{\text{TST}}$	$V_{\text{DD}}$	X	1	0	9.8304	2.4576	Disabled	PTA1 and PTA4 voltages are required. $\overline{\text{RST}}$ and OSC1 functions are active
Forced monitor mode	$V_{\text{DD}}$	X	\$FF (blank)	X	X	9.8304	2.4576	Disabled	OSC1 function is active. $\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ only available if later configured.
Forced monitor mode	$V_{\text{SS}}$	X	\$FF (blank)	X	X	X	3.2	Disabled	$\overline{\text{RST}}$ , $\overline{\text{IRQ}}$ , and OSC1 only available if later configured.
User mode	$V_{\text{DD}}$ or $V_{\text{SS}}$	X	Not \$FF (programmed)	X	X	X	—	Enabled	Enters user mode $\overline{\text{RST}}$ pin only available if later configured

If entering monitor mode without high voltage on  $\overline{\text{IRQ}}$  (above condition set 2 or 3, where applied voltage is  $V_{\text{DD}}$  or  $V_{\text{SS}}$ ), then startup port pin requirements and conditions, (PTA1/PTA4) are not in effect. This is to reduce circuit requirements when performing in-circuit programming.

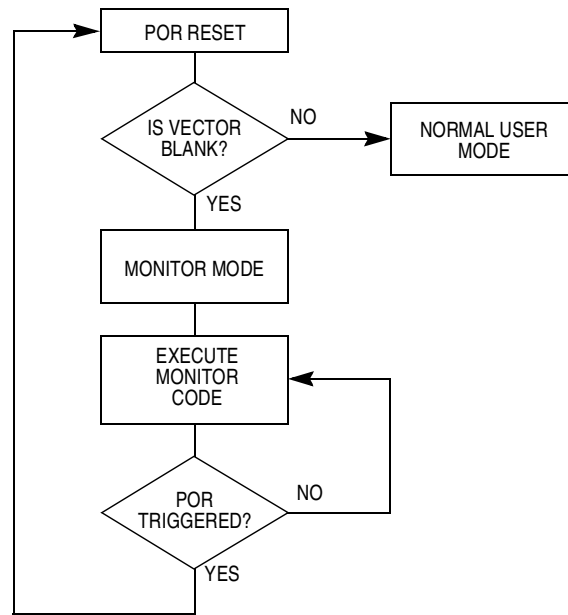
**NOTE:** *If the reset vector is blank and monitor mode is entered, the chip will see an additional reset cycle after the initial power-on reset (POR). Once the part has been programmed, the traditional method of applying a voltage,  $V_{\text{TST}}$ , to  $\overline{\text{IRQ}}$  must be used to enter monitor mode.*

The computer operating properly (COP) module is disabled in monitor mode based on these conditions:

- If monitor mode was entered as a result of the reset vector being blank (above condition set 2 or 3), the COP is always disabled regardless of the state of  $\overline{\text{IRQ}}$ .
- If monitor mode was entered with  $V_{\text{TST}}$  on  $\overline{\text{IRQ}}$  (condition set 1), then the COP is disabled as long as  $V_{\text{TST}}$  is applied to  $\overline{\text{IRQ}}$ .

**NOTE:** *The PTA0 pin must be at logic 1 (pullup) during chip power up to enter monitor mode properly.*

**Figure 9-4** shows a simplified diagram of the monitor mode entry when the reset vector is blank and just  $1 \times V_{DD}$  voltage is applied to the  $\overline{IRQ}$  pin. An external oscillator of 9.8304 MHz is required for a baud rate of 9600, as the internal bus frequency is automatically set to the external frequency divided by four. No external clock is required if  $\overline{IRQ} = 0$  since chip clock will be drive by internal clock generator.



**Figure 9-4. Low-Voltage Monitor Mode Entry Flowchart**

Enter monitor mode with pin configuration shown in **Figure 9-1** by pulling  $\overline{RST}$  low and then high. The rising edge of  $\overline{RST}$  latches monitor mode. Once monitor mode is latched, the values on the specified pins can change.

Once out of reset, the MCU waits for the host to send eight security bytes (see **9.5 Security**). After the security bytes, the MCU sends a break signal (10 consecutive logic 0s) to the host, indicating that it is ready to receive a command.



### 9.4.1 Forced Monitor Mode

If the voltage applied to the  $\overline{\text{IRQ1}}$  is less than  $V_{\text{TST}}$ , the MCU will come out of reset in user mode. The MENRST module is monitoring the reset vector fetches and will assert an internal reset if it detects that the reset vectors are erased (\$FF). When the MCU comes out of reset, it is forced into monitor mode without requiring high voltage on the  $\overline{\text{IRQ1}}$  pin. Once out of reset, the monitor code is initially executing off the internal clock at its default frequency.

If  $\overline{\text{IRQ}}$  is tied high, all pins will default to regular input port functions except for PTA0 and PTA5 which will operate as a serial communication port and OSC1 input respectively. That will allow the clock to be driven from an external source through OSC1 pin.

If  $\overline{\text{IRQ}}$  is tied low, all pins will default to regular input port function except for PTA0 which will operate as serial communication port.

The COP module is disabled in forced monitor mode. Any reset other than a power-on reset (POR) will automatically force the MCU to come back to the forced monitor mode.

In monitor mode, the MCU uses different vectors for reset, SWI (software interrupt), and break interrupt than those for user mode. The alternate vectors are in the \$FE page instead of the \$FF page and allow code execution from the internal monitor firmware instead of user code.

**NOTE:** *Exiting monitor mode after it has been initiated by having a blank reset vector requires a power-on reset (POR). Pulling  $\overline{\text{RST}}$  (when  $\overline{\text{RST}}$  pin available) low will not exit monitor mode in this situation.*

**Table 9-2** summarizes the differences between user mode and monitor mode regarding vectors.

**Table 9-2. Mode Difference**

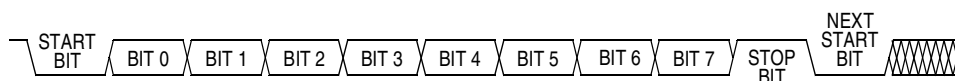
Modes	Functions					
	Reset Vector High	Reset Vector Low	Break Vector High	Break Vector Low	SWI Vector High	SWI Vector Low
User	\$FFFE	\$FFFF	\$FFFC	\$FFFD	\$FFFC	\$FFFD
Monitor	\$FEFE	\$FEFF	\$FEFC	\$FEFD	\$FEFC	\$FEFD

## 9.4.2 $V_{TST}$ Monitor Mode

$\overline{RST}$  and OSC1 functions will be active on the PTA3 and PTA5 pins respectively as long as  $V_{TST}$  is applied to  $\overline{IRQ}$  pin. If the  $\overline{IRQ}$  pin is lowered (no longer  $V_{TST}$ ) then the chip will still be operating in monitor mode, but the pin functions will be determined by the settings in the configuration registers (see [Section 5. Configuration Register \(CONFIG\)](#)) when  $V_{TST}$  was lowered.

## 9.4.3 Data Format

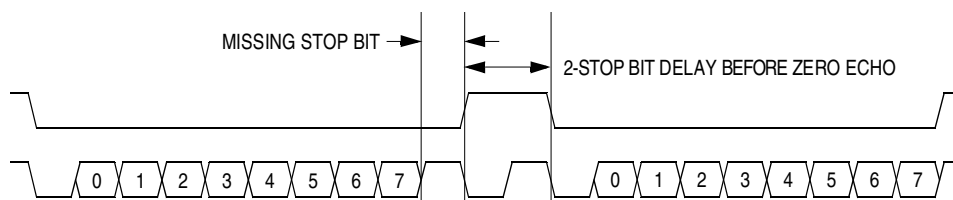
Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. Transmit and receive baud rates must be identical.



**Figure 9-5. Monitor Data Format**

## 9.4.4 Break Signal

A start bit (logic 0) followed by nine logic 0 bits is a break signal. When the monitor receives a break signal, it drives the PTA0 pin high for the duration of two bits and then echoes back the break signal.



**Figure 9-6. Break Transaction**

## 9.4.5 Baud Rate

The communication baud rate is controlled by the external frequency and the divide ratio is 1024.

**Table 9-3** has the external frequency required to achieve a standard baud rate of 9600 bps. Other standard baud rates can be accomplished using proportionally higher or lower frequency generators. If a crystal is used as the source, be aware of the upper frequency limit that the MCU can operate.

**Table 9-3. Monitor Baud Rate Selection**

External Frequency	$\overline{\text{IRQ}}$	Internal Frequency	Baud Rate (bps)
9.8304 MHz	$V_{\text{TST}}$ or $V_{\text{DD}}$	2.4576 MHz	9600
—	$V_{\text{SS}}$	3.2 MHz (Trimmed)	9600

### 9.4.6 Commands

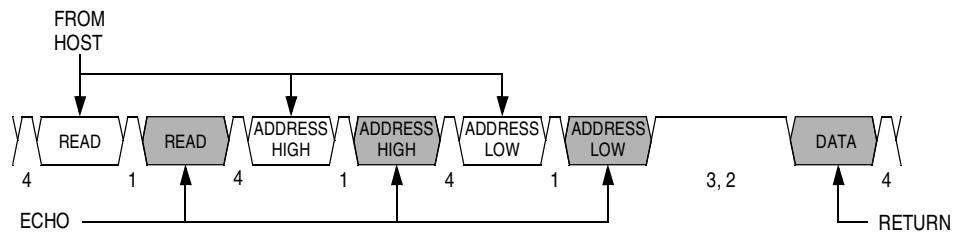
The monitor ROM firmware uses these commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

The monitor ROM firmware echoes each received byte back to the PTA0 pin for error checking. An 11-bit delay at the end of each command allows the host to send a break character to cancel the command. A delay of two bit times occurs before each echo and before READ, IREAD, or READSP data is returned. The data returned by a read command appears after the echo of the last byte of the command.

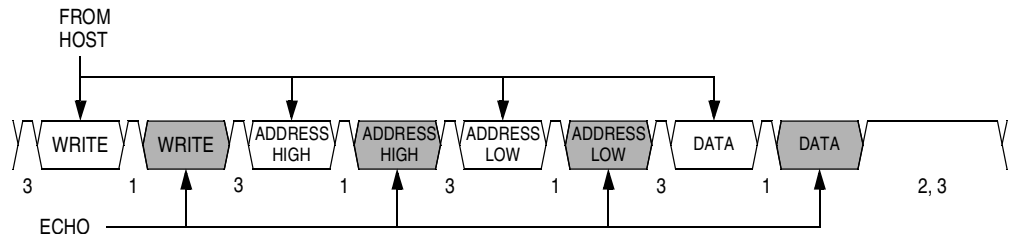
**NOTE:** *Wait one bit time after each echo before sending the next byte.*

# Monitor ROM (MON)



Notes:  
 1 = Echo delay, 2 bit times  
 2 = Data return delay, 2 bit times  
 3 = Cancel command delay, 11 bit times  
 4 = Wait 1 bit time before sending next byte.

**Figure 9-7. Read Transaction**



Notes:  
 1 = Echo delay, 2 bit times  
 2 = Cancel command delay, 11 bit times  
 3 = Wait 1 bit time before sending next byte.

**Figure 9-8. Write Transaction**

A brief description of each monitor mode command is given in [Table 9-4](#) through [Table 9-9](#).

**Table 9-4. READ (Read Memory) Command**

<b>Description</b>	Read byte from memory
<b>Operand</b>	2-byte address in high-byte:low-byte order
<b>Data Returned</b>	Returns contents of specified address
<b>Opcode</b>	\$4A
<b>Command Sequence</b>	
<p>SENT TO MONITOR</p> <p>READ ADDRESS HIGH ADDRESS LOW DATA</p> <p>ECHO</p> <p>RETURN</p>	

**Table 9-5. WRITE (Write Memory) Command**

<b>Description</b>	Write byte to memory
<b>Operand</b>	2-byte address in high-byte:low-byte order; low byte followed by data byte
<b>Data Returned</b>	None
<b>Opcode</b>	\$49
<b>Command Sequence</b>	

**Table 9-6. IREAD (Indexed Read) Command**

<b>Description</b>	Read next 2 bytes in memory from last address accessed
<b>Operand</b>	2-byte address in high byte:low byte order
<b>Data Returned</b>	Returns contents of next two addresses
<b>Opcode</b>	\$1A
<b>Command Sequence</b>	

**Table 9-7. IWRITE (Indexed Write) Command**

<b>Description</b>	Write to last address accessed + 1
<b>Operand</b>	Single data byte
<b>Data Returned</b>	None
<b>Opcode</b>	\$19
<b>Command Sequence</b>	

A sequence of IREAD or IWRITE commands can access a block of memory sequentially over the full 64-Kbyte memory map.

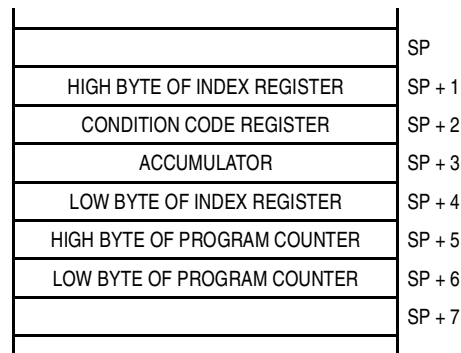
**Table 9-8. READSP (Read Stack Pointer) Command**

<b>Description</b>	Reads stack pointer
<b>Operand</b>	None
<b>Data Returned</b>	Returns incremented stack pointer value (SP + 1) in high-byte:low-byte order
<b>Opcode</b>	\$0C
<b>Command Sequence</b>	

**Table 9-9. RUN (Run User Program) Command**

<b>Description</b>	Executes PULH and RTI instructions
<b>Operand</b>	None
<b>Data Returned</b>	None
<b>Opcode</b>	\$28
<b>Command Sequence</b>	

The MCU executes the SWI and PSHH instructions when it enters monitor mode. The RUN command tells the MCU to execute the PULH and RTI instructions. Before sending the RUN command, the host can modify the stacked CPU registers to prepare to run the host program. The READSP command returns the incremented stack pointer value, SP + 1. The high and low bytes of the program counter are at addresses SP + 5 and SP + 6.



**Figure 9-9. Stack Pointer at Monitor Mode Entry**

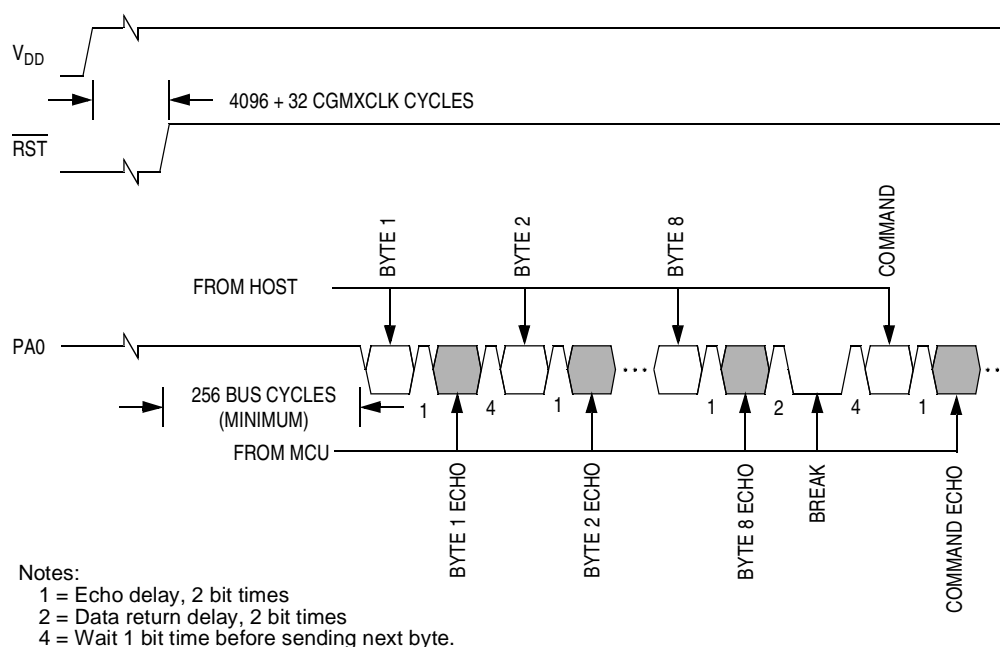
## 9.5 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations \$FFF6–\$FFFD. Locations \$FFF6–\$FFFD contain user-defined data.

**NOTE:** *Do not leave locations \$FFF6–\$FFFD blank. For security reasons, program locations \$FFF6–\$FFFD even if they are not used for vectors.*

During monitor mode entry, the MCU waits after the power-on reset for the host to send the eight security bytes on pin PTA0. If the received bytes match those at locations \$FFF6–\$FFFD, the host bypasses the security feature and can read all FLASH locations and execute code from FLASH. Security remains bypassed until a power-on reset occurs. If the reset was not a power-on reset, security remains bypassed and security code entry is not required. See [Figure 9-10](#).





**Figure 9-10. Monitor Mode Entry Timing**

Upon power-on reset, if the received bytes of the security code do not match the data at locations \$FFF6–\$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading a FLASH location returns an invalid value and trying to execute code from FLASH causes an illegal address reset. After receiving the eight security bytes from the host, the MCU transmits a break character, signifying that it is ready to receive a command.

**NOTE:** *The MCU does not transmit a break character until after the host sends the eight security bytes.*

To determine whether the security code entered is correct, check to see if bit 6 of RAM address \$80 is set. If it is, then the correct security code has been entered and FLASH can be accessed.

If the security sequence fails, the device should be reset by a power-on reset and brought up in monitor mode to attempt another entry. After failing the security sequence, the FLASH module can also be mass erased by executing an erase routine that was downloaded into internal RAM. The mass erase operation clears the security code locations so that all eight security bytes become \$FF (blank).

## Monitor ROM (MON)

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## Section 10. Timer Interface Module (TIM)

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## 10.2 Introduction

This section describes the timer interface module (TIM). The TIM is a two-channel timer that provides a timing reference with input capture, output compare, and pulse-width-modulation functions. [Figure 10-1](#) is a block diagram of the TIM.

## 10.3 Features

Features of the TIM include the following:

- Two input capture/output compare channels
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
- Buffered and unbuffered pulse width modulation (PWM) signal generation
- Programmable TIM clock input with 7-frequency internal bus clock prescaler selection
- Free-running or modulo up-count operation
- Toggle any channel pin on overflow
- TIM counter stop and reset bits

## 10.4 Pin Name Conventions

The TIM shares two input/output (I/O) pins with two port A I/O pins. The full names of the TIM I/O pins are listed in [Table 10-1](#). The generic pin name appear in the text that follows.

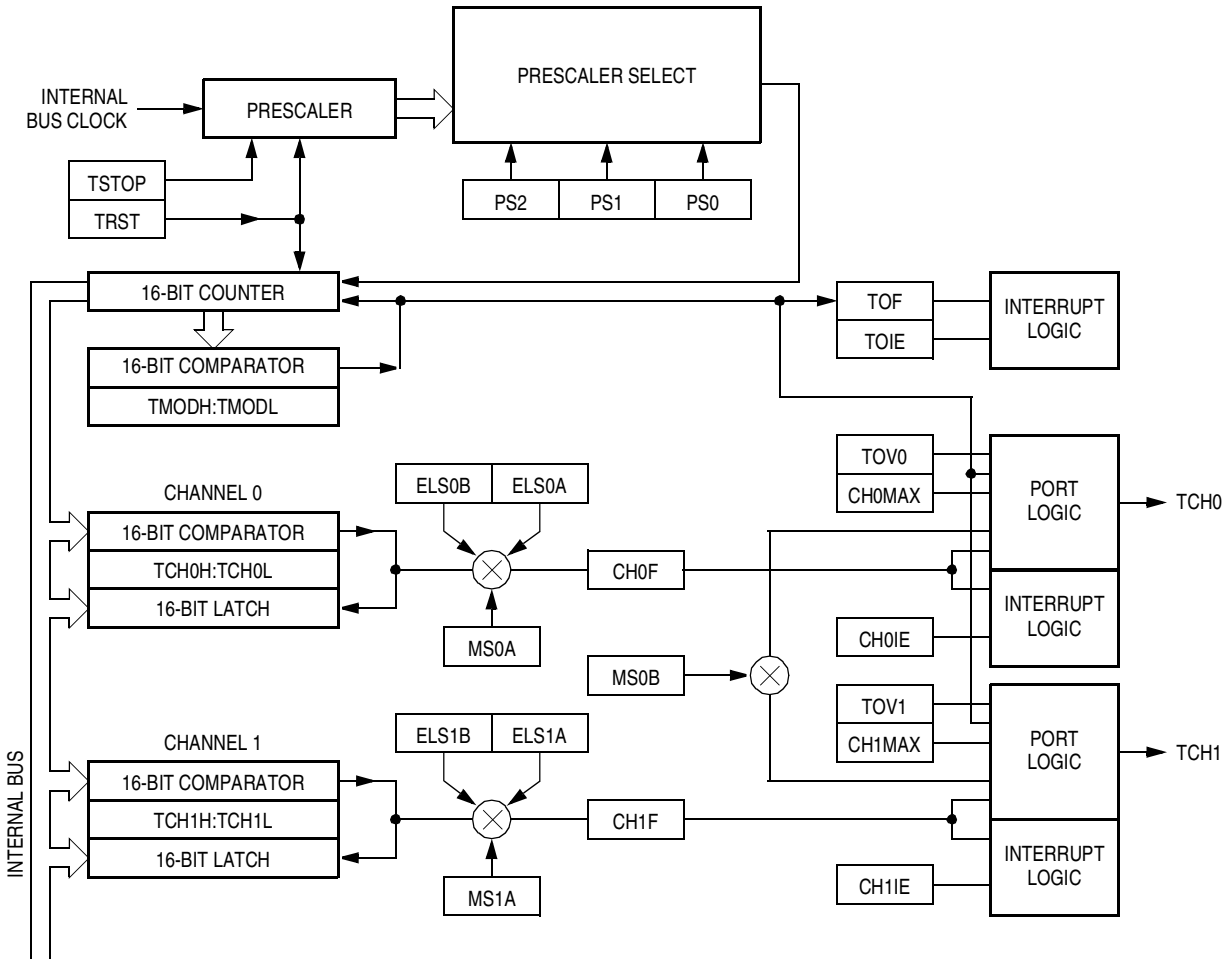
**Table 10-1. Pin Name Conventions**

TIM Generic Pin Names:	TCH0	TCH1
Full TIM Pin Names:	PTA0/TCH0	PTA1/TCH1

## 10.5 Functional Description

**Figure 10-1** shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

The two TIM channels are programmable independently as input capture or output compare channels.



**Figure 10-1. TIM Block Diagram**

# Timer Interface Module (TIM)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0020	TIM Status and Control Register (TSC) <a href="#">See page 143.</a>	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
\$0021	TIM Counter Register High (TCNTH) <a href="#">See page 146.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0022	TIM Counter Register Low (TCNTL) <a href="#">See page 146.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0023	TIM Counter Modulo Register High (TMODH) <a href="#">See page 146.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0024	TIM Counter Modulo Register Low (TMODL) <a href="#">See page 146.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0025	TIM Channel 0 Status and Control Register (TSC0) <a href="#">See page 147.</a>	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0026	TIM Channel 0 Register High (TCH0H) <a href="#">See page 151.</a>	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
\$0027	TIM Channel 0 Register Low (TCH0L) <a href="#">See page 151.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
\$0028	TIM Channel 1 Status and Control Register (TSC1) <a href="#">See page 147.</a>	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

**Figure 10-2. TIM I/O Register Summary**

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0029	TIM Channel 1 Register High (TCH1H)	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
	Reset:	Indeterminate after reset								
\$002A	TIM Channel 1 Register Low (TCH1L)	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
	Reset:	Indeterminate after reset								
				= Unimplemented						

**Figure 10-2. TIM I/O Register Summary (Continued)**

### 10.5.1 TIM Counter Prescaler

The TIM clock source is one of the seven prescaler outputs. The prescaler generates seven clock rates from the internal bus clock. The prescaler select bits, PS[2:0], in the TIM status and control register (TSC) select the TIM clock source.

### 10.5.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the TIM counter into the TIM channel registers, TCHxH:TCHxL. The polarity of the active edge is programmable. Input captures can generate TIM central processor unit (CPU) interrupt requests.

### 10.5.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM can set, clear, or toggle the channel pin. Output compares can generate TIM CPU interrupt requests.

### 10.5.3.1 Unbuffered Output Compare

Any output compare channel can generate unbuffered output compare pulses as described in [10.5.3 Output Compare](#). The pulses are unbuffered because changing the output compare value requires writing the new value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change an output compare value could cause incorrect operation for up to two counter overflow periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that counter overflow period. Also, using a TIM overflow interrupt routine to write a new, smaller output compare value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use the following methods to synchronize unbuffered changes in the output compare value on channel x:

- When changing to a smaller value, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current output compare pulse. The interrupt routine has until the end of the counter overflow period to write the new value.
- When changing to a larger output compare value, enable TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current counter overflow period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same counter overflow period.



### 10.5.3.2 Buffered Output Compare

Channels 0 and 1 can be linked to form a buffered output compare channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the output.

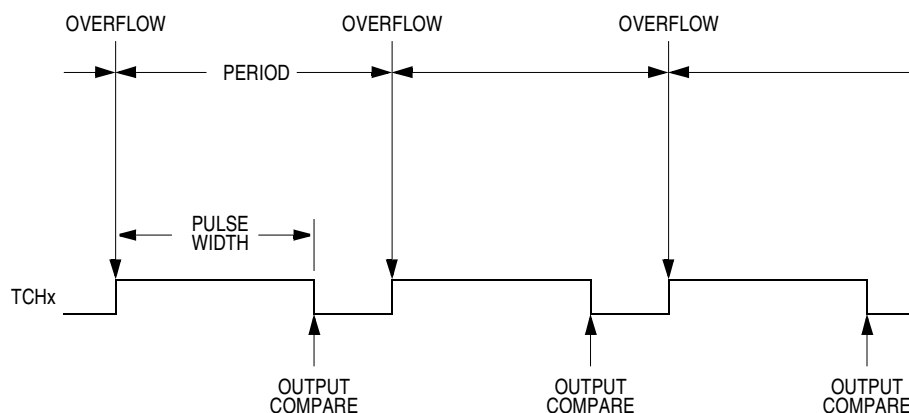
Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The output compare value in the TIM channel 0 registers initially controls the output on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the output after the TIM overflows. At each subsequent overflow, the TIM channel registers (0 or 1) that control the output are the ones written to last. TSC0 controls and monitors the buffered output compare function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

**NOTE:** *In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.*

### 10.5.4 Pulse Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIM can generate a PWM signal. The value in the TIM counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIM counter modulo registers. The time between overflows is the period of the PWM signal.

As [Figure 10-3](#) shows, the output compare value in the TIM channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIM to clear the channel pin on output compare if the state of the PWM pulse is logic 1. Program the TIM to set the pin if the state of the PWM pulse is logic 0.



**Figure 10-3. PWM Period and Pulse Width**

The value in the TIM counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing \$00FF (255) to the TIM counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is 000. See [10.10.1 TIM Status and Control Register](#).

The value in the TIM channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing \$0080 (128) to the TIM channel registers produces a duty cycle of 128/256 or 50%.

### 10.5.4.1 Unbuffered PWM Signal Generation

Any output compare channel can generate unbuffered PWM pulses as described in [10.5.4 Pulse Width Modulation \(PWM\)](#). The pulses are unbuffered because changing the pulse width requires writing the new pulse width value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change a pulse width value could cause incorrect operation for up to two PWM periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that PWM period. Also, using a TIM overflow interrupt routine to write a new, smaller pulse width value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use the following methods to synchronize unbuffered changes in the PWM pulse width on channel x:

- When changing to a shorter pulse width, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current pulse. The interrupt routine has until the end of the PWM period to write the new value.
- When changing to a longer pulse width, enable TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current PWM period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same PWM period.

**NOTE:** *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare also can cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

#### 10.5.4.2 Buffered PWM Signal Generation

Channels 0 and 1 can be linked to form a buffered PWM channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The TIM channel 0 registers initially control the pulse width on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIM channel registers (0 or 1) that control the pulse width are the ones written to last. TSC0 controls and monitors the buffered PWM function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

**NOTE:** *In buffered PWM signal generation, do not write new pulse width values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered PWM signals.*

### 10.5.4.3 PWM Initialization

To ensure correct operation when generating unbuffered or buffered PWM signals, use the following initialization procedure:

1. In the TIM status and control register (TSC):
  - a. Stop the TIM counter by setting the TIM stop bit, TSTOP.
  - b. Reset the TIM counter and prescaler by setting the TIM reset bit, TRST.
2. In the TIM counter modulo registers (TMODH:TMODL), write the value for the required PWM period.
3. In the TIM channel x registers (TCHxH:TCHxL), write the value for the required pulse width.
4. In TIM channel x status and control register (TSCx):
  - a. Write 0:1 (for unbuffered output compare or PWM signals) or 1:0 (for buffered output compare or PWM signals) to the mode select bits, MSxB:MSxA. See [Table 10-3](#).
  - b. Write 1 to the toggle-on-overflow bit, TOVx.
  - c. Write 1:0 (to clear output on compare) or 1:1 (to set output on compare) to the edge/level select bits, ELSxB:ELSxA. The output action on compare must force the output to the complement of the pulse width level. See [Table 10-3](#).

**NOTE:** *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare can also cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

5. In the TIM status control register (TSC), clear the TIM stop bit, TSTOP.

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIM channel 0 registers (TCH0H:TCH0L) initially control the buffered PWM output. TIM status control register 0 (TSCR0) controls and monitors the PWM signal from the linked channels. MS0B takes priority over MS0A.

Clearing the toggle-on-overflow bit, TOVx, inhibits output toggles on TIM overflows. Subsequent output compares try to force the output to a state it is already in and have no effect. The result is a 0% duty cycle output.

Setting the channel x maximum duty cycle bit (CHxMAX) and setting the TOVx bit generates a 100% duty cycle output. See [10.10.4 TIM Channel Status and Control Registers](#).

## 10.6 Interrupts

The following TIM sources can generate interrupt requests:

- TIM overflow flag (TOF) — The TOF bit is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. The TIM overflow interrupt enable bit, TOIE, enables TIM overflow CPU interrupt requests. TOF and TOIE are in the TIM status and control register.
- TIM channel flags (CH1F:CH0F) — The CHxF bit is set when an input capture or output compare occurs on channel x. Channel x TIM CPU interrupt requests are controlled by the channel x interrupt enable bit, CHxIE. Channel x TIM CPU interrupt requests are enabled when CHxIE = 1. CHxF and CHxIE are in the TIM channel x status and control register.

## 10.7 Wait Mode

The WAIT instruction puts the MCU in low power-consumption standby mode.

The TIM remains active after the execution of a WAIT instruction. In wait mode the TIM registers are not accessible by the CPU. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

If TIM functions are not required during wait mode, reduce power consumption by stopping the TIM before executing the WAIT instruction.

### 10.8 TIM During Break Interrupts

A break interrupt stops the TIM counter.

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See [7.9.3 Break Flag Control Register](#).

To allow software to clear status bits during a break interrupt, write a logic 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at logic 0. After the break, doing the second step clears the status bit.

### 10.9 Input/Output Signals

Port A shares two of its pins with the TIM. The two TIM channel I/O pins are PTA0/TCH0 and PTA1/TCH1.

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. PTA0/TCH0 can be configured as a buffered output compare or buffered PWM pin.

## 10.10 Input/Output Registers

The following I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM control registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0 and TSC1)
- TIM channel registers (TCH0H:TCH0L and TCH1H:TCH1L)


### 10.10.1 TIM Status and Control Register

The TIM status and control register (TSC) does the following:

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: \$0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

 = Unimplemented

**Figure 10-4. TIM Status and Control Register (TSC)**

### TOF — TIM Overflow Flag Bit

This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a logic 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing logic 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a logic 1 to TOF has no effect.

1 = TIM counter has reached modulo value

0 = TIM counter has not reached modulo value

### TOIE — TIM Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled

0 = TIM overflow interrupts disabled

### TSTOP — TIM Stop Bit

This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.

1 = TIM counter stopped

0 = TIM counter active

**NOTE:** *Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode.*

### TRST — TIM Reset Bit

Setting this write-only bit resets the TIM counter and the TIM prescaler. Setting TRST has no effect on any other registers. Counting resumes from \$0000. TRST is cleared automatically after the TIM counter is reset and always reads as logic 0. Reset clears the TRST bit.

1 = Prescaler and TIM counter cleared

0 = No effect

**NOTE:** *Setting the TSTOP and TRST bits simultaneously stops the TIM counter at a value of \$0000.*



### PS[2:0] — Prescaler Select Bits

These read/write bits select one of the seven prescaler outputs as the input to the TIM counter as [Table 10-2](#) shows. Reset clears the PS[2:0] bits.

**Table 10-2. Prescaler Selection**

PS2	PS1	PS0	TIM Clock Source
0	0	0	Internal bus clock ÷ 1
0	0	1	Internal bus clock ÷ 2
0	1	0	Internal bus clock ÷ 4
0	1	1	Internal bus clock ÷ 8
1	0	0	Internal bus clock ÷ 16
1	0	1	Internal bus clock ÷ 32
1	1	0	Internal bus clock ÷ 64
1	1	1	Not available

### 10.10.2 TIM Counter Registers

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

**NOTE:** *If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.*

## Timer Interface Module (TIM)

Address:	\$0021 TCNTH							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0
Address:	\$0022 TCNTL							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

**Figure 10-5. TIM Counter Registers (TCNTH:TCNTL)**

### 10.10.3 TIM Counter Modulo Registers

The read/write TIM modulo registers contain the modulo value for the TIM counter. When the TIM counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM counter resumes counting from \$0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

Address:	\$0023 TMODH							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Write:								
Reset:	1	1	1	1	1	1	1	1
Address:	\$0024 TMODL							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Write:								
Reset:	1	1	1	1	1	1	1	1

**Figure 10-6. TIM Counter Modulo Registers (TMODH:TMODL)**

**NOTE:** Reset the TIM counter before writing to the TIM counter modulo registers.

### 10.10.4 TIM Channel Status and Control Registers

Each of the TIM channel status and control registers does the following:

- Flags input captures and output compares
- Enables input capture and output compare interrupts
- Selects input capture, output compare, or PWM operation
- Selects high, low, or toggling output on output compare
- Selects rising edge, falling edge, or any edge as the active input capture trigger
- Selects output toggling on TIM overflow
- Selects 0% and 100% PWM duty cycle
- Selects buffered or unbuffered output compare/PWM operation

Address: \$0025		TSC0						
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Address: \$0028		TSC1						
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

**Figure 10-7. TIM Channel Status and Control Registers (TSC0:TSC1)**

#### CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM counter registers matches the value in the TIM channel x registers.

When TIM CPU interrupt requests are enabled ( $CHxIE = 1$ ), clear  $CHxF$  by reading the TIM channel x status and control register with  $CHxF$  set and then writing a logic 0 to  $CHxF$ . If another interrupt request occurs before the clearing sequence is complete, then writing logic 0 to  $CHxF$  has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of  $CHxF$ .

Reset clears the  $CHxF$  bit. Writing a logic 1 to  $CHxF$  has no effect.

1 = Input capture or output compare on channel x

0 = No input capture or output compare on channel x

### CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIM CPU interrupt service requests on channel x. Reset clears the  $CHxIE$  bit.

1 = Channel x CPU interrupt requests enabled

0 = Channel x CPU interrupt requests disabled

### MSxB — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation.  $MSxB$  exists only in the TIM channel 0 status and control register.

Setting  $MS0B$  disables the channel 1 status and control register and reverts  $TCH1$  to general-purpose I/O.

Reset clears the  $MSxB$  bit.

1 = Buffered output compare/PWM operation enabled

0 = Buffered output compare/PWM operation disabled

### MSxA — Mode Select Bit A

When  $ELSxB:A \neq 00$ , this read/write bit selects either input capture operation or unbuffered output compare/PWM operation.

See [Table 10-3](#).

1 = Unbuffered output compare/PWM operation

0 = Input capture operation

When  $ELSxB:A = 00$ , this read/write bit selects the initial output level of the  $TCHx$  pin (see [Table 10-3](#)). Reset clears the  $MSxA$  bit.

1 = Initial output level low

0 = Initial output level high

**NOTE:** Before changing a channel function by writing to the MSxB or MSxA bit, set the TSTOP and TRST bits in the TIM status and control register (TSC).

**ELSxB and ELSxA — Edge/Level Select Bits**

When channel x is an input capture channel, these read/write bits control the active edge-sensing logic on channel x.

When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to an I/O port, and pin TCHx is available as a general-purpose I/O pin. **Table 10-3** shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.

**Table 10-3. Mode, Edge, and Level Selection**

MSxB	MSxA	ELSxB	ELSxA	Mode	Configuration
X	0	0	0	Output preset	Pin under port control; initial output level high
X	1	0	0		Pin under port control; initial output level low
0	0	0	1	Input capture	Capture on rising edge only
0	0	1	0		Capture on falling edge only
0	0	1	1		Capture on rising or falling edge
0	1	0	1	Output compare or PWM	Toggle output on compare
0	1	1	0		Clear output on compare
0	1	1	1		Set output on compare
1	X	0	1	Buffered output compare or buffered PWM	Toggle output on compare
1	X	1	0		Clear output on compare
1	X	1	1		Set output on compare

**NOTE:** Before enabling a TIM channel register for input capture operation, make sure that the TCHx pin is stable for at least two bus clocks.

## TOVx — Toggle-On-Overflow Bit

When channel x is an output compare channel, this read/write bit controls the behavior of the channel x output when the TIM counter overflows. When channel x is an input capture channel, TOVx has no effect. Reset clears the TOVx bit.

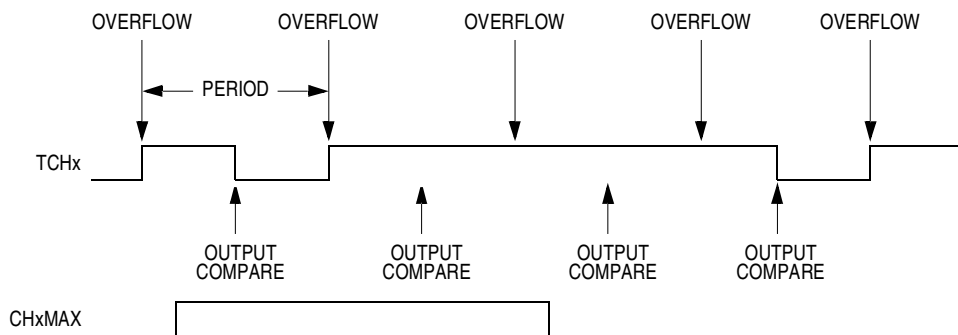
1 = Channel x pin toggles on TIM counter overflow.

0 = Channel x pin does not toggle on TIM counter overflow.

**NOTE:** When TOVx is set, a TIM counter overflow takes precedence over a channel x output compare if both occur at the same time.

## CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at logic 1, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100%. As [Figure 10-8](#) shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at the 100% duty cycle level until the cycle after CHxMAX is cleared.



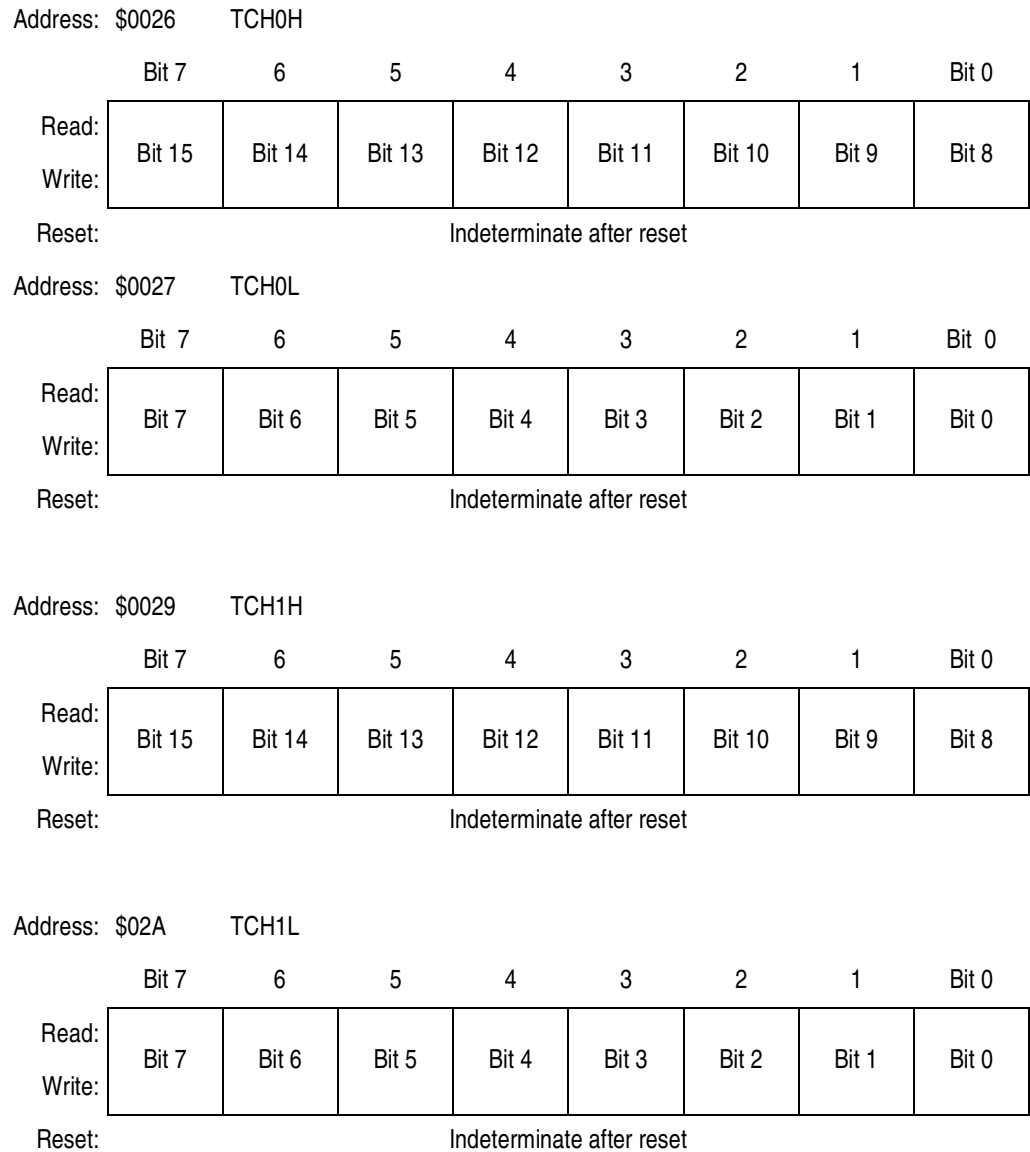
**Figure 10-8. CHxMAX Latency**

### 10.10.5 TIM Channel Registers

These read/write registers contain the captured TIM counter value of the input capture function or the output compare value of the output compare function. The state of the TIM channel registers after reset is unknown.

In input capture mode ( $MSxB:MSxA = 0:0$ ), reading the high byte of the TIM channel x registers (TCHxH) inhibits input captures until the low byte (TCHxL) is read.

In output compare mode ( $MSxB:MSxA \neq 0:0$ ), writing to the high byte of the TIM channel x registers (TCHxH) inhibits output compares until the low byte (TCHxL) is written.



**Figure 10-9. TIM Channel Registers (TCH0H/L:TCH1H/L)**





## Section 11. Analog-to-Digital Converter (ADC)

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### 11.2 Introduction

This section describes the analog-to-digital converter (ADC). The ADC is an 8-bit, 4-channel analog-to-digital converter. The ADC module is only available on the MC68HC908QY2, MC68HC908QT2, MC68HC908QY4, and MC68HC908QT4.

## 11.3 Features

Features of the ADC module include:

- 4 channels with multiplexed input
- Linear successive approximation with monotonicity
- 8-bit resolution
- Single or continuous conversion
- Conversion complete flag or conversion complete interrupt
- Selectable ADC clock

Figure 11-1 provides a summary of the input/output (I/O) registers.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$003C	ADC Status and Control Register (ADSCR) <a href="#">See page 159.</a>	Read:	COCO	AIEN	ADCO	CH4	CH3	CH2	CH1	CH0
		Write:								
		Reset:	0	0	0	1	1	1	1	1
\$003D	Unimplemented									
\$003E	ADC Data Register (ADR) <a href="#">See page 161.</a>	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Write:								
		Reset:	Indeterminate after reset							
\$003F	ADC Input Clock Register (ADICLK) <a href="#">See page 161.</a>	Read:	ADIV2	ADIV1	ADIV0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

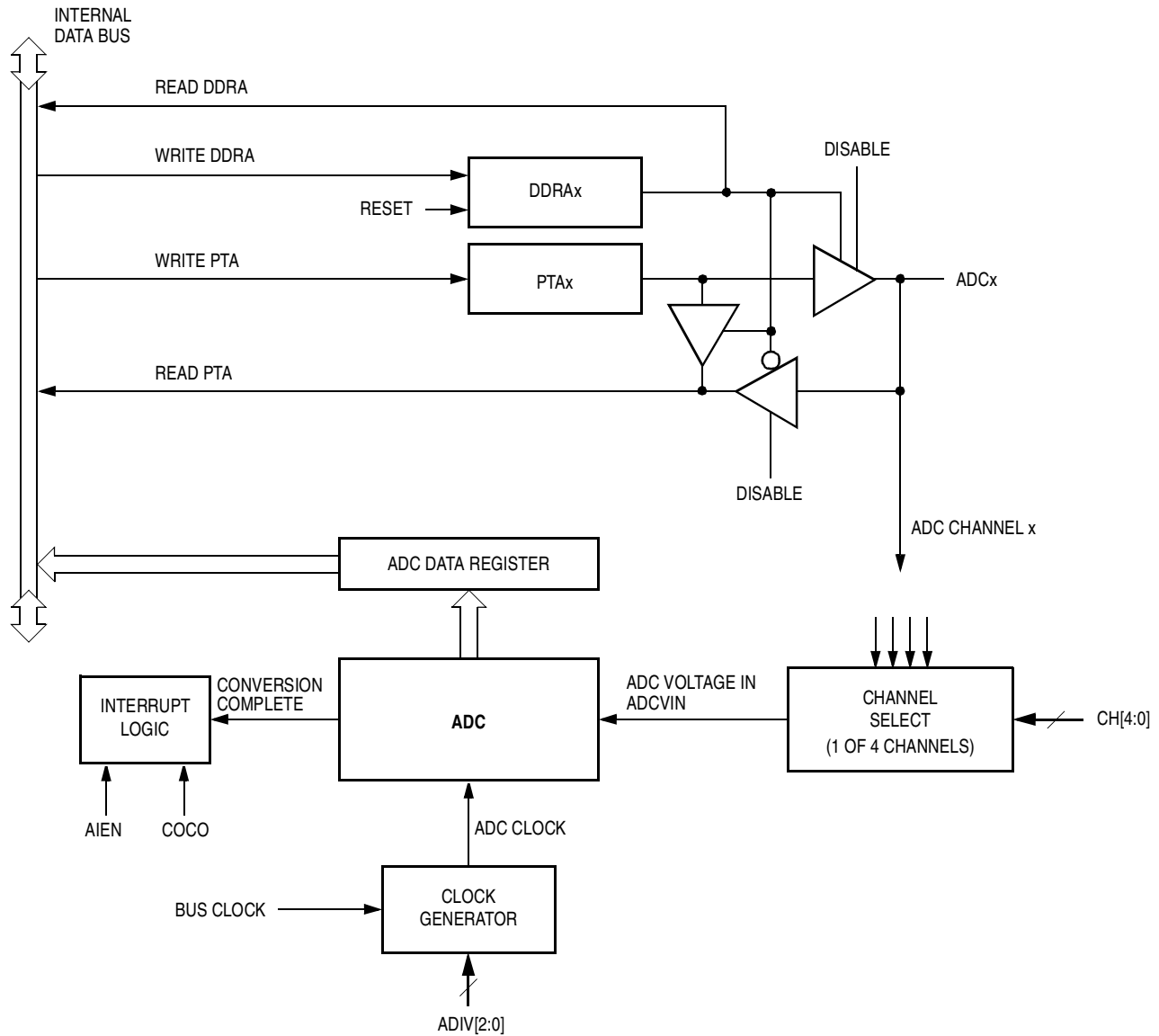
**Figure 11-1. ADC I/O Register Summary**

## 11.4 Functional Description

Four ADC channels are available for sampling external sources at pins PTA0, PTA1, PTA4, and PTA5. An analog multiplexer allows the single ADC converter to select one of the four ADC channels as an ADC

voltage input (ADCVIN). ADCVIN is converted by the successive approximation register-based counters. The ADC resolution is eight bits. When the conversion is completed, ADC puts the result in the ADC data register and sets a flag or generates an interrupt.

**Figure 11-2** shows a block diagram of the ADC.



**Figure 11-2. ADC Block Diagram**

### 11.4.1 ADC Port I/O Pins

PTA0, PTA1, PTA4, and PTA5 are general-purpose I/O pins that are shared with the ADC channels. The channel select bits (ADC status and control register (ADSCR), \$003C), define which ADC channel/port pin will be used as the input signal. The ADC overrides the port I/O logic by forcing that pin as input to the ADC. The remaining ADC channels/port pins are controlled by the port I/O logic and can be used as general-purpose I/O. Writes to the port register or data direction register (DDR) will not have any effect on the port pin that is selected by the ADC. Read of a port pin which is in use by the ADC will return a logic 0 if the corresponding DDR bit is at logic 0. If the DDR bit is at logic 1, the value in the port data latch is read.

### 11.4.2 Voltage Conversion

When the input voltage to the ADC equals  $V_{DD}$ , the ADC converts the signal to \$FF (full scale). If the input voltage equals  $V_{SS}$ , the ADC converts it to \$00. Input voltages between  $V_{DD}$  and  $V_{SS}$  are a straight-line linear conversion. All other input voltages will result in \$FF if greater than  $V_{DD}$  and \$00 if less than  $V_{SS}$ .

**NOTE:** *Input voltage should not exceed the analog supply voltages.*

### 11.4.3 Conversion Time

Sixteen ADC internal clocks are required to perform one conversion. The ADC starts a conversion on the first rising edge of the ADC internal clock immediately following a write to the ADSCR. If the ADC internal clock is selected to run at 1 MHz, then one conversion will take 16  $\mu$ s to complete. With a 1-MHz ADC internal clock the maximum sample rate is 62.5 kHz.

$$\text{Conversion Time} = \frac{16 \text{ ADC Clock Cycles}}{\text{ADC Clock Frequency}}$$

$$\text{Number of Bus Cycles} = \text{Conversion Time} \times \text{Bus Frequency}$$

#### 11.4.4 Continuous Conversion

In the continuous conversion mode, the ADC continuously converts the selected channel filling the ADC data register (ADR) with new data after each conversion. Data from the previous conversion will be overwritten whether that data has been read or not. Conversions will continue until the ADCO bit is cleared. The COCO bit (ADSCR, \$003C) is set after each conversion and can be cleared by writing the ADC status and control register or reading of the ADC data register.

#### 11.4.5 Accuracy and Precision

The conversion process is monotonic and has no missing codes.

### 11.5 Interrupts

When the AIEN bit is set, the ADC module is capable of generating a central processor unit (CPU) interrupt after each ADC conversion. A CPU interrupt is generated if the COCO bit is at logic 0. The COCO bit is not used as a conversion complete flag when interrupts are enabled.

### 11.6 Low-Power Modes

The following subsections describe the ADC in low-power modes.

#### 11.6.1 Wait Mode

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the microcontroller unit (MCU) out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting the CH[4:0] bits in ADSCR to logic 1's before executing the WAIT instruction.

### 11.6.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode. Allow one conversion cycle to stabilize the analog circuitry before attempting a new ADC conversion after exiting stop mode.

### 11.7 Input/Output Signals

The ADC module has four channels that are shared with I/O port A.

ADC voltage in (ADCVIN) is the input voltage signal from one of the four ADC channels to the ADC module.

### 11.8 Input/Output Registers

These I/O registers control and monitor ADC operation:

- ADC status and control register (ADSCR)
- ADC data register (ADR)
- ADC clock register (ADICLK)

### 11.8.1 ADC Status and Control Register

The following paragraphs describe the function of the ADC status and control register (ADSCR).

Address: \$003C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COCO	AIEN	ADCO	CH4	CH3	CH2	CH1	CH0
Write:								
Reset:	0	0	0	1	1	1	1	1

= Unimplemented

**Figure 11-3. ADC Status and Control Register (ADSCR)**

#### COCO — Conversions Complete Bit

When the AIEN bit is a logic 0, the COCO is a read-only bit which is set each time a conversion is completed. This bit is cleared whenever ADSCR is written or whenever the ADR is read. Reset clears this bit.

1 = Conversion completed (AIEN = 0)

0 = Conversion not completed (AIEN = 0)

When the AIEN bit is a logic 1 (CPU interrupt enabled), the COCO is a read-only bit, and will always be logic 0 when read.

#### AIEN — ADC Interrupt Enable Bit

When this bit is set, an interrupt is generated at the end of an ADC conversion. The interrupt signal is cleared when ADR is read or ADSCR is written. Reset clears the AIEN bit.

1 = ADC interrupt enabled

0 = ADC interrupt disabled

#### ADCO — ADC Continuous Conversion Bit

When set, the ADC will convert samples continuously and update ADR at the end of each conversion. Only one conversion is allowed when this bit is cleared. Reset clears the ADCO bit.

1 = Continuous ADC conversion

0 = One ADC conversion

## CH[4:0] — ADC Channel Select Bits

CH4, CH3, CH2, CH1, and CH0 form a 5-bit field which is used to select one of the four ADC channels. The five select bits are detailed in [Table 11-1](#). Care should be taken when using a port pin as both an analog and a digital input simultaneously to prevent switching noise from corrupting the analog signal.

The ADC subsystem is turned off when the channel select bits are all set to 1. This feature allows for reduced power consumption for the MCU when the ADC is not used. Reset sets all of these bits to a logic 1.

**NOTE:** *Recovery from the disabled state requires one conversion cycle to stabilize.*

**Table 11-1. MUX Channel Select**

CH4	CH3	CH2	CH1	CH0	ADC Channel	Input Select
0	0	0	0	0	ADC0	PTA0
0	0	0	0	1	ADC1	PTA1
0	0	0	1	0	ADC2	PTA4
0	0	0	1	1	ADC3	PTA5
0	0	1	0	0	—	Unused <sup>(1)</sup>
↓	↓	↓	↓	↓	—	
1	1	0	1	0	—	
1	1	0	1	1	—	Reserved
1	1	1	0	0	—	Unused
1	1	1	0	1	—	V <sub>DDA</sub> <sup>(2)</sup>
1	1	1	1	0	—	V <sub>SSA</sub> <sup>(2)</sup>
1	1	1	1	1	—	ADC power off

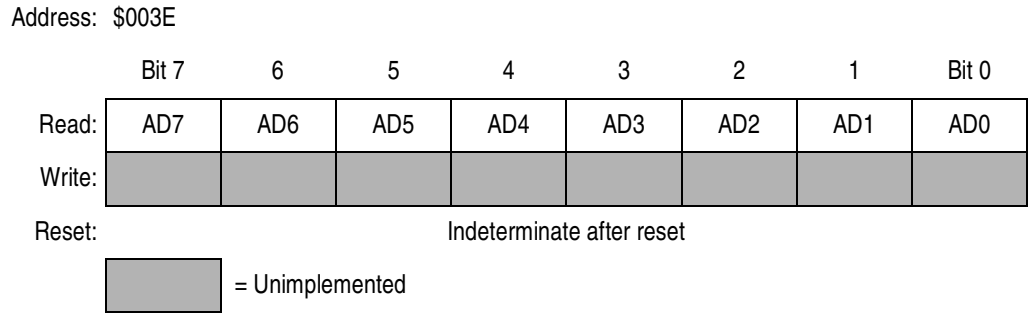
1. If any unused channels are selected, the resulting ADC conversion will be unknown.

2. The voltage levels supplied from internal reference nodes, as specified in the table, are used to verify the operation of the ADC converter both in production test and for user applications.



### 11.8.2 ADC Data Register

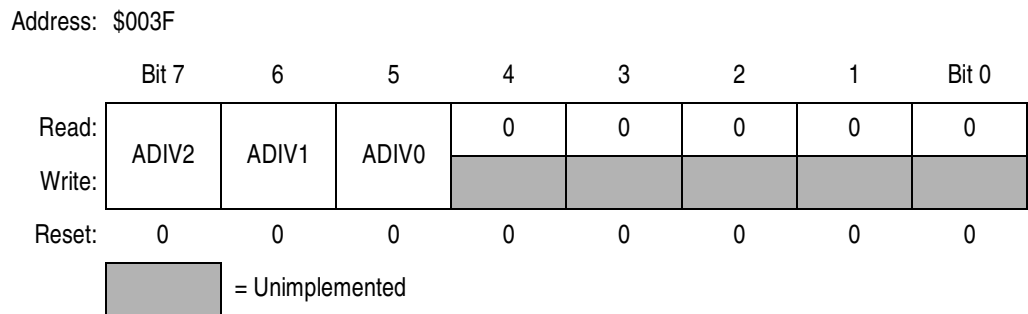
One 8-bit result register is provided. This register is updated each time an ADC conversion completes.



**Figure 11-4. ADC Data Register (ADR)**

### 11.8.3 ADC Input Clock Register

This register selects the clock frequency for the ADC.



**Figure 11-5. ADC Input Clock Register (ADICLK)**

#### ADIV2–ADIV0 — ADC Clock Prescaler Bits

ADIV2, ADIV1, and ADIV0 form a 3-bit field which selects the divide ratio used by the ADC to generate the internal ADC clock. [Table 11-2](#) shows the available clock configurations. The ADC clock should be set to approximately 1 MHz.

**Table 11-2. ADC Clock Divide Ratio**

ADIV2	ADIV1	ADIV0	ADC Clock Rate
0	0	0	Bus clock ÷ 1
0	0	1	Bus clock ÷ 2
0	1	0	Bus clock ÷ 4
0	1	1	Bus clock ÷ 8
1	X	X	Bus clock ÷ 16

X = don't care

## Section 12. Input/Output (I/O) Ports

### 12.1 Contents

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### 12.2 Introduction

The MC68HC908QT1, MC68HC908QT2, and MC68HC908QT4 have five bidirectional input-output (I/O) pins and one input only pin. The MC68HC908QY1, MC68HC908QY2, and MC68HC908QY4 have thirteen bidirectional pins and one input only pin. All I/O pins are programmable as inputs or outputs.

**NOTE:** *Connect any unused I/O pins to an appropriate logic level, either  $V_{DD}$  or  $V_{SS}$ . Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*

**Figure 12-1** provides a summary of the I/O registers.

## Input/Output (I/O) Ports

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$0000	Port A Data Register (PTA) <a href="#">See page 165.</a>	Read:	0	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	Unaffected by reset							
\$0001	Port B Data Register (PTB) <a href="#">See page 169.</a>	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
\$0004	Data Direction Register A (DDRA) <a href="#">See page 166.</a>	Read:	0	0	DDRA5	DDRA4	DDRA3	0	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0005	Data Direction Register B (DDRB) <a href="#">See page 170.</a>	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000B	Port A Input Pullup Enable Register (PTAPUE) <a href="#">See page 168.</a>	Read:	OSC2EN		PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000C	Port B Input Pullup Enable Register (PTBPUE) <a href="#">See page 171.</a>	Read:	PTBPUE7	PTBPUE6	PTBPUE5	PTBPUE4	PTBPUE3	PTBPUE2	PTBPUE1	PTBPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

**Figure 12-1. I/O Port Register Summary**

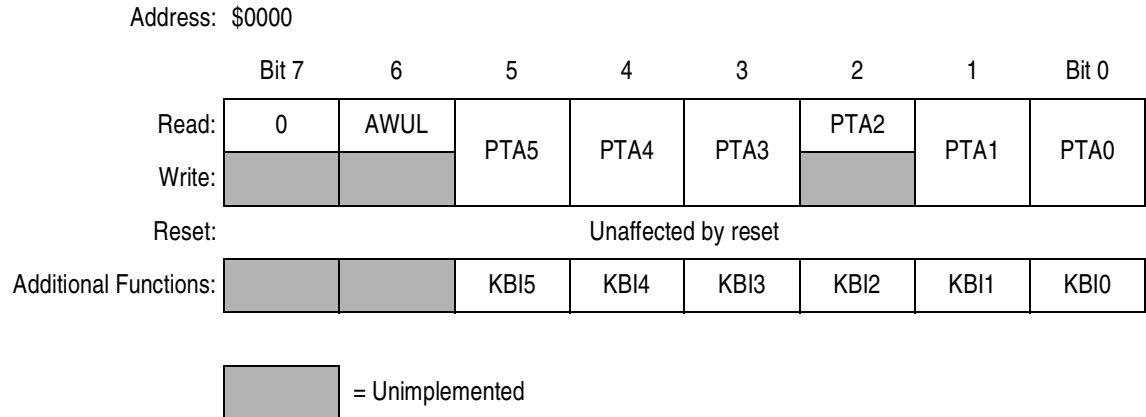
### 12.3 Port A

Port A is an 6-bit special function port that shares all six of its pins with the keyboard interrupt (KBI) module (see [Section 14. Keyboard Interrupt Module \(KBI\)](#)). Each port A pin also has a software configurable pullup device if the corresponding port pin is configured as an input port.

**NOTE:** *PTA2 is input only.*

### 12.3.1 Port A Data Register

The port A data register (PTA) contains a data latch for each of the six port A pins.



**Figure 12-2. Port A Data Register (PTA)**

#### PTA[5:0] — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

#### AWUL — Auto Wake-up Latch Data Bit

This is a read-only bit which has the value of the auto wake-up interrupt request latch. The wake-up request signal is generated internally (see [14.4.4 Auto Wake-up Interrupt Request](#)). There is no PTA6 port nor any of the associated bits such as PTA6 data register, pullup enable or direction.

#### KBI[5:0] — Port A Keyboard Interrupts


The keyboard interrupt enable bits, KBIE5–KBIE0, in the keyboard interrupt control enable register (KBIER) enable the port A pins as external interrupt pins (see [Section 14. Keyboard Interrupt Module \(KBI\)](#)).

## 12.3.2 Data Direction Register A

Data direction register A (DDRA) determines whether each port A pin is an input or an output. Writing a logic 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a logic 0 disables the output buffer.

Address: \$0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRA5	DDRA4	DDRA3	0	DDRA1	DDRA0
Write:								
Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

**Figure 12-3. Data Direction Register A (DDRA)**

### DDRA[5:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[5:0], configuring all port A pins as inputs.

1 = Corresponding port A pin configured as output

0 = Corresponding port A pin configured as input

**NOTE:** *Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1.*

Figure 12-4 shows the port A I/O logic.

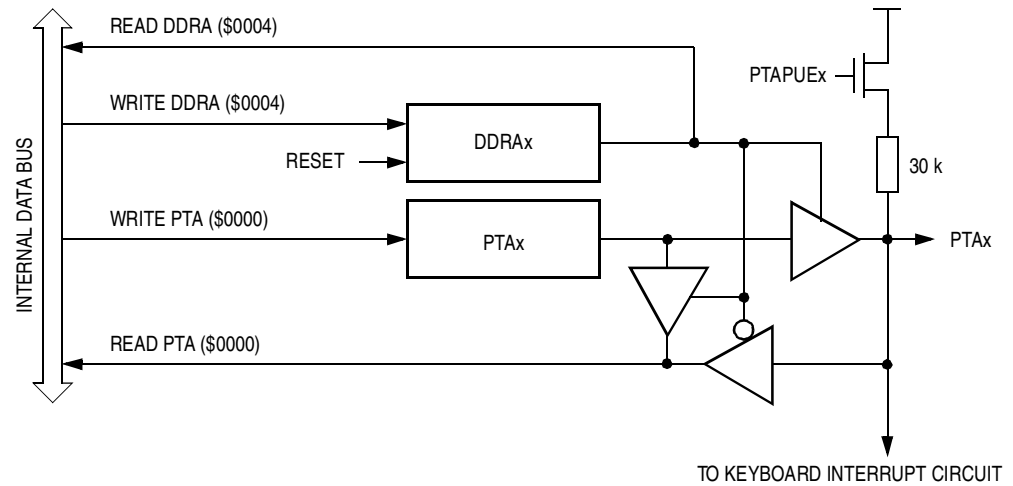


Figure 12-4. Port A I/O Circuit

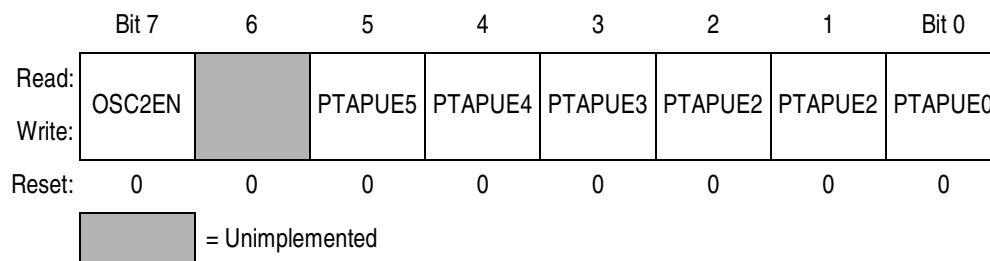
**NOTE:** Figure 12-4 does not apply to PTA2

When DDR<sub>x</sub> is a logic 1, reading address \$0000 reads the PT<sub>x</sub> data latch. When DDR<sub>x</sub> is a logic 0, reading address \$0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

## 12.3.3 Port A Input Pullup Enable Register

The port A input pullup enable register (PTAPUE) contains a software configurable pullup device for each of the six port A pins. Each bit is individually configurable and requires the corresponding data direction register, DDRAx, to be configured as input. Each pullup device is automatically and dynamically disabled when its corresponding DDRAx bit is configured as output.

Address: \$000B



**Figure 12-5. Port A Input Pull-up Enable Register (PTAPUE)**

### OSC2EN — Enable PTA4 on OSC2 Pin

This read/write bit configures the OSC2 pin function when internal oscillator or RC oscillator option is selected. This bit has no effect for the XTAL oscillator option.

1 = OSC2 pin outputs the internal or RC oscillator clock (2OSCOU)

0 = OSC2 pin configured for PTA4 I/O, having all the interrupt and pullup functions

### PTAPUE[5:0] — Port A Input Pullup Enable Bits

These read/write bits are software programmable to enable pullup devices on port A pins.

1 = Corresponding port A pin configured to have internal pull if its DDRA bit is set to 0

0 = Pullup device is disconnected on the corresponding port A pin regardless of the state of its DDRA bit

**Table 12-1** summarizes the operation of the port A pins.



**Table 12-1. Port A Pin Functions**

PTAPUE Bit	DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
				Read/Write	Read	Write
1	0	X <sup>(1)</sup>	Input, V <sub>DD</sub> <sup>(2)</sup>	DDRA5–DDRA0	Pin	PTA5–PTA0 <sup>(3)</sup>
0	0	X	Input, Hi-Z <sup>(4)</sup>	DDRA5–DDRA0	Pin	PTA5–PTA0 <sup>(3)</sup>
X	1	X	Output	DDRA5–DDRA0	PTA5–PTA0	PTA5–PTA0 <sup>(5)</sup>

1. X = don't care
2. I/O pin pulled to V<sub>DD</sub> by internal pullup.
3. Writing affects data register, but does not affect input.
4. Hi-Z = high impedance
5. Output does not apply to PTA2

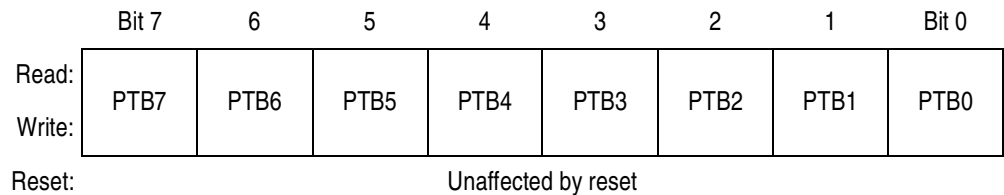
## 12.4 Port B

Port B is an 8-bit general purpose I/O port. Port B is only available on the MC68HC908QY1, MC68HC908QY2, and MC68HC908QY4.

### 12.4.1 Port B Data Register

The port B data register (PTB) contains a data latch for each of the eight port B pins.

Address: \$0001



**Figure 12-6. Port B Data Register (PTB)**

#### PTB[7:0] — Port B Data Bits

These read/write bits are software programmable. Data direction of each port B pin is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

## 12.4.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output. Writing a logic 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a logic 0 disables the output buffer.

Address: \$0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Write:								
Reset:	0	0	0	0	0	0	0	0

**Figure 12-7. Data Direction Register B (DDRB)**

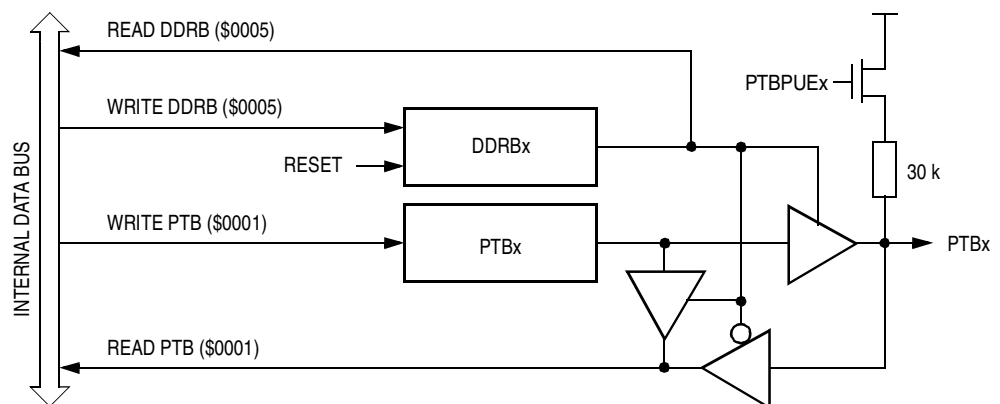
### DDRB[7:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[7:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output

0 = Corresponding port B pin configured as input

**NOTE:** Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1. [Figure 12-8](#) shows the port B I/O logic.



**Figure 12-8. Port B I/O Circuit**

When DDRBx is a logic 1, reading address \$0001 reads the PTBx data latch. When DDRBx is a logic 0, reading address \$0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. **Table 12-2** summarizes the operation of the port B pins.

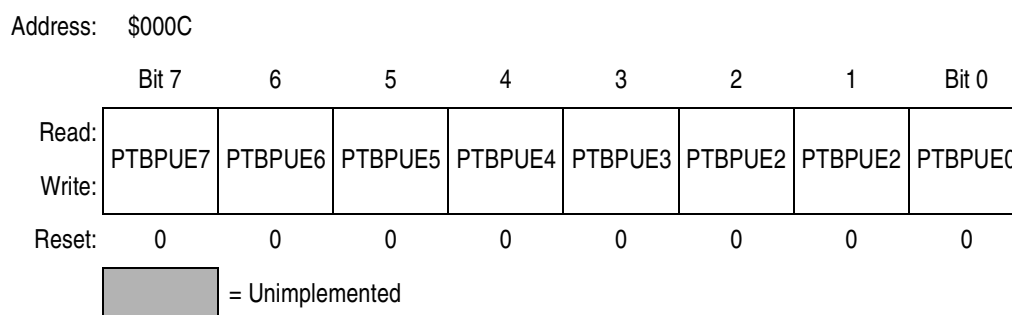
**Table 12-2. Port B Pin Functions**

DDRB Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB		Accesses to PTB	
			Read/Write	Read	Write	
0	X <sup>(1)</sup>	Input, Hi-Z <sup>(2)</sup>	DDRB7–DDRB0	Pin	PTB7–PTB0 <sup>(3)</sup>	
1	X	Output	DDRB7–DDRB0	Pin	PTB7–PTB0	

1. X = don't care
2. Hi-Z = high impedance
3. Writing affects data register, but does not affect the input.

### 12.4.3 Port B Input Pullup Enable Register

The port B input pullup enable register (PTBPUE) contains a software configurable pullup device for each of the eight port B pins. Each bit is individually configurable and requires the corresponding data direction register, DDRBx, be configured as input. Each pullup device is automatically and dynamically disabled when its corresponding DDRBx bit is configured as output.



**Figure 12-9. Port B Input Pullup Enable Register (PTBPUE)**

## PTBPUE[7:0] — Port B Input Pullup Enable Bits

These read/write bits are software programmable to enable pullup devices on port B pins

1 = Corresponding port B pin configured to have internal pull if its DDRB bit is set to 0

0 = Pullup device is disconnected on the corresponding port B pin regardless of the state of its DDRB bit.

**Table 12-3** summarizes the operation of the port B pins.

**Table 12-3. Port B Pin Functions**

PTBPUE Bit	DDR B Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PTB	
				Read/Write	Read	Write
1	0	X <sup>(1)</sup>	Input, V <sub>DD</sub> <sup>(2)</sup>	DDR B7–DDR B0	Pin	PTB7–PTB0 <sup>(3)</sup>
0	0	X	Input, Hi-Z <sup>(4)</sup>	DDR B7–DDR B0	Pin	PTB7–PTB0 <sup>(3)</sup>
X	1	X	Output	DDR B7–DDR B0	PTB7–PTB0	PTB7–PTB0

1. X = don't care
2. I/O pin pulled to V<sub>DD</sub> by internal pullup.
3. Writing affects data register, but does not affect input.
4. Hi-Z = high impedance

## Section 13. External Interrupt (IRQ)

### 13.1 Contents

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### 13.2 Introduction

The  $\overline{\text{IRQ}}$  pin (external interrupt), shared with PTA2 (general purpose input) and keyboard interrupt (KBI), provides a maskable interrupt input.

### 13.3 Features

Features of the IRQ module include the following:

- External interrupt pin,  $\overline{\text{IRQ}}$
- $\overline{\text{IRQ}}$  interrupt control bits
- Hysteresis buffer
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Selectable internal pullup resistor

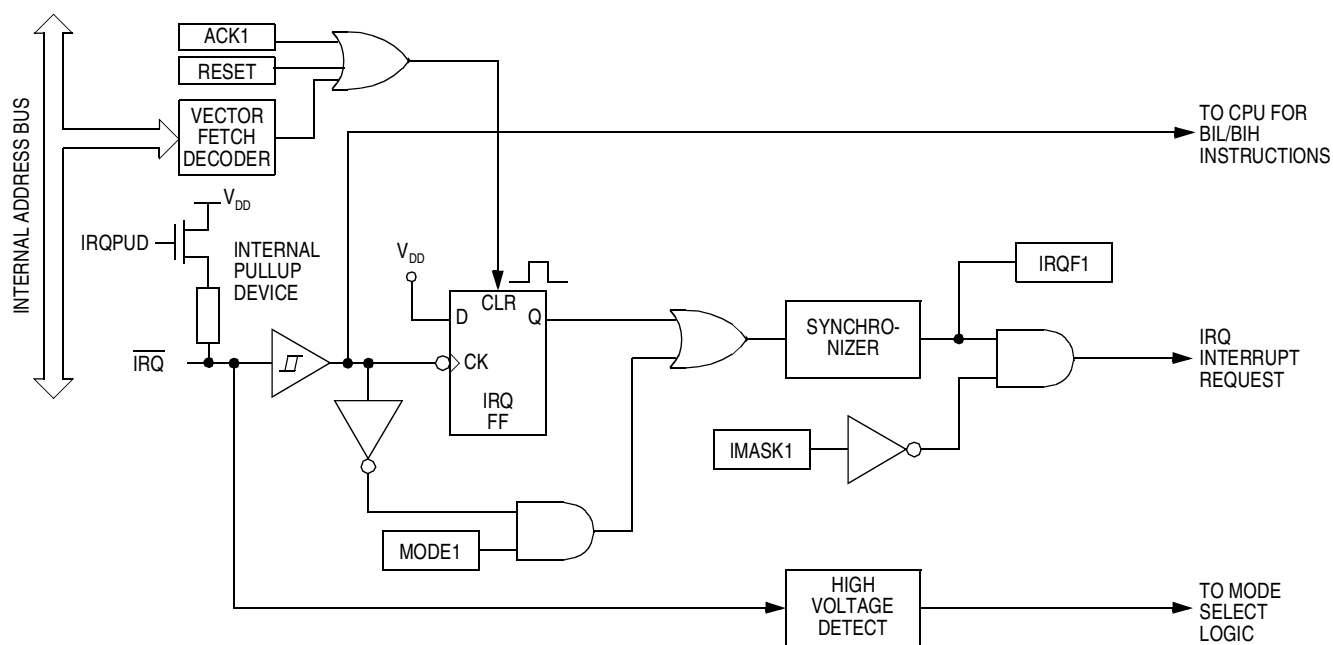
## 13.4 Functional Description

$\overline{\text{IRQ}}$  pin functionality is enabled by setting configuration register 2 (CONFIG2) IRQEN bit accordingly. A 0 disables the IRQ function and  $\overline{\text{IRQ}}$  will assume the other shared functionalities. A 1 enables the IRQ function.

A logic 0 applied to the external interrupt pin can latch a central processor unit (CPU) interrupt request. **Figure 13-1** shows the structure of the IRQ module.

Interrupt signals on the  $\overline{\text{IRQ}}$  pin are latched into the IRQ latch. An interrupt latch remains set until one of the following actions occurs:

- Vector fetch — A vector fetch automatically generates an interrupt acknowledge signal that clears the IRQ latch.
- Software clear — Software can clear the interrupt latch by writing to the acknowledge bit in the interrupt status and control register (ISCR). Writing a logic 1 to the ACK1 bit clears the IRQ latch.
- Reset — A reset automatically clears the interrupt latch.



**Figure 13-1. IRQ Module Block Diagram**

The external interrupt pin is falling-edge-triggered and is software-configurable to be either falling-edge or falling-edge and low-level triggered. The MODE1 bit in the ISCR controls the triggering sensitivity of the  $\overline{\text{IRQ}}$  pin.

When the interrupt pin is edge-triggered only, the CPU interrupt request remains set until a vector fetch, software clear, or reset occurs.

When the interrupt pin is both falling-edge and low-level triggered, the CPU interrupt request remains set until both of the following occur:

- Vector fetch or software clear
- Return of the interrupt pin to logic 1

The vector fetch or software clear may occur before or after the interrupt pin returns to logic 1. As long as the pin is low, the interrupt request remains pending. A reset will clear the latch and the MODE1 control bit, thereby clearing the interrupt even if the pin stays low.

When set, the IMASK1 bit in the ISCR mask all external interrupt requests. A latched interrupt request is not presented to the interrupt priority logic unless the IMASK1 bit is clear.

**NOTE:** *The interrupt mask (I) in the condition code register (CCR) masks all interrupt requests, including external interrupt requests. See [7.7 Exception Control](#).*

**Figure 13-2** provides a summary of the IRQ I/O register.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$001D	IRQ Status and Control Register (INTSCR) <a href="#">See page 178.</a>	Read:	0	0	0	0	IRQF1	0	IMASK1	MODE1
		Write:						ACK1		
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

**Figure 13-2. IRQ I/O Register Summary**

### 13.5 $\overline{\text{IRQ}}$ Pin

A logic 0 on the  $\overline{\text{IRQ}}$  pin can latch an interrupt request into the IRQ latch. A vector fetch, software clear, or reset clears the IRQ latch.

If the MODE1 bit is set, the  $\overline{\text{IRQ}}$  pin is both falling-edge sensitive and low-level sensitive. With MODE1 set, both of the following actions must occur to clear IRQ:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the latch. Software may generate the interrupt acknowledge signal by writing a logic 1 to the ACK1 bit in the interrupt status and control register (ISCR). The ACK1 bit is useful in applications that poll the  $\overline{\text{IRQ}}$  pin and require software to clear the IRQ latch. Writing to the ACK1 bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACK1 does not affect subsequent transitions on the  $\overline{\text{IRQ}}$  pin. A falling edge that occurs after writing to the ACK1 bit latches another interrupt request. If the IRQ mask bit, IMASK1, is clear, the CPU loads the program counter with the vector address at locations \$FFFA and \$FFFB.
- Return of the  $\overline{\text{IRQ}}$  pin to logic 1 — As long as the  $\overline{\text{IRQ}}$  pin is at logic 0, IRQ remains active.

The vector fetch or software clear and the return of the  $\overline{\text{IRQ}}$  pin to logic 1 may occur in any order. The interrupt request remains pending as long as the  $\overline{\text{IRQ}}$  pin is at logic 0. A reset will clear the latch and the MODE1 control bit, thereby clearing the interrupt even if the pin stays low.

If the MODE1 bit is clear, the  $\overline{\text{IRQ}}$  pin is falling-edge sensitive only. With MODE1 clear, a vector fetch or software clear immediately clears the IRQ latch.

The IRQF1 bit in the ISCR register can be used to check for pending interrupts. The IRQF1 bit is not affected by the IMASK1 bit, which makes it useful in applications where polling is preferred.

**NOTE:** Use the BIH or BIL instruction to read the logic level on the  $\overline{\text{IRQ}}$  pin.

**NOTE:** When using the level-sensitive interrupt trigger, avoid false interrupts by masking interrupt requests in the interrupt routine.



*An internal pullup resistor to  $V_{DD}$  is connected to the  $\overline{IRQ}$  pin; this can be disabled by setting the  $IRQPUD$  bit in the  $CONFIG2$  register ( $\$001E$ ).*

## 13.6 IRQ Module During Break Interrupts

The system integration module (SIM) controls whether the IRQ latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear the latches during the break state. See [Section 7. System Integration Module \(SIM\)](#).

To allow software to clear the IRQ latch during a break interrupt, write a logic 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latches during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), writing to the ACK1 bit in the IRQ status and control register during the break state has no effect on the IRQ latch.

## 13.7 IRQ Status and Control Register

The IRQ status and control register (ISCR) controls and monitors operation of the IRQ module, see [Section 5. Configuration Register \(CONFIG\)](#).


The ISCR has the following functions:

- Shows the state of the IRQ flag
- Clears the IRQ latch
- Masks IRQ and interrupt request
- Controls triggering sensitivity of the  $\overline{IRQ}$  interrupt pin

## External Interrupt (IRQ)

Address: \$001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF1		IMASK1	MODE1
Write:						ACK1		
Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

**Figure 13-3. IRQ Status and Control Register (INTSCR)**

### IRQF1 — IRQ Flag

This read-only status bit is high when the IRQ interrupt is pending.

1 =  $\overline{\text{IRQ}}$  interrupt pending

0 =  $\overline{\text{IRQ}}$  interrupt not pending

### ACK1 — IRQ Interrupt Request Acknowledge Bit

Writing a logic 1 to this write-only bit clears the IRQ latch. ACK1 always reads as logic 0. Reset clears ACK1.

### IMASK1 — IRQ Interrupt Mask Bit

Writing a logic 1 to this read/write bit disables IRQ interrupt requests. Reset clears IMASK1.

1 = IRQ interrupt requests disabled

0 = IRQ interrupt requests enabled

### MODE1 — IRQ Edge/Level Select Bit

This read/write bit controls the triggering sensitivity of the  $\overline{\text{IRQ}}$  pin. Reset clears MODE1.

1 =  $\overline{\text{IRQ}}$  interrupt requests on falling edges and low levels

0 =  $\overline{\text{IRQ}}$  interrupt requests on falling edges only

## Section 14. Keyboard Interrupt Module (KBI)

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### 14.2 Introduction

The keyboard interrupt module (KBI) provides six independently maskable external interrupts, which are accessible via the PTA0–PTA5 pins, plus one internal maskable interrupt controlled by the auto wake-up logic.


## 14.3 Features

Features of the keyboard interrupt module include:

- Six keyboard interrupt pins with separate keyboard interrupt enable bits and one keyboard interrupt mask
- One internal interrupt controlled by the auto wake-up logic, with separate interrupt enable bit, sharing the same keyboard interrupt mask
- Software configurable pullup device if input pin is configured as input port bit
- Programmable edge-only or edge and level interrupt sensitivity
- Exit from low-power modes

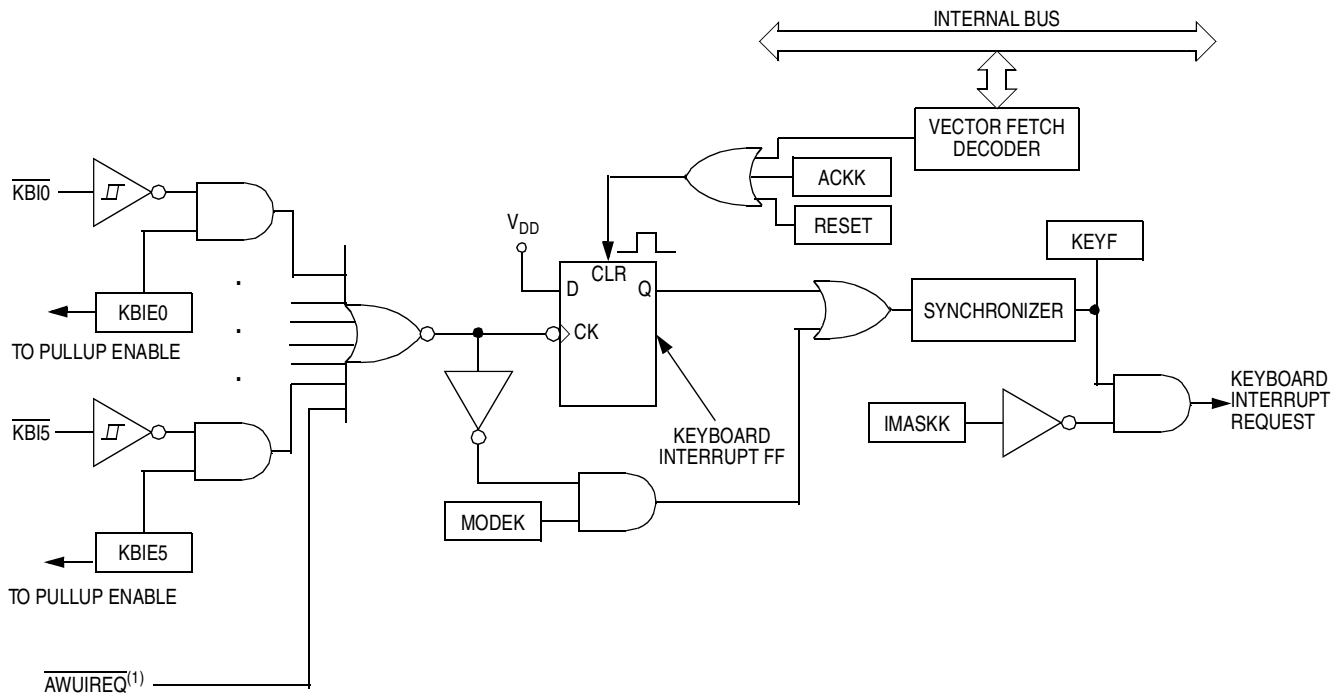
**Figure 14-1** provides a summary of the input/output (I/O) registers

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$001A	Keyboard Status and Control Register (KBSCR) <a href="#">See page 185.</a>	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:						ACKK		
		Reset:	0	0	0	0	0	0	0	0
\$001B	Keyboard Interrupt Enable Register (KBIER) <a href="#">See page 186.</a>	Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

**Figure 14-1. KBI I/O Register Summary**

## 14.4 Functional Description



1. For AWUGEN logic refer to [Figure 14-5](#).

**Figure 14-2. Keyboard Interrupt Block Diagram**

Writing to the KBIE0–KBIE5 bits in the keyboard interrupt enable register (KBIER) independently enables or disables each port A pin as a keyboard interrupt pin. Enabling a keyboard interrupt pin in port A also enables its internal pullup device irrespective of PTAPUE<sub>x</sub> bits in the port A input pullup enable register (see [12.3.3 Port A Input Pullup Enable Register](#)). A logic 0 applied to an enabled keyboard interrupt pin latches a keyboard interrupt request.

Writing the AWUIE bit in the keyboard interrupt enable register enables or disables the auto wake-up interrupt input (see [Figure 14-5](#)). A logic 1 applied to the AWUIREQ input with auto wake-up interrupt request enabled, latches a keyboard interrupt request.

## Keyboard Interrupt Module (KBI)

A keyboard interrupt is latched when one or more keyboard interrupt inputs goes low after all were high. The MODEK bit in the keyboard status and control register controls the triggering mode of the keyboard interrupt.

- If the keyboard interrupt is edge-sensitive only, a falling edge on a keyboard interrupt input does not latch an interrupt request if another keyboard pin is already low. To prevent losing an interrupt request on one input because another input is still low, software can disable the latter input while it is low.
- If the keyboard interrupt is falling edge and low-level sensitive, an interrupt request is present as long as any keyboard interrupt input is low.

If the MODEK bit is set, the keyboard interrupt inputs are both falling edge and low-level sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a logic 1 to the ACKK bit in the keyboard status and control register (KBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt inputs and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt inputs. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the central processor unit (CPU) loads the program counter with the vector address at locations \$FFE0 and \$FFE1.
- Return of all enabled keyboard interrupt inputs to logic 1 — As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set. The auto wake-up interrupt input, AWUIREQ, will be cleared only by writing to ACKK bit in KBSCR or reset.

The vector fetch or software clear and the return of all enabled keyboard interrupt pins to logic 1 may occur in any order.

If the MODEK bit is clear, the keyboard interrupt pin is falling-edge sensitive only. With MODEK clear, a vector fetch or software clear immediately clears the keyboard interrupt request.

Reset clears the keyboard interrupt request and the MODEK bit, clearing the interrupt request even if a keyboard interrupt input stays at logic 0.

The keyboard flag bit (KEYF) in the keyboard status and control register can be used to see if a pending interrupt exists. The KEYF bit is not affected by the keyboard interrupt mask bit (IMASKK) which makes it useful in applications where polling is preferred.

To determine the logic level on a keyboard interrupt pin, use the data direction register to configure the pin as an input and then read the data register.

**NOTE:** *Setting a keyboard interrupt enable bit (KBIE<sub>x</sub>) forces the corresponding keyboard interrupt pin to be an input, overriding the data direction register. However, the data direction register bit must be a logic 0 for software to read the pin.*

Auto wake-up latch, AWUL, can be read directly from the bit 6 position of port A data register (PTA). This is a read-only bit which is occupying and empty bit position on PTA. No PTA associated registers, such as PTA6 data, PTA6 direction, and PTA6 pullup exist for this bit.

#### 14.4.1 Keyboard Initialization

When a keyboard interrupt pin is enabled, it takes time for the internal pullup to reach a logic 1. Therefore a false interrupt can occur as soon as the pin is enabled. This does not apply to an auto wake-up interrupt, which is internally generated without pullup.

To prevent a false interrupt on keyboard initialization:

1. Mask keyboard interrupts by setting the IMASKK bit in the keyboard status and control register.
2. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.
3. Write to the ACKK bit in the keyboard status and control register to clear any false interrupts.
4. Clear the IMASKK bit.

An interrupt signal on an edge-triggered pin can be acknowledged immediately after enabling the pin. An interrupt signal on an edge- and level-triggered interrupt pin must be acknowledged after a delay that depends on the external load.

Another way to avoid a false interrupt:

1. Configure the keyboard pins as outputs by setting the appropriate DDRA bits in the data direction register A.
2. Write logic 1s to the appropriate port A data register bits.
3. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.

### 14.4.2 Keyboard Status and Control Register


The keyboard status and control register (KBSCR):

- Flags keyboard interrupt requests
- Acknowledges keyboard interrupt requests
- Masks keyboard interrupt requests
- Controls keyboard interrupt triggering sensitivity



Address: \$001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
Write:						ACKK		
Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

**Figure 14-3. Keyboard Status and Control Register (KBSCR)**

Bits 7–4 — Not used

These read-only bits always read as logic 0s.

**KEYF** — Keyboard Flag Bit

This read-only bit is set when a keyboard interrupt is pending on port A or auto wake-up. Reset clears the KEYF bit.

1 = Keyboard interrupt pending

0 = No keyboard interrupt pending

**ACKK** — Keyboard Acknowledge Bit

Writing a logic 1 to this write-only bit clears the keyboard interrupt request on port A and auto wake-up logic. ACKK always reads as logic 0. Reset clears ACKK.

**IMASKK** — Keyboard Interrupt Mask Bit

Writing a logic 1 to this read/write bit prevents the output of the keyboard interrupt mask from generating interrupt requests on port A or auto wake-up. Reset clears the IMASKK bit.

1 = Keyboard interrupt requests masked

0 = Keyboard interrupt requests not masked

**MODEK** — Keyboard Triggering Sensitivity Bit

This read/write bit controls the triggering sensitivity of the keyboard interrupt pins on port A and auto wake-up. Reset clears MODEK.

1 = Keyboard interrupt requests on falling edges and low levels

0 = Keyboard interrupt requests on falling edges only

## 14.4.3 Keyboard Interrupt Enable Register

The port A keyboard interrupt enable register (KBIER) enables or disables each port A pin or auto wake-up to operate as a keyboard interrupt input.

Address: \$001B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
Write:								
Reset:	0	0	0	0	0	0	0	0

**Figure 14-4. Keyboard Interrupt Enable Register (KBIER)**

### KBIE5–KBIE0 — Port A Keyboard Interrupt Enable Bits

Each of these read/write bits enables the corresponding keyboard interrupt pin on port A to latch interrupt requests. Reset clears the keyboard interrupt enable register.

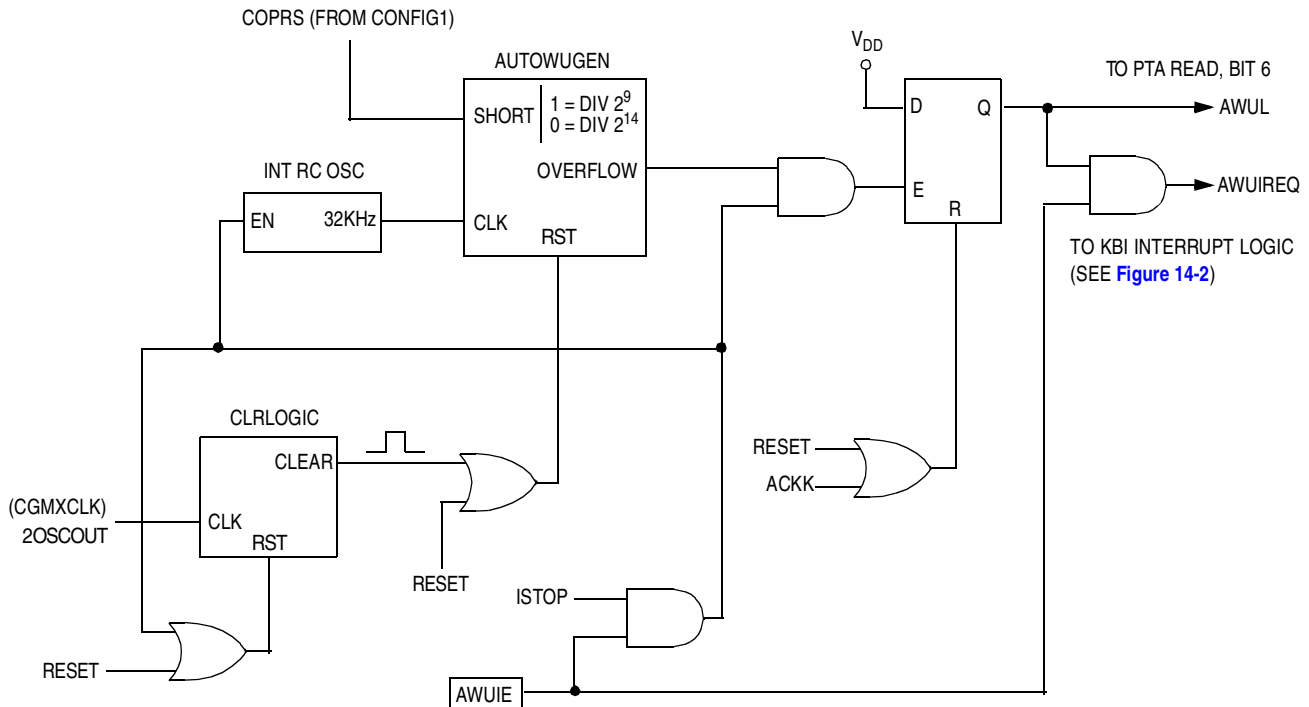
- 1 = KBIx pin enabled as keyboard interrupt pin
- 0 = KBIx pin not enabled as keyboard interrupt pin

### AWUIE — Auto Wake-up Interrupt Enable Bit

This read/write bit enables the auto wake-up interrupt input to latch interrupt requests. Reset clears AWUIE.

- 1 = Auto wake-up enabled as interrupt input
- 0 = Auto wake-up not enabled as interrupt input

### 14.4.4 Auto Wake-up Interrupt Request



**Figure 14-5. Auto Wake-up Interrupt Request Generation Logic**

The function of the auto wake-up logic is to generate periodic wake-up requests to bring the microcontroller unit (MCU) out of stop mode. The wake-up requests are treated as regular keyboard interrupt requests, with the difference that instead of a pin, the interrupt signal is generated by an internal logic.

Entering stop mode will enable the auto wake-up generation logic. An internal RC oscillator (exclusive for the auto wake-up feature) drives the wake-up request generator. Once the overflow count is reached in the generator counter, a wake-up request, AWUIREQ, is latched and sent to the KBI logic (see [Figure 14-2](#)).

Wake-up interrupt requests will only be serviced if the associated interrupt enable bit, AWUIE, in KBIER is set.

The overflow count can be selected from two options defined by the COPRS bit in CONFIG1. This bit was “borrowed” from the computer operating properly (COP) using the fact that the COP feature is idle (no MCU clock available) in stop mode. The typical values of the periodic wake-up request (5 V, room temperature) are:

- COPRS = 0: 512 ms
- COPRS = 1: 16 ms

The auto wake-up RC oscillator is highly dependent on operating voltage and temperature.

The wake-up request is latched to allow the interrupt source identification. The latched value, AWUL, can be read directly from the bit 6 position of PTA data register. This is a read-only bit which is occupying an empty bit position on PTA. No PTA associated registers, such as PTA6 data, PTA6 direction, and PTA6 pullup exist for this bit. The latch can be cleared by writing to the ACKK bit in the KBSCR register. Reset also clears the latch. AWUIE bit in KBI interrupt enable register (see [Figure 14-2](#)) has no effect on AWUL reading.

### 14.5 Wait Mode

The keyboard module remains active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

### 14.6 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

## 14.7 Keyboard Module During Break Interrupts

The system integration module (SIM) controls whether the keyboard interrupt latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state.

To allow software to clear the keyboard interrupt latch during a break interrupt, write a logic 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latch during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), writing to the keyboard acknowledge bit (ACKK) in the keyboard status and control register during the break state has no effect.

## Keyboard Interrupt Module (KBI)

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## Section 15. Computer Operating Properly (COP)

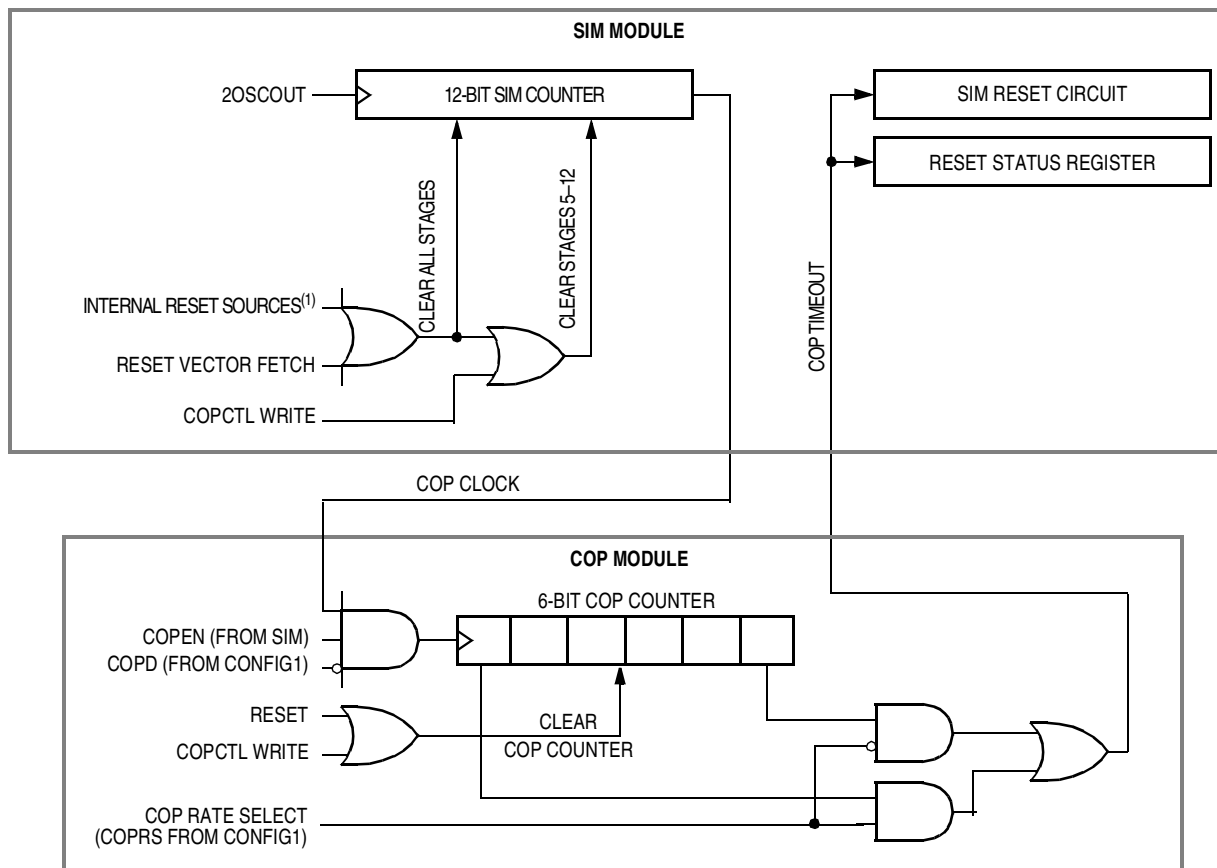
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### 15.2 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the configuration 1 (CONFIG1) register.

## 15.3 Functional Description



1. See [Section 7. System Integration Module \(SIM\)](#) for more details.

**Figure 15-1. COP Block Diagram**

The COP counter is a free-running 6-bit counter preceded by the 12-bit system integration module (SIM) counter. If not cleared by software, the COP counter overflows and generates an asynchronous reset after  $2^{18} - 2^4$  or  $2^{13} - 2^4$  20SCOUT cycles; depending on the state of the COP rate select bit, COPRS, in configuration register 1. With a  $2^{18} - 2^4$  20SCOUT cycle overflow option, a 8-MHz crystal gives a COP timeout period of 32.766 ms. Writing any value to location \$FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 12–5 of the SIM counter.



**NOTE:** Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.

A COP reset pulls the  $\overline{\text{RST}}$  pin low for  $32 \times 2\text{OSCOUT}$  cycles and sets the COP bit in the reset status register (RSR). See [7.9.2 SIM Reset Status Register](#).

**NOTE:** Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.

## 15.4 I/O Signals

The following paragraphs describe the signals shown in [Figure 15-1](#).

### 15.4.1 2OSCOUT

2OSCOUT is the oscillator output signal. 2OSCOUT frequency is equal to the crystal frequency or the RC-oscillator frequency.

### 15.4.2 COPCTL Write

Writing any value to the COP control register (CCOPCTL) (see [15.5 COP Control Register](#)) clears the COP counter and clears bits 12–5 of the SIM counter. Reading the COP control register returns the low byte of the reset vector.

### 15.4.3 Power-On Reset

The power-on reset (POR) circuit in the SIM clears the SIM counter  $4096 \times 2\text{OSCOUT}$  cycles after power up.

## 15.4.4 Internal Reset

An internal reset clears the SIM counter and the COP counter.

## 15.4.5 Reset Vector Fetch

A reset vector fetch occurs when the vector address appears on the data bus. A reset vector fetch clears the SIM counter.

## 15.4.6 COPD (COP Disable)

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register (CONFIG). See [Section 5. Configuration Register \(CONFIG\)](#).

## 15.4.7 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register 1 (CONFIG1). See [Section 5. Configuration Register \(CONFIG\)](#).

## 15.5 COP Control Register

The COP control register (COPCTL) is located at address \$FFFF and overlaps the reset vector. Writing any value to \$FFFF clears the COP counter and starts a new timeout period. Reading location \$FFFF returns the low byte of the reset vector.

Address: \$FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LOW BYTE OF RESET VECTOR							
Write:	CLEAR COP COUNTER							
Reset:	Unaffected by reset							

**Figure 15-2. COP Control Register (COPCTL)**

## 15.6 Interrupts

The COP does not generate CPU interrupt requests.

## 15.7 Monitor Mode

The COP is disabled in monitor mode when  $V_{DD} + V_{HI}$  is present on the  $\overline{IRQ}$  pin.

## 15.8 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

### 15.8.1 Wait Mode

The COP continues to operate during wait mode. To prevent a COP reset during wait mode, periodically clear the COP counter.

### 15.8.2 Stop Mode

Stop mode turns off the 2OSCOU input to the COP and clears the SIM counter. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

## 15.9 COP Module During Break Mode

The COP is disabled during a break interrupt with monitor mode when BDCOP bit is set in break auxiliary register (BRKAR).



## Section 16. Low-Voltage Inhibit (LVI)

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### 16.2 Introduction

This section describes the low-voltage inhibit (LVI) module, which monitors the voltage on the  $V_{DD}$  pin and can force a reset when the  $V_{DD}$  voltage falls below the LVI trip falling voltage,  $V_{TRIPF}$ .

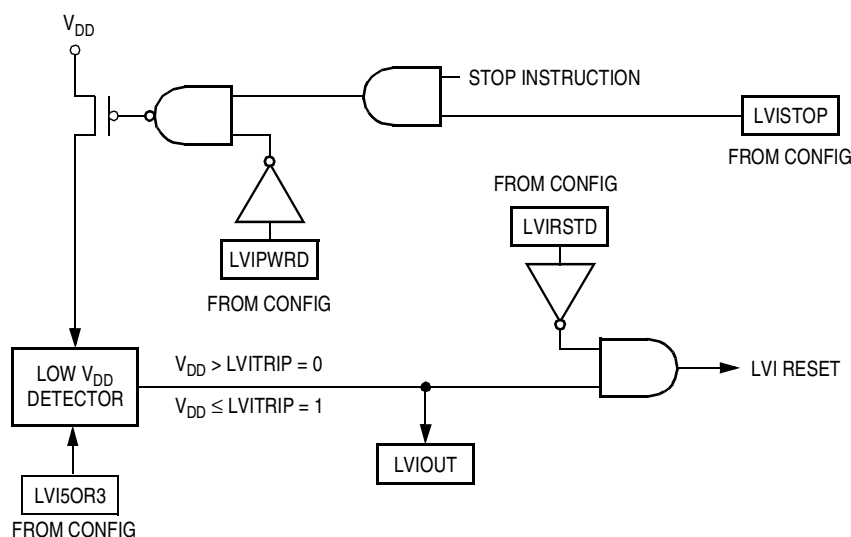
## 16.3 Features

Features of the LVI module include:

- Programmable LVI reset
- Programmable power consumption
- Selectable LVI trip voltage
- Programmable stop mode operation

## 16.4 Functional Description

**Figure 16-1** shows the structure of the LVI module. LVISTOP, LVIPWRD, LVI5OR3, and LVIRSTD are user selectable options found in the configuration register (CONFIG1). See [Section 5. Configuration Register \(CONFIG\)](#).



**Figure 16-1. LVI Module Block Diagram**

The LVI is enabled out of reset. The LVI module contains a bandgap reference circuit and comparator. Clearing the LVI power disable bit, LVIPWRD, enables the LVI to monitor  $V_{DD}$  voltage. Clearing the LVI reset disable bit, LVIRSTD, enables the LVI module to generate a reset when  $V_{DD}$  falls below a voltage,  $V_{TRIP}$ . Setting the LVI enable in stop

mode bit, LVISTOP, enables the LVI to operate in stop mode. Setting the LVI 5-V or 3-V trip point bit, LVI5OR3, enables the trip point voltage,  $V_{TRIPF}$ , to be configured for 5-V operation. Clearing the LVI5OR3 bit enables the trip point voltage,  $V_{TRIPF}$ , to be configured for 3-V operation. The actual trip thresholds are specified in [18.6 5-V DC Electrical Characteristics](#) and [18.9 3-V DC Electrical Characteristics](#).

**NOTE:** *After a power-on reset, the LVI's default mode of operation is 3 volts. If a 5-V system is used, the user must set the LVI5OR3 bit to raise the trip point to 5-V operation.*

*If the user requires 5-V mode and sets the LVI5OR3 bit after power-on reset while the  $V_{DD}$  supply is not above the  $V_{TRIPR}$  for 5-V mode, the microcontroller unit (MCU) will immediately go into reset. The next time the LVI releases the reset, the supply will be above the  $V_{TRIPR}$  for 5-V mode.*

Once an LVI reset occurs, the MCU remains in reset until  $V_{DD}$  rises above a voltage,  $V_{TRIPR}$ , which causes the MCU to exit reset. See [Section 7. System Integration Module \(SIM\)](#) for the reset recovery sequence.

The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR) and can be used for polling LVI operation when the LVI reset is disabled.

### 16.4.1 Polled LVI Operation

In applications that can operate at  $V_{DD}$  levels below the  $V_{TRIPF}$  level, software can monitor  $V_{DD}$  by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be at logic 0 to enable the LVI module, and the LVIRSTD bit must be at logic 1 to disable LVI resets.

### 16.4.2 Forced Reset Operation

In applications that require  $V_{DD}$  to remain above the  $V_{TRIPF}$  level, enabling LVI resets allows the LVI module to reset the MCU when  $V_{DD}$  falls below the  $V_{TRIPF}$  level. In the configuration register, the LVIPWRD and LVIRSTD bits must be at logic 0 to enable the LVI module and to enable LVI resets.

### 16.4.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having  $V_{DD}$  fall below  $V_{TRIPF}$ ), the LVI will maintain a reset condition until  $V_{DD}$  rises above the rising trip point voltage,  $V_{TRIPR}$ . This prevents a condition in which the MCU is continually entering and exiting reset if  $V_{DD}$  is approximately equal to  $V_{TRIPF}$ .  $V_{TRIPR}$  is greater than  $V_{TRIPF}$  by the hysteresis voltage,  $V_{HYS}$ .

### 16.4.4 LVI Trip Selection

The LVI5OR3 bit in the configuration register selects whether the LVI is configured for 5-V or 3-V protection.

**NOTE:** *The microcontroller is guaranteed to operate at a minimum supply voltage. The trip point ( $V_{TRIPF}$  [5 V] or  $V_{TRIPF}$  [3 V]) may be lower than this. See [18.6 5-V DC Electrical Characteristics](#) and [18.9 3-V DC Electrical Characteristics](#) for the actual trip point voltages.*



## 16.5 LVI Status Register

The LVI status register (LVISR) indicates if the  $V_{DD}$  voltage was detected below the  $V_{TRIPF}$  level while LVI resets have been disabled.

Address: \$FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	0	0	0	0	0	R
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented
  = Reserved

**Figure 16-2. LVI Status Register (LVISR)**

### LVIOUT — LVI Output Bit

This read-only flag becomes set when the  $V_{DD}$  voltage falls below the  $V_{TRIPF}$  trip voltage and is cleared when  $V_{DD}$  voltage rises above  $V_{TRIPR}$ . The difference in these threshold levels results in a hysteresis that prevents oscillation into and out of reset (see [Table 16-1](#)). Reset clears the LVIOUT bit.

**Table 16-1. LVIOUT Bit Indication**

$V_{DD}$	LVIOUT
$V_{DD} > V_{TRIPR}$	0
$V_{DD} < V_{TRIPF}$	1
$V_{TRIPF} < V_{DD} < V_{TRIPR}$	Previous value

### 16.6 LVI Interrupts

The LVI module does not generate interrupt requests.

### 16.7 Low-Power Modes

The STOP and WAIT instructions put the MCU in low power-consumption standby modes.

#### 16.7.1 Wait Mode

If enabled, the LVI module remains active in wait mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of wait mode.

#### 16.7.2 Stop Mode

When the LVIPWRD bit in the configuration register is cleared and the LVISTOP bit in the configuration register is set, the LVI module remains active in stop mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of stop mode.

## Section 17. Break Module (BREAK)

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### 17.2 Introduction

This section describes the break module. The break module can generate a break interrupt that stops normal program flow at a defined address to enter a background program.

### 17.3 Features

Features of the break module include:

- Accessible input/output (I/O) registers during the break Interrupt
- Central processor unit (CPU) generated break interrupts
- Software-generated break interrupts
- Computer operating properly (COP) disabling during break interrupts

### 17.4 Functional Description

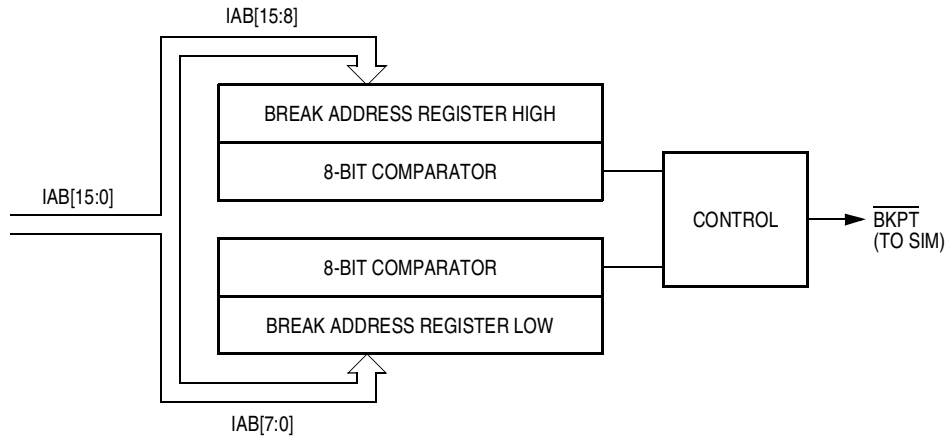
When the internal address bus matches the value written in the break address registers, the break module issues a breakpoint signal ( $\overline{\text{BKPT}}$ ) to the system integration module (SIM). The SIM then causes the CPU to load the instruction register with a software interrupt instruction (SWI) after completion of the current CPU instruction. The program counter vectors to \$FFFC and \$FFFD (\$FEFC and \$FEFD in monitor mode).

The following events can cause a break interrupt to occur:

- A CPU generated address (the address in the program counter) matches the contents of the break address registers.
- Software writes a logic 1 to the BRKA bit in the break status and control register.

When a CPU generated address matches the contents of the break address registers, the break interrupt begins after the CPU completes its current instruction. A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the microcontroller unit (MCU) to normal operation. **Figure 17-1** shows the structure of the break module.

**Figure 17-2** provides a summary of the I/O registers.



**Figure 17-1. Break Module Block Diagram**

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$FE00	Break Status Register (BSR) <a href="#">See page 210.</a>	Read:	R	R	R	R	R	SBSW	R	
		Write:						Note <sup>(1)</sup>		
		Reset:	0							
\$FE02	Break Auxiliary Register (BRKAR) <a href="#">See page 209.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FE03	Break Flag Control Register (BFCR) <a href="#">See page 211.</a>	Read:	BCFE	R	R	R	R	R	R	
		Write:								
		Reset:	0							
\$FE09	Break Address High Register (BRKH) <a href="#">See page 208.</a>	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FE0A	Break Address Low Register (BRKL) <a href="#">See page 208.</a>	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FE0B	Break Status and Control Register (BRKSCR) <a href="#">See page 207.</a>	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

1. Writing a logic 0 clears SBSW.

= Unimplemented      R = Reserved

**Figure 17-2. Break I/O Register Summary**

### 17.4.1 Flag Protection During Break Interrupts

The system integration module (SIM) controls whether or not module status bits can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See [7.9.3 Break Flag Control Register](#) and the **Break Interrupts** subsection for each module.

### 17.4.2 CPU During Break Interrupts

The CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with \$FFFC:\$FFFD (\$FEFC:\$FEFD in monitor mode)

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

### 17.4.3 TIM During Break Interrupts

A break interrupt stops the timer counter.

### 17.4.4 COP During Break Interrupts

The COP is disabled during a break interrupt with monitor mode when BDCOP bit is set in break auxiliary register (BRKAR).

## 17.5 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- Break status register (BSR)
- Break flag control register (BFCR)

### 17.5.1 Break Status and Control Register

The break status and control register (BRKSCR) contains break module enable and status bits.

Address: \$FE0B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BRKE	BRKA	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

**Figure 17-3. Break Status and Control Register (BRKSCR)**

#### BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a logic 0 to bit 7. Reset clears the BRKE bit.

- 1 = Breaks enabled on 16-bit address match
- 0 = Breaks disabled

#### BRKA — Break Active Bit

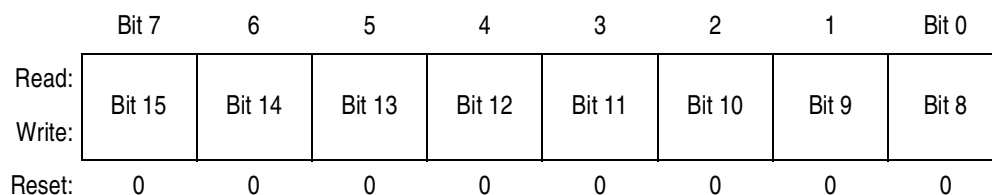
This read/write status and control bit is set when a break address match occurs. Writing a logic 1 to BRKA generates a break interrupt. Clear BRKA by writing a logic 0 to it before exiting the break routine. Reset clears the BRKA bit.

- 1 = Break address match
- 0 = No break address match

## 17.5.2 Break Address Registers

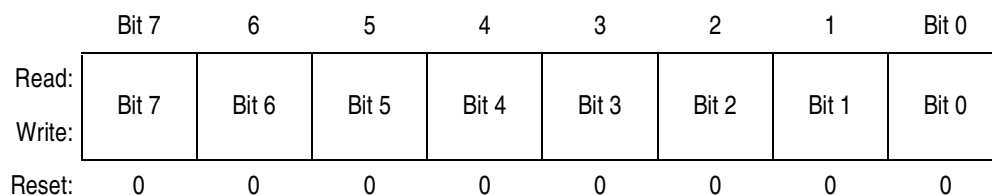
The break address registers (BRKH and BRKL) contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.

Address: \$FE09



**Figure 17-4. Break Address Register High (BRKH)**

Address: \$FE0A



**Figure 17-5. Break Address Register Low (BRKL)**



### 17.5.3 Break Auxiliary Register

The break auxiliary register (BRKAR) contains a bit that enables software to disable the COP while the MCU is in a state of break interrupt with monitor mode.

Address: \$FE02

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	BDCOP
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

**Figure 17-6. Break Auxiliary Register (BRKAR)**

#### BDCOP — Break Disable COP Bit

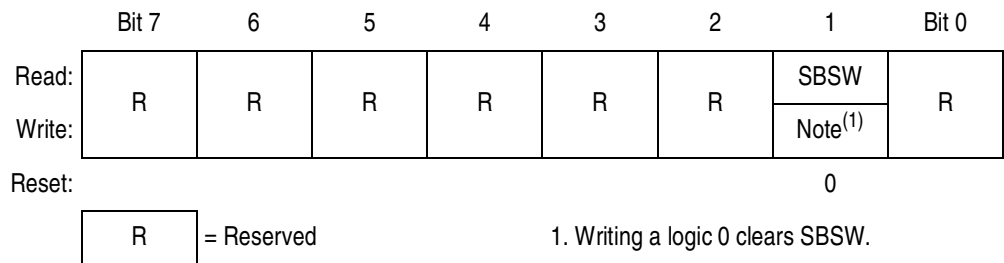
This read/write bit disables the COP during a break interrupt. Reset clears the BDCOP bit.

- 1 = COP disabled during break interrupt
- 0 = COP enabled during break interrupt.

## 17.5.4 Break Status Register

The break status register (BSR) contains a flag to indicate that a break caused an exit from stop or wait mode.

Address: \$FE00



**Figure 17-7. Break Status Register (BSR)**

### SBSW — SIM Break Stop/Wait

This status bit is useful in applications requiring a return to wait or stop mode after exiting from a break interrupt. Clear SBSW by writing a logic 0 to it. Reset clears SBSW.

1 = Stop mode or wait mode was exited by break interrupt

0 = Stop mode or wait mode was not exited by break interrupt

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it. The following code is an example of this. Writing 0 to the SBSW bit clears it.

```

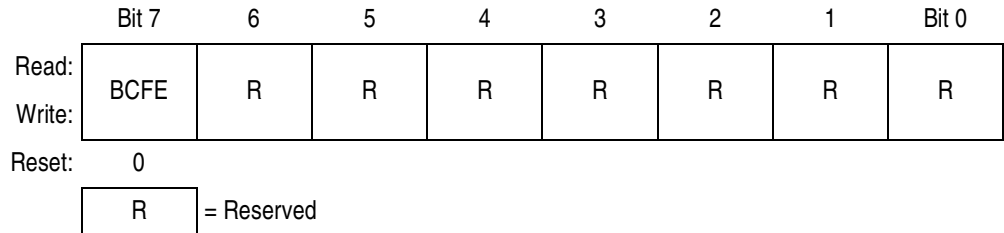
; This code works if the H register has been pushed onto the stack in the break
; service routine software. This code should be executed at the end of the
; break service routine software.
HIBYTE EQU 5
LOBYTE EQU 6
; If not SBSW, do RTI
BRCLR SBSW,BSR, RETURN ; See if wait mode or stop mode was exited
; by break.
TST LOBYTE,SP ; If RETURNLO is not zero,
BNE DOLO ; then just decrement low byte.
DEC HIBYTE,SP ; Else deal with high byte, too.
DOLO DEC LOBYTE,SP ; Point to WAIT/STOP opcode.
RETURN PULH ; Restore H register.
RTI

```

### 17.5.5 Break Flag Control Register

The break control register (BFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.

Address: \$FE03



**Figure 17-8. Break Flag Control Register (BFCR)**

#### BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break

0 = Status bits not clearable during break

## 17.6 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes. If enabled, the break module will remain enabled in wait and stop modes. However, since the internal address bus does not increment in these modes, a break interrupt will never be triggered.

## Break Module (BREAK)

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## Section 18. Electrical Specifications

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### 18.2 Introduction

This section contains electrical and timing specifications.

## 18.3 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the microcontroller unit (MCU) can be exposed without permanently damaging it.

**NOTE:** *This device is not guaranteed to operate properly at the maximum ratings. Refer to [18.6 5-V DC Electrical Characteristics](#) and [18.9 3-V DC Electrical Characteristics](#) for guaranteed operating conditions.*

Characteristic <sup>(1)</sup>	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to +6.0	V
Input voltage	$V_{IN}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Mode entry voltage, $\overline{IRQ}$ pin	$V_{DD} + V_{HI}$	$V_{SS} - 0.3$ to +9.0	V
Maximum current per pin excluding PTA0–PTA5, $V_{DD}$ , and $V_{SS}$	I	±15	mA
Maximum current for pins PTA0–PTA5	$I_{PTA0} - I_{PTA4}$	±25	mA
Storage temperature	$T_{STG}$	-55 to +150	°C
Maximum current out of $V_{SS}$	$I_{MVSS}$	100	mA
Maximum current into $V_{DD}$	$I_{MVDD}$	100	mA

1. Voltages references to  $V_{SS}$ .

**NOTE:** *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that  $V_{IN}$  and  $V_{OUT}$  be constrained to the range  $V_{SS} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{DD}$ . Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either  $V_{SS}$  or  $V_{DD}$ .)*

## 18.4 Functional Operating Range

Characteristic	Symbol	Value		Unit
Operating temperature range	$T_A$	-40 to +125 -40 to +85	-40 to +125 -40 to +85	°C
Operating voltage range	$V_{DD}$	5 V ± 10%	3 V ± 10%	V

## 18.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 8-pin PDIP 8-pin SOIC 16-pin PDIP 16-pin SOIC 16-pin TSSOP	$\theta_{JA}$	95 70 66 70 70	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation <sup>(1)</sup>	$P_D$	$P_D = (I_{DD} \times V_{DD})$ $+ P_{I/O} = K/(T_J + 273^\circ\text{C})$	W
Constant <sup>(2)</sup>	K	$P_D \times (T_A + 273^\circ\text{C})$ $+ P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	$T_J$	$T_A + (P_D \times \theta_{JA})$	°C
Maximum junction temperature	$T_{JM}$	100	°C

1. Power dissipation is a function of temperature.

2. K constant unique to the device. K can be determined for a known  $T_A$  and measured  $P_D$ . With this value of K,  $P_D$  and  $T_J$  can be determined for any value of  $T_A$ .

## 18.6 5-V DC Electrical Characteristics

Characteristic <sup>(1)</sup>	Symbol	Min	Typ <sup>(2)</sup>	Max	Unit
Output high voltage $I_{Load} = -2.0$ mA, all I/O pins $I_{Load} = -10.0$ mA, all I/O pins $I_{Load} = -15.0$ mA, PTA0–PTA5 only	$V_{OH}$	$V_{DD}-0.4$ $V_{DD}-1.5$ $V_{DD}-0.8$	— — —	— — —	V
Output low voltage $I_{Load} = 1.6$ mA, all I/O pins $I_{Load} = 10.0$ mA, all I/O pins $I_{Load} = 15.0$ mA, PTA0–PTA5 only	$V_{OL}$	— — —	— — —	0.4 1.5 0.8	V
Input high voltage PTA0–PTA5, PTB0–PTB7, $\overline{RST}$ , $\overline{IRQ}$ , OSC1	$V_{IH}$	$0.7 \times V_{DD}$	—	$V_{DD}$	V
Input low voltage PTA0–PTA5, PTB0–PTB7, $\overline{RST}$ , $\overline{IRQ}$ , OSC1	$V_{IL}$	$V_{SS}$	—	$0.3 \times V_{DD}$	V
DC injection current, all ports	$I_{INJ}$	-2	—	+2	mA
Total dc current injection (sum of all I/O)	$I_{INJTOT}$	-25	—	+25	mA
$V_{DD}$ supply current Run, $f_{OP} = 4$ MHz <sup>(3)</sup> Wait <sup>(4)</sup> Stop <sup>(5)</sup> , -40°C to 85°C	$I_{DD}$	— — —	7 5 1	10 5.5 5	mA mA $\mu$ A
Digital I/O ports Hi-Z leakage current	$I_{IL}$	—	—	$\pm 10$	$\mu$ A
Input current	$I_{IN}$	—	—	$\pm 1$	$\mu$ A
Capacitance Ports (as input or output)	$C_{OUT}$ $C_{IN}$	— —	— —	12 8	pF
POR rearm voltage <sup>(6)</sup>	$V_{POR}$	0	—	100	mV
POR rise time ramp rate <sup>(7)</sup>	$R_{POR}$	0.035	—	—	V/ms
Monitor mode entry voltage	$V_{DD}+V_{HI}$	$V_{DD} + 2.5$	—	$V_{DD} + 4.0$	V
Pullup resistors <sup>(8)</sup> $\overline{RST}$ , $\overline{IRQ}$ , PTA0–PTA5, PTB0–PTB7	$R_{PU}$	16	26	36	k $\Omega$
Low-voltage inhibit reset, trip falling voltage	$V_{TRIPF}$	3.90	4.20	4.50	V

Continued on next page



Characteristic <sup>(1)</sup>	Symbol	Min	Typ <sup>(2)</sup>	Max	Unit
Low-voltage inhibit reset, trip rising voltage	$V_{TRIPR}$	4.00	4.30	4.60	V
Low-voltage inhibit reset/recover hysteresis	$V_{HYS}$	—	100	—	mV

- $V_{DD} = 4.5$  to  $5.5$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$ , unless otherwise noted.
- Typical values reflect average measurements at midpoint of voltage range,  $25^\circ\text{C}$  only.
- Run (operating)  $I_{DD}$  measured using external square wave clock source. All inputs  $0.2$  V from rail. No dc loads. Less than  $100$  pF on all outputs.  $C_L = 20$  pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run  $I_{DD}$ . Measured with all modules enabled.
- Wait  $I_{DD}$  measured using external square wave clock source ( $f_{OP} = 4$  MHz); all inputs  $0.2$  V from rail; no dc loads; less than  $100$  pF on all outputs.  $C_L = 20$  pF on OSC2; all ports configured as inputs; OSC2 capacitance linearly affects wait  $I_{DD}$ .
- Stop  $I_{DD}$  measured with OSC1 grounded, no port pins sourcing current. LVI is disabled.
- Maximum is highest voltage that POR is guaranteed.
- If minimum  $V_{DD}$  is not reached before the internal POR reset is released,  $\overline{RST}$  must be driven low externally until minimum  $V_{DD}$  is reached.
- $R_{PU1}$  and  $R_{PU2}$  are measured at  $V_{DD} = 5.0$  V.

## 18.7 5-V Control Timing

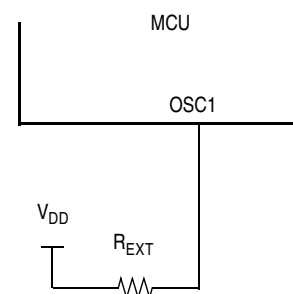
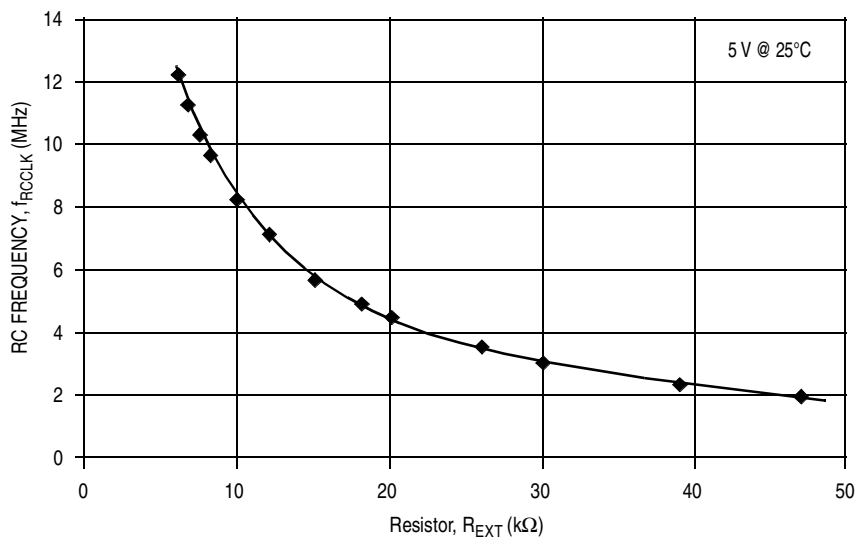
Characteristic <sup>(1)</sup>	Symbol	Min	Max	Unit
Internal operating frequency <sup>(2)</sup>	$f_{OP}$	—	8	MHz
$\overline{RST}$ input pulse width low <sup>(3)</sup>	$t_{IRL}$	750	—	ns

- $V_{DD} = 4.5$  to  $5.5$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$ ; timing shown with respect to  $20\%$   $V_{DD}$  and  $70\%$   $V_{SS}$ , unless otherwise noted.
- Some modules may require a minimum frequency greater than dc for proper operation; see appropriate table for this information.
- Minimum pulse width reset is guaranteed to be recognized. It is possible for a smaller pulse width to cause a reset.

## 18.8 5-V Oscillator Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator frequency	$f_{INTCLK}$	—	3.2	—	MHz
Crystal frequency, XTALCLK	$f_{OSCCLK}$	1	—	32	MHz
RC oscillator frequency, RCCLK	$f_{RCCLK}$	2	—	12	MHz
External clock reference frequency <sup>(1)</sup>	$f_{OSCCLK}$	dc	—	32	MHz
Crystal load capacitance <sup>(2)</sup>	$C_L$	—	—	—	—
Crystal fixed capacitance <sup>(2)</sup>	$C_1$	—	$2 \times C_L$	—	—
Crystal tuning capacitance <sup>(2)</sup>	$C_2$	—	$2 \times C_L$	—	—
Feedback bias resistor	$R_B$	—	10	—	M $\Omega$
Series resistor <sup>(2), (3)</sup>	$R_S$	—	—	—	—
RC oscillator external resistor	$R_{EXT}$	See <a href="#">Figure 18-1</a>			—

1. No more than 10% duty cycle deviation from 50%.
2. Consult crystal vendor data sheet.
3. Not required for high frequency crystals



**Figure 18-1. RC versus Frequency (5 Volts @ 25°C)**

## 18.9 3-V DC Electrical Characteristics

Characteristic <sup>(1)</sup>	Symbol	Min	Typ <sup>(2)</sup>	Max	Unit
Output high voltage $I_{Load} = -0.6$ mA, all I/O pins $I_{Load} = -4.0$ mA, all I/O pins $I_{Load} = -10.0$ mA, PTA0-PTA4 only	$V_{OH}$	$V_{DD}-0.3$ $V_{DD}-1.0$ $V_{DD}-0.6$	— — —	— — —	V
Output low voltage $I_{Load} = 0.5$ mA, all I/O pins $I_{Load} = 6.0$ mA, all I/O pins $I_{Load} = 10.0$ mA, PTA0-PTA5 only	$V_{OL}$	— — —	— — —	0.3 1.0 0.6	V
Input high voltage PTA0-PTA5, PTB0-PTB7, $\overline{RST}$ , $\overline{IRQ}$ , OSC1	$V_{IH}$	$0.7 \times V_{DD}$	—	$V_{DD}$	V
Input low voltage PTA0-PTA5, PTB0-PTB7, $\overline{RST}$ , $\overline{IRQ}$ , OSC1	$V_{IL}$	$V_{SS}$	—	$0.3 \times V_{DD}$	V
DC injection current, all ports	$I_{INJ}$	-2	—	+2	mA
Total dc current injection (sum of all I/O)	$I_{INJTOT}$	-25	—	+25	mA
$V_{DD}$ supply current Run, $f_{OP} = 2$ MHz <sup>(3)</sup> Wait, $f_{OP} = 2$ MHz <sup>(4)</sup> Stop <sup>(5)</sup> , -40°C to 85°C	$I_{DD}$	— — —	5 1 1	8 2.5 5	mA mA μA
Digital I/O ports Hi-Z leakage current	$I_{IL}$	—	—	± 10	μA
Input leakage current	$I_{IN}$	—	—	± 1	μA
Capacitance Ports (as input or output)	$C_{OUT}$ $C_{IN}$	— —	— —	12 8	pF
POR rearm voltage <sup>(6)</sup>	$V_{POR}$	0	—	100	mV
POR rise time ramp rate <sup>(7)</sup>	$R_{POR}$	0.035	—	—	V/ms
Monitor mode entry voltage	$V_{DD}+V_{HI}$	$V_{DD}+2.5$	—	$V_{DD}+4.0$	V
Pullup resistors <sup>(8)</sup> $\overline{RST}$ , $\overline{IRQ}$ , PTA0-PTA5, PTB0-PTB7	$R_{PU}$	16	26	36	kΩ
Low-voltage inhibit reset, trip falling voltage	$V_{TRIPF}$	2.40	2.55	2.70	V

Continued on next page

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## Electrical Specifications

Characteristic <sup>(1)</sup>	Symbol	Min	Typ <sup>(2)</sup>	Max	Unit
Low-voltage inhibit reset, trip rising voltage	$V_{TRIPR}$	2.50	2.65	2.80	V
Low-voltage inhibit reset/recover hysteresis	$V_{HYS}$	—	60	—	mV

- $V_{DD} = 2.7$  to  $3.3$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$ , unless otherwise noted.
- Typical values reflect average measurements at midpoint of voltage range,  $25^\circ\text{C}$  only.
- Run (operating)  $I_{DD}$  measured using external square wave clock source. All inputs  $0.2$  V from rail. No dc loads. Less than  $100$  pF on all outputs.  $C_L = 20$  pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run  $I_{DD}$ . Measured with all modules enabled.
- Wait  $I_{DD}$  measured using external square wave clock source ( $f_{OP} = 4$  MHz); all inputs  $0.2$  V from rail; no dc loads; less than  $100$  pF on all outputs.  $C_L = 20$  pF on OSC2; all ports configured as inputs; OSC2 capacitance linearly affects wait  $I_{DD}$ .
- Stop  $I_{DD}$  measured with OSC1 grounded, no port pins sourcing current. LVI is disabled.
- Maximum is highest voltage that POR is guaranteed.
- If minimum  $V_{DD}$  is not reached before the internal POR reset is released,  $\overline{RST}$  must be driven low externally until minimum  $V_{DD}$  is reached.
- $R_{PU1}$  and  $R_{PU2}$  are measured at  $V_{DD} = 5.0$  V

### 18.10 3-V Control Timing

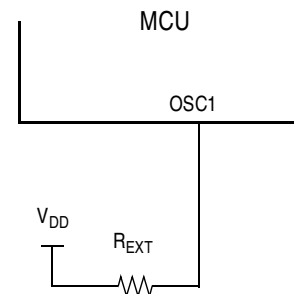
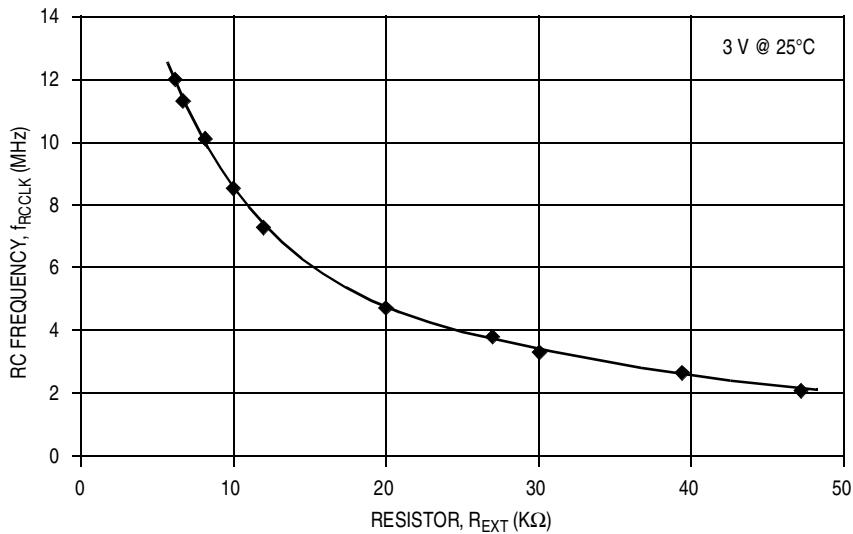
Characteristic <sup>(1)</sup>	Symbol	Min	Max	Unit
Internal operating frequency <sup>(2)</sup>	$f_{OP}$	—	4	MHz
$\overline{RST}$ input pulse width low <sup>(3)</sup>	$t_{IRL}$	1.5	—	$\mu\text{s}$

- $V_{DD} = 2.7$  to  $3.3$  Vdc,  $V_{SS} = 0$  Vdc,  $T_A = T_L$  to  $T_H$ ; timing shown with respect to  $20\%$   $V_{DD}$  and  $70\%$   $V_{DD}$ , unless otherwise noted.
- Some modules may require a minimum frequency greater than dc for proper operation; see appropriate table for this information.
- Minimum pulse width reset is guaranteed to be recognized. It is possible for a smaller pulse width to cause a reset.

## 18.11 3-V Oscillator Characteristics

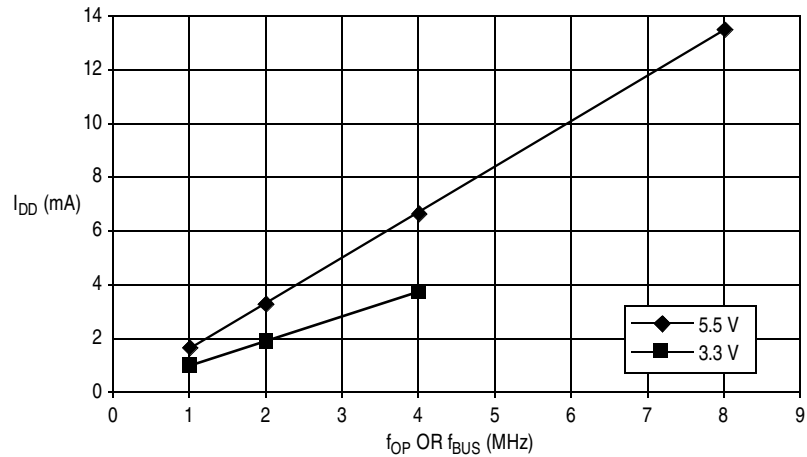
Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator frequency	$f_{INTCLK}$	—	3.2	—	MHz
Crystal frequency, XTALCLK	$f_{OSCXCLK}$	1	—	16	MHz
RC oscillator frequency, RCCLK	$f_{RCCLK}$	2	—	12	MHz
External clock reference frequency <sup>(1)</sup>	$f_{OSCXCLK}$	dc	—	16	MHz
Crystal load capacitance <sup>(2)</sup>	$C_L$	—	—	—	—
Crystal fixed capacitance <sup>(2)</sup>	$C_1$	—	$2 \times C_L$	—	—
Crystal tuning capacitance <sup>(2)</sup>	$C_2$	—	$2 \times C_L$	—	—
Feedback bias resistor	$R_B$	—	10	—	$M\Omega$
Series resistor <sup>(2), (3)</sup>	$R_S$	—	—	—	—
RC oscillator external resistor	$R_{EXT}$	See <a href="#">Figure 18-2</a>			—

1. No more than 10% duty cycle deviation from 50%
2. Consult crystal vendor data sheet
3. Not required for high frequency crystals

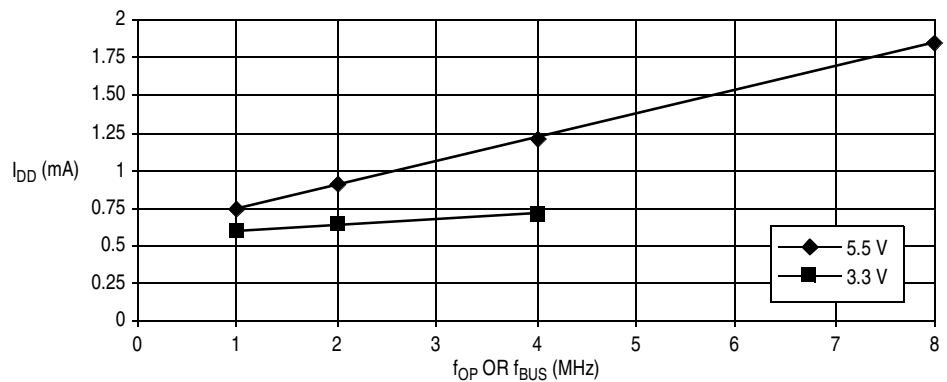


**Figure 18-2. RC versus Frequency (3 Volts @ 25°C)**

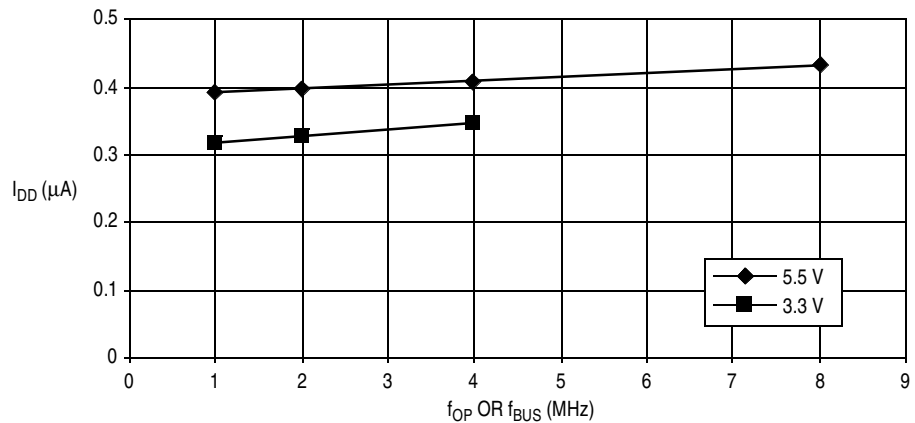
## 18.12 Typical Supply Currents



**Figure 18-3. Typical Operating  $I_{DD}$ , with All Modules Turned On (25°C)**



**Figure 18-4. Typical Wait Mode  $I_{DD}$ , with ADC Turned On (25°C)**



**Figure 18-5. Typical Stop Mode  $I_{DD}$ , with all Modules Disabled (25°C)**

## 18.13 Analog-to-Digital Converter Characteristics

Characteristic	Symbol	Min	Max	Unit	Comments
Supply voltage	$V_{DDAD}$	2.7 ( $V_{DD}$ min)	5.5 ( $V_{DD}$ max)	V	—
Input voltages	$V_{ADIN}$	$V_{SS}$	$V_{DD}$	V	—
Resolution	$B_{AD}$	8	8	Bits	—
Absolute accuracy	$A_{AD}$	$\pm 0.5$	$\pm 1.5$	LSB	Includes quantization
ADC internal clock	$f_{ADIC}$	0.5	1.048	MHz	$t_{ADIC} = 1/f_{ADIC}$ , tested only at 1 MHz
Conversion range	$R_{AD}$	$V_{SS}$	$V_{DD}$	V	—
Power-up time	$t_{ADPU}$	16		$t_{ADIC}$ cycles	$t_{ADIC} = 1/f_{ADIC}$
Conversion time	$t_{ADC}$	16	17	$t_{ADIC}$ cycles	$t_{ADIC} = 1/f_{ADIC}$
Sample time <sup>(1)</sup>	$t_{ADS}$	5	—	$t_{ADIC}$ cycles	$t_{ADIC} = 1/f_{ADIC}$
Zero input reading <sup>(2)</sup>	$Z_{ADI}$	00	01	Hex	$V_{IN} = V_{SS}$
Full-scale reading <sup>(3)</sup>	$F_{ADI}$	FE	FF	Hex	$V_{IN} = V_{DD}$
Input capacitance	$C_{ADI}$	—	8	pF	Not tested
Input leakage <sup>(3)</sup>	—	—	$\pm 1$	$\mu A$	—

1. Source impedances greater than 10 k $\Omega$  adversely affect internal RC charging time during input sampling.
2. Zero-input/full-scale reading requires sufficient decoupling measures for accurate conversions.
3. The external system error caused by input leakage current is approximately equal to the product of R source and input current.

## 18.14 Memory Characteristics

Characteristic	Symbol	Min	Max	Unit
RAM data retention voltage	$V_{RDR}$	1.3	—	V
FLASH program bus clock frequency	—	1	—	MHz
FLASH read bus clock frequency	$f_{Read}^{(1)}$	32 k	8M	Hz
FLASH page erase time	$t_{Erase}^{(2)}$	1	—	ms
FLASH mass erase time	$t_{MErase}^{(3)}$	4	—	ms
FLASH PGM/ERASE to HVEN set up time	$t_{nvs}$	10	—	us
FLASH high-voltage hold time	$t_{nvh}$	5	—	us
FLASH high-voltage hold time (mass erase)	$t_{nvhl}$	100	—	us
FLASH program hold time	$t_{pgs}$	5	—	us
FLASH program time	$t_{PROG}$	30	40	us
FLASH return to read time	$t_{rcv}^{(4)}$	1	—	us
FLASH cumulative program hv period	$t_{HV}^{(5)}$	—	4	ms
FLASH row erase endurance <sup>(6)</sup>	—	10 k	—	Cycles
FLASH row program endurance <sup>(7)</sup>	—	10 k	—	Cycles
FLASH data retention time <sup>(8)</sup>	—	10	—	Years

- $f_{Read}$  is defined as the frequency range for which the FLASH memory can be read.
- If the page erase time is longer than  $t_{Erase}$  (Min), there is no erase disturb, but it reduces the endurance of the FLASH memory.
- If the mass erase time is longer than  $t_{MErase}$  (Min), there is no erase disturb, but it reduces the endurance of the FLASH memory.
- $t_{rcv}$  is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to logic 0.
- $t_{HV}$  is defined as the cumulative high voltage programming time to the same row before next erase.  
 $t_{HV}$  must satisfy this condition:  $t_{nvs} + t_{nvh} + t_{pgs} + (t_{PROG} \times 64) \leq t_{HV} \text{ max.}$
- The minimum row endurance value specifies each row of the FLASH memory is guaranteed to work for at least this many erase/program cycles.
- The minimum row endurance value specifies each row of the FLASH memory is guaranteed to work for at least this many erase/program cycles.
- The FLASH is guaranteed to retain data over the entire operating temperature range for at least the minimum time specified.



## Section 19. Mechanical Specifications

### 19.1 Contents

19.2	Introduction . . . . .	225
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19.7	16-Pin Thin Shrink Small Outline Package (Case #948F) . . . . .	228

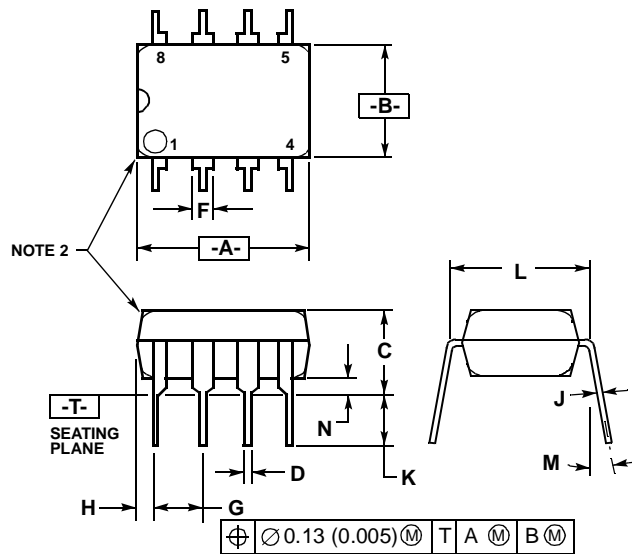
### 19.2 Introduction

This section gives the dimensions for:

- 8-pin plastic dual in-line package (PDIP)
- 8-pin small outline integrated circuit (SOIC) package
- 16-pin PDIP
- 16-pin SOIC
- 16-pin thin shrink small outline package (TSSOP)

# Mechanical Specifications

## 19.3 8-Pin Plastic Dual In-Line Package (Case #626)



### NOTES:

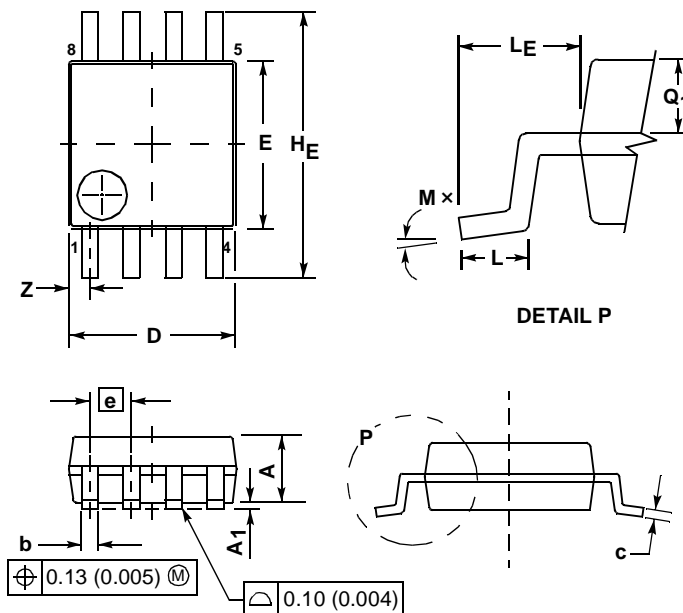
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

### STYLE 1:

1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8.  $V_{CC}$

## 19.4 8-Pin Small Outline Integrated Circuit Package (Case #968)



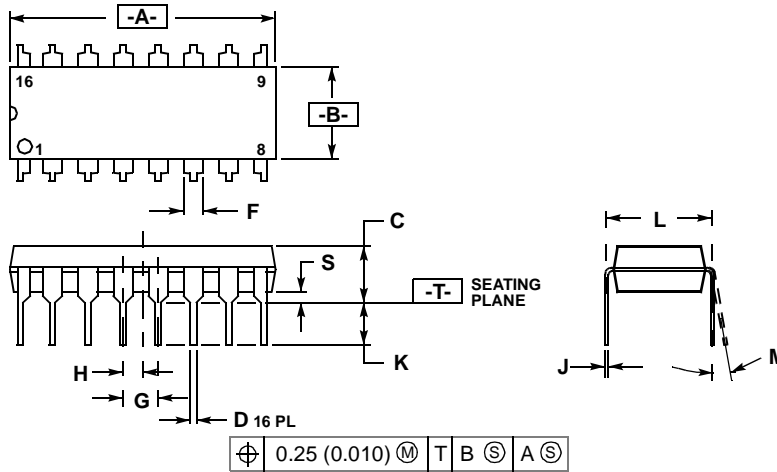
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSION D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	5.10	5.50	0.201	0.217
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	0.94	---	0.037

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

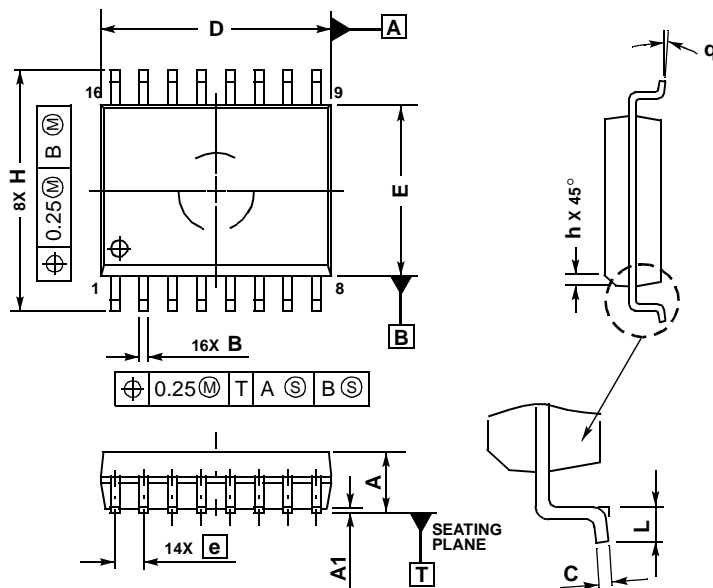
### 19.5 16-Pin Plastic Dual In-Line Package (Case #648D)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010).
  6. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.760	18.80	19.30
B	0.245	0.260	6.23	6.60
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.120	0.140	3.05	3.55
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.015	0.035	0.39	0.88

### 19.6 16-Pin Small Outline Integrated Circuit Package (Case #751G)

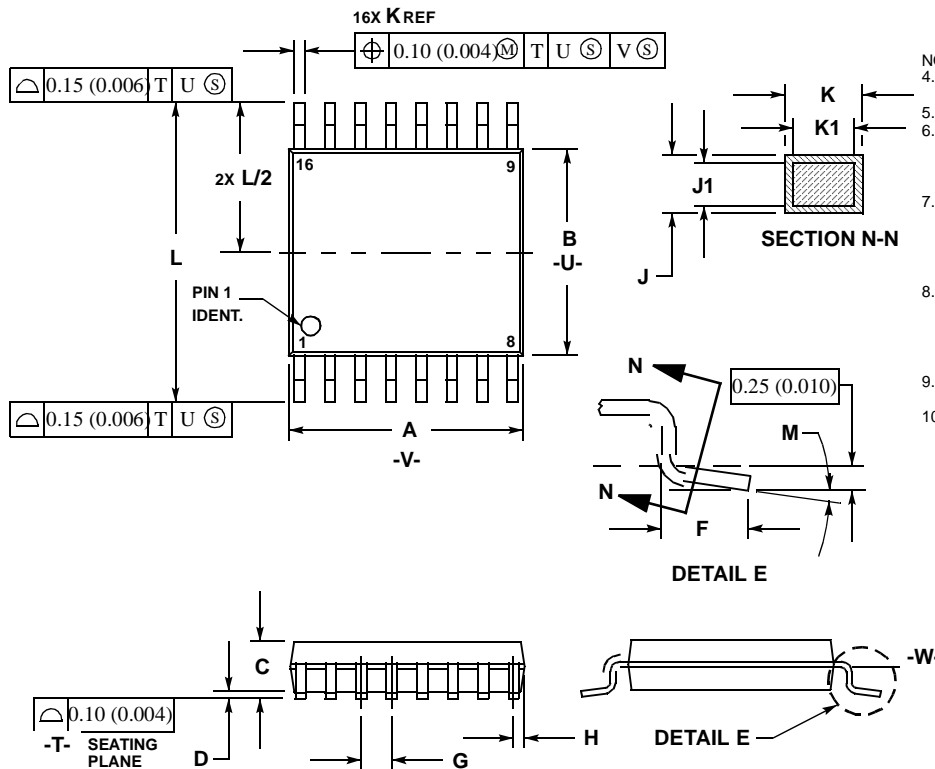


- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.40	1.00
q	0°	7°

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## 19.7 16-Pin Thin Shrink Small Outline Package (Case #948F)



**NOTES:**

4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
7. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
8. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
9. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
10. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

## Section 20. Ordering Information

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20.3 MC Order Numbers . . . . .229

### 20.2 Introduction

This section contains ordering numbers for MC68HC908QY1, MC68HC908QY2, MC68HC908QY4, MC68HC908QT1, MC68HC908QT2, and MC69HC908QT4.

### 20.3 MC Order Numbers

**Table 20-1. MC Order Numbers**

MC Order Number	ADC	FLASH Memory	Package
MC68HC908QY1	—	1536 bytes	16-pin package
MC68HC908QY2	Yes	1536 bytes	
MC68HC908QY4	Yes	4096 bytes	
MC68HC908QT1	—	1536 bytes	8-pin package
MC68HC908QT2	Yes	1536 bytes	
MC68HC908QT4	Yes	4096 bytes	

Temperature and package designators:  
 C = -40°C to +85°C  
 M = -40°C to +125°C (available for V<sub>DD</sub> = 5 V only)  
 P = Plastic dual in-line package (PDIP)  
 DW = Small outline integrated circuit package (SOIC)  
 SD = Shrink Small Outline package (SSOP)

## Ordering Information

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## Appendix A. ROM Versions

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A.12.4	ADC Clock Register .....	248

## A.2 Introduction

This appendix reflects the difference data for the ROM versions:

- MC68HC08QT4
- MC68HC08QY4
- MC68HC08QT2
- MC68HC08QY2
- MC68HC08QT1
- MC68HC08QY1

With the exceptions shown here, the information in this document applies to each member of this family of devices:

- Replace **Figure 1-1. Block Diagram** with **Figure A-1. Block Diagram**
- Replace **Figure 2-1. Memory Map** with **Figure A-2. Memory Map**
- Replace **Section 4. FLASH Memory (FLASH)** with **A.5 Read-Only Memory (ROM)**
- Note that the forced monitor mode described in **Section 9. Monitor ROM (MON)** does not apply to the ROM versions
- Replace **Section 11. Analog-to-Digital Converter (ADC)** with **A.6 Analog-to-Digital Converter (ADC)**

## A.3 Block Diagram

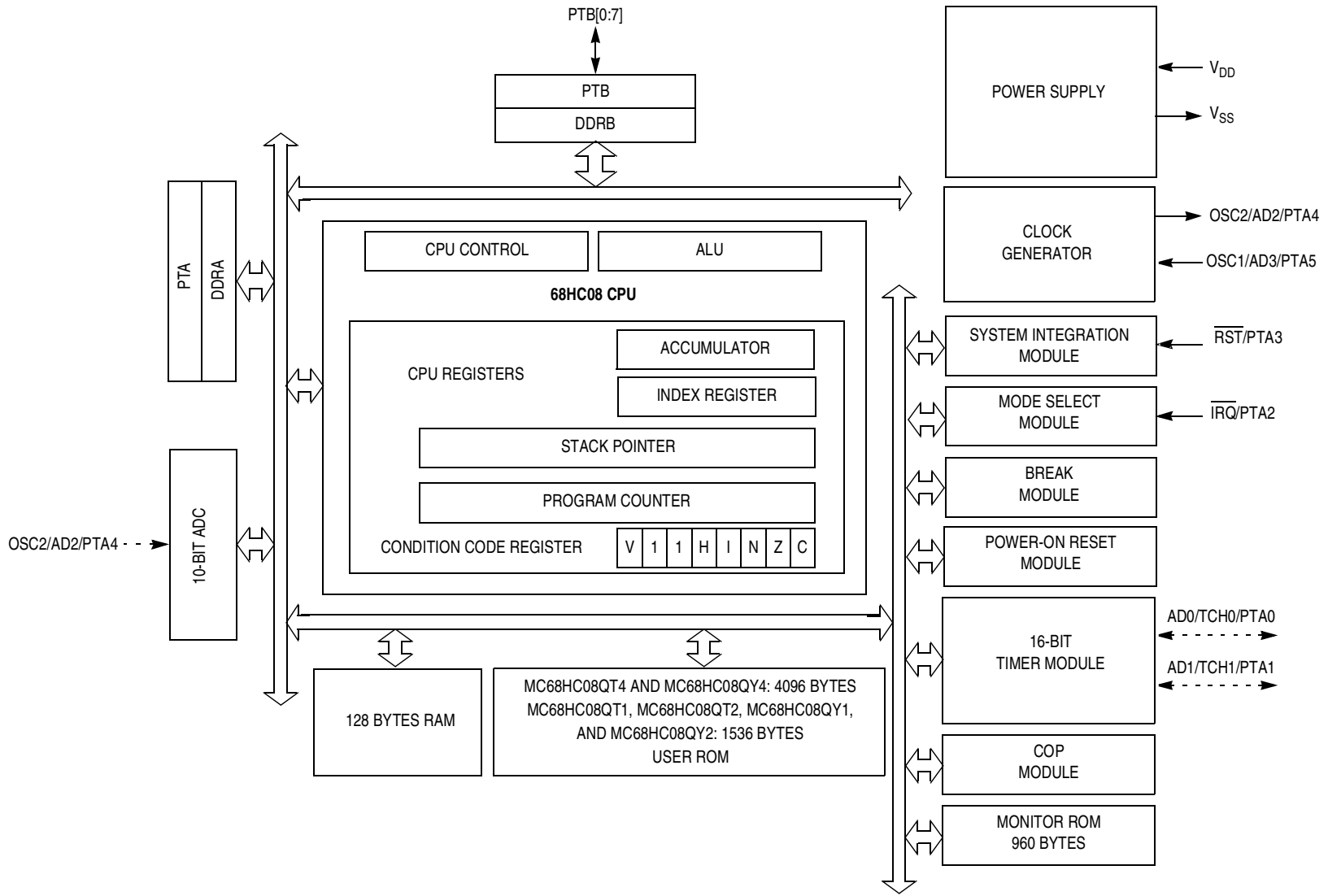
See **Figure A-1. Block Diagram**.

## A.4 Memory Map

See **Figure A-2. Memory Map**.



MC68HC908QY4 • MC68HC908QT4 • MC68HC908QY2 • MC68HC908QT2 • MC68HC908QY1 • MC68HC908QT1



$\overline{\text{RST}}$ ,  $\overline{\text{IRQ}}$ : Pins have internal 30K pull up  
 PTA[0:5]: High current sink source capability  
 PTA[0:5]: Pins have programmable keyboard interrupt and pull up  
 PTB[0:7]: Not available on 8-pin devices – MC68HC08QT1, MC68HC08QT2, and MC68HC08QT4

Figure A-1. Block Diagram

# ROM Versions

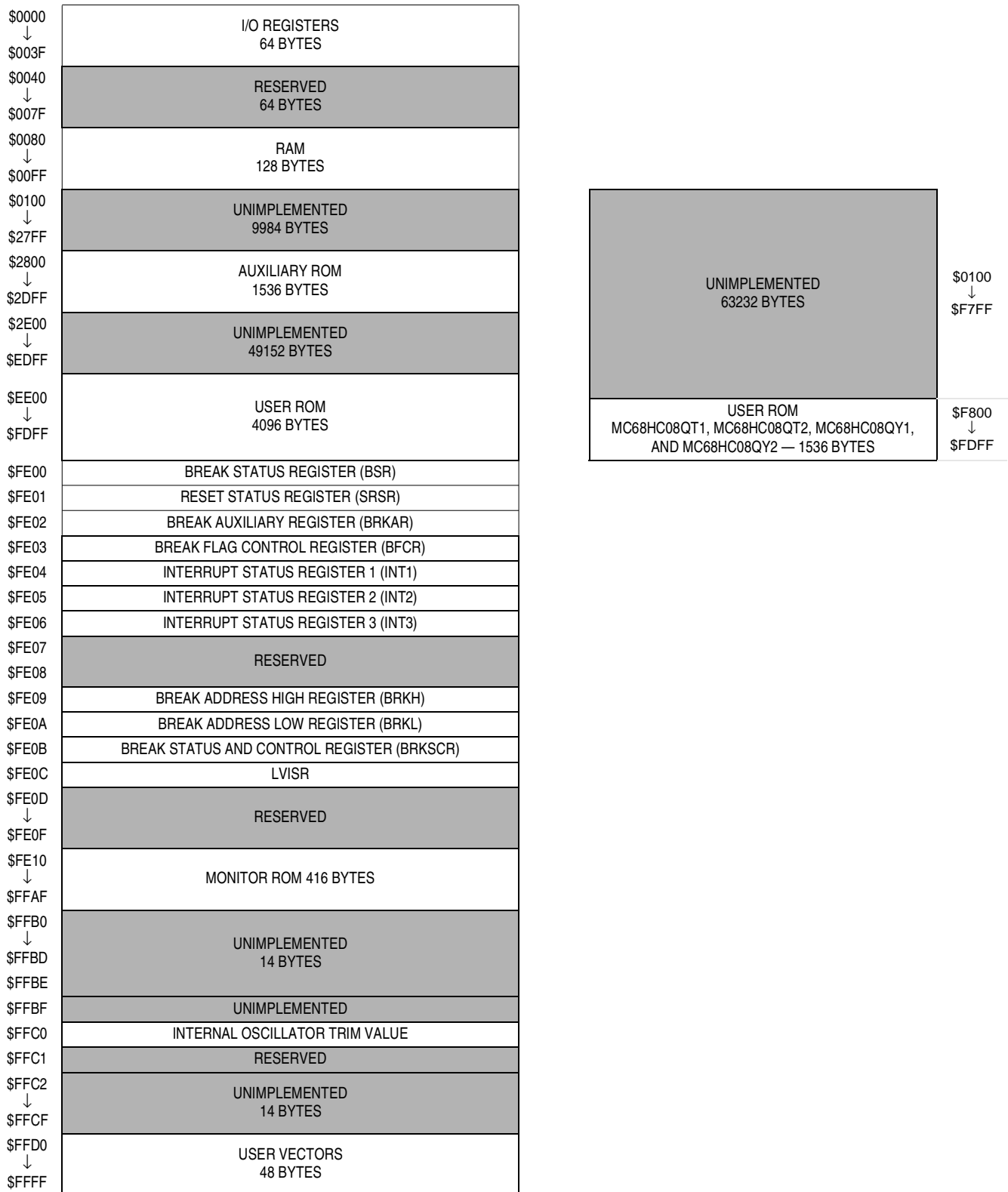


Figure A-2. Memory Map

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1

## A.5 Read-Only Memory (ROM)

The user ROM consists of 4 kbytes of user ROM, 0.5 kbytes of monitor ROM, and 1.5 kbytes used for test support routines for a total 6 kbytes. See [Figure A-2](#).

## A.6 Analog-to-Digital Converter (ADC)

This subsection describes the 10-bit analog-to-digital converter (ADC). The ADC module is only available on the MC68HC08QY2, MC68HC08QT2, MC68HC08QY4, and MC68HC08QT4.

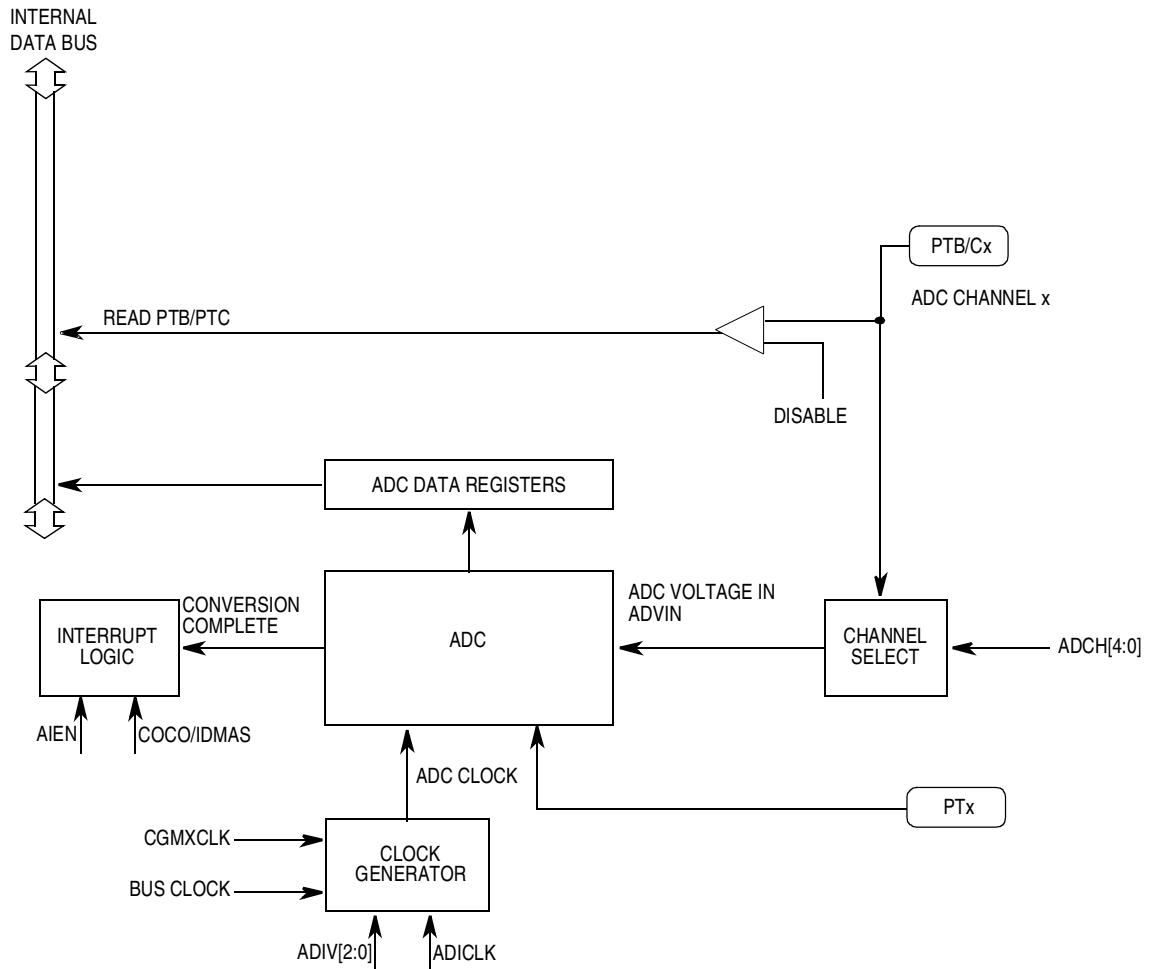
## A.7 Features

Features of the ADC module include:

- 10 channels with multiplexed input
- Linear successive approximation
- 10-bit resolution, 8-bit accuracy
- Single or continuous conversion
- Conversion complete flag or conversion complete interrupt
- Selectable ADC clock
- Left or right justified result
- Left justified sign data mode
- High impedance buffered ADC input

## A.8 Functional Description

Ten ADC channels are available for sampling external sources at pins PTC1/ATD9:PTC0/ATD8 and PTB7:PTB0. To achieve the best possible accuracy, these pins are implemented as input-only pins when the analog-to-digital (A/D) feature is enabled. An analog multiplexer allows the single ADC to select one of the 10 ADC channels as ADC voltage IN (ADCVIN). ADCVIN is converted by the successive approximation algorithm. When the conversion is completed, the ADC places the result in the ADC data register (ADRH and ADRL) and sets a flag or generates an interrupt. See [Figure A-3](#).



**Figure A-3. ADC Block Diagram**

## A.8.1 ADC Port I/O Pins

PTC1/ATD9:PTC0/ATD8 and PTB7:PTB0 are general-purpose I/O pins that are shared with the ADC channels.

The channel select bits define which ADC channel/port pin will be used as the input signal. The ADC overrides the port logic when that port is selected by the ADC multiplexer. The remaining ADC channels/port pins are controlled by the port logic and can be used as general-purpose input/output (I/O) pins. Writes to the port register or DDR will not have any effect on the port pin that is selected by the ADC. Read of a port pin which is in use by the ADC will return a logic 0.

## A.8.2 Voltage Conversion

When the input voltage to the ADC equals  $V_{REFH}$ , the ADC converts the signal to \$3FF (full scale). If the input voltage equals  $V_{REFL}$ , the ADC converts it to \$000. Input voltages between  $V_{REFH}$  and  $V_{REFL}$  are straight-line linear conversions. All other input voltages will result in \$3FF if greater than  $V_{REFH}$  and \$000 if less than  $V_{REFL}$ .

**NOTE:** *Input voltage should not exceed the analog supply voltages.*

## A.8.3 Conversion Time

Conversion starts after a write to the ADSCR. A conversion is between 16 and 17 ADC clock cycles, therefore:

$$\text{Conversion time} = \frac{16 \text{ to } 17 \text{ ADC Cycles}}{\text{ADC Frequency}}$$

$$\text{Number of Bus Cycles} = \text{Conversion Time} \times \text{Bus Frequency}$$

The ADC conversion time is determined by the clock source chosen and the divide ratio selected. The clock source is either the bus clock or CGMXCLK and is selectable by ADICLK located in the ADC clock register. For example, if CGMXCLK is 4 MHz and is selected as the ADC input clock source, the ADC input clock divide-by-2 prescale is selected and the bus frequency is 8 MHz:

$$\text{Conversion Time} = \frac{16 \text{ to } 17 \text{ ADC Cycles}}{4 \text{ MHz}/2} = 8 \text{ to } 8.5 \mu\text{s}$$

$$\text{Number of bus cycles} = 8 \text{ ms} \times 8 \text{ MHz} = 64 \text{ to } 68 \text{ cycles}$$

**NOTE:** *The ADC frequency must be between  $f_{ADIC}$  minimum and  $f_{ADIC}$  maximum to meet A/D specifications.*

Since an ADC cycle may be comprised of several bus cycles (four in the previous example) and the start of a conversion is initiated by a bus cycle write to the ADSCR, from zero to four additional bus cycles may occur before the start of the initial ADC cycle. This results in a fractional ADC cycle and is represented as the 17th cycle.

### A.8.4 Continuous Conversion

In continuous conversion mode, the ADC data registers ADRH and ADRL will be filled with new data after each conversion. Data from the previous conversion will be overwritten whether that data has been read or not. Conversions will continue until the ADCO bit is cleared. The COCO bit is set after the first conversion and will stay set for the next several conversions until the next write of the ADC status and control register or the next read of the ADC data register.

### A.8.5 Result Justification

The conversion result may be formatted in four different ways:

1. Left justified
2. Right justified
3. Left Justified sign data mode
4. 8-bit truncation mode

All four of these modes are controlled using MODE0 and MODE1 bits located in the ADC clock register (ADCR).

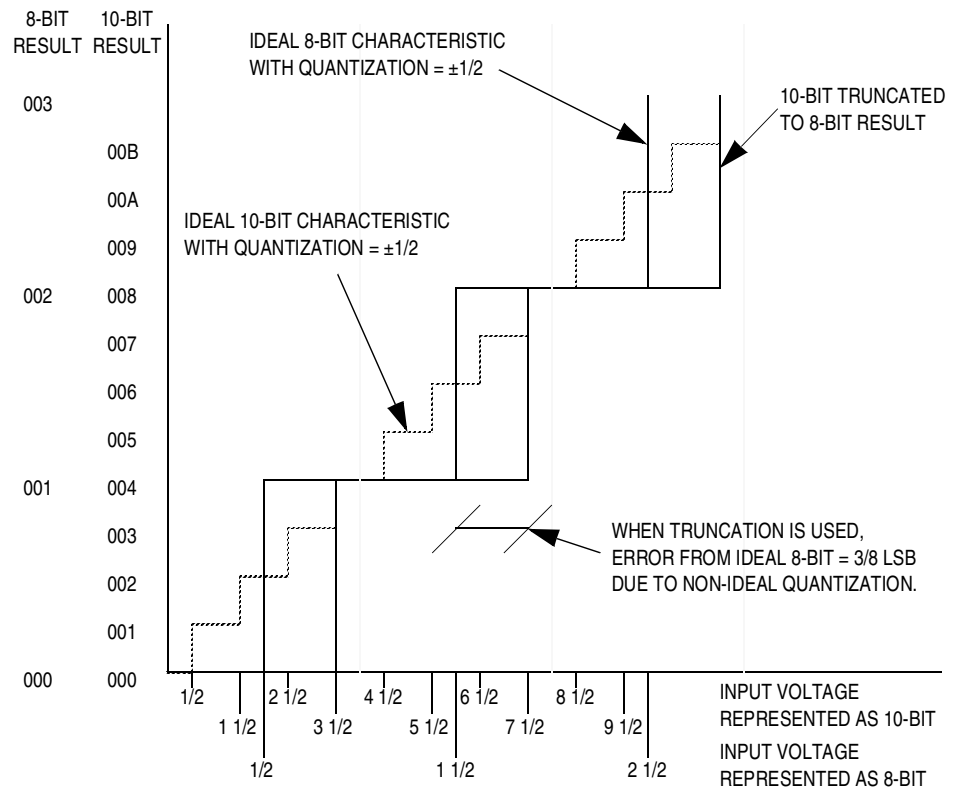
Left justification will place the eight most significant bits (MSB) in the corresponding ADC data register high, ADRH. This may be useful if the result is to be treated as an 8-bit result where the two least significant bits (LSB), located in the ADC data register low, ADRL, can be ignored. However, ADRL must be read after ADRH or else the interlocking will prevent all new conversions from being stored.

Right justification will place only the two MSBs in the corresponding ADC data register high, ADRH, and the eight LSBs in ADC data register low, ADRL. This mode of operation typically is used when a 10-bit unsigned result is desired.

Left justified sign data mode is similar to left justified mode with one exception. The MSB of the 10-bit result, AD9 located in ADRH, is complemented. This mode of operation is useful when a result, represented as a signed magnitude from mid-scale, is needed. Finally, 8-bit truncation mode will place the eight MSBs in ADC data register low,

ADRL. The two LSBs are dropped. This mode of operation is used when compatibility with 8-bit ADC designs are required. No interlocking between ADRH and ADRL is present.

**NOTE:** Quantization error is affected when only the most significant eight bits are used as a result. See [Figure A-4](#).



**Figure A-4. 8-Bit Truncation Mode Error**

### A.8.6 Monotonicity

The conversion process is monotonic and has no missing codes.

### A.9 Interrupts

When the AIEN bit is set, the ADC module is capable of generating a CPU interrupt after each ADC conversion. A CPU interrupt is generated if the COCO bit is at logic 0. The COCO bit is not used as a conversion complete flag when interrupts are enabled.

### A.10 Wait Mode

The WAIT instruction can put the MCU in low power-consumption standby mode.

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the MCU out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting ADCH[4:0] in the ADC status and control register before executing the WAIT instruction.

### A.11 I/O Signals

The ADC module has 10 input signals that are shared with port B and port C.

#### A.11.1 ADC Analog Power Pin ( $V_{DDAD}$ )

The ADC analog portion uses  $V_{DDAD}$  as its power pin. Connect the  $V_{DDAD}$  pin to the same voltage potential as  $V_{DD}$ . External filtering may be necessary to ensure clean  $V_{DDAD}$  for good results.

**NOTE:** Route  $V_{DDAD}$  carefully for maximum noise immunity and place bypass capacitors as close as possible to the package.

#### A.11.2 ADC Analog Ground Pin ( $V_{SSAD}$ )

The ADC analog portion uses  $V_{SSAD}$  as its ground pin. Connect the  $V_{SSAD}$  pin to the same voltage potential as  $V_{SS}$ .



### A.11.3 ADC Voltage Reference Pin ( $V_{REFH}$ )

$V_{REFH}$  is the power supply for setting the reference voltage  $V_{REFH}$ . Connect the  $V_{REFH}$  pin to the same voltage potential as  $V_{DDAD}$ . There will be a finite current associated with  $V_{REFH}$ . See [Section 18. Electrical Specifications](#).

**NOTE:** *Route  $V_{REFH}$  carefully for maximum noise immunity and place bypass capacitors as close as possible to the package.*

### A.11.4 ADC Voltage Reference Low Pin ( $V_{REFL}$ )

$V_{REFL}$  is the lower reference supply for the ADC. Connect the  $V_{REFL}$  pin to the same voltage potential as  $V_{SSAD}$ . A finite current will be associated with  $V_{REFL}$ . See [Section 18. Electrical Specifications](#).

**NOTE:** *In the 56-pin shrink dual in-line package (SDIP),  $V_{REFL}$  and  $V_{SSAD}$  are tied together.*

### A.11.5 ADC Voltage In (ADVIN)

ADVIN is the input voltage signal from one of the 10 ADC channels to the ADC module.

### A.11.6 ADC External Connections

This section describes the ADC external connections:  $V_{REFH}$  and  $V_{REFL}$ , ANx, and grounding.

#### A.11.6.1 $V_{REFH}$ and $V_{REFL}$

Both ac and dc current are drawn through the  $V_{REFH}$  and  $V_{REFL}$  loop. The AC current is in the form of current spikes required to supply charge to the capacitor array at each successive approximation step. The current flows through the internal resistor string. The best external component to meet both these current demands is a capacitor in the 0.01  $\mu\text{F}$  to 1  $\mu\text{F}$  range with good high frequency characteristics. This capacitor is connected between  $V_{REFH}$  and  $V_{REFL}$  and must be placed

as close as possible to the package pins. Resistance in the path is not recommended because the dc current will cause a voltage drop which could result in conversion errors.

### A.11.6.2 ANx

Empirical data shows that capacitors from the analog inputs to  $V_{REFL}$  improve ADC performance. 0.01- $\mu$ F and 0.1- $\mu$ F capacitors with good high-frequency characteristics are sufficient. These capacitors must be placed as close as possible to the package pins.

### A.11.6.3 Grounding

In cases where separate power supplies are used for analog and digital power, the ground connection between these supplies should be at the  $V_{SSA}$  pin. This should be the only ground connection between these supplies if possible. The  $V_{SSA}$  pin makes a good single point ground location. Connect the  $V_{REFL}$  pin to the same potential as  $V_{SSAD}$  at the single point ground location.

## A.12 I/O Registers

These I/O registers control and monitor operation of the ADC:

- ADC status and control register, ADSCR
- ADC data registers, ADRH and ARDL
- ADC clock register, ADCLK

### A.12.1 ADC Status and Control Register

This section describes the function of the ADC status and control register (ADSCR). Writing ADSCR aborts the current conversion and initiates a new conversion.

Address: \$0040

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:								
Reset:	0	0	0	1	1	1	1	1

**Figure A-5. ADC Status and Control Register (ADSCR)**

#### COCO — Conversions Complete Bit

When AIEN bit is a logic 0, the COCO is a read-only bit which is set each time a conversion is completed except in the continuous conversion mode where it is set after the first conversion. This bit is cleared whenever the ADC status and control register is written or whenever the ADC data register is read.

If AIEN bit is a logic 1, the COCO is a read/write bit. Reset clears this bit.

1 = Conversion completed (AIEN = 0)

0 = Conversion not completed (AIEN = 0)/CPU interrupt (AIEN = 1)

#### AIEN — ADC Interrupt Enable Bit

When this bit is set, an interrupt is generated at the end of an ADC conversion. The interrupt signal is cleared when the data register is read or the status/control register is written. Reset clears the AIEN bit.

1 = ADC interrupt enabled

0 = ADC interrupt disabled

#### ADCO — ADC Continuous Conversion Bit

When set, the ADC will convert samples continuously and update the ADR register at the end of each conversion. Only one conversion is allowed when this bit is cleared. Reset clears the ADCO bit.

1 = Continuous ADC conversion

0 = One ADC conversion

### ADCH[4:0] — ADC Channel Select Bits

ADCH4, ADCH3, ADCH2, ADCH1, and ADCH0 form a 5-bit field which is used to select one of 10 ADC channels. The ADC channels are detailed in [Table A-1](#).

**NOTE:** *Take care to prevent switching noise from corrupting the analog signal when simultaneously using a port pin as both an analog and digital input.*

The ADC subsystem is turned off when the channel select bits are all set to 1. This feature allows for reduced power consumption for the MCU when the ADC is not used.

**NOTE:** *Recovery from the disabled state requires one conversion cycle to stabilize.*

The voltage levels supplied from internal reference nodes as specified in [Table A-1](#) are used to verify the operation of the ADC both in production test and for user applications.

Table A-1. Mux Channel Select

ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	Input Select
0	0	0	0	0	PTB0
0	0	0	0	1	PTB1
0	0	0	1	0	PTB2
0	0	0	1	1	PTB3
0	0	1	0	0	PTB4
0	0	1	0	1	PTB5
0	0	1	1	0	PTB6
0	0	1	1	1	PTB7
0	1	0	0	0	PTC0/ATD8
0	1	0	0	1	PTC1/ATD9 ***
0	1	0	1	0	Unused *
0	1	0	1	1	↓
0	1	1	0	0	↓
0	1	1	0	1	↓
0	1	1	1	0	↓
0	1	1	1	1	↓
1	0	0	0	0	↓
1	1	0	1	0	Unused *
1	1	0	1	1	Reserved **
1	1	1	0	0	Unused *
1	1	1	0	1	V <sub>REFH</sub>
1	1	1	1	0	V <sub>REFL</sub>
1	1	1	1	1	ADC power off

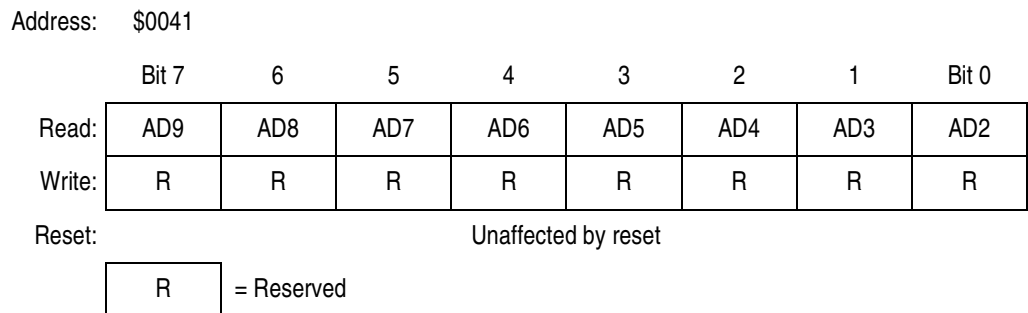
\* If any unused channels are selected, the resulting ADC conversion will be unknown.

\*\* Used for factory testing.

\*\*\* ATD9 is not available in the 56-pin SDIP package.

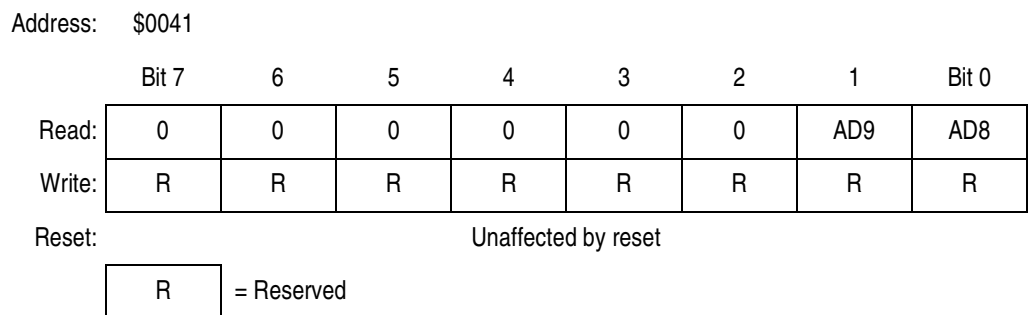
## A.12.2 ADC Data Register High

In left justified mode, this 8-bit result register holds the eight MSBs of the 10-bit result. This register is updated each time an ADC single channel conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. Until ADRL is read, all subsequent ADC results will be lost.



**Figure A-6. ADC Data Register High (ADRH)  
Left Justified Mode**

In right justified mode, this 8-bit result register holds the two MSBs of the 10-bit result. All other bits read as 0. This register is updated each time a single channel ADC conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. Until ADRL is read, all subsequent ADC results will be lost.



**Figure A-7. ADC Data Register High (ADRH)  
Right Justified Mode**

### A.12.3 ADC Data Register Low

In left justified mode, this 8-bit result register holds the two LSBs of the 10-bit result. All other bits read as 0. This register is updated each time a single channel ADC conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. Until ADRL is read, all subsequent ADC results will be lost.

Address: \$0042

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	AD1	AD0	0	0	0	0	0	0
Write:	R	R	R	R	R	R	R	R

Reset: Unaffected by reset

R = Reserved

**Figure A-8. ADC Data Register Low (ADRL)  
Left Justified Mode**

In right justified mode, this 8-bit result register holds the eight LSBs of the 10-bit result. This register is updated each time an ADC conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. Until ADRL is read, all subsequent ADC results will be lost.

Address: \$0042

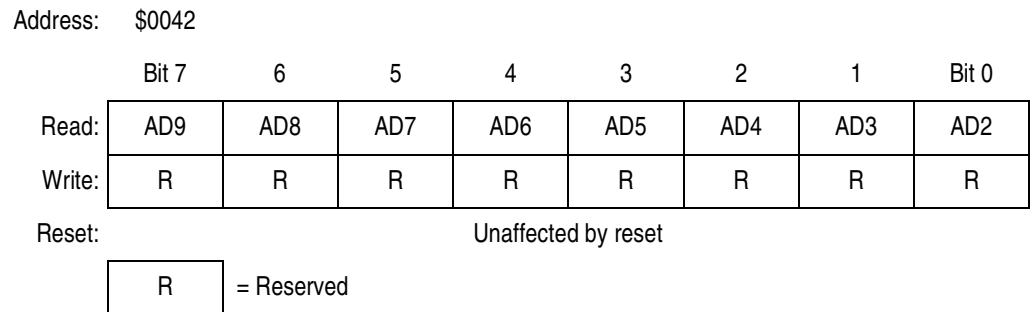
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Write:	R	R	R	R	R	R	R	R

Reset: Unaffected by reset

R = Reserved

**Figure A-9. ADC Data Register Low (ADRL)  
Right Justified Mode**

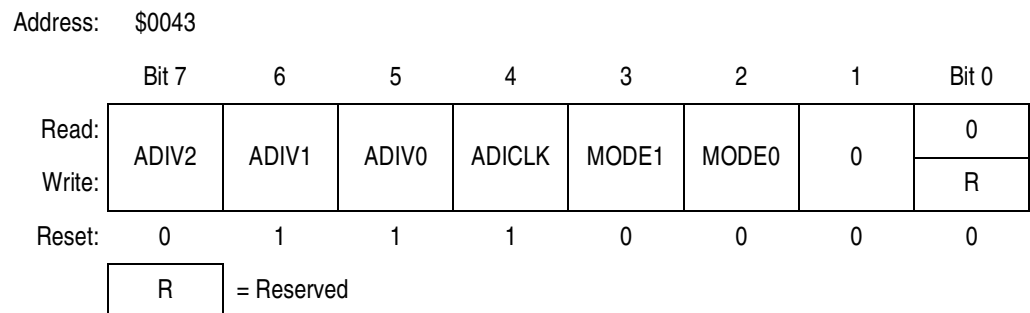
In 8-bit mode, this 8-bit result register holds the eight MSBs of the 10-bit result. This register is updated each time an ADC conversion completes. In 8-bit mode, this register contains no interlocking with ADRH.



**Figure A-10. ADC Data Register Low (ADRL) 8-Bit Mode**

## A.12.4 ADC Clock Register

This register selects the clock frequency for the ADC, selecting between modes of operation.



**Figure A-11. ADC Clock Register (ADCLK)**

### ADIV2:ADIV0 — ADC Clock Prescaler Bits

ADIV2, ADIV1, and ADIV0 form a 3-bit field which selects the divide ratio used by the ADC to generate the internal ADC clock.

**Table A-2** shows the available clock configurations.



**Table A-2. ADC Clock Divide Ratio**

ADIV2	ADIV1	ADIV0	ADC Clock Rate
0	0	0	ADC input clock /1
0	0	1	ADC input clock /2
0	1	0	ADC input clock /4
0	1	1	ADC input clock /8
1	X	X	ADC input clock /16

X = don't care

#### ADICLK — ADC Input Clock Select Bit

ADICLK selects either bus clock or CGMXCLK as the input clock source to generate the internal ADC clock. Reset selects CGMXCLK as the ADC clock source.

If the external clock (CGMXCLK) is equal to or greater than 1 MHz, CGMXCLK can be used as the clock source for the ADC. If CGMXCLK is less than 1 MHz, use the PLL-generated bus clock as the clock source. As long as the internal ADC clock is at  $f_{ADIC}$ , correct operation can be guaranteed. See [18.13 Analog-to-Digital Converter Characteristics](#).

1 = Internal bus clock

0 = External clock, CGMXCLK

$$f_{ADIC} = \frac{\text{CGMXCLK or bus frequency}}{\text{ADIV}[2:0]}$$

#### MODE1:MODE0 — Modes of Result Justification Bits

MODE1:MODE0 selects among four modes of operation. The manner in which the ADC conversion results will be placed in the ADC data registers is controlled by these modes of operation. Reset returns right-justified mode.

00 = 8-bit truncation mode

01 = Right justified mode

10 = Left justified mode

11 = Left justified sign data mode

MC68HC908QY4•MC68HC908QT4•MC68HC908QY2•MC68HC908QT2•MC68HC908QY1•MC68HC908QT1



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