DG441, DG442

Monolithic Quad SPST CMOS Analog Switches

December 1994

Features

- **ON-Resistance 85Ω Max**
- **Low Power Consumption (P_D <1.6mW)**
- **Fast Switching Action**
  - **t_{ON} <250ns**
  - **t_{OFF} <120ns (DG441)**
- **Low Charge Injection**
- **Upgrade from DG201A/DG202**
- **TTL, CMOS Compatible**
- **Single or Split Supply Operation**

Applications

- **Audio Switching**
- **Battery Operated Systems**
- **Data Acquisition**
- **Hi-Rel Systems**
- **Sample and Hold Circuits**
- **Communication Systems**
- **Automatic Test Equipment**

Description

The DG441 and DG442 monolithic CMOS analog switches are drop-in replacements for the popular DG201A and DG202 series devices. They include four independent single pole single throw (SPST) analog switches, TTL and CMOS compatible digital inputs, and a voltage reference for logic thresholds.

These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} < 250ns) compared to the DG201A and DG202. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG441 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 40V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG441 and DG442 are identical, differing only in the polarity of the selection logic.

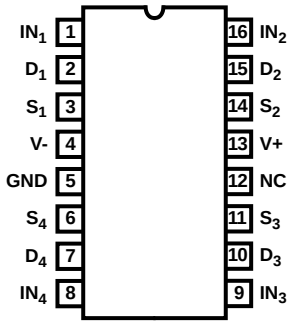
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG441AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG441DJ	-40°C to +85°C	16 Lead Plastic DIP
DG441DY	-40°C to +85°C	16 Lead SOIC (N)
DG441EJ (Note)	-40°C to +85°C	16 Lead Plastic DIP
DG441EY (Note)	-40°C to +85°C	16 Lead SOIC (N)
DG442AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG442DJ	-40°C to +85°C	16 Lead Plastic DIP
DG442DY	-40°C to +85°C	16 Lead SOIC (N)
DG442EJ (Note)	-40°C to +85°C	16 Lead Plastic DIP
DG442EY (Note)	-40°C to +85°C	16 Lead SOIC (N)

NOTE: Avionics Process Flow

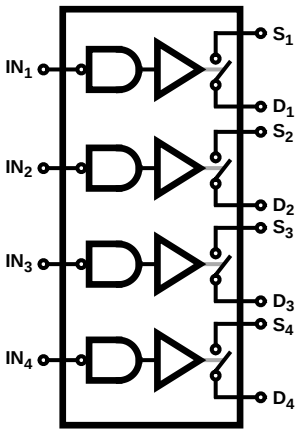
Pinout

DG441, DG442
(PDIP, CDIP, SOIC)
TOP VIEW

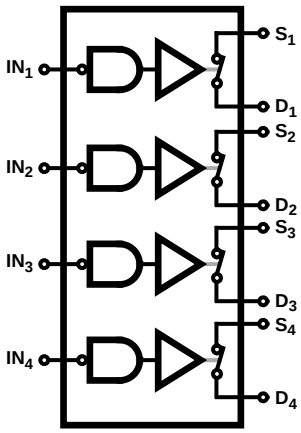


Functional Diagrams

DG441



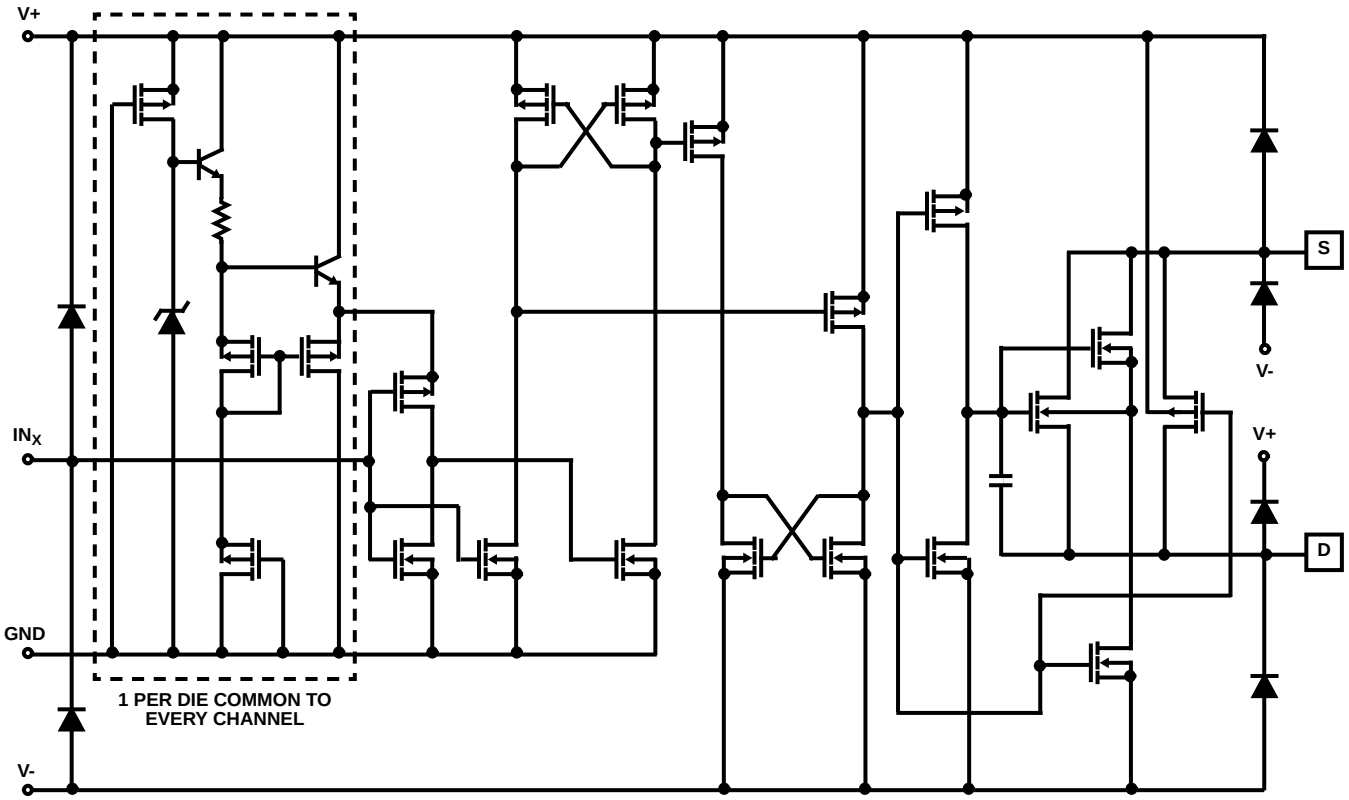
DG442



SWITCHES SHOWN FOR LOGIC "1" INPUT

File Number **3281.3**

Schematic Diagram (One Channel)



Absolute Maximum Ratings

V+ to V- . . . . . +44.0V
GND to V- 25V
Digital Inputs (Note 1) . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current, S or D (Note 1) . . . . . ±30mA
Peak Current, S or D (Note 1) . . . . . ±100mA
(Pulsed 1ms, 10% Duty Cycle)
Storage Temperature Range (D Suffix) . . . . . -65^oC to $+125^oC$

Thermal Information

Thermal Resistance (Note 3) θ_{JA}
Plastic DIP Package . . . . . $145^oC/W$
SOIC Package . . . . . $115^oC/W$
Operating Temperature(D Suffix) . . . . . -40^oC to $+85^oC$
Junction Temperature (PDIP, SOIC) . . . . . $+150^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . ±20V Max
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Input Low Voltage . . . . . 0.8V Max
Input High Voltage . . . . . 2.4V Min
Input Rise and Fall Time . . . . . ≤20ns

Electrical Specifications

(Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, $V_{ANALOG} = V_S$, V_D, Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 2) TEMP	D SUFFIX -40^oC TO $+85^oC$ MIN	(NOTE 4) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, T_{ON}	R_1 = 1kΩ, C_L = 35pF, V_S = ±10V, See Figure 18	$+25^oC$	-	150	250	ns
Turn-OFF Time, T_{OFF}		$+25^oC$				
DG441			-	90	120	ns
DG442			-	110	210	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, V_{GEN} = 0V, R_{GEN} = 0Ω	$+25^oC$	-	-1	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	$+25^oC$	-	60	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz	$+25^oC$	-	-100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz	$+25^oC$	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz	$+25^oC$	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$	V_{ANALOG} = 0	$+25^oC$	-	16	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}	Note 4	Full	-15	-	15	V
Drain-Source ON Resistance, $R_{DS(ON)}$	I_S = 10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	$+25^oC$	-	50	85	Ω
		Hot	-	-	100	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	$+25^oC$	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	$+25^oC$	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, $V_S = V_D$ = ±15.5V	$+25^oC$	-0.5	0.08	0.5	nA
		Hot	-10	-	10	nA

Electrical Specifications (Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, $V_{ANALOG} = V_S, V_D$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	(NOTE 2) TEMP	D SUFFIX -40°C TO +85°C MIN	(NOTE 4) TYP	MAX	UNITS
DIGITAL CONTROL						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	µA
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	Full	-	15	100	µA
Negative Supply Current, I-		+25°C	-1	-0.0001	-	µA
		Full	-5	-	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{IN} = 2.4V, 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 2) TEMP	D SUFFIX -40°C TO +85°C MIN	(NOTE 4) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, T_{ON}	R_L = 1KΩ, C_L = 35pF, See Test Circuit, V_S = 8V	+25°C	-	300	450	ns
Turn-OFF Time, T_{OFF}		+25°C	-	60	200	ns
Charge Injection, Q	C_L = 1nF, V_{GEN} = 6V, R_{GEN} = 0Ω	+25°C	-	2	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $R_{DS(ON)}$	I_S = 10mA, V_D = 3V, 8V V+ = 10.8V	+25°C	-	100	160	Ω
		Full	-	-	200	Ω
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5V	Full	-	15	100	µA
Negative Supply Current, I-		+25°C	-1	-0.0001	-	µA
		Full	-100	-0.0001	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	µA

NOTES:

1. All leads soldered to PC Board.
2. Room: +25°C. Cold: D suffix -40°C. Hot: D suffix +85°C
3. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.

Typical Performance Curves

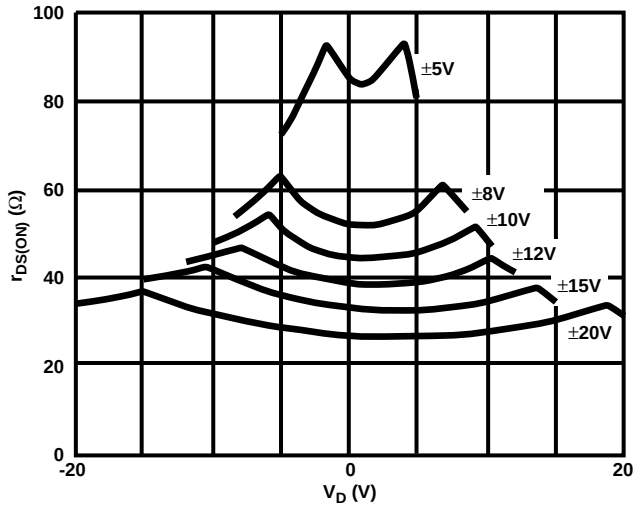


FIGURE 1. $R_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

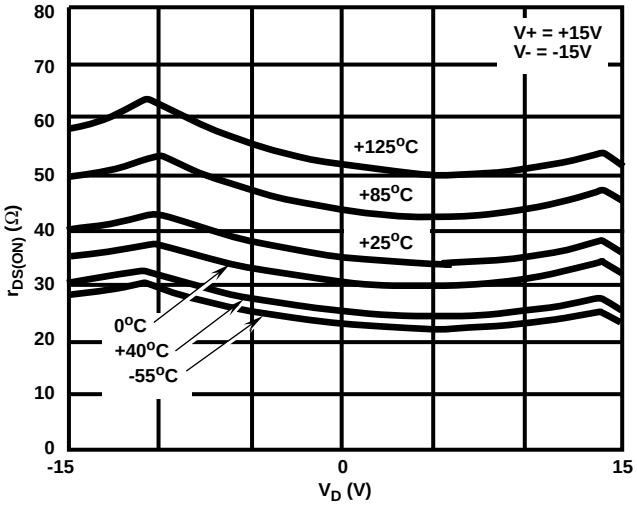


FIGURE 2. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

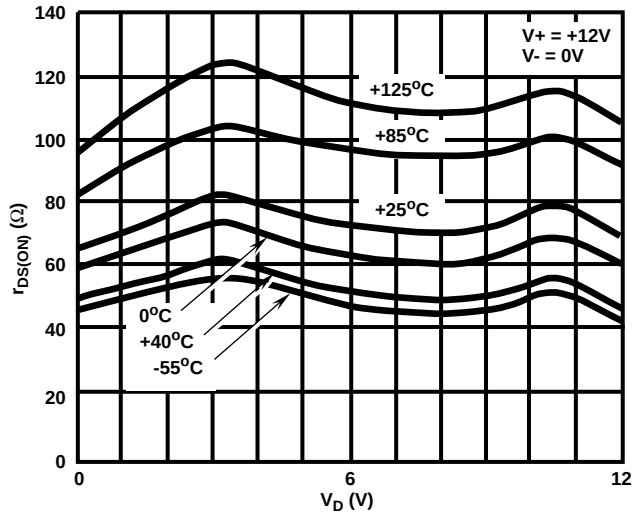


FIGURE 3. $R_{DS(ON)}$ vs V_D AND TEMPERATURE (SINGLE 12V SUPPLY)

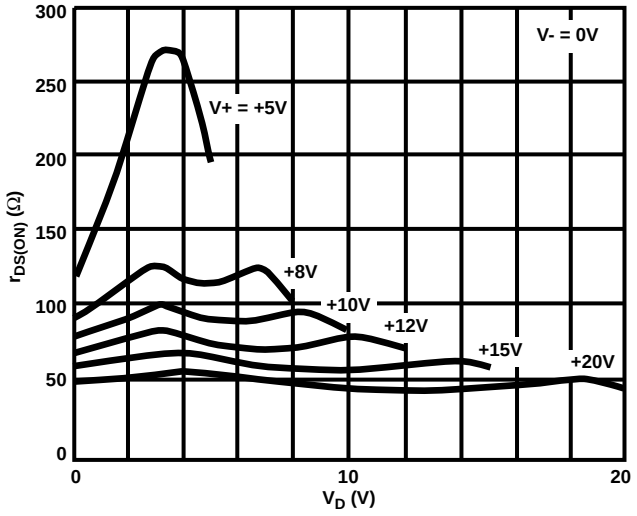


FIGURE 4. $R_{DS(ON)}$ vs V_D AND UNIPOLAR POWER SUPPLY VOLTAGE

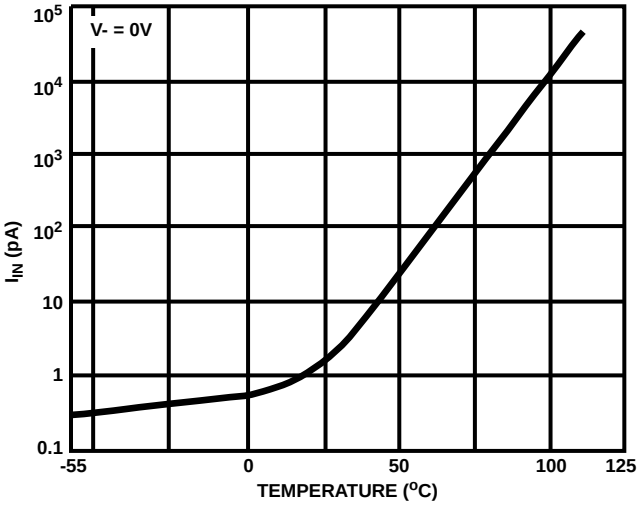


FIGURE 5. INPUT CURRENT vs TEMPERATURE

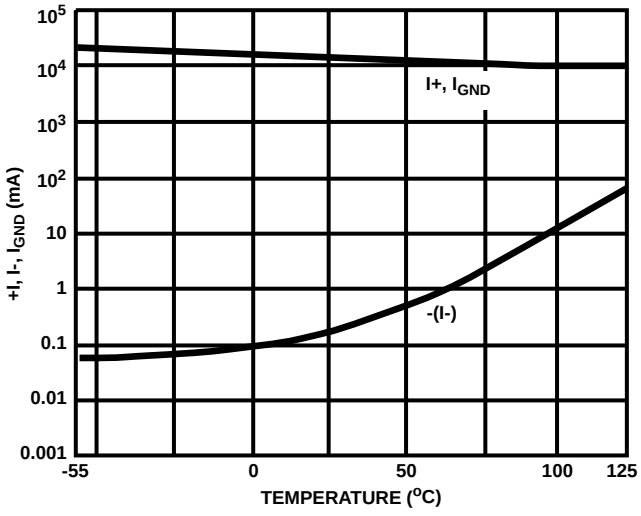


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

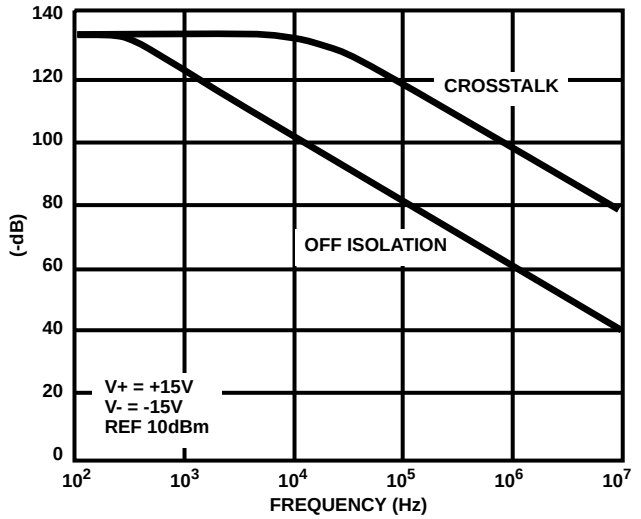


FIGURE 7. CROSSTALK AND OFF ISOLATION vs FREQUENCY

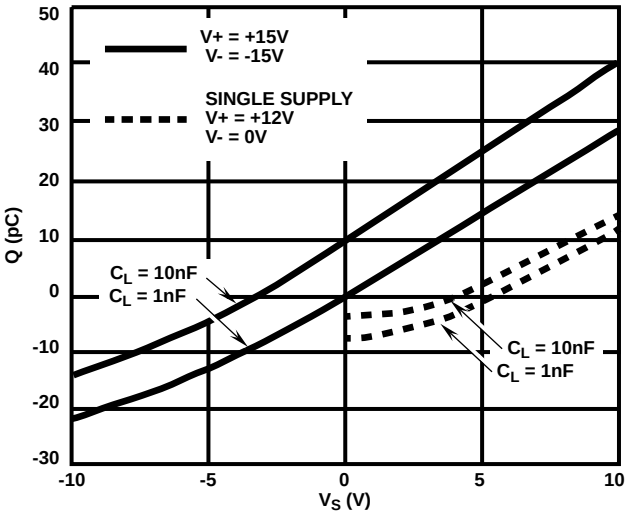


FIGURE 8. CHARGE INJECTION vs SOURCE VOLTAGE

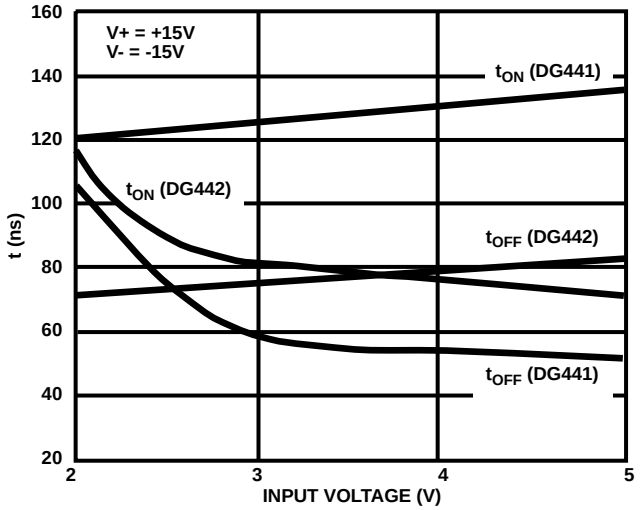


FIGURE 9. SWITCHING TIMES vs INPUT VOLTAGE

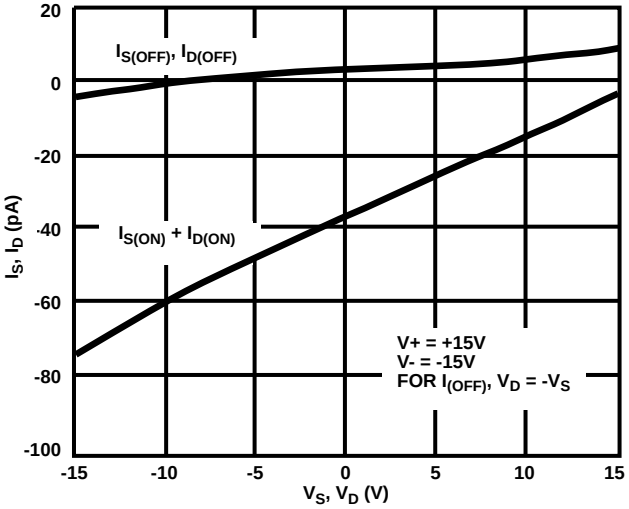


FIGURE 10. SOURCE/DRAIN LEAKAGE CURRENTS

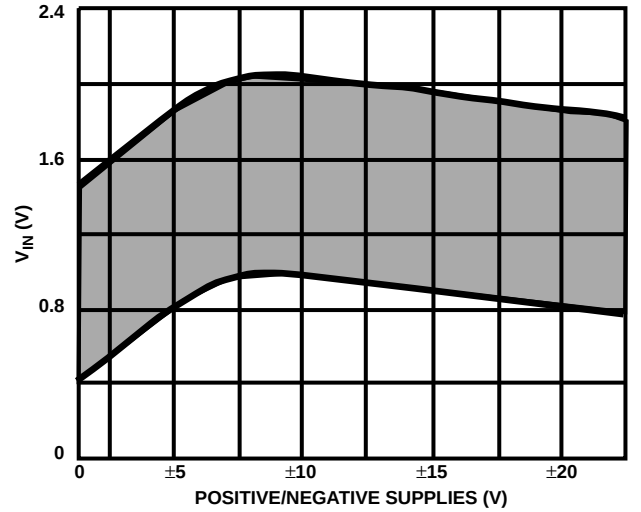


FIGURE 11. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

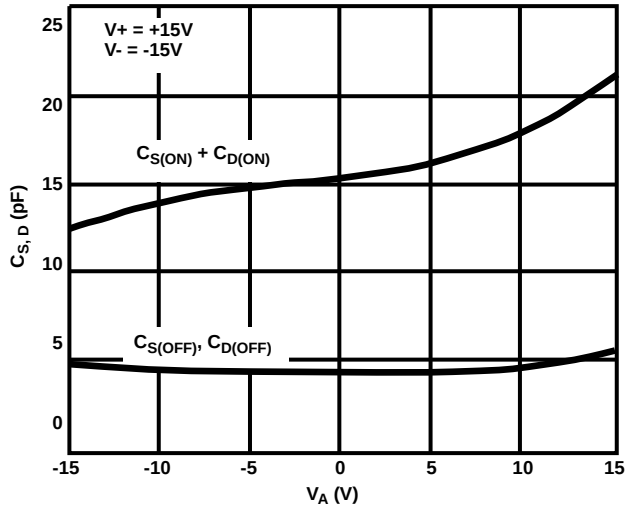


FIGURE 12. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

Typical Performance Curves (Continued)

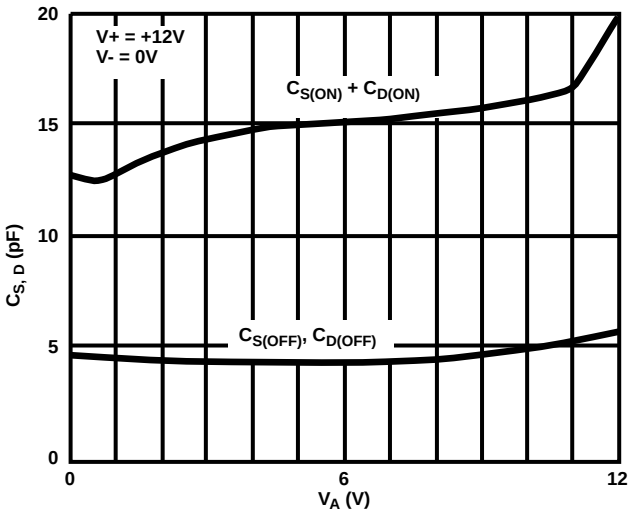


FIGURE 13. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

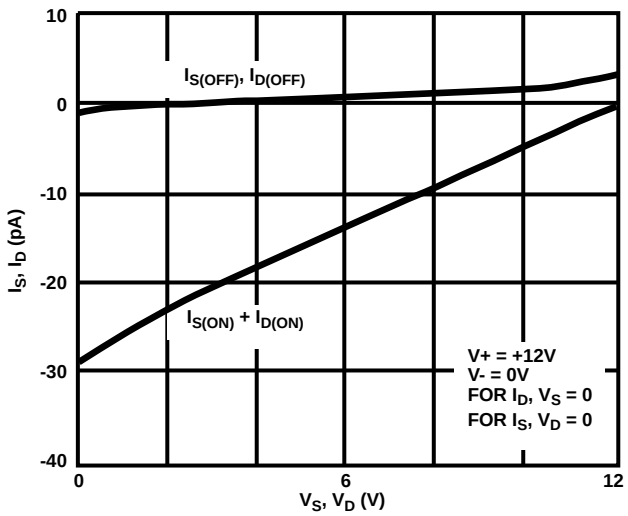


FIGURE 14. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

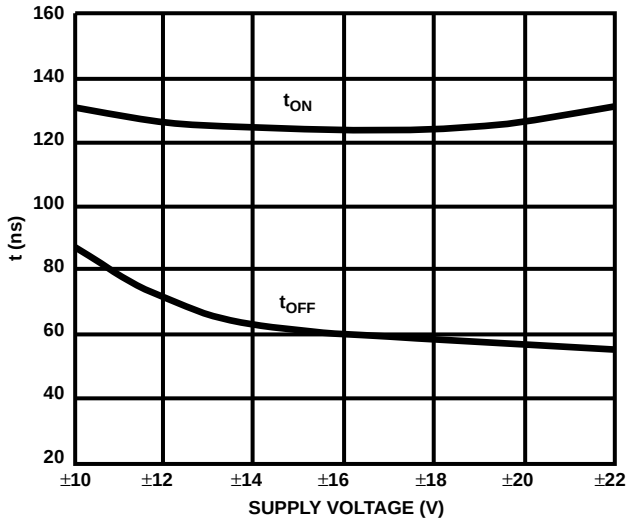


FIGURE 15. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)

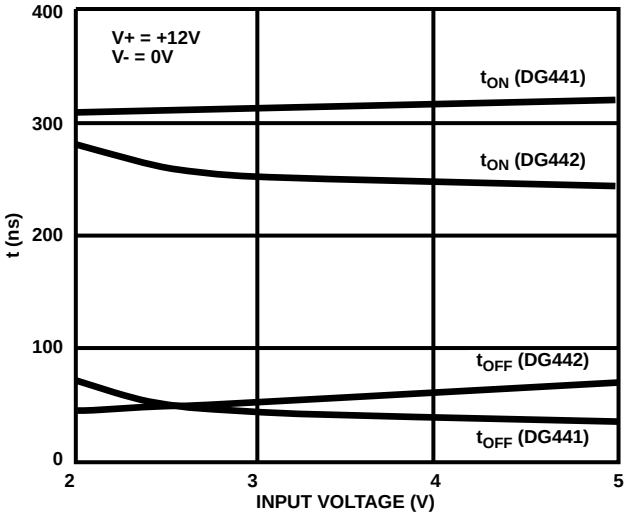


FIGURE 16. SWITCHING TIMES vs INPUT VOLTAGE

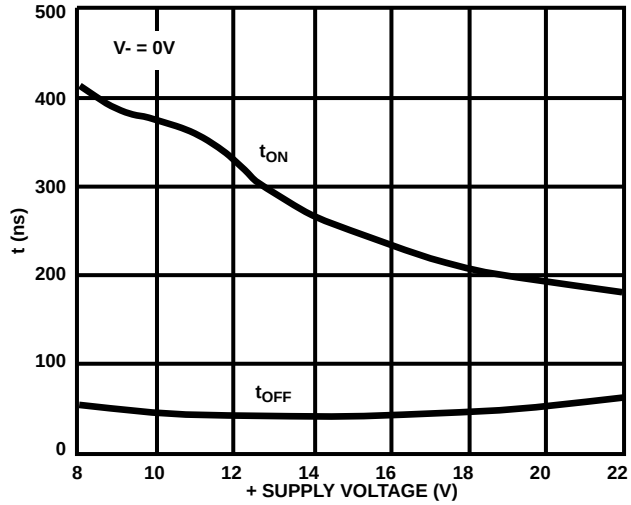


FIGURE 17. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)

Pin Description

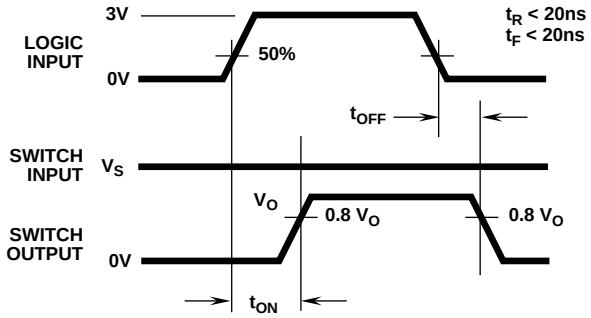
PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic control for switch 1
2	D_1	Drain (output) terminal for switch 1
3	S_1	Source (input) terminal for switch 1
4	V-	Negative power supply terminal
5	GND	Ground terminal (Logic Common)
6	S_4	Source (input) terminal for switch 4
7	D_4	Drain (output) terminal for switch 4
8	IN_4	Logic control for switch 4
9	IN_3	Logic control for switch 3
10	D_3	Drain (output) terminal for switch 3
11	S_3	Source (input) terminal for switch 3
12	NC	No internal connection
13	V+	Positive power supply terminal (substrate)
14	S_2	Source (input) terminal for switch 2
15	D_2	Drain (output) terminal for switch 2
16	IN_2	Logic control for switch 2

TRUTH TABLE

LOGIC	V_{IN}	DG441	DG442
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

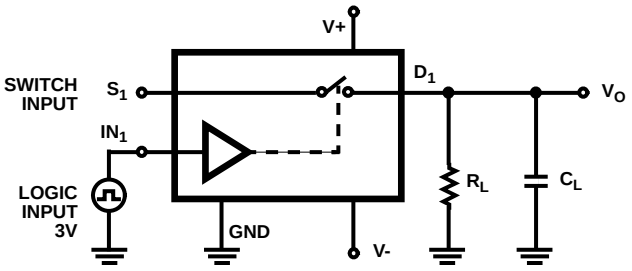
Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 18A.



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 18B.

FIGURE 18. SWITCHING TIME

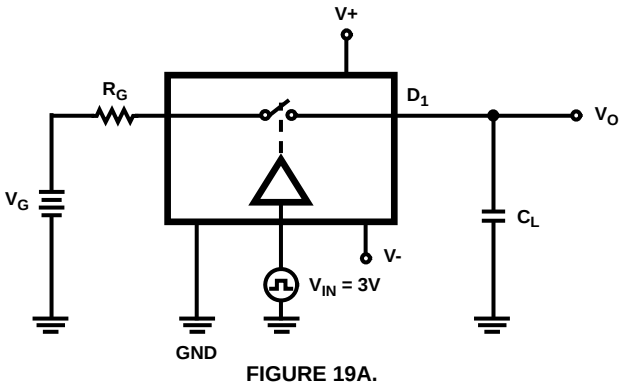


FIGURE 19A.

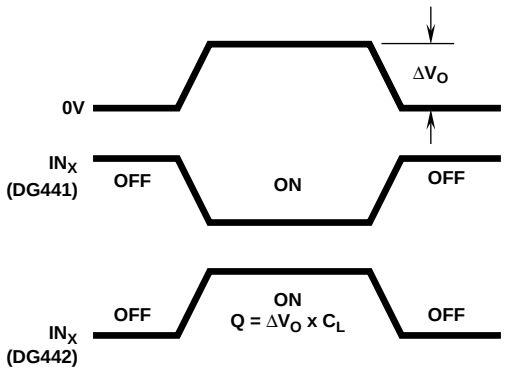


FIGURE 19B.

FIGURE 19. CHARGE INJECTION

Test Circuits (Continued)

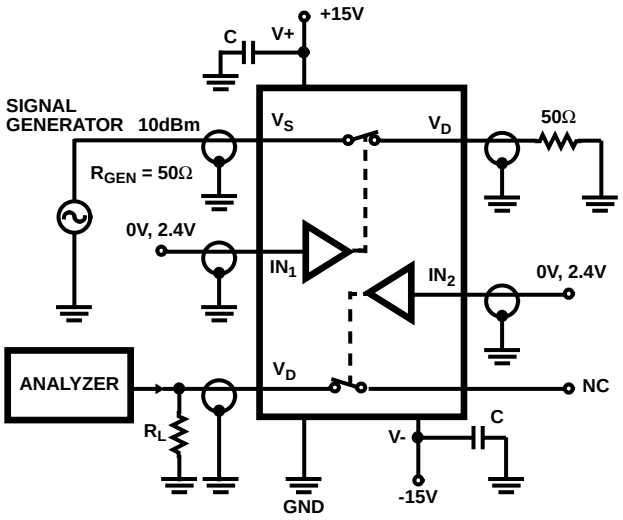


FIGURE 20. CROSSTALK

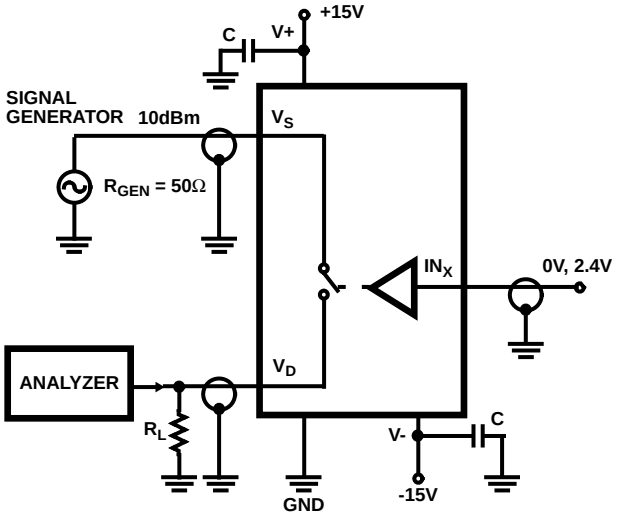


FIGURE 21. OFF ISOLATION

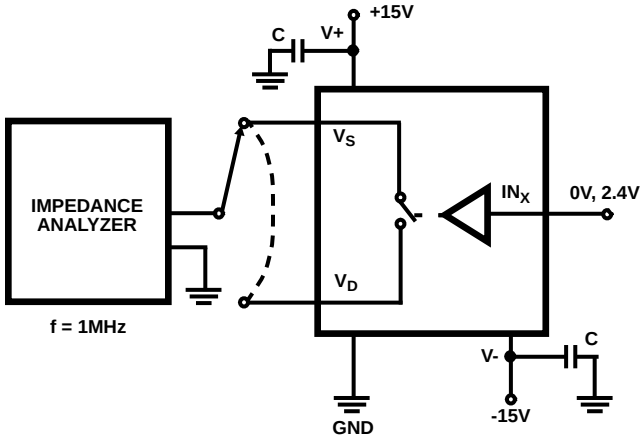
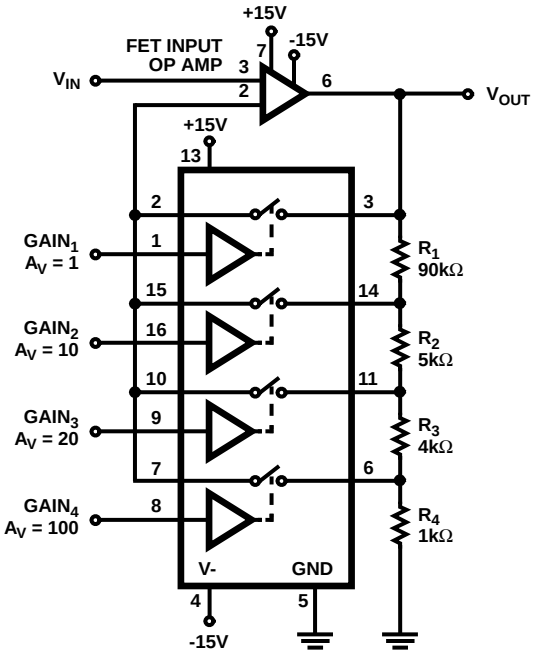


FIGURE 22. SOURCE/DRAIN CAPACITANCES

Applications

GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE. OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OF CIRCUIT



$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW_4 CLOSED

FIGURE 23. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

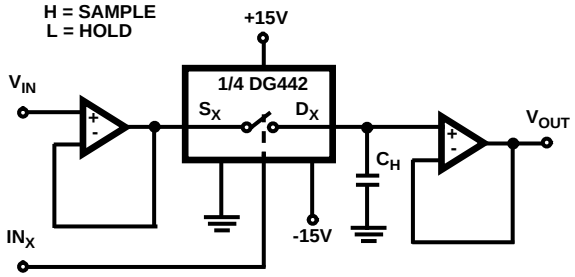


FIGURE 24. OPEN LOOP SAMPLE AND HOLD

Die Characteristics

DIE DIMENSIONS:
2160µm x 1760µm x 485 ± 25µm

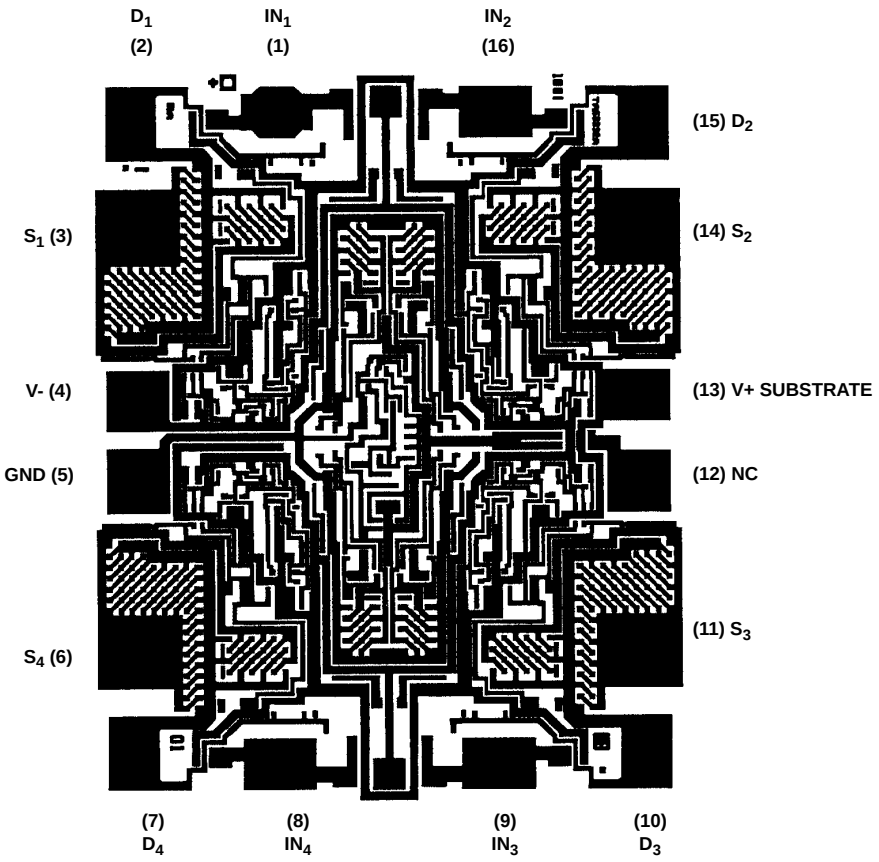
METALLIZATION:
Type: CuAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

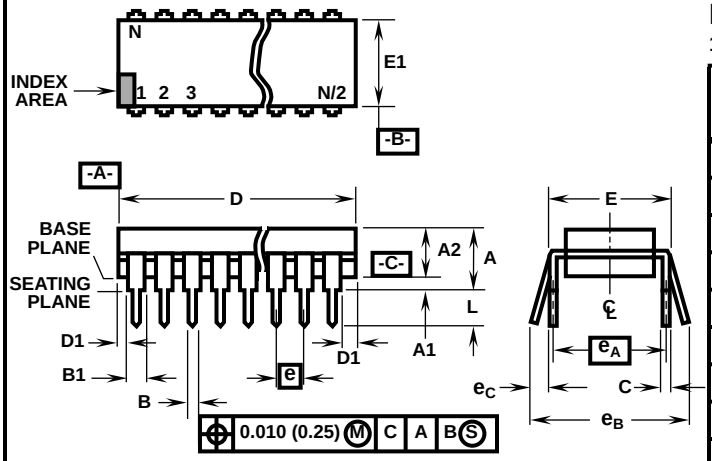
WORST CASE CURRENT DENSITY:
$9.1 \times 10^4 A/cm^2$

Metallization Mask Layout

DG441, DG442



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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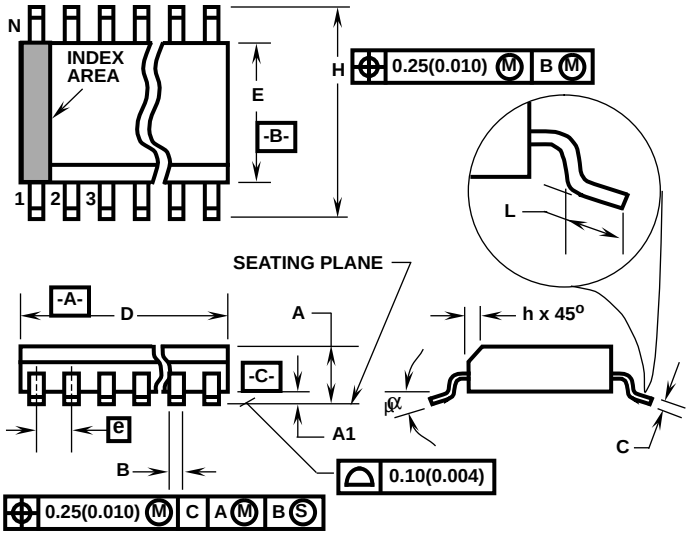
Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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