

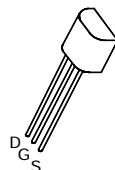
# P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

## ZVP2110A

ISSUE 2 – MARCH 94

### FEATURES

- \* 100 Volt  $V_{DS}$
- \*  $R_{DS(on)}=8\Omega$



E-Line  
TO92 Compatible

### ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	-100	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	$I_D$	-230	mA
Pulsed Drain Current	$I_{DM}$	-3	A
Gate Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation at $T_{amb}=25^{\circ}C$	$P_{tot}$	700	mW
Operating and Storage Temperature Range	$T_j:T_{stg}$	-55 to +150	$^{\circ}C$

### ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

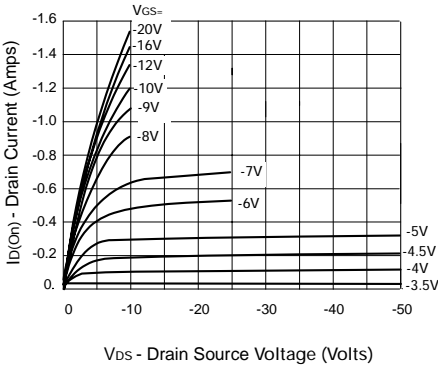
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	$BV_{DSS}$	-100		V	$I_D=-1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D=-1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	$I_{GSS}$		20	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	$I_{DSS}$		-1 -100	$\mu A$ $\mu A$	$V_{DS}=-100V, V_{GS}=0$ $V_{DS}=-80V, V_{GS}=0V, T=125^{\circ}C(2)$
On-State Drain Current(1)	$I_{D(on)}$	-750		mA	$V_{DS}=-25V, V_{GS}=-10V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		8	$\Omega$	$V_{GS}=-10V, I_D=-375mA$
Forward Transconductance (1)(2)	$g_{fs}$	125		mS	$V_{DS}=-25V, I_D=-375mA$
Input Capacitance (2)	$C_{iss}$		100	pF	$V_{DS}=-25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	$C_{oss}$		35	pF	
Reverse Transfer Capacitance (2)	$C_{rss}$		10	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	$V_{DD}\approx -25V, I_D=-375mA$
Rise Time (2)(3)	$t_r$		15	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		12	ns	
Fall Time (2)(3)	$t_f$		15	ns	

(1) Measured under pulsed conditions. Width=300 $\mu s$ . Duty cycle  $\leq 2\%$

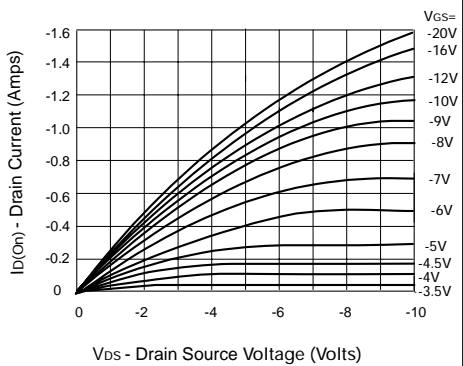
(2) Sample test.

# ZVP2110A

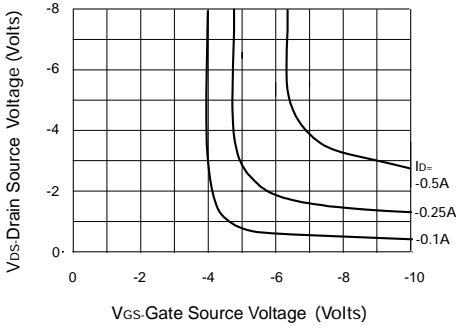
## TYPICAL CHARACTERISTICS



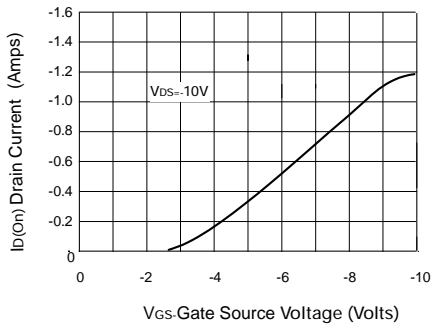
**Output Characteristics**



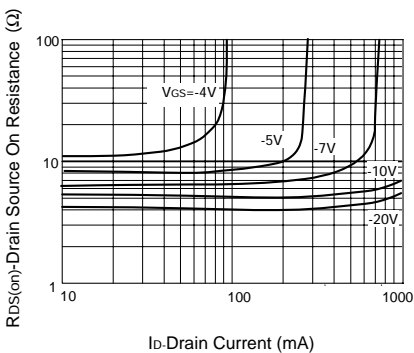
**Saturation Characteristics**



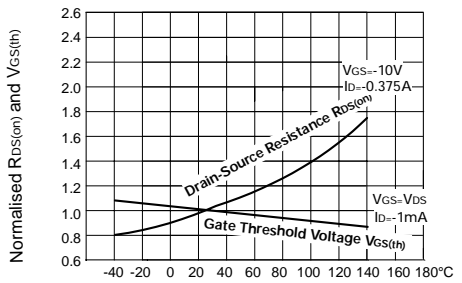
**Voltage Saturation Characteristics**



**Transfer Characteristics**

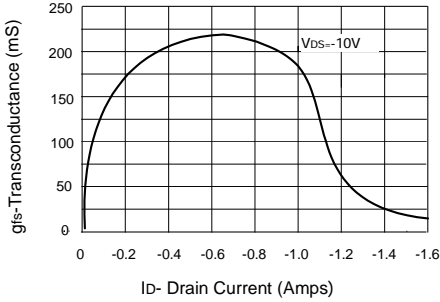


**On-resistance v drain current**

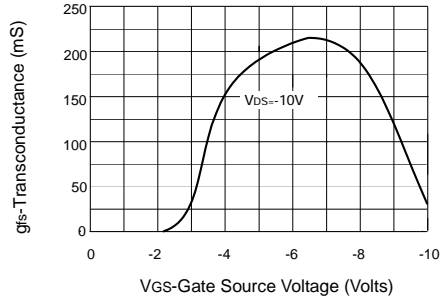


**Normalised RDS(on) and VGS(th) vs Temperature**

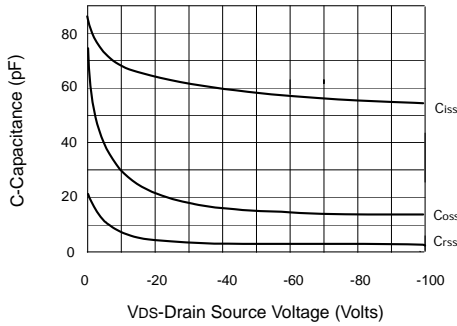
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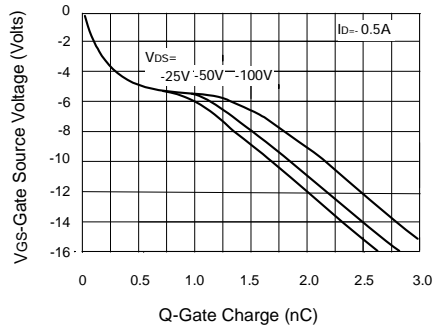
**Transconductance v drain current**



**Transconductance v gate-source voltage**



**Capacitance v drain-source voltage**



**Gate charge v gate-source voltage**