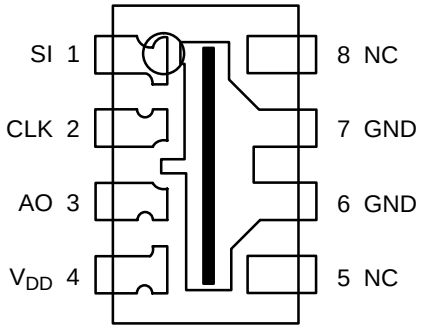
- **128 × 1 Sensor-Element Organization**
- **400 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity**
- **Wide Dynamic Range . . . 4000:1 (72 dB)**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 8 MHz**
- **Single 3-V to 5-V Supply**
- **Rail-to-Rail Output Swing (AO)**
- **No External Load Resistor Required**
- **Replacement for TSL1401 and TSL1401R**
- **RoHS Compliant**

DIP PACKAGE
(TOP VIEW)

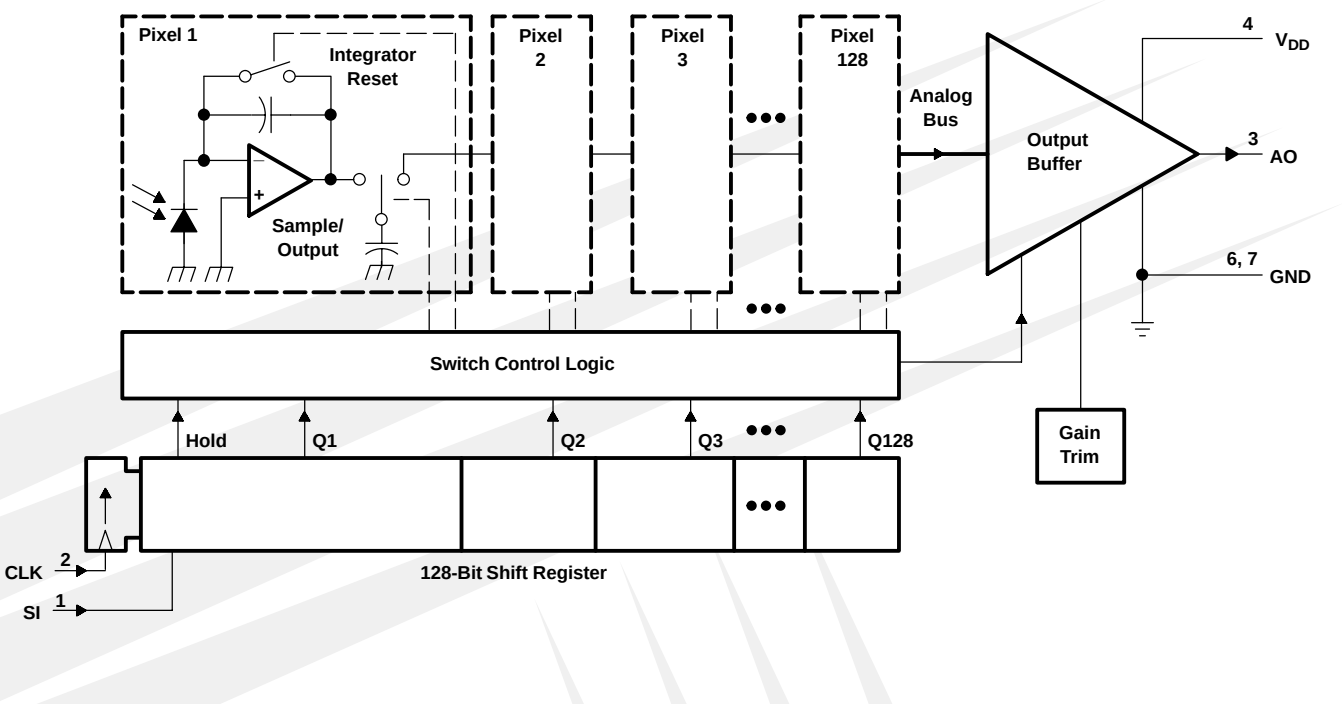


NC − No internal connection

Description

The TSL1401R−LF linear sensor array consists of a 128 × 1 array of photodiodes, associated charge amplifier circuitry, and an internal pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The pixels measure 63.5 µm (H) by 55.5 µm (W) with 63.5-µm center-to-center spacing and 8-µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

Functional Block Diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO	3	Analog output.
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.
NC	5, 8	No internal connection.
SI	1	Serial input. SI defines the start of the data-out sequence.
V_{DD}	4	Supply voltage. Supply voltage for both analog and digital circuits.

Detailed Description

The sensor consists of 128 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time.

The output and reset of the integrators is controlled by a 128-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. For proper operation, after meeting the minimum hold time condition, SI must go low before the next rising edge of the clock. An internal signal, called Hold, is generated from the rising edge of SI and transmitted to analog switches in the pixel circuit. This causes all 128 sampling capacitors to be disconnected from their respective integrators and starts an integrator reset period. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO. Simultaneously, during the first 18 clock cycles, all pixel integrators are reset, and the next integration cycle begins on the 19th clock. On the 129th clock rising edge, the SI pulse is clocked out of the shift register and the analog output AO assumes a high impedance state. Note that this 129th clock pulse is required to terminate the output of the 128th pixel, and return the internal logic to a known state. If a minimum integration time is desired, the next SI pulse may be presented after a minimum delay of t_{qt} (pixel charge transfer time) after the 129th clock pulse.

AO is an op amp-type output that does not require an external pull-down resistor. This design allows a rail-to-rail output voltage swing. With V_{DD} = 5 V, the output is nominally 0 V for no light input, 2 V for normal white level, and 4.8 V for saturation light level. When the device is not in the output phase, AO is in a high-impedance state.

The voltage developed at analog output (AO) is given by:

$$\mathbf{V_{out} = V_{drk} + (R_e)\,(E_e)(t_{int})}$$

where:

- V_{out} is the analog output voltage for white condition
- V_{drk} is the analog output voltage for dark condition
- R_e is the device responsivity for a given wavelength of light given in V/(μJ/cm^2)
- E_e is the incident irradiance in μW/cm^2
- t_{int} is integration time in seconds

A 0.1 μF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

The TSL1401R−LF is intended for use in a wide variety of applications, including: image scanning, mark and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning, and optical linear and rotary encoding.

Absolute Maximum Ratings†

Supply voltage range, V_{DD} . . . . . −0.3 V to 6 V
Input voltage range, V_I . . . . . −0.3 V to V_{DD} + 0.3V
Input clamp current, I_{IK} (V_I < 0) or (V_I > V_{DD}) . . . . . −20 mA to 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) . . . . . −25 mA to 25 mA
Voltage range applied to any output in the high impedance or power-off state, V_O . . . −0.3 V to V_{DD} + 0.3 V
Continuous output current, I_O (V_O = 0 to V_{DD}) . . . . . −25 mA to 25 mA
Continuous current through V_{DD} or GND . . . . . −40 mA to 40 mA
Analog output current range, I_O . . . . . −25 mA to 25 mA
Maximum light exposure at 638 nm . . . . . 5 mJ/cm^2
Operating free-air temperature range, T_A . . . . . −25°C to 85°C
Storage temperature range, T_{stg} . . . . . −25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds‡ . . . . . 260°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Not recommended for solder reflow.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		8000	kHz
Sensor integration time, t_{int} (see Note 1)	0.03375		100	ms
Setup time, serial input, $t_{su(SI)}$	20			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 2)	0			ns
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. Integration time is calculated as follows:

t_{int} = (128 − 18) × clock period + 20 μs

where *128* is the number of pixels in series, *18* is the required logic setup clocks, and *20 μs* is the pixel charge transfer time (t_{qt})

2. SI must go low before the rising edge of the next clock pulse.

Electrical Characteristics at f_{clock} = 1 MHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 640 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 11 μW/cm² (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{out}	Analog output voltage (white, average over 128 pixels)	See Note 4	1.6	2	2.4	V
V_{drk}	Analog output voltage (dark, average over 128 pixels)	E_e = 0	0	0.1	0.2	V
PRNU	Pixel response nonuniformity	See Note 5		±4%	±7.5%	
	Nonlinearity of analog output voltage	See Note 6		±0.4%		FS
	Output noise voltage	See Note 7		1		mVrms
R_e	Responsivity	See Note 8	25	35	45	V/(μJ/cm²)
V_{sat}	Analog output saturation voltage	V_{DD} = 5 V, R_L = 330 Ω	4.5	4.8		V
		V_{DD} = 3 V, R_L = 330 Ω	2.5	2.8		
SE	Saturation exposure	V_{DD} = 5 V, See Note 9		136		nJ/cm²
		V_{DD} = 3 V, See Note 9		78		
DSNU	Dark signal nonuniformity	All pixels, E_e = 0, See Note 10		0.02	0.05	V
IL	Image lag	See Note 11		0.5%		
I_{DD}	Supply current	V_{DD} = 5 V, E_e = 0		2.8	4.5	mA
		V_{DD} = 3 V, E_e = 0		2.6	4.5	
I_{IH}	High-level input current	$V_I = V_{DD}$			1	μA
I_{IL}	Low-level input current	V_I = 0			1	μA
C_i	Input capacitance			5		pF

NOTES: 3. All measurements made with a 0.1 μF capacitor connected between V_{DD} and ground.
4. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640 nm.
5. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated at the white irradiance level. PRNU includes DSNU.
6. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
7. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
8. $R_{e(min)} = [V_{out(min)} - V_{drk(max)}] \div (E_e \times t_{int})$
9. $SE(min) = [V_{sat(min)} - V_{drk(min)}] \times \langle E_e \times t_{int}) \div [V_{out(max)} - V_{drk(min)}]$
10. DSNU is the difference between the maximum and minimum output voltage for all pixels in the absence of illumination.
11. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out\ (IL)} - V_{drk}}{V_{out\ (white)} - V_{drk}} \times 100$$

Timing Requirements (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
$t_{su(SI)}$	Setup time, serial input (see Note 12)	20			ns
$t_{h(SI)}$	Hold time, serial input (see Note 12 and Note 13)	0			ns
t_w	Pulse duration, clock high or low	50			ns
t_r, t_f	Input transition (rise and fall) time	0		500	ns
t_{qt}	Pixel charge transfer time	20			μs

NOTES: 12. Input pulses have the following characteristics: t_r = 6 ns, t_f = 6 ns.
13. SI must go low before the rising edge of the next clock pulse.

Dynamic Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 7 and 8)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 10 pF		120		ns

TYPICAL CHARACTERISTICS

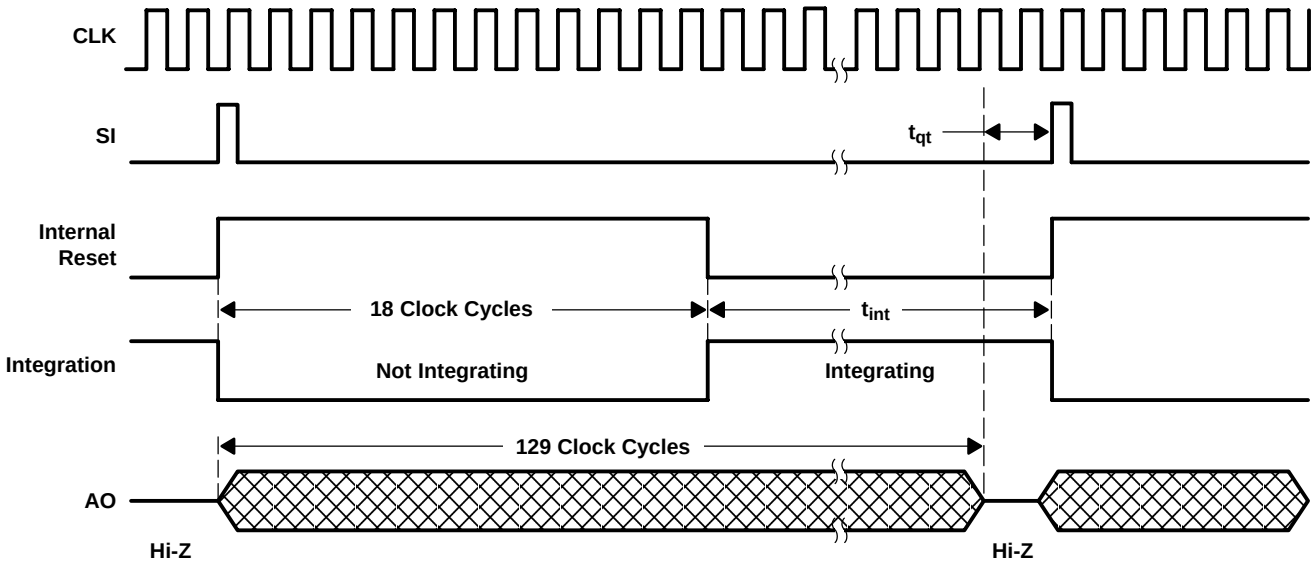


Figure 1. Timing Waveforms

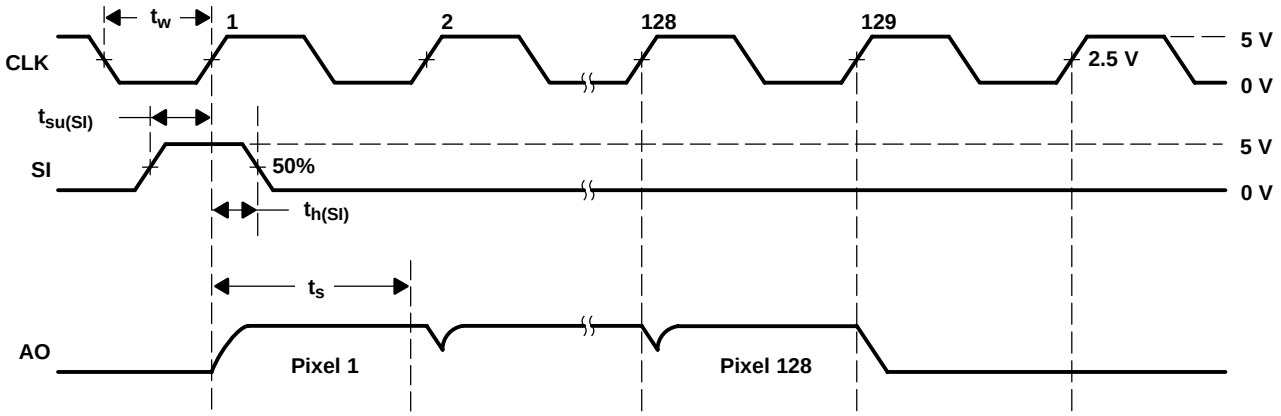


Figure 2. Operational Waveforms

TYPICAL CHARACTERISTICS

PHOTODIODE SPECTRAL RESPONSIVITY

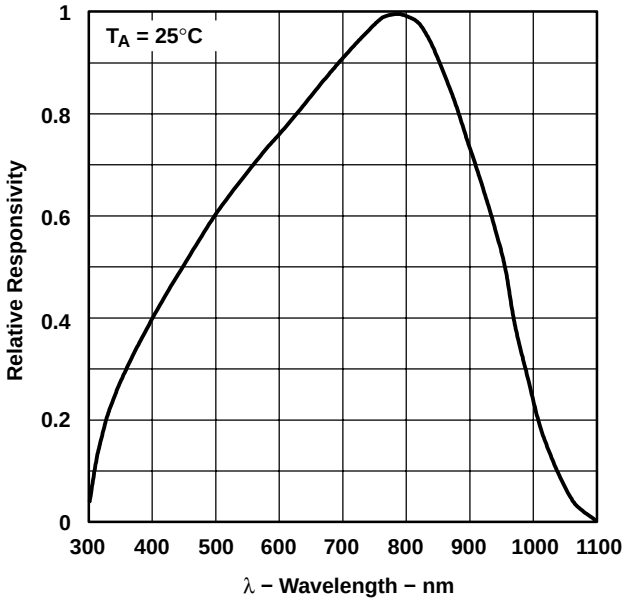


Figure 3

NORMALIZED IDLE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

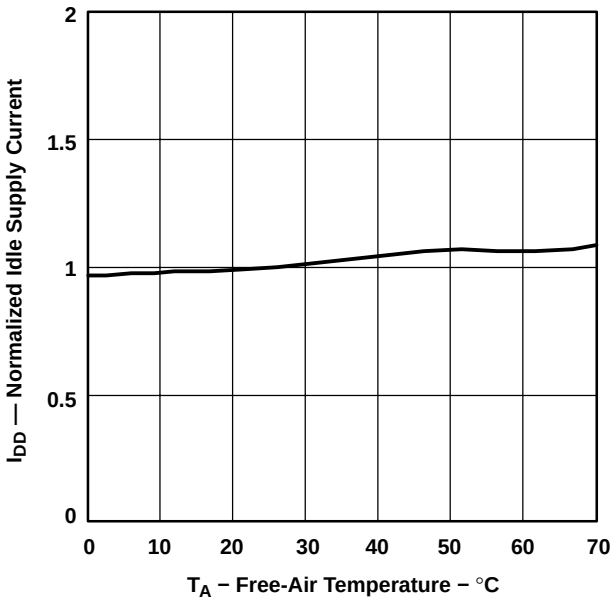


Figure 4

WHITE OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

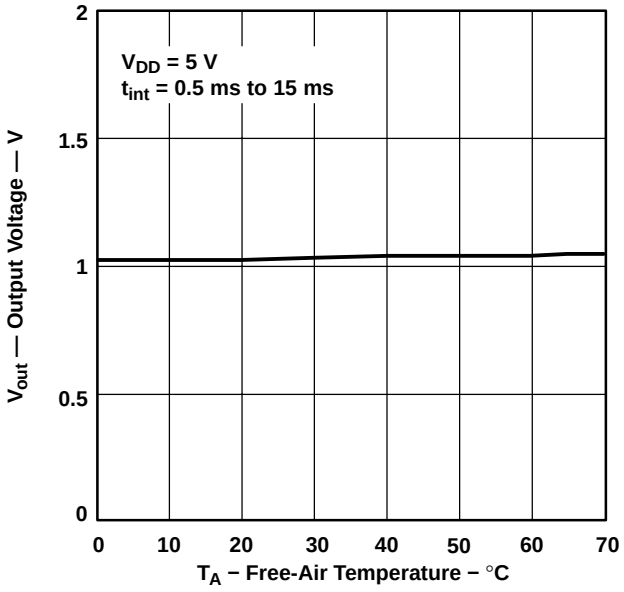


Figure 5

DARK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

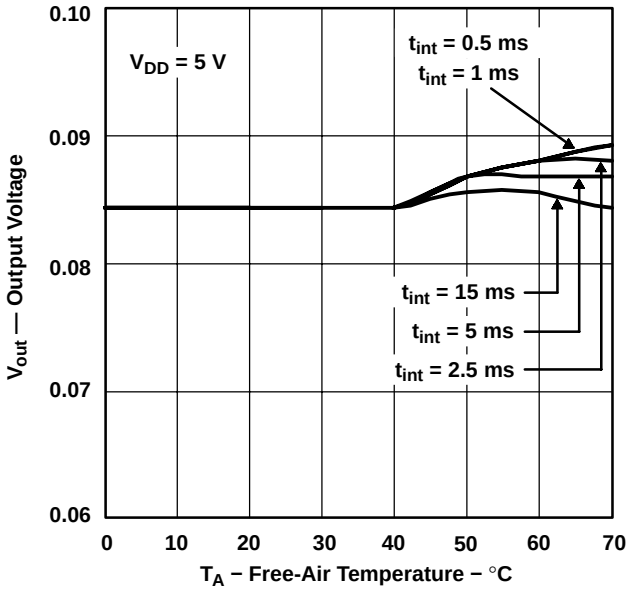


Figure 6

TYPICAL CHARACTERISTICS

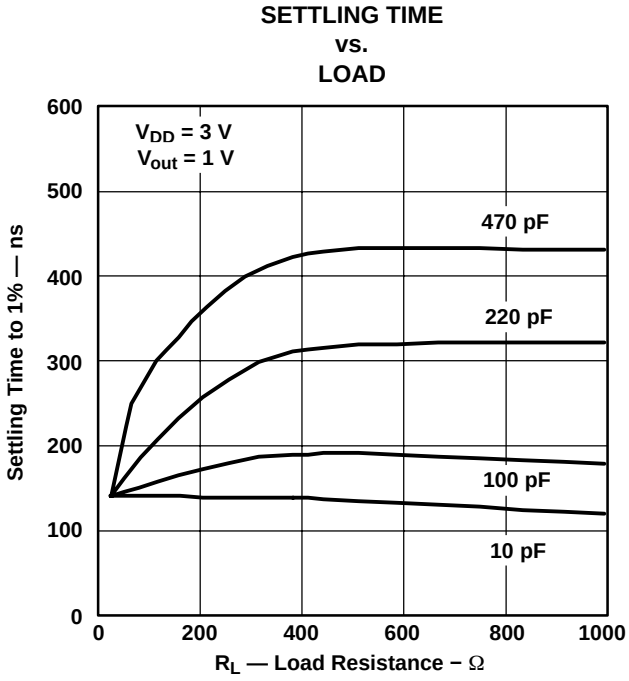


Figure 7

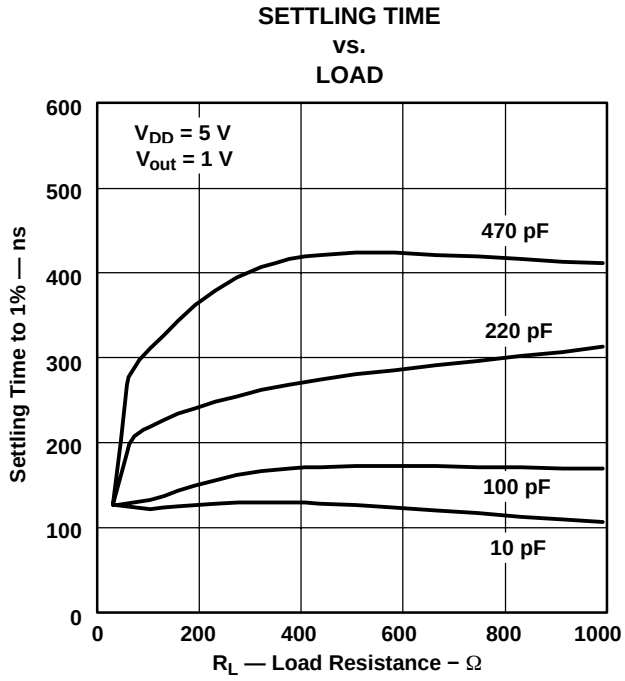
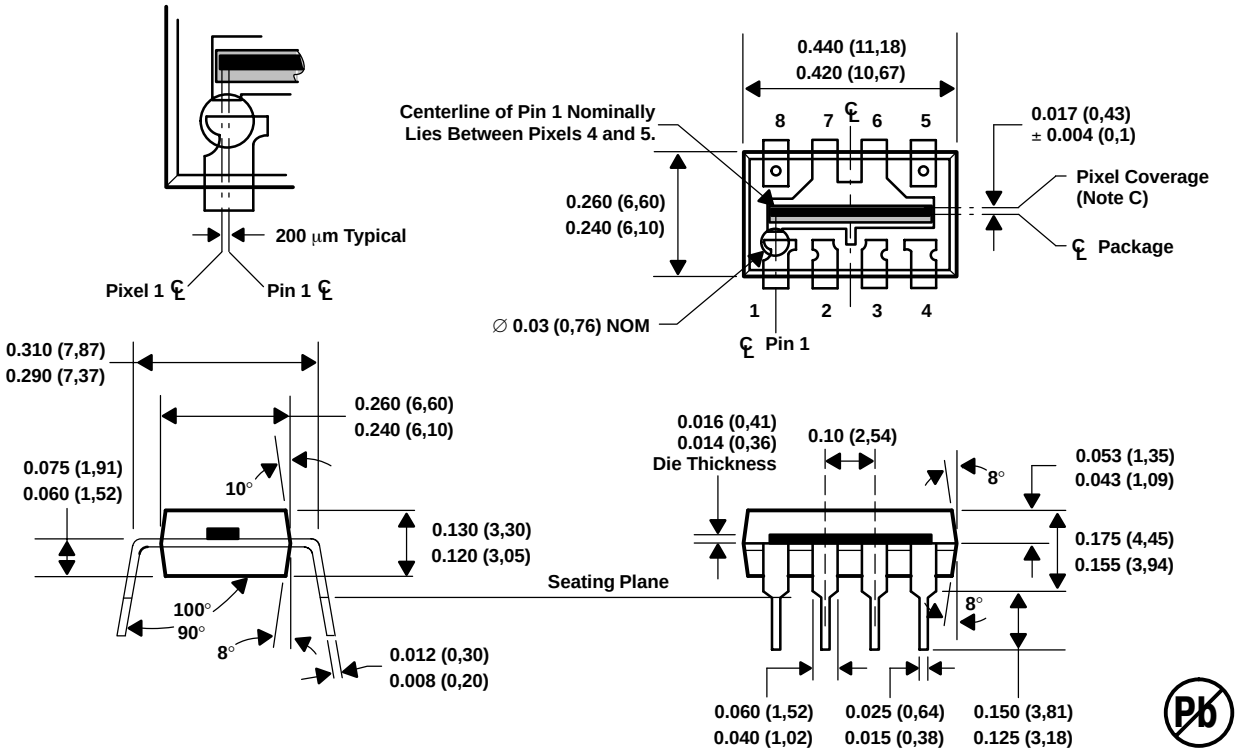


Figure 8

MECHANICAL INFORMATION

This dual-in-line package consists of an integrated circuit mounted on a lead frame and encapsulated in an electrically nonconductive clear plastic compound.



NOTES: A. All linear dimensions are in inches and (millimeters).
B. Index of refraction of clear plastic is 1.55.
C. Center of pixel active areas typically located under this line.
D. Lead finish is NiPd.
E. This drawing is subject to change without notice.

Figure 9. Packaging Configuration

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