G3R30MT12J
1200 V 30 mΩ SiC MOSFET

GeneSiC™
SEMICONDUCTOR

Silicon Carbide MOSFET
N-Channel Enhancement Mode

|		
V_{DS}	=	1200 V
$R_{DS(ON)(Typ.)}$	=	30 mΩ
I_D (Tc = 100°C)	=	68 A

Features

- G3R™ Technology - +15 V / -5 V Gate Drive
- Superior Q_G x $R_{DS(ON)}$ Figure of Merit
- Low Capacitances and Low Gate Charge
- Normally-Off Stable Operation up to 175°C
- Fast and Reliable Body Diode
- High Avalanche and Short Circuit Ruggedness
- Low Conduction Losses at High Temperatures
- Optimized Package with Separate Driver Source Pin

Package

Case (D)

G3R30MT12J

G KS S
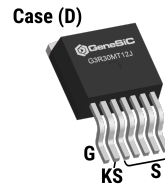
TO-263-7
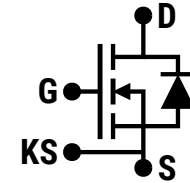
D = Drain
G = Gate
S = Source
KS = Kelvin Source

✔ RoHS

✔ REACH

Advantages

- Increased Power Density for Compact System
- High Frequency Switching
- Reduced Losses for Higher System Efficiency
- Minimized Gate Ringing
- Improved Thermal Capability
- Superior Cost-Performance Index
- Ease of Paralleing without Thermal Runaway
- Simple to Drive

Applications

- Solar Inverters
- Motor Drives
- EV Charging
- High Voltage DC-DC Converters
- Switched Mode Power Supplies
- UPS
- Smart Grid Transmission and Distribution
- Induction Heating and Welding

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	1200	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +20	V	
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +15	V	
Continuous Forward Current	I_D	T_C = 25°C, V_{GS} = -5 / +15 V	96	A	Fig. 15
		T_C = 100°C, V_{GS} = -5 / +15 V	68		
		T_C = 135°C, V_{GS} = -5 / +15 V	50		
Pulsed Drain Current	$I_{D(pulse)}$	t_P ≤ 10µs, D ≤ 1%, Note 1	200	A	Fig. 14
Power Dissipation	P_D	T_C = 25°C	459	W	Fig. 16
Operating and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

Thermal/Package Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Thermal Resistance, Junction - Case	R_{thJC}			0.26	0.33	°C/W	Fig. 13
Weight	W_T			1.45		g	

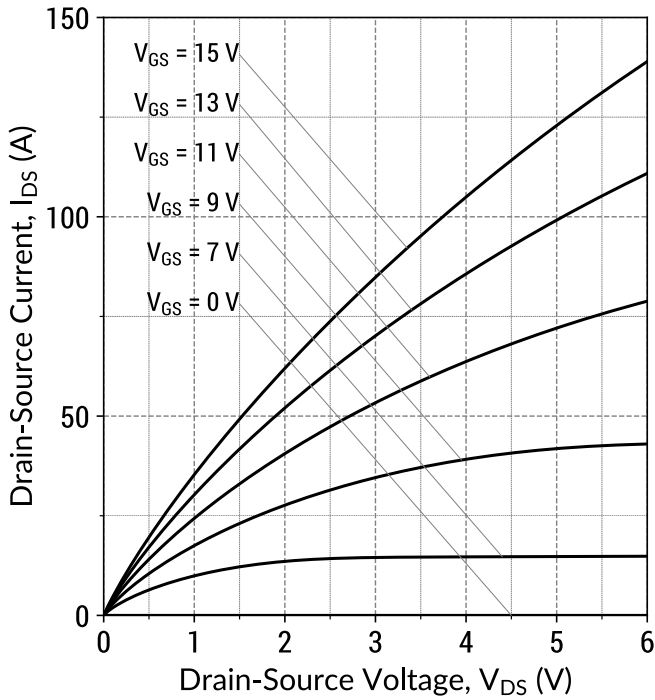*Note 1: Pulse Width t_P Limited by $T_{j(max)}$*

Electrical Characteristics (At T$_C$ = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Drain-Source Breakdown Voltage	V$_{DSS}$	V$_{GS}$ = 0 V, I$_D$ = 100 µA	1200			V	
Zero Gate Voltage Drain Current	I$_{DSS}$	V$_{DS}$ = 1200 V, V$_{GS}$ = 0 V		1		µA	
Gate Source Leakage Current	I$_{GSS}$	V$_{DS}$ = 0 V, V$_{GS}$ = 20 V			100	nA	
		V$_{DS}$ = 0 V, V$_{GS}$ = -10 V			-100		
Gate Threshold Voltage	V$_{GS(th)}$	V$_{DS}$ = V$_{GS}$, I$_D$ = 12.0 mA		2.69		V	Fig. 9
		V$_{DS}$ = V$_{GS}$, I$_D$ = 12.0 mA, T$_j$ = 175°C		2.05			
Transconductance	g$_{fs}$	V$_{DS}$ = 10 V, I$_D$ = 50 A		20.7		S	Fig. 4
		V$_{DS}$ = 10 V, I$_D$ = 50 A, T$_j$ = 175°C		23.2			
Drain-Source On-State Resistance	R$_{DS(ON)}$	V$_{GS}$ = 15 V, I$_D$ = 50 A		30	36	mΩ	Fig. 5-8
		V$_{GS}$ = 15 V, I$_D$ = 50 A, T$_j$ = 175°C		41			
Input Capacitance	C$_{iss}$	V$_{DS}$ = 800 V, V$_{GS}$ = 0 V f = 1 MHz, V$_{AC}$ = 25mV		3901		pF	Fig. 11
Output Capacitance	C$_{oss}$			151			
Reverse Transfer Capacitance	C$_{rss}$			23.9			
C$_{oss}$ Stored Energy	E$_{oss}$			60		µJ	Fig. 12
C$_{oss}$ Stored Charge	Q$_{oss}$			214		nC	
Gate-Source Charge	Q$_{gs}$	V$_{DS}$ = 800 V, V$_{GS}$ = -5 / +15 V I$_D$ = 50 A Per IEC607478-4		45		nC	Fig. 10
Gate-Drain Charge	Q$_{gd}$			72			
Total Gate Charge	Q$_g$			155			
Internal Gate Resistance	R$_{G(int)}$	f = 1 MHz, V$_{AC}$ = 25 mV		1.7		Ω	

Reverse Diode Characteristics

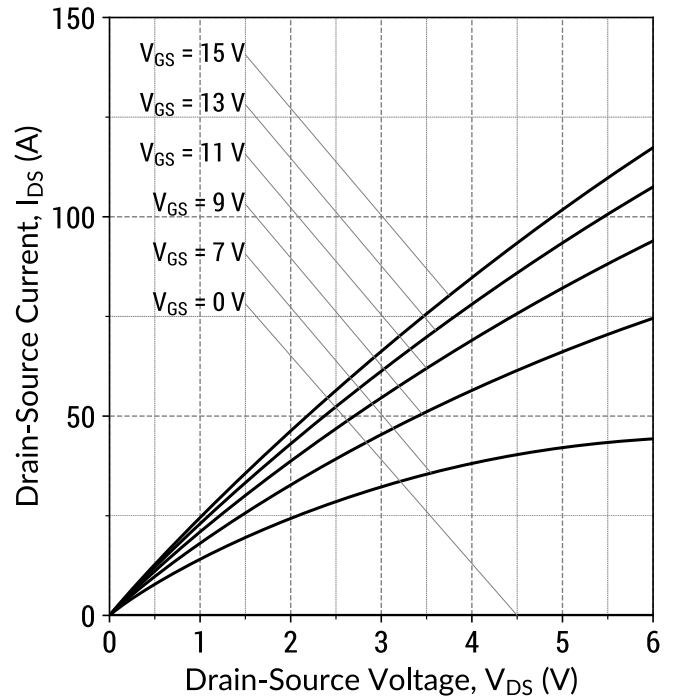| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Diode Forward Voltage	V$_{SD}$	V$_{GS}$ = -5 V, I$_{SD}$ = 25 A		4.9		V	Fig. 17-18
		V$_{GS}$ = -5 V, I$_{SD}$ = 25 A, T$_j$ = 175°C		4.4			
Continuous Diode Forward Current	I$_S$	V$_{GS}$ = -5 V, T$_c$ = 100°C	41			A	
Diode Pulse Current	I$_{S(pulse)}$	V$_{GS}$ = -5 V, Note 1		164		A	

G3R30MT12J
1200 V 30 mΩ SiC MOSFET

GeneSiC™ SEMICONDUCTOR

Figure 1: Output Characteristics (T_j = 25°C)

V_{GS} = 15 V
V_{GS} = 13 V
V_{GS} = 11 V
V_{GS} = 9 V
V_{GS} = 7 V
V_{GS} = 0 V

Drain-Source Current, I_{DS} (A)
Drain-Source Voltage, V_{DS} (V)

$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 2: Output Characteristics (T_j = 175°C)

V_{GS} = 15 V
V_{GS} = 13 V
V_{GS} = 11 V
V_{GS} = 9 V
V_{GS} = 7 V
V_{GS} = 0 V

Drain-Source Current, I_{DS} (A)
Drain-Source Voltage, V_{DS} (V)

$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 3: Output Characteristics (V_GS = 15 V)

T_j = 175°C
T_j = 150°C
T_j = 125°C
T_j = 25°C

Drain-Source Current, I_{DS} (A)
Drain-Source Voltage, V_{DS} (V)
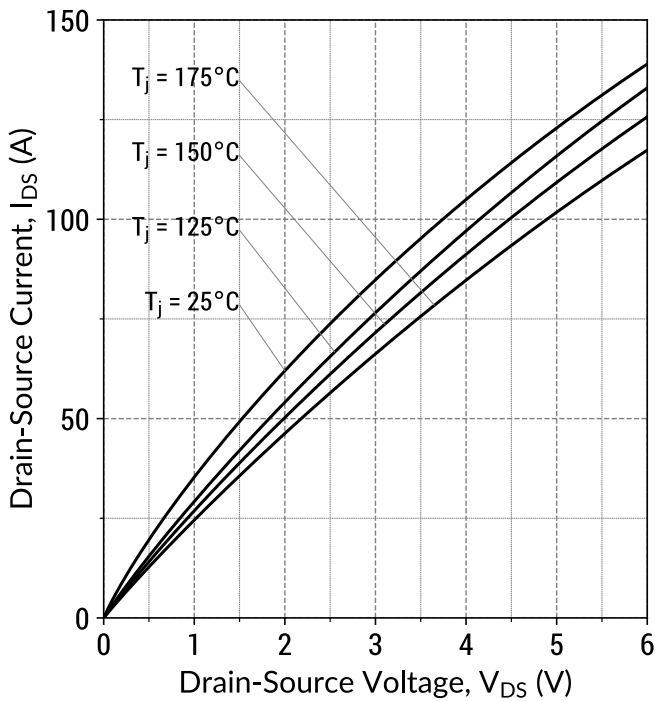
$I_D = f(V_{DS}, T_j)$; t_P = 250 µs

Figure 4: Transfer Characteristics (V_DS = 10 V)

T_j = 175°C
T_j = 25°C

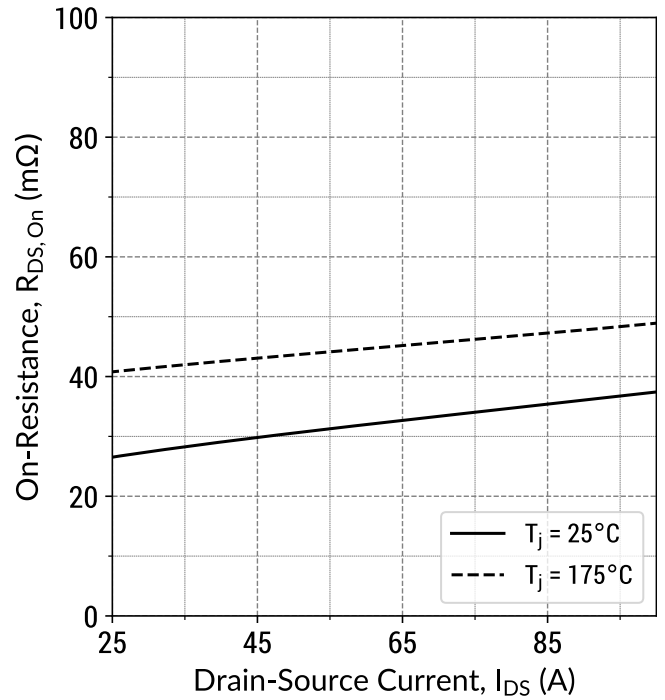Drain-Source Current, I_{DS} (A)
Gate-Source Voltage, V_{GS} (V)
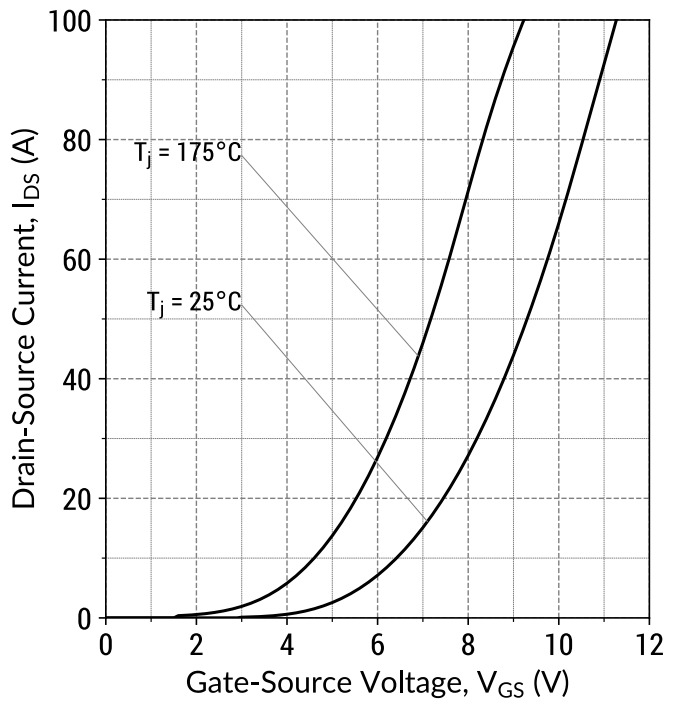
$I_D = f(V_{GS}, T_j)$; t_P = 100 µs
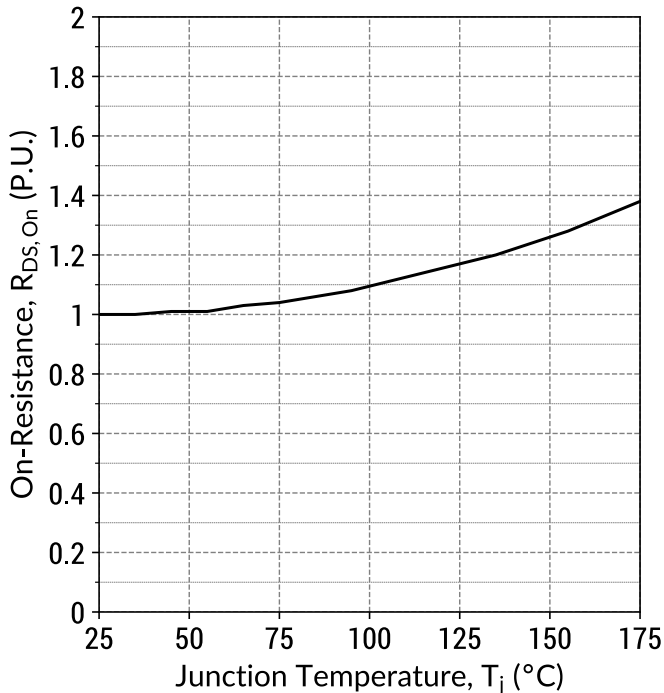
Figure 5: On-State Resistance v/s Temperature
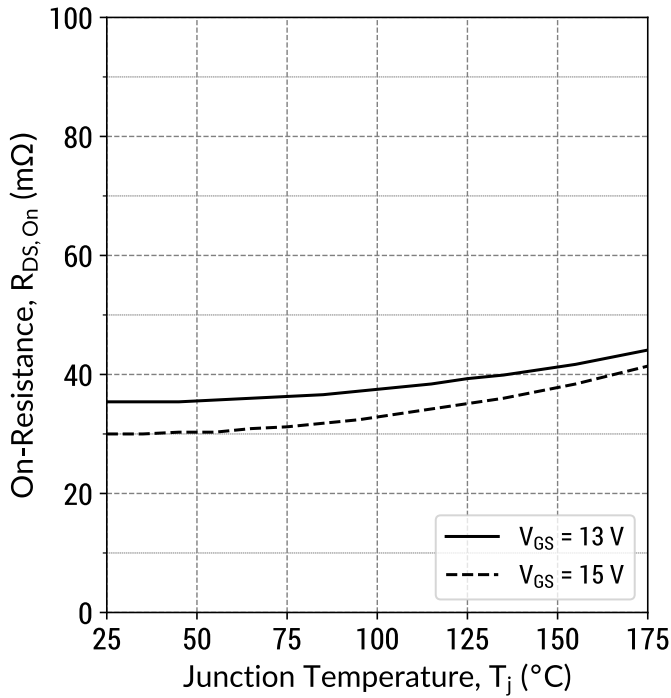
$R_{DS(ON)} = f(T_j, V_{GS})$; $t_P = 250$ μs; $I_D = 50$ A
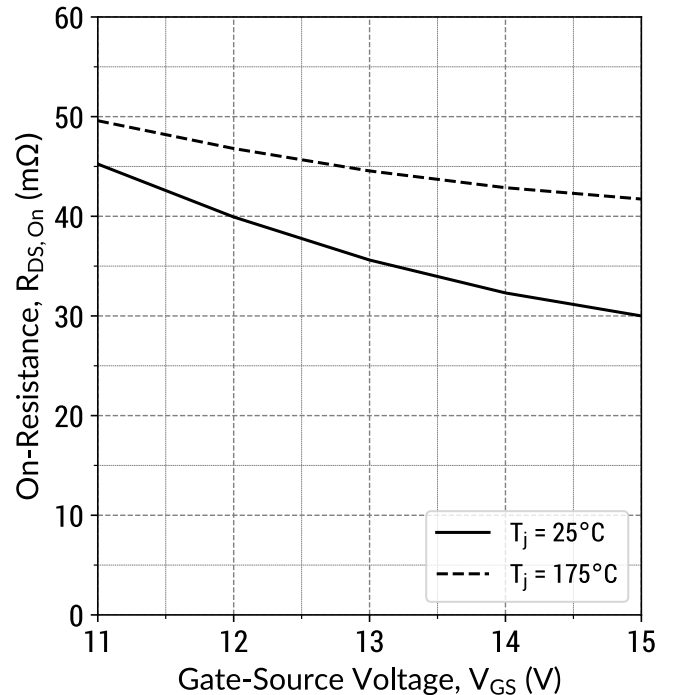
Figure 6: On-State Resistance v/s Drain Current

$R_{DS(ON)} = f(T_j, I_D)$; $t_P = 250$ μs; $V_{GS} = 15$ V

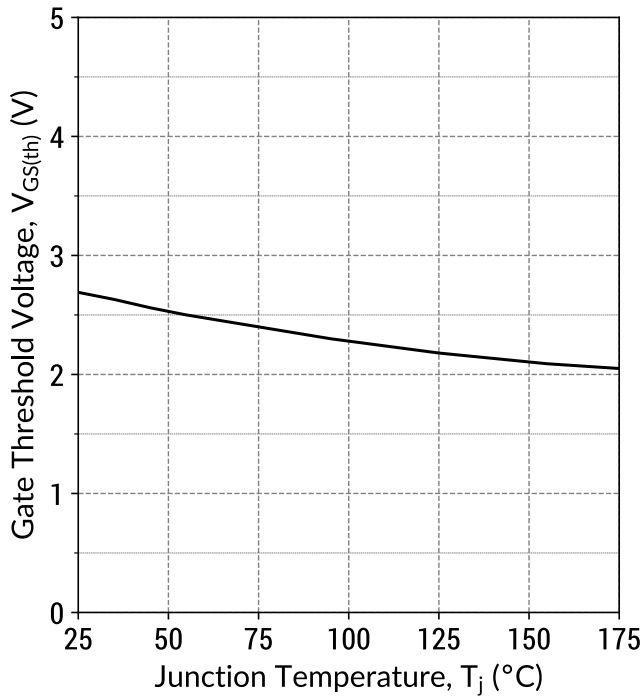## Figure 7: Normalized On-State Resistance v/s Temperature

$R_{DS(ON)} = f(T_j)$; $t_P = 250$ μs; $I_D = 50$ A; $V_{GS} = 15$ V

Figure 8: On-State Resistance v/s Gate Voltage
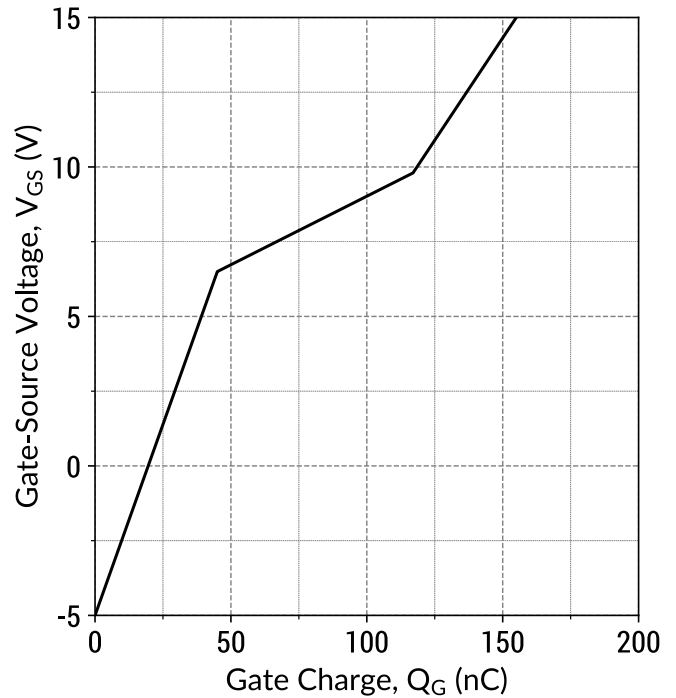

$R_{DS(ON)} = f(T_j, V_{GS})$; $t_P = 250$ μs; $I_D = 50$ A

Figure 9: Threshold Voltage Characteristics

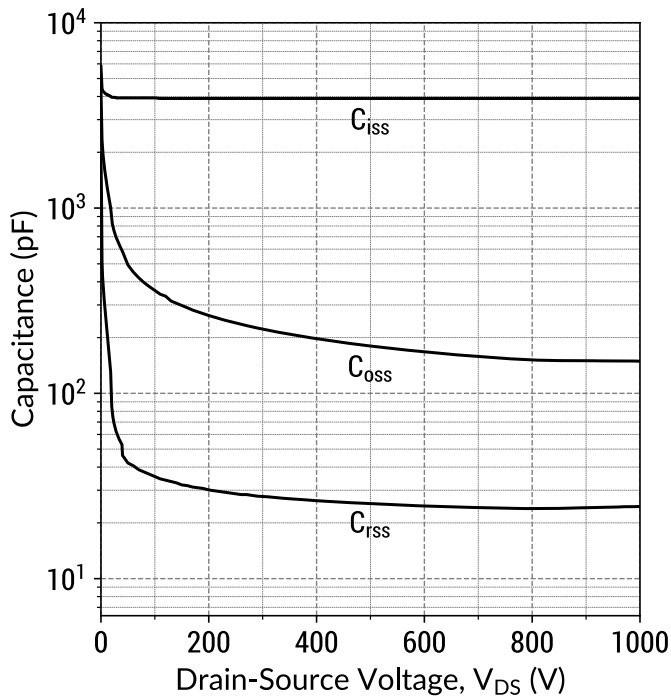$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; $I_D = 12.0$ mA
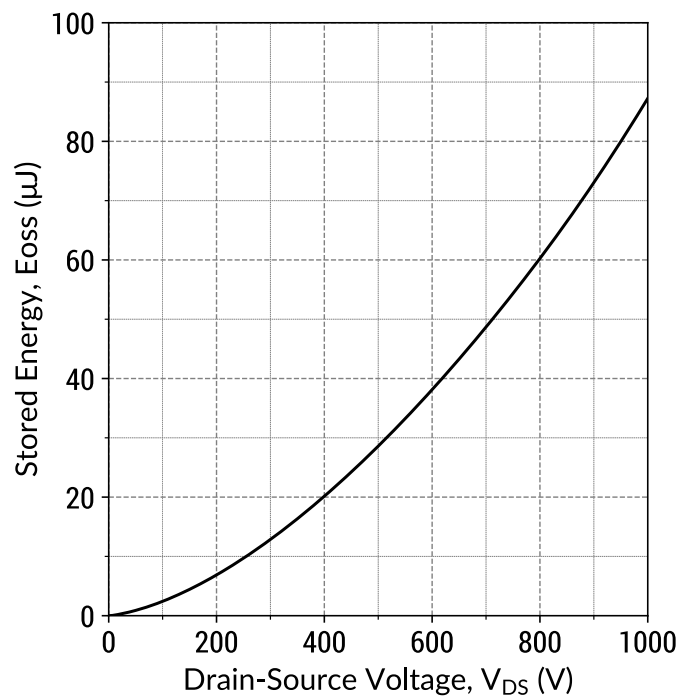
Figure 10: Gate Charge Characteristics

$I_D = 50$ A; $V_{DS} = 800$ V; $T_c = 25°C$

Figure 11: Capacitance v/s Drain-Source Voltage
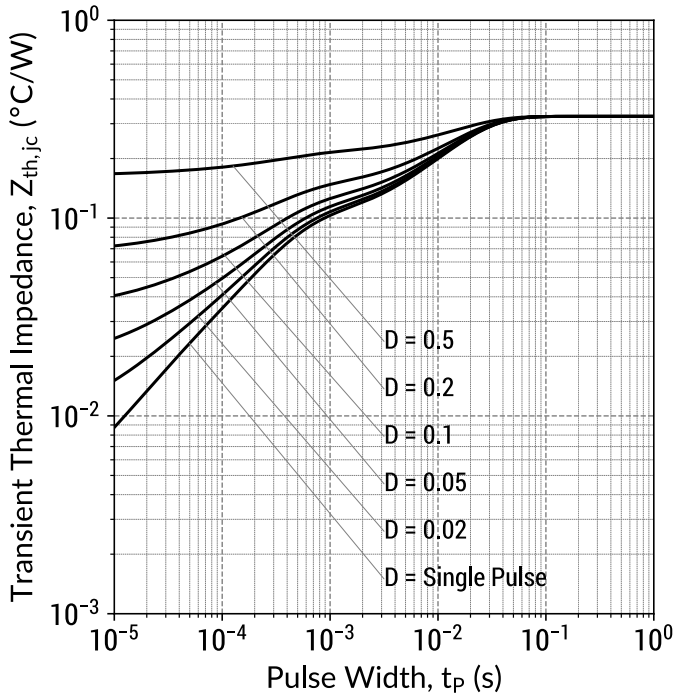

$f = 1$ MHz; $V_{AC} = 25$mV

Figure 12: Output Capacitor Stored Energy

$E_{oss} = f(V_{DS})$
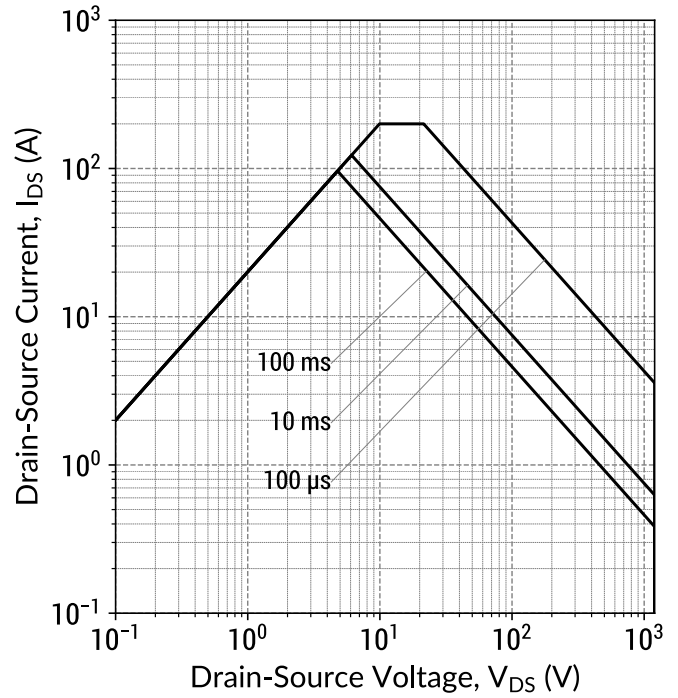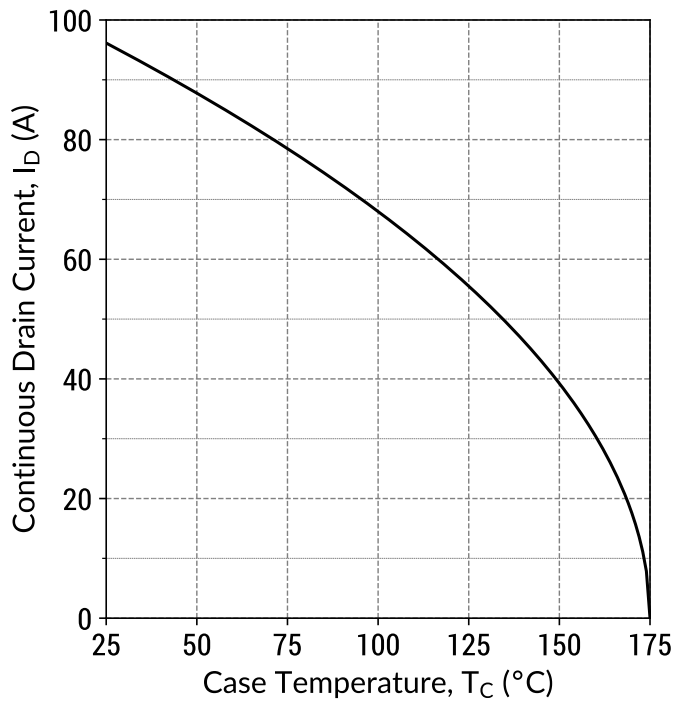
Figure 13: Transient Thermal Impedance

D = 0.5
D = 0.2
D = 0.1
D = 0.05
D = 0.02
D = Single Pulse

$Z_{th,jc}$ = f(t_P,D); D = t_P/T

Figure 14: Safe Operating Area (T_c = 25°C)

100 ms
10 ms
100 μs

I_D = f(V_{DS}, t_P); T_j ≤ 175°C; D = 0

Figure 15: Current De-rating Curve

I_D = f(T_C); T_j ≤ 175°C

Figure 16: Power De-rating Curve
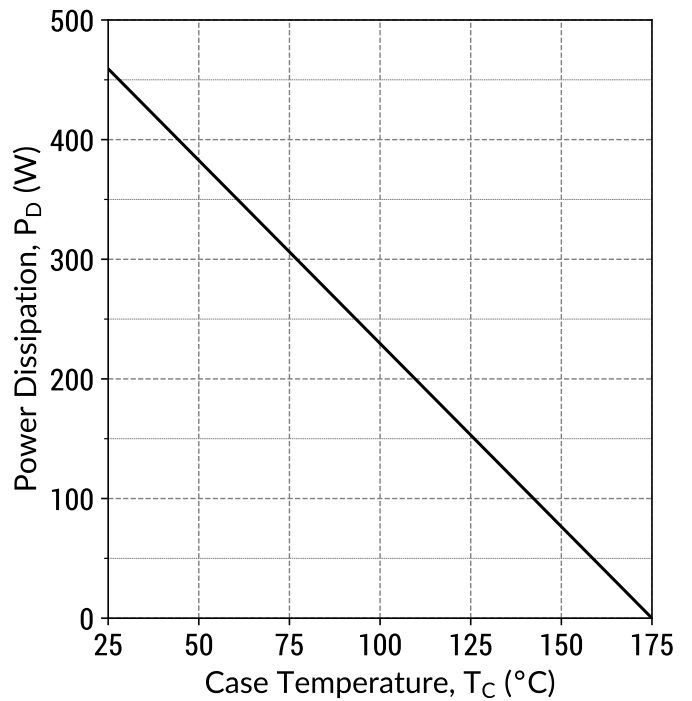
P_D = f(T_C); T_j ≤ 175°C

Figure 17: Body Diode Characteristics (T_j = 25°C)
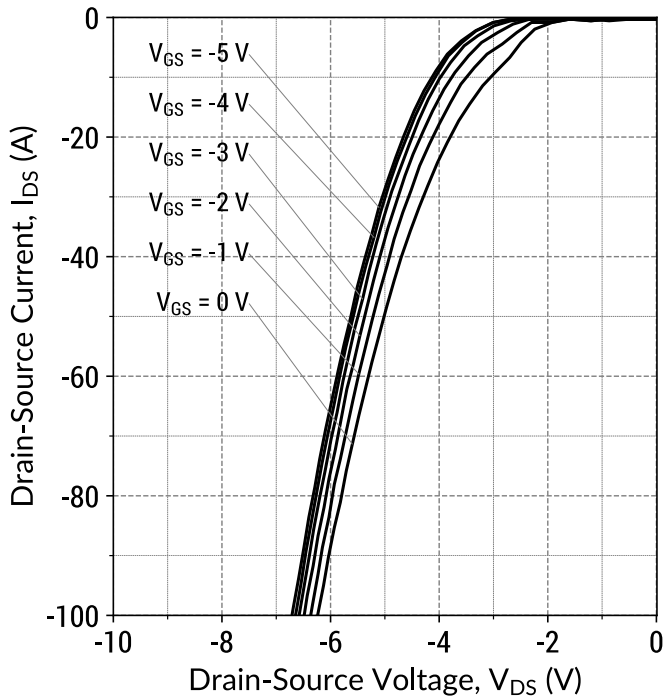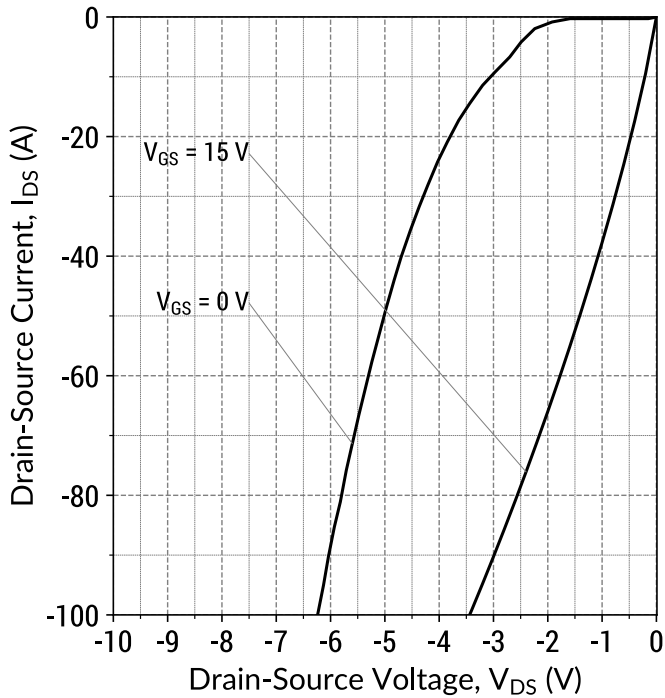

$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 18: Body Diode Characteristics (T_j = 175°C)
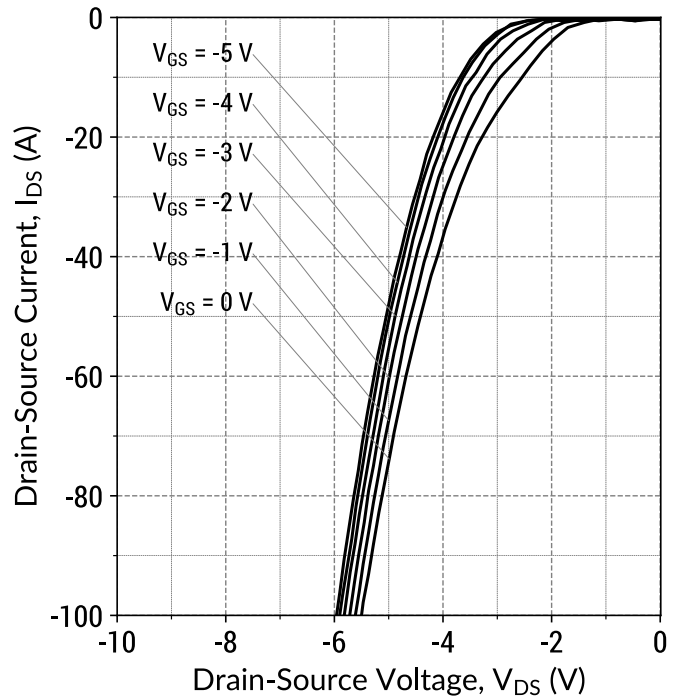
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 19: Third Quadrant Characteristics (T_j = 25°C)

$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

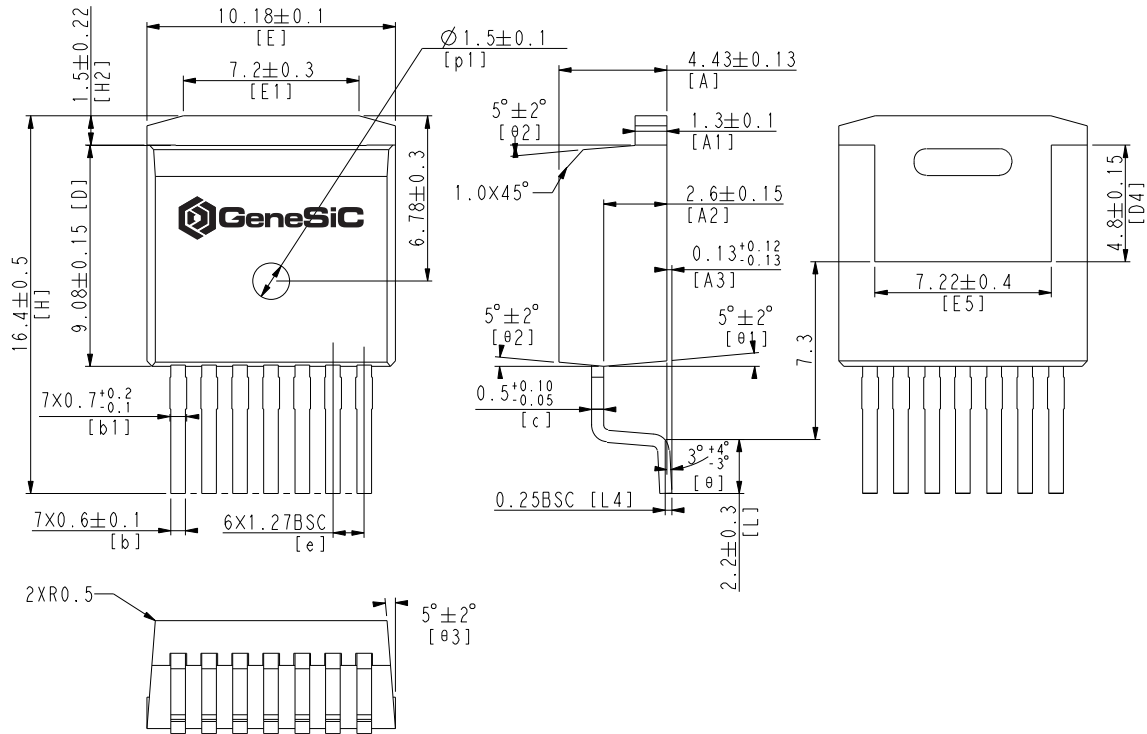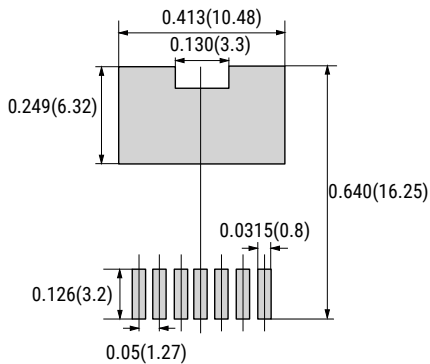## Figure 20: Third Quadrant Characteristics (T_j = 175°C)
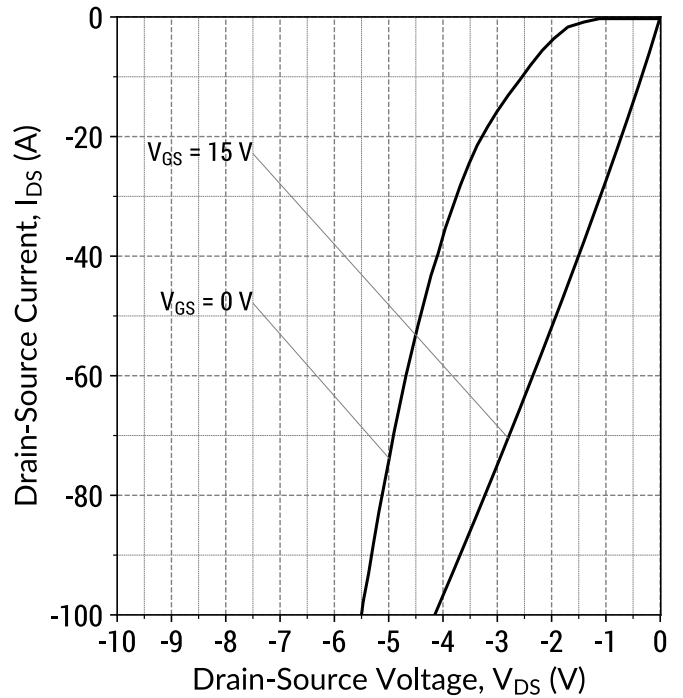
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Package Dimensions

TO-263-7 Package Outline

Recommended Solder Pad Layout

Package View

Case (D)

G KS S
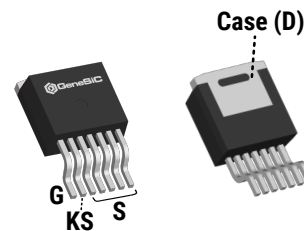
NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

Disclaimer

GeneSiC Semiconductor, Inc. reserves right to make changes to the product specifications and data in this document without notice. GeneSiC disclaims all and any warranty and liability arising out of use or application of any product. No license, express or implied to any intellectual property rights is granted by this document.

Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.

Related Links

- SPICE Models: https://www.genesicsemi.com/sic-mosfet/G3R30MT12J/G3R30MT12J_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-mosfet/G3R30MT12J/G3R30MT12J_PLECS.zip
- CAD Models: https://www.genesicsemi.com/sic-mosfet/G3R30MT12J/G3R30MT12J_3D.zip
- Gate Driver Reference: https://www.genesicsemi.com/technical-support
- Evaluation Boards: https://www.genesicsemi.com/technical-support
- Reliability: https://www.genesicsemi.com/reliability
- Compliance: https://www.genesicsemi.com/compliance
- Quality Manual: https://www.genesicsemi.com/quality

Revision History

Date	Revision	Comments	Supersedes
Aug. 25, 2020	Rev 2	Recommended Gate Voltage Changed from +20 V/-5 V to +15 V/-5 V	Rev 1
Jun. 2, 2020	Rev 1	Initial Release	

www.genesicsemi.com/sic-mosfet/

Aug. 20 Rev 2
Copyright© 2020 GeneSiC Semiconductor Inc.
All Rights Reserved.

Published by GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155, Dulles, VA 20166; USA
Page 9 of 9