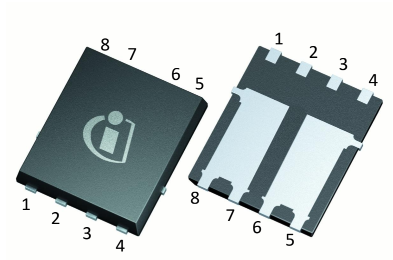
MOSFET

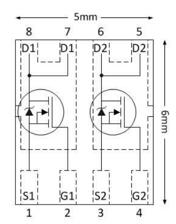
MOSFET - StrongIRFET™

Benefits

- Optimized for broadest availability from distribution partners
- 175°C junction temperature rated
- 100% UIL tested
- Product validation according to JEDEC standard
- Pb-Free ; RoHS Compliant ; Halogen-Free

SSO8 dual (TDSON-8-4)





Potential applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),typ}$	5.1	mΩ
$R_{DS(on),max}$	6.2	mΩ
I_D	65	A

Type / Ordering Code	Package	Marking	Related Links
IRF40H233	PG-TDSON-8-4	H233	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	65 46 35	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_C=25 °C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	260	A	T_C=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	71	mJ	I_D=35 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	50 3.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=40 °C/W[4]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom[5]	R_{thJC}	-	-	3	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	45	°C/W	-
Device on PCB, 6 cm² cooling area[4]	R_{thJA}	-	-	40	°C/W	-
Device on PCB, RTHJA(<10s)	R_{thJA}	-	-	25	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information
[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[5] RthJC is measured at TJ approximately 90°C.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=250 uA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	41	-	mV/°C	I_D=1 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.9	V	V_{DS}=V_{GS}, I_D=50 µA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 150	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	5.1	6.2	mΩ	V_{GS}=10 V, I_D=35 A
Gate resistance[1)]	R_G	-	1.8	-	Ω	-
Transconductance	g_{fs}	-	60	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=35 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	2200	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	380	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	260	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	V_{DD}=26 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=2.7 Ω
Rise time	t_r	-	67	-	ns	V_{DD}=26 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=2.7 Ω
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	V_{DD}=26 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=2.7 Ω
Fall time	t_f	-	30	-	ns	V_{DD}=26 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=2.7 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	12	-	nC	V_{DD}=20 V, I_D=35 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	6.7	-	nC	V_{DD}=20 V, I_D=35 A, V_{GS}=0 to 10 V
Gate to drain charge[1)]	Q_{gd}	-	15.7	-	nC	V_{DD}=20 V, I_D=35 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	20.6	-	nC	V_{DD}=20 V, I_D=35 A, V_{GS}=0 to 10 V
Gate charge total[1)]	Q_g	-	45	57	nC	V_{DD}=20 V, I_D=35 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	V_{DD}=20 V, I_D=35 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	38	-	-	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[2)]	Q_{oss}	-	13	-	-	V_{DS}=20 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See "Gate charge waveforms" for parameter definition

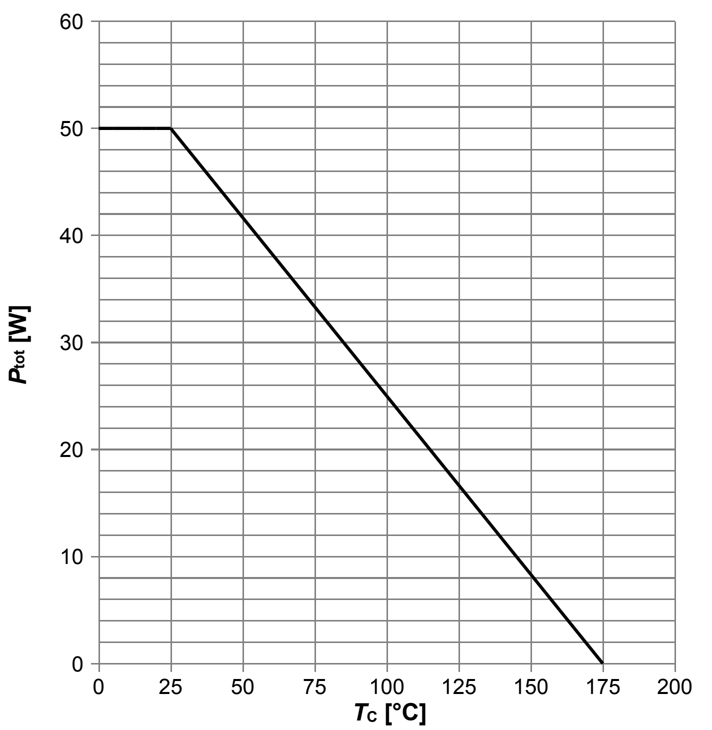
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	39	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	260	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.94	1.3	V	V_{GS}=0 V, I_F=35 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	22	-	ns	V_R=34 V, I_F=35 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	16	-	nC	V_R=34 V, I_F=35 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

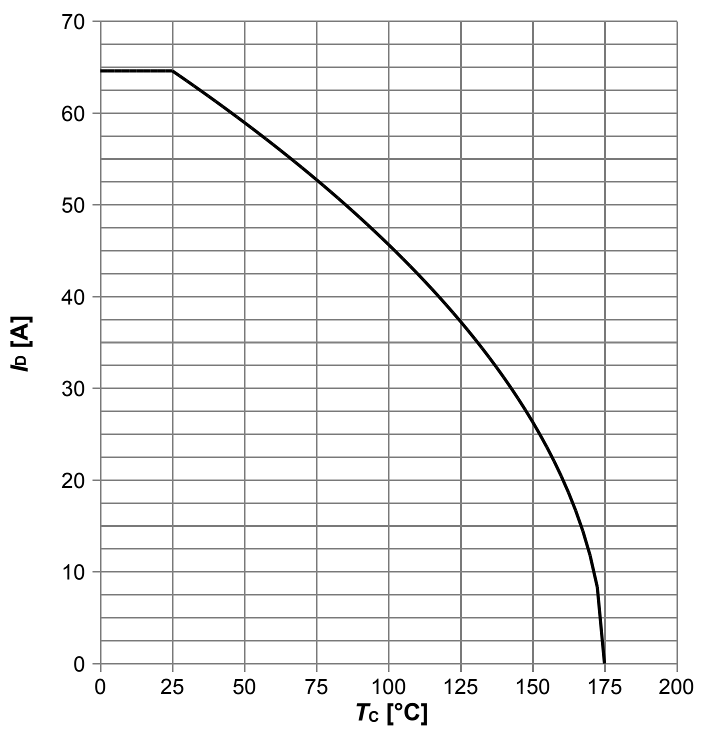
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



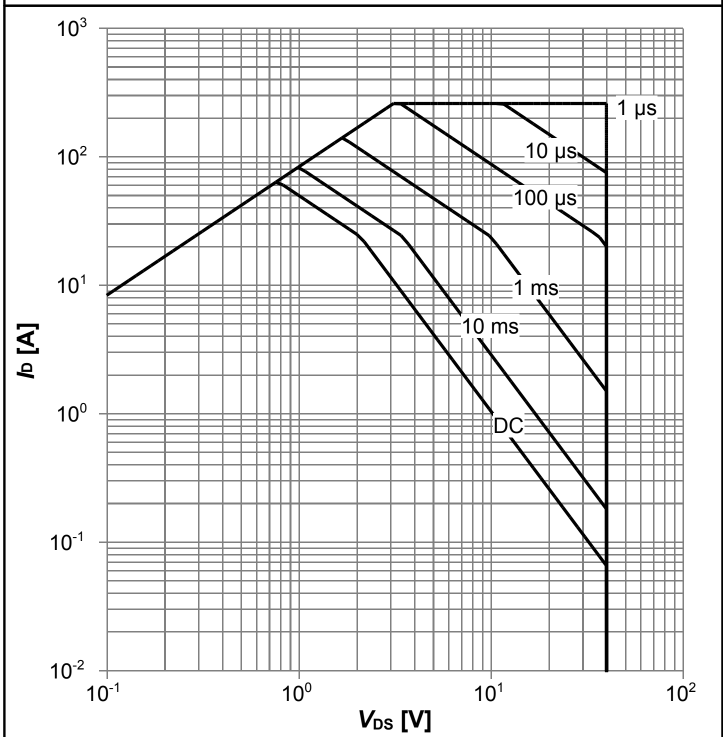
P_{tot}=f(T_C)

Diagram 2: Drain current



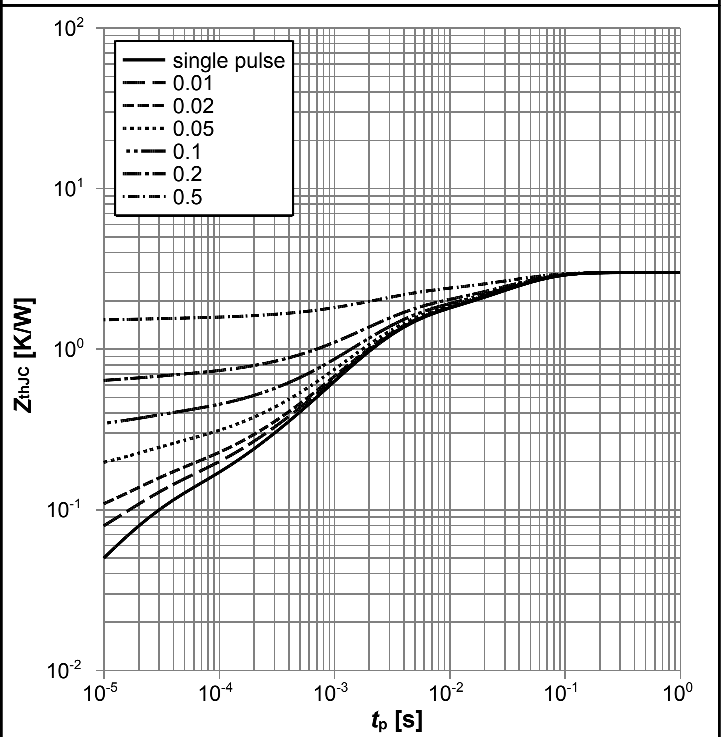
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



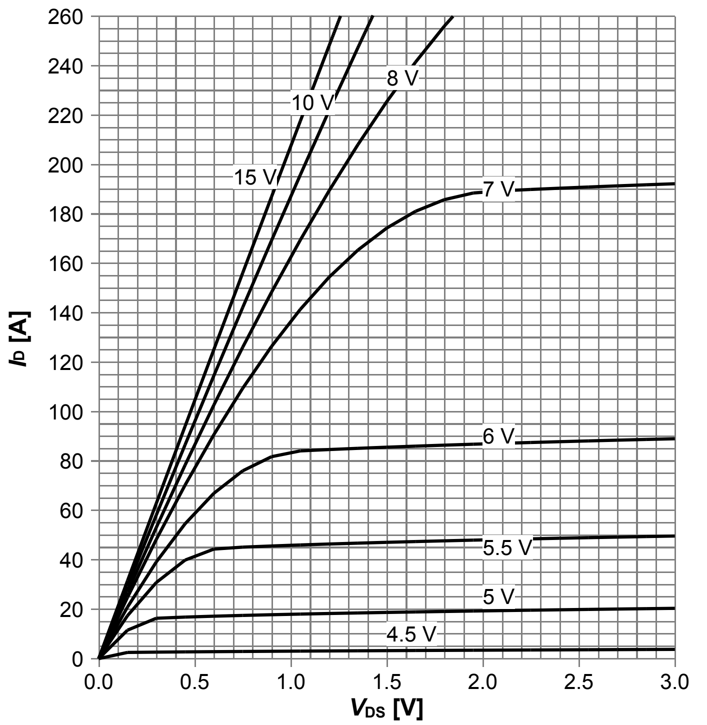
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



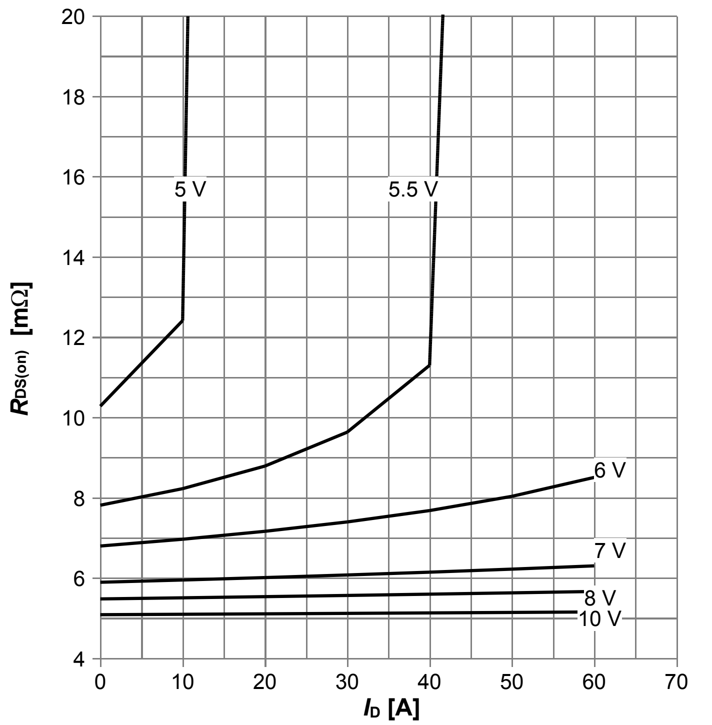
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



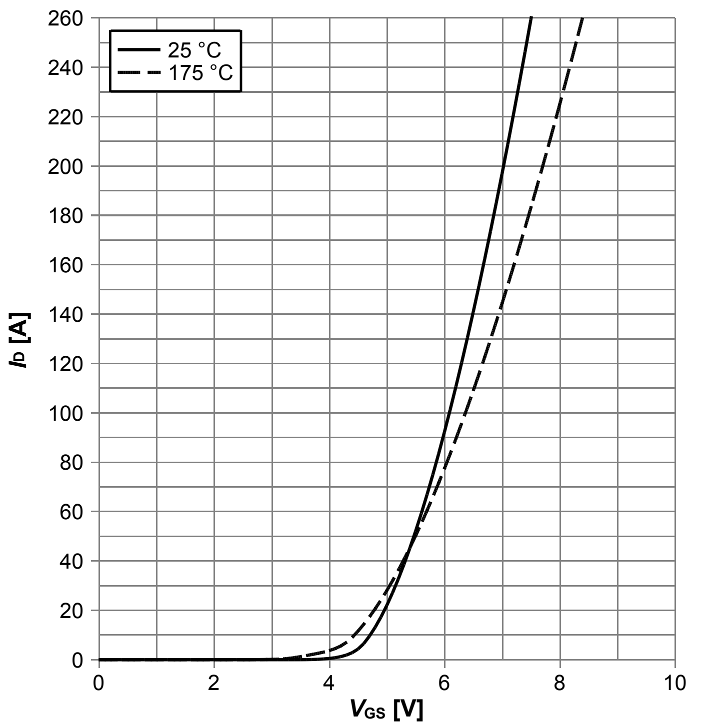
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



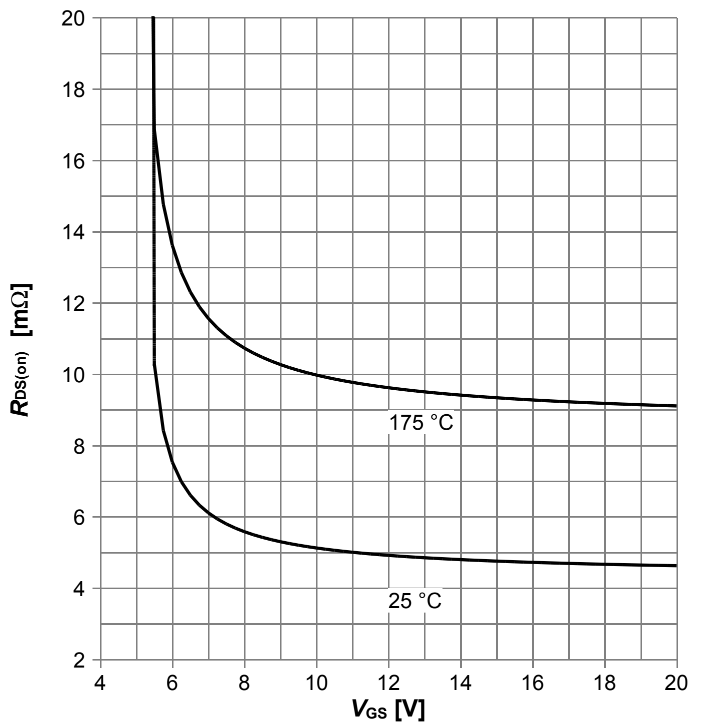
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



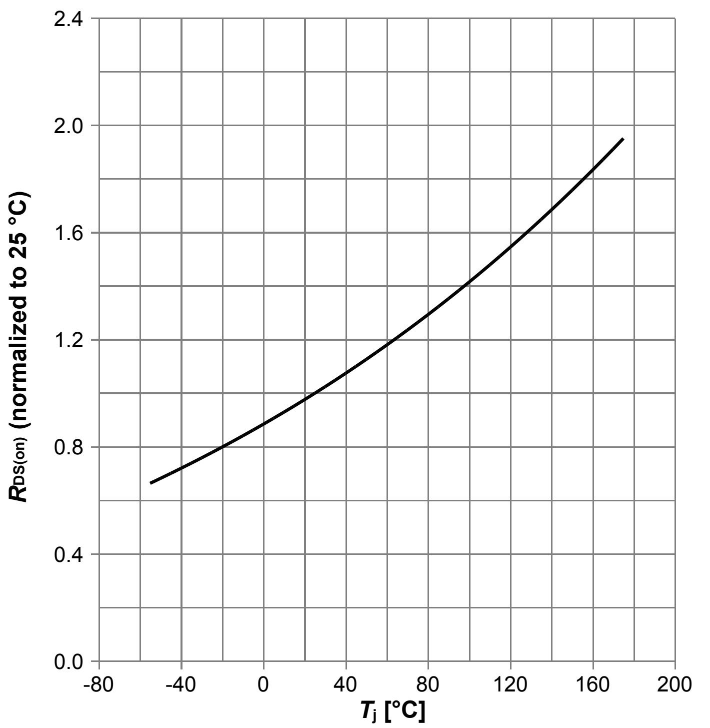
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



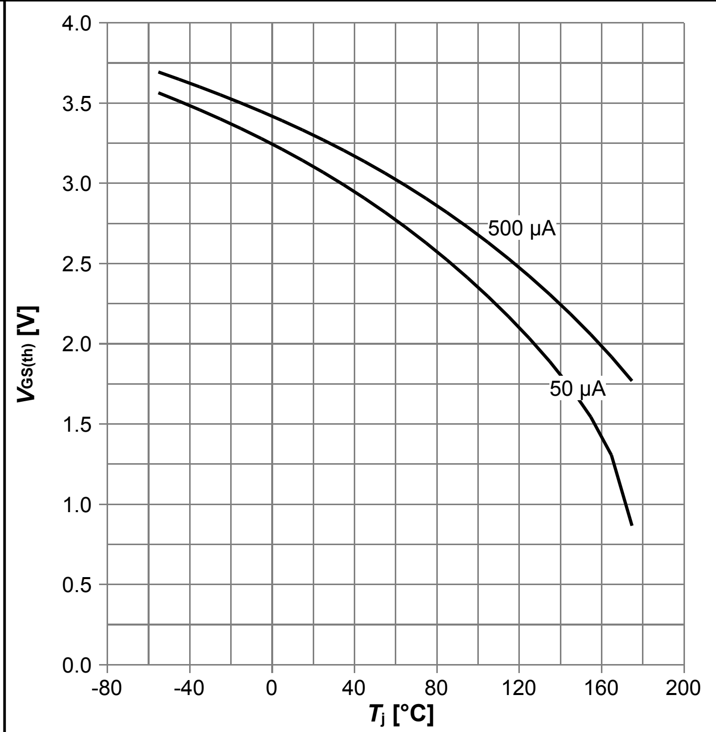
$R_{DS(on)}$=f(V_{GS}), I_D=35 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



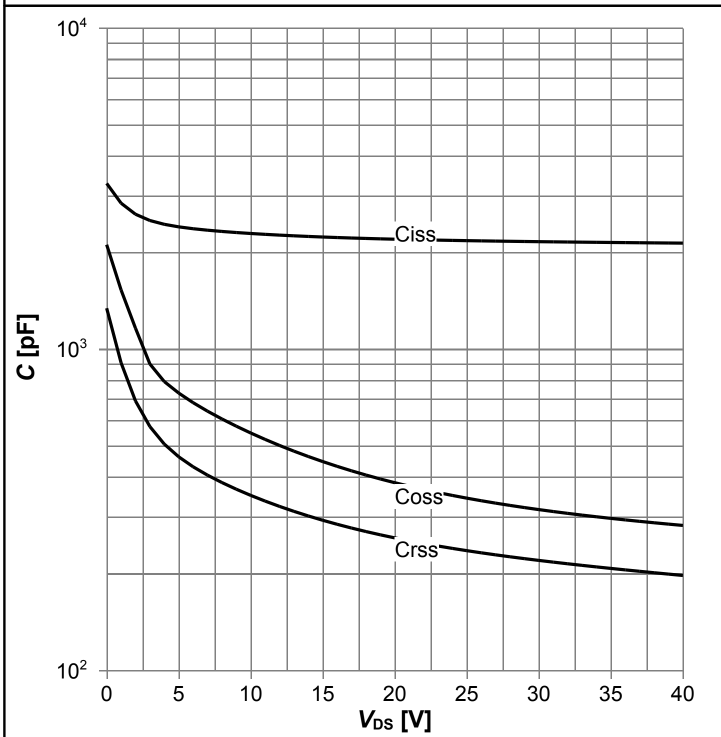
$R_{DS(on)}$=f(T_j), I_D=35 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



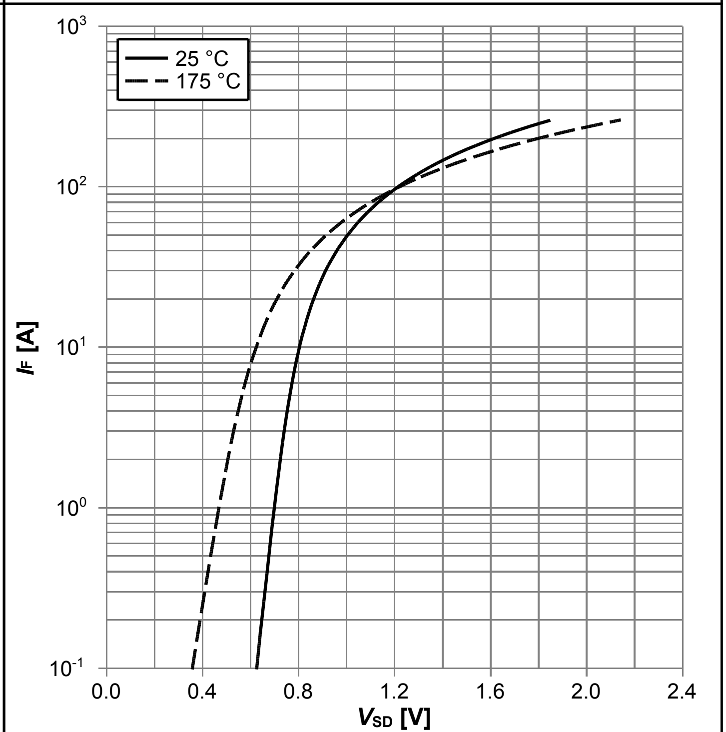
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



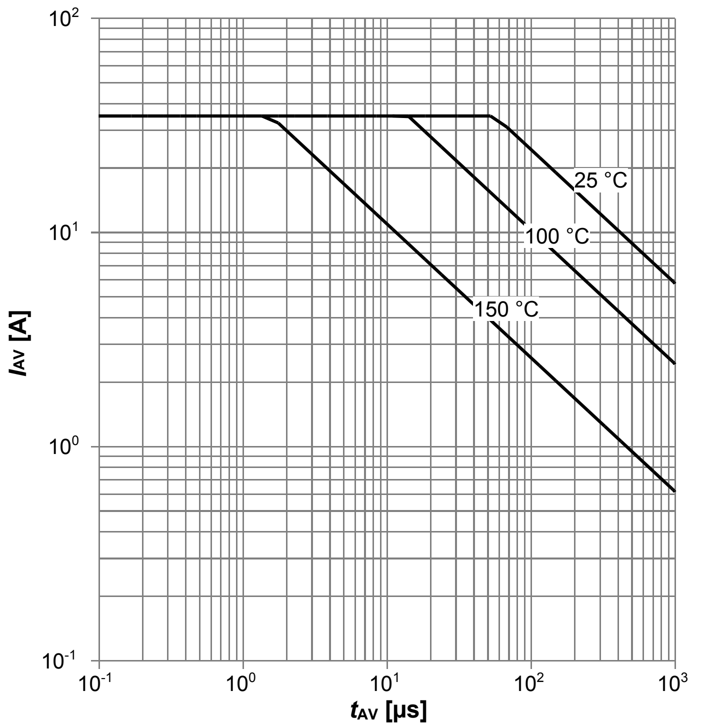
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



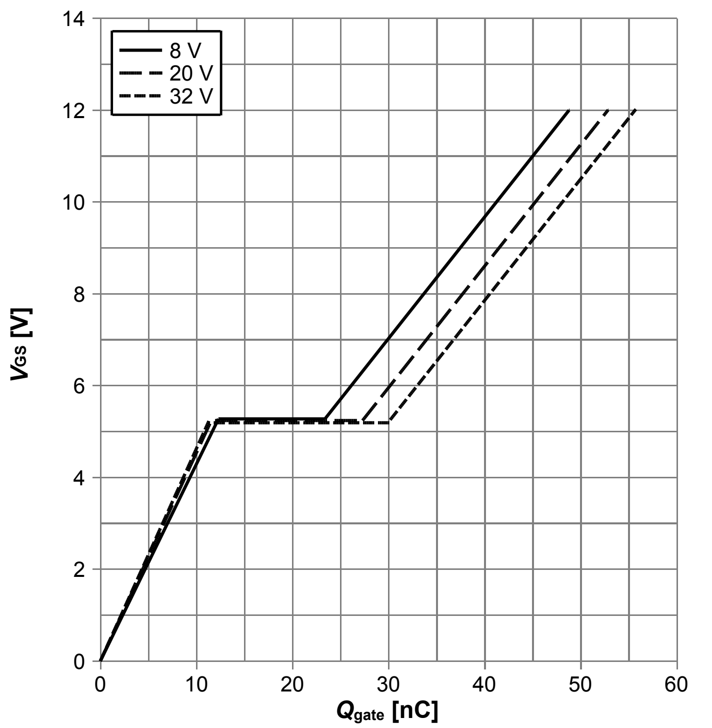
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



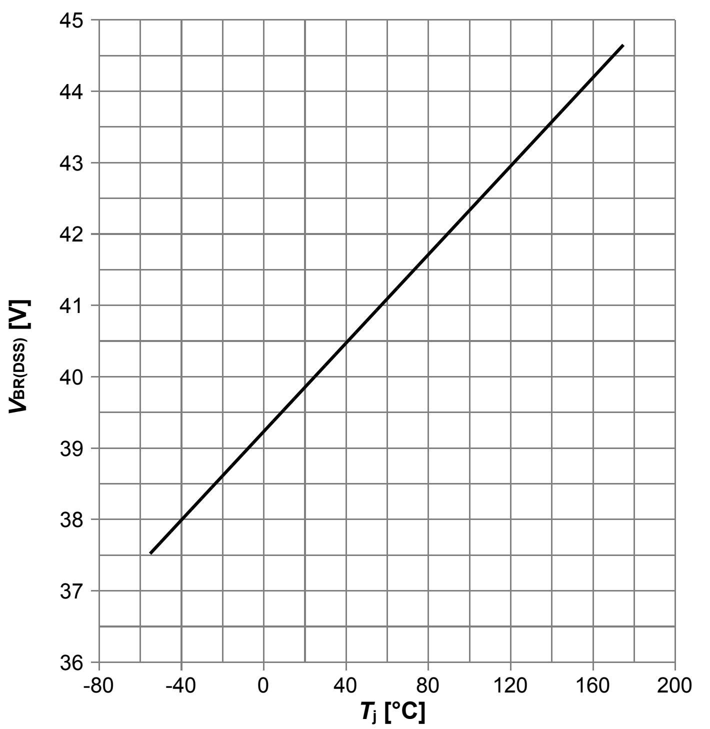
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



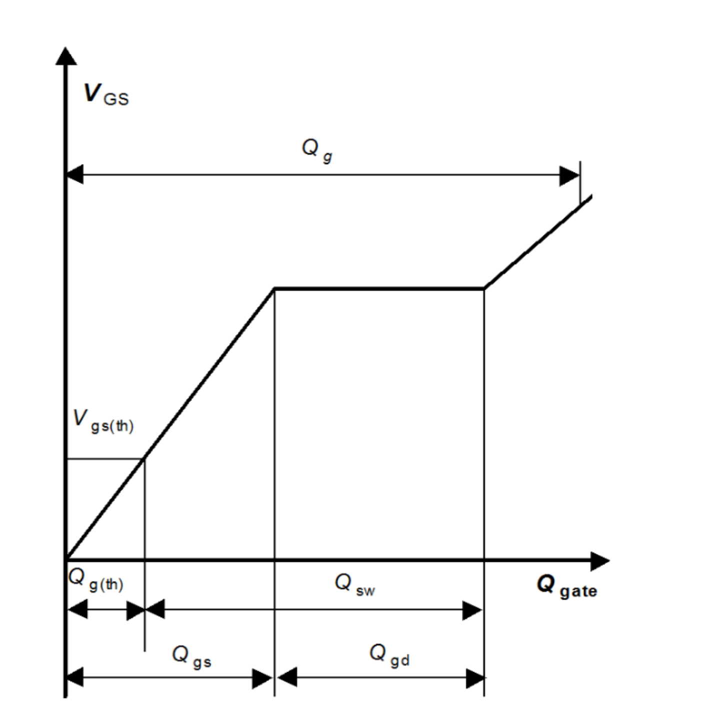
V_{GS}=f(Q_{gate}), I_D=35 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

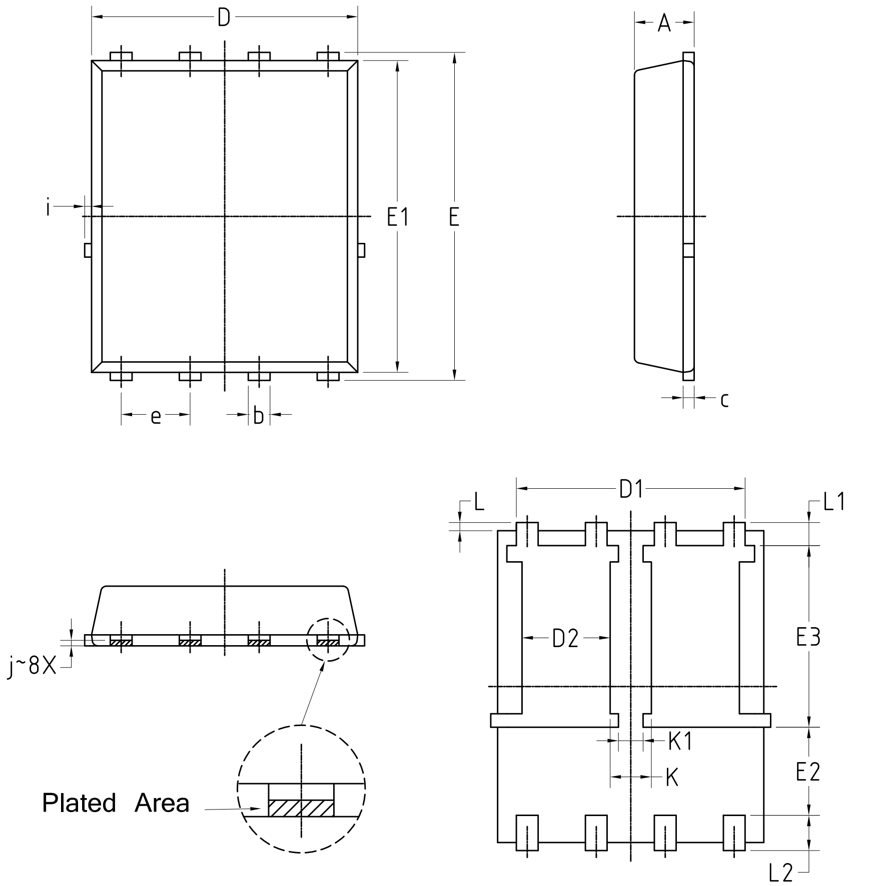


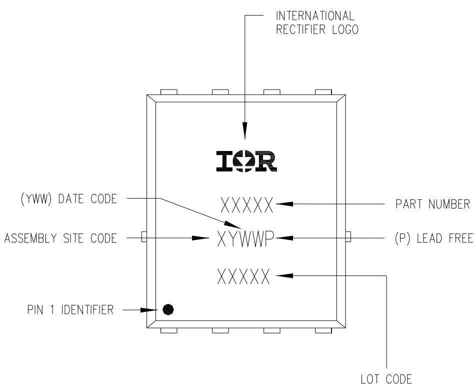
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines

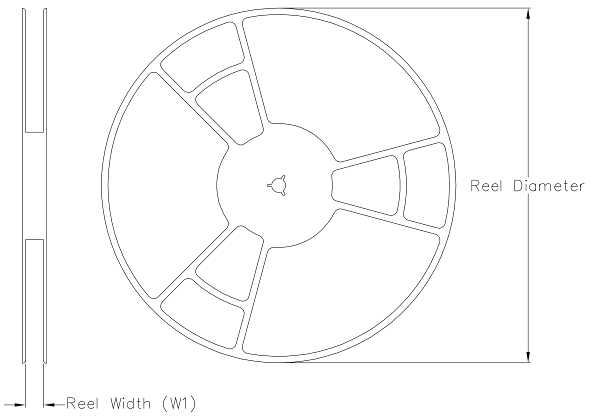




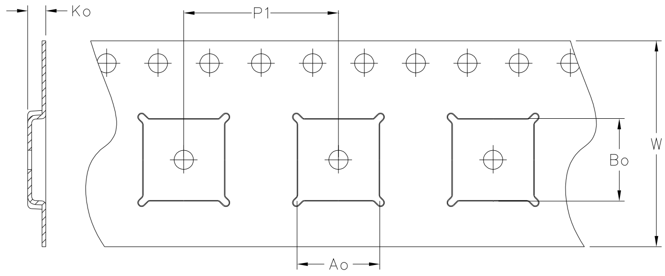
SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.00	1.20	0.039	0.047
b	0.30	0.50	0.012	0.020
c	0.203 BSC		0.008 BSC	
D	4.80	5.00	0.189	0.197
D1	4.06	4.36	0.160	0.172
D2	1.47	1.77	0.058	0.070
E	5.90	6.20	0.232	0.244
E1	5.65	5.85	0.222	0.230
E2	1.45	—	0.057	—
E3	3.20	3.50	0.126	0.138
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.002	0.010
L1	0.325	0.525	0.013	0.021
L2	0.500	0.800	0.020	0.031
i	—	0.20	—	0.008
K	0.61	0.91	0.024	0.036
K1	0.31	0.60	0.012	0.024
j	0.1015 BSC		0.004BSC	

Figure 1 Outline PG-TDSON-8-4, dimensions in mm/inches

REEL DIMENSIONS

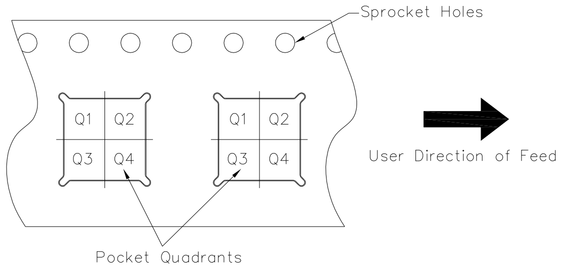


TAPE DIMENSIONS



	DESCRIPTION
	Dimension design to accommodate the component width
	Dimension design to accommodate the component lenght
	Dimension design to accommodate the component thickness
	Overall width of the carrier tape
	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Figure 2 Outline PG-TDSON-8-4, dimensions in mm/inches

Revision History

IRF40H233

Revision: 2020-06-29, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2018-07-05	Release of preliminary version
2.0	2018-07-12	Release of final version
2.1	2018-07-16	Update Potential Application
2.2	2020-01-20	Update from IR MOSFT/StrongIRFET™ to StrongIRFET™
2.3	2020-06-29	Updated Datasheet based on new current rating and application note:App-AN_1912_PL51_2001_180356

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