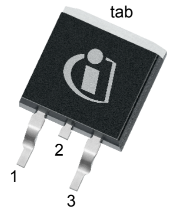
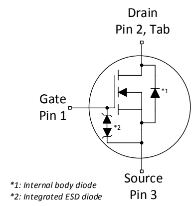
MOSFET

650V CoolMOS™ CFD7 SJ Power Device

The latest 650 V CoolMOS™ CFD7 extends the voltage class offering of the CFD7 family and is a successor to the 650 V CoolMOS™ CFD2. Resulting from improved switching performance and excellent thermal behavior, 650 V CooMOS™ CFD7 offers highest efficiency in resonant switching topologies, such as LLC and phase-shift-full-bridge (ZVS). As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions.

D²PAK





Features

- Ultra-fast body diode
- 650V break down voltage
- Best-in-class $R_{DS(on)}$
- Reduced switching losses
- Low $R_{DS(on)}$ dependency over temperature

Benefits

- Excellent hard commutation ruggedness
- Extra safety margin for designs with increased bus voltage
- Enabling increased power density solutions
- Outstanding light load efficiency in industrial SMPS applications
- Improved full load efficiency in industrial SMPS applications
- Price competitiveness over previous CoolMOS™ families

Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging, Solar

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	125	mΩ
$Q_{g,typ}$	36	nC
$I_{D,pulse}$	72	A
E_{oss} @ 400V	5.1	µJ
Body diode di_F/dt	1300	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPB65R125CFD7	PG-TO263-3	65R125F7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	19 12	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	72	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	85	mJ	I_D=4.1A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.42	mJ	I_D=4.1A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	4.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	98	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current[1]	I_S	-	-	19	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	72	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	70	V/ns	V_{DS}=0...400V, I_{SD}<=8.5A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt	-	-	1300	A/µs	V_{DS}=0...400V, I_{SD}<=8.5A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.27	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	V_{DS}=V_{GS}, I_D=0.42mA
Zero gate voltage drain current[1]	I_{DSS}	- -	- 7	1 37	µA	V_{DS}=650V, V_{GS}=0V, T_j=25°C V_{DS}=650V, V_{GS}=0V, T_j=125°C
Gate-source leakage current	I_{GSS}	-	-	1000	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.1 0.222	0.125 -	Ω	V_{GS}=10V, I_D=8.5A, T_j=25°C V_{GS}=10V, I_D=8.5A, T_j=150°C
Gate resistance	R_G	-	8.5	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1694	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	28	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[2]	$C_{o(er)}$	-	64	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[3]	$C_{o(tr)}$	-	661	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8.5A, R_G=10.2Ω; see table 9
Rise time	t_r	-	14	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8.5A, R_G=10.2Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	112	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8.5A, R_G=10.2Ω; see table 9
Fall time	t_f	-	5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8.5A, R_G=10.2Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10	-	nC	V_{DD}=400V, I_D=8.5A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	11	-	nC	V_{DD}=400V, I_D=8.5A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	36	-	nC	V_{DD}=400V, I_D=8.5A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=400V, I_D=8.5A, V_{GS}=0 to 10V

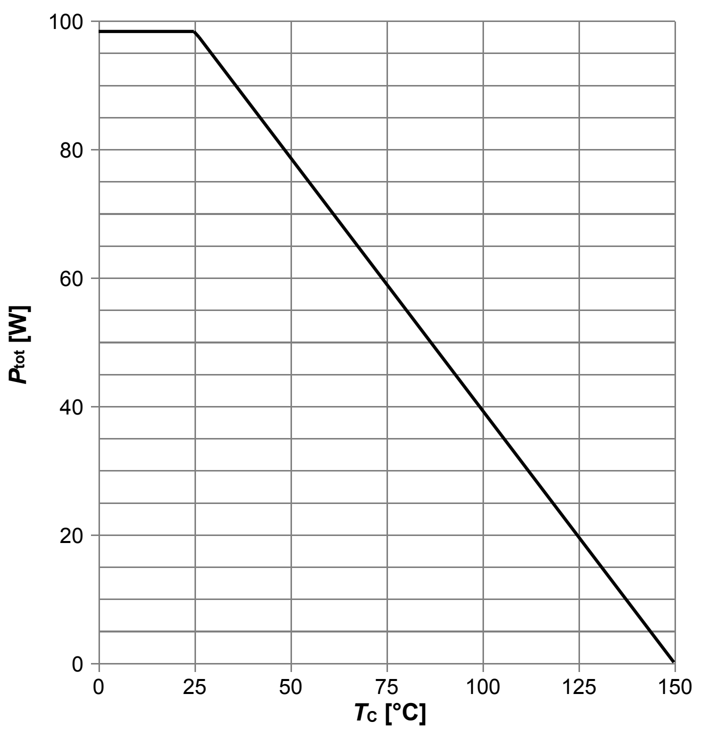
[1] Maximum specification is defined by calculated six sigma upper confidence bound
[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	V_{GS}=0V, I_F=8.5A, T_j=25°C
Reverse recovery time	t_{rr}	-	104	156	ns	V_R=400V, I_F=8.5A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	0.52	1.04	µC	V_R=400V, I_F=8.5A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	8.6	-	A	V_R=400V, I_F=8.5A, di_F/dt=100A/µs; see table 8

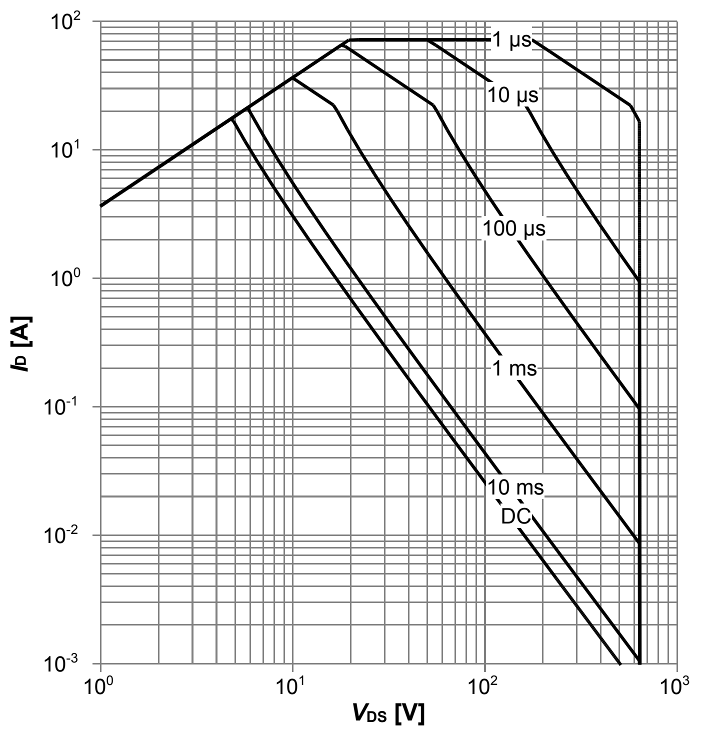
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



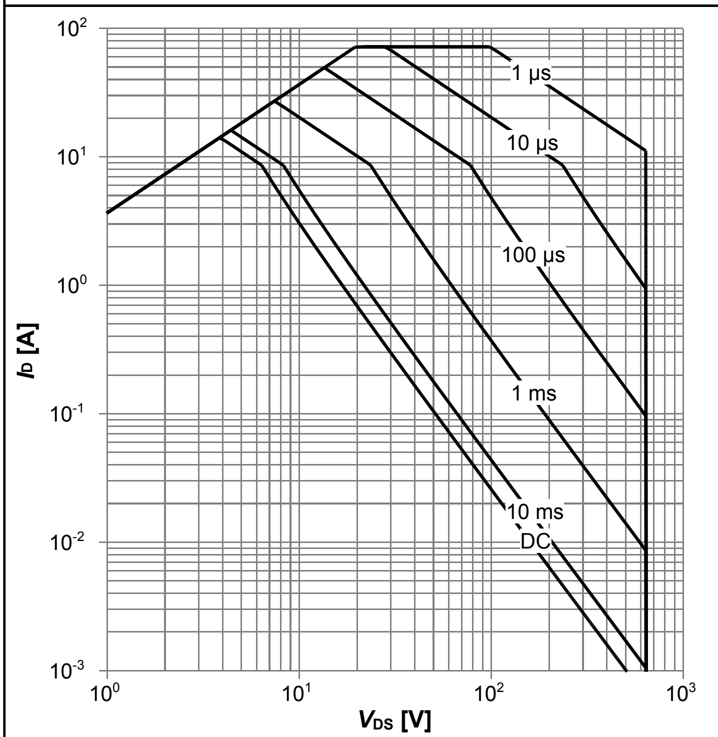
P_{tot}=f(T_C)

Diagram 2: Safe operating area



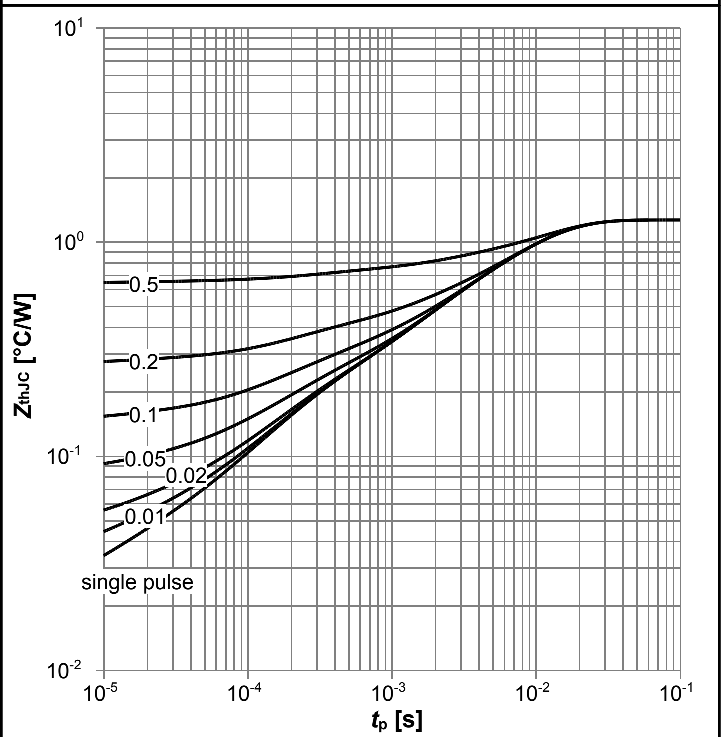
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



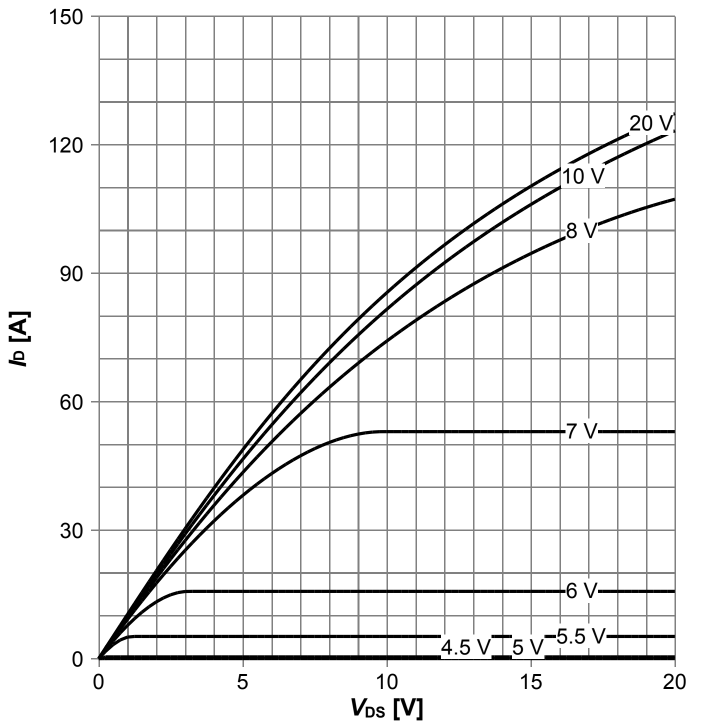
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



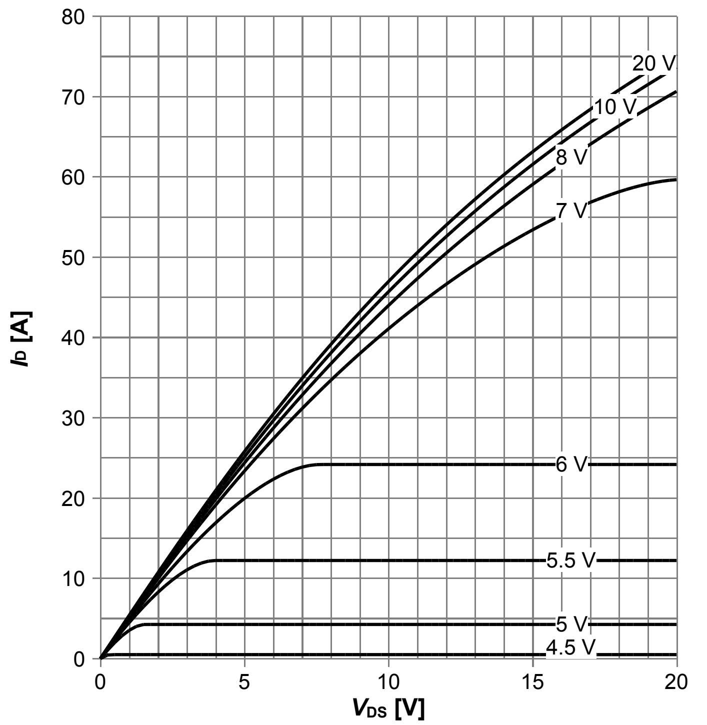
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



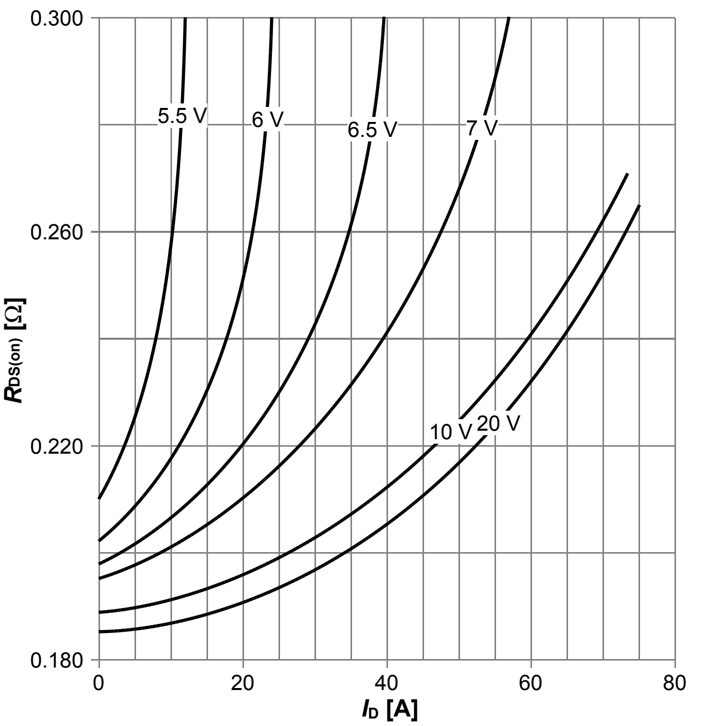
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



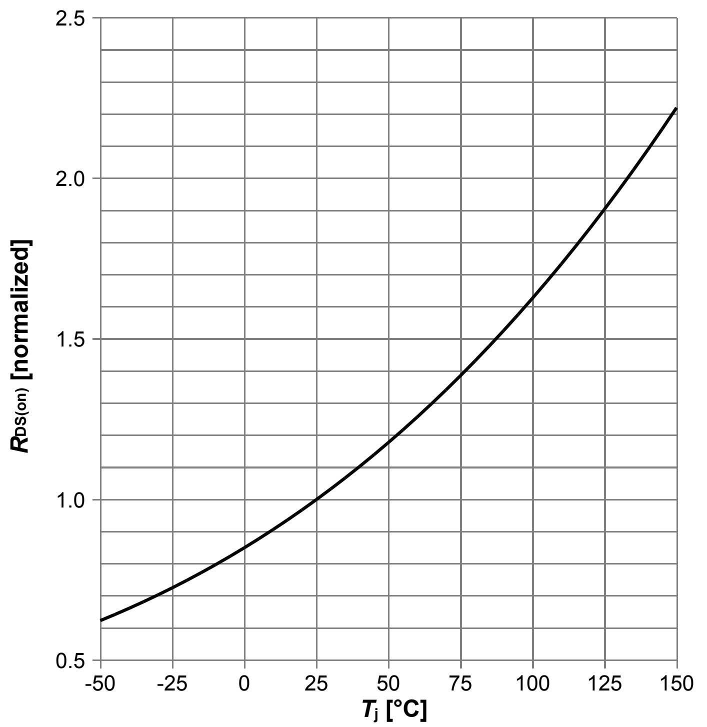
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



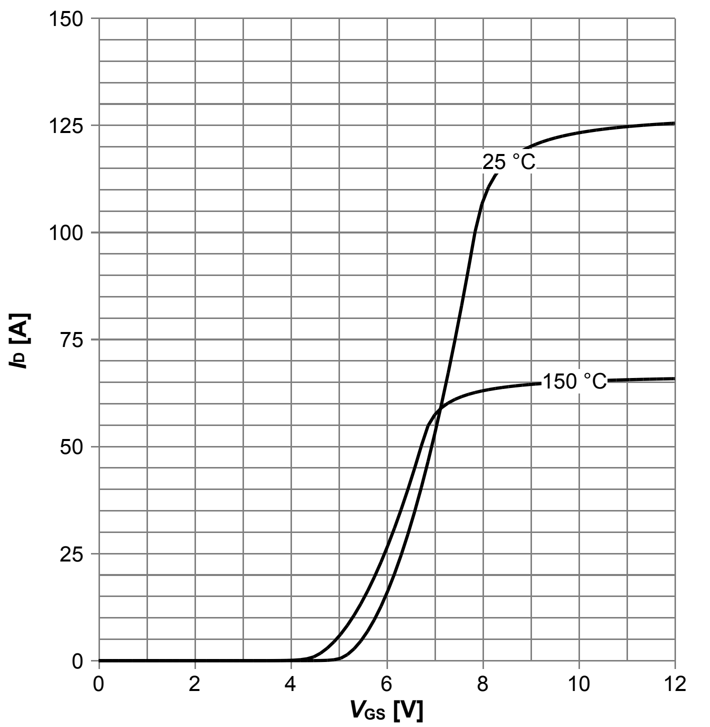
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



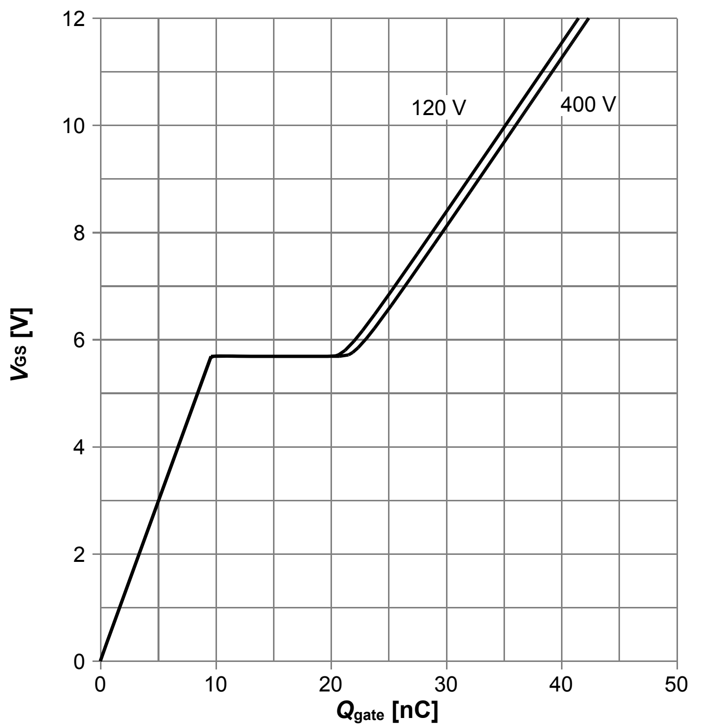
$R_{DS(on)}$=f(T_j); I_D=8.5 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



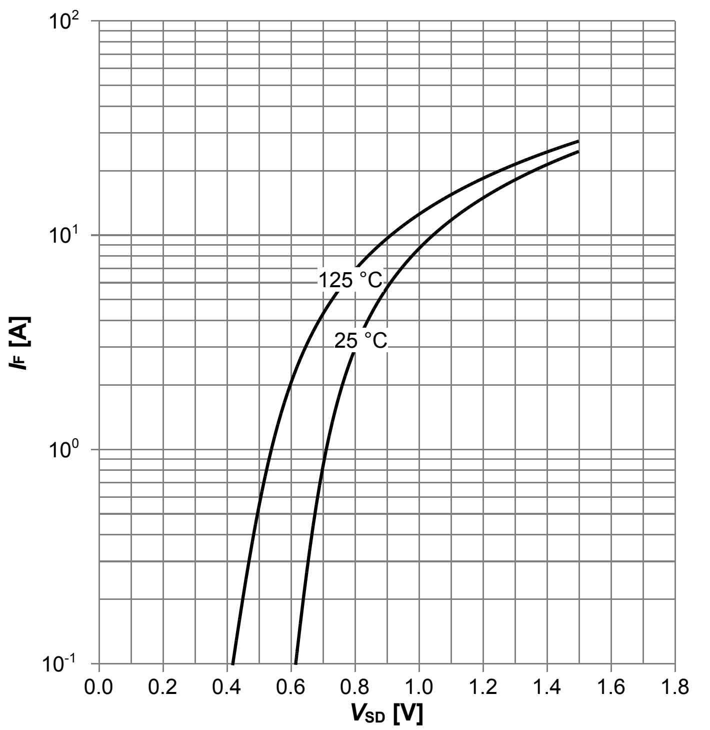
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



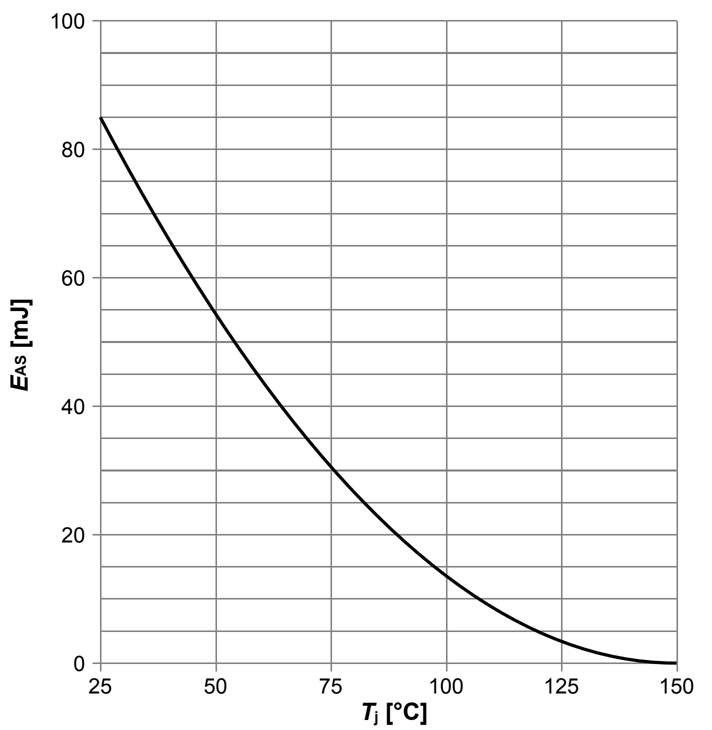
V_{GS}=f(Q_{gate}); I_D=8.5 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



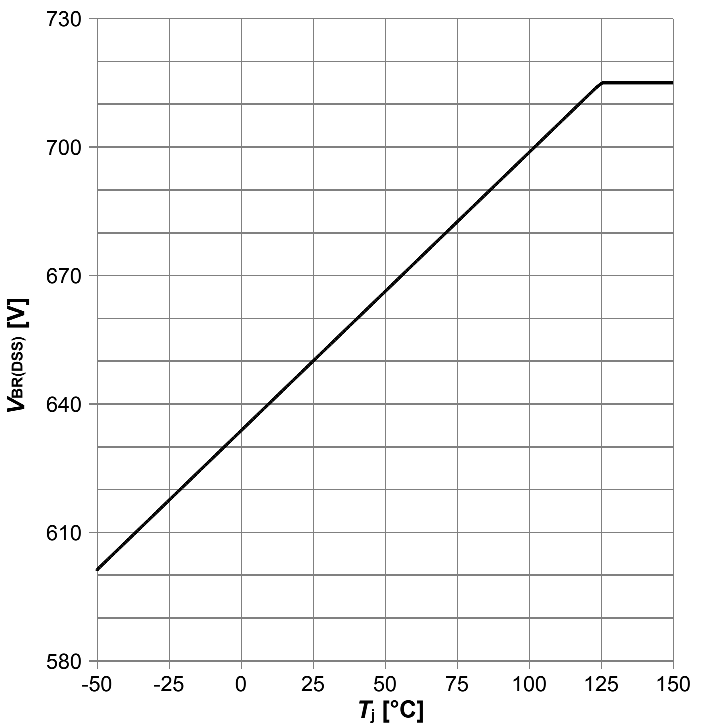
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



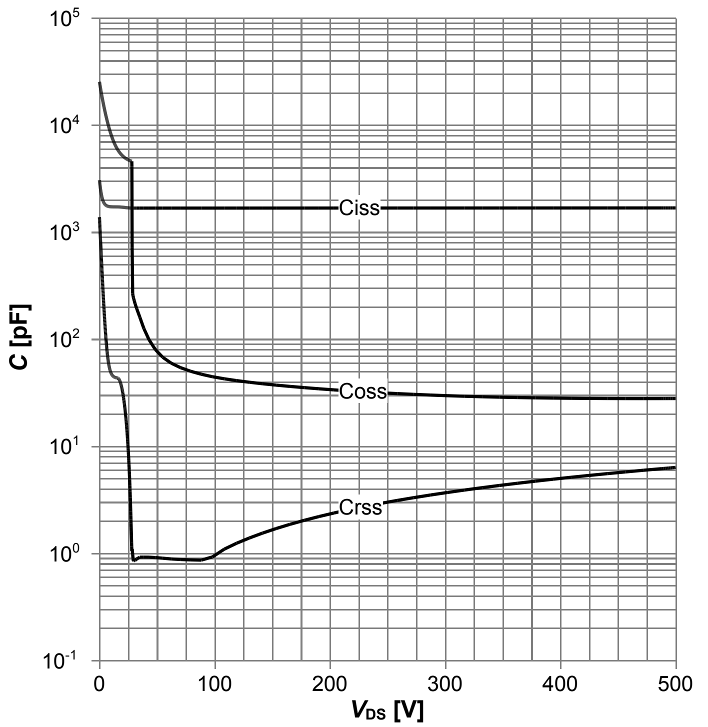
E_{AS}=f(T_j); I_D=4.1 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



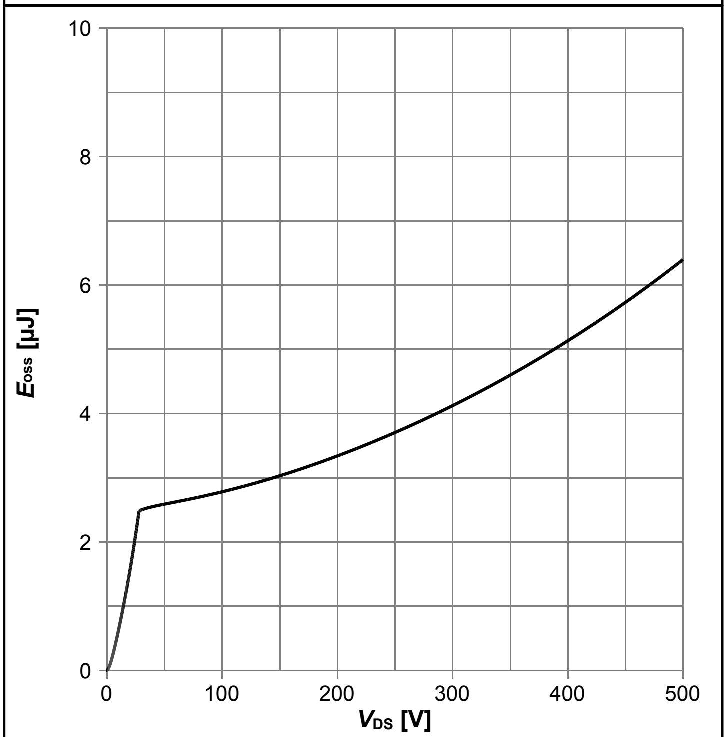
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

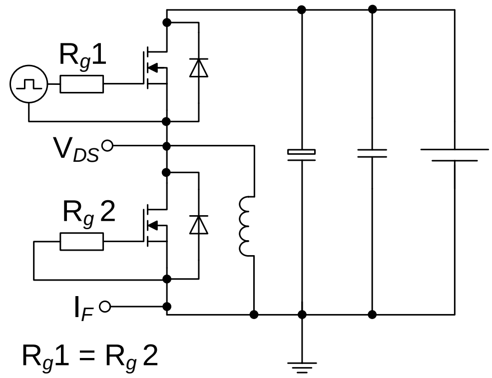
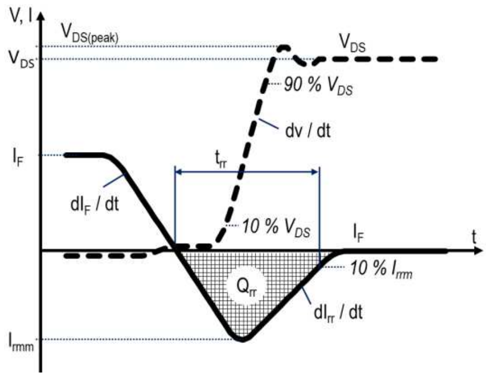
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

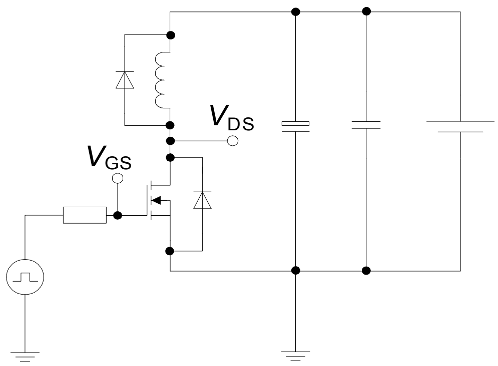
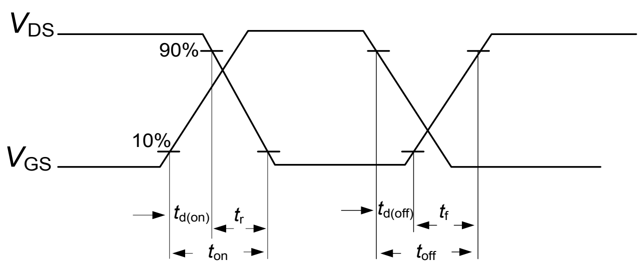
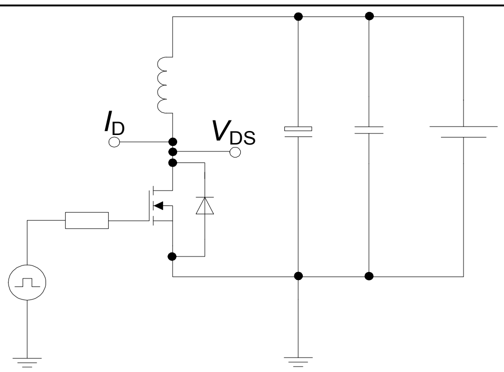
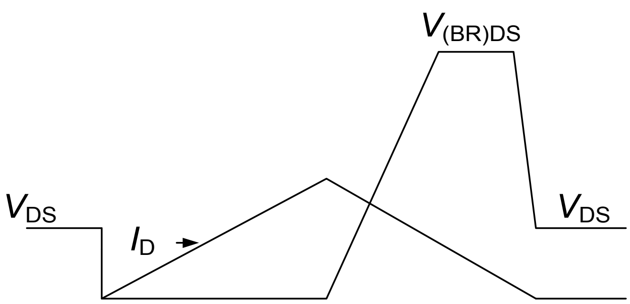
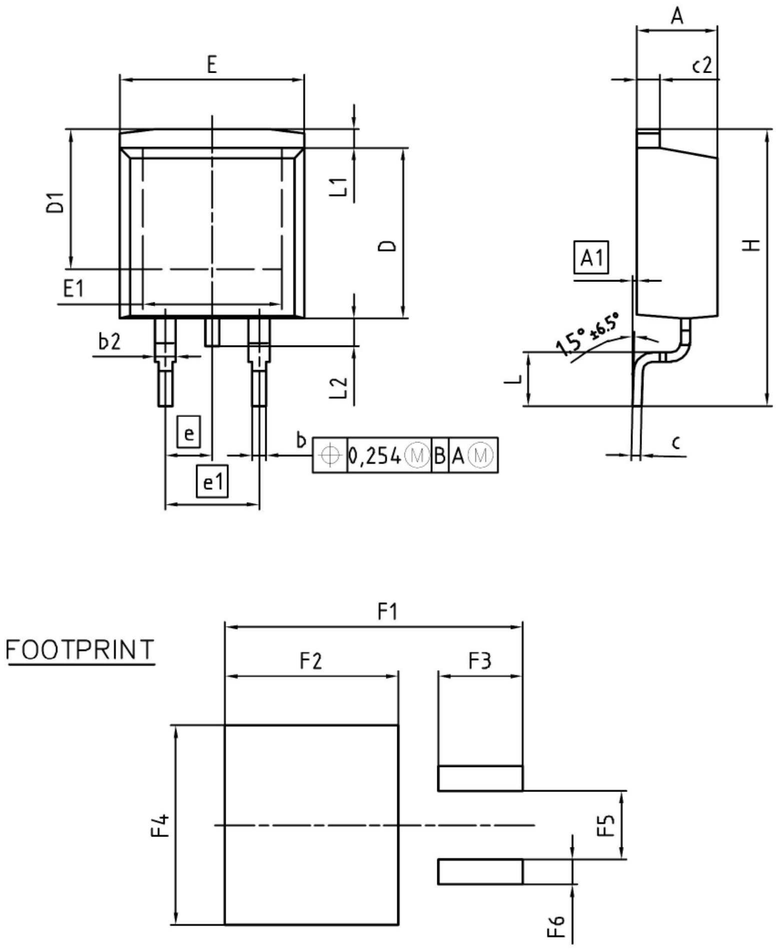
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

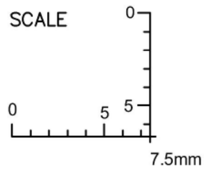
6 Package Outlines



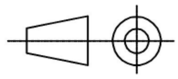
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

DOCUMENT NO.
Z8B00003324

SCALE



EUROPEAN PROJECTION



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30-08-2007

REVISION
01

Figure 1 Outline PG-TO263-3, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS CFD7 650V Webpage:** www.infineon.com
- **IFX CoolMOS CFD7 650V application note:** www.infineon.com
- **IFX CoolMOS CFD7 650V simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPB65R125CFD7

Revision: 2020-10-19, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2020-10-19	Release of final version

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