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82C55A Address to Read/Write Set Up Time

Introduction

This Tech Brief applies only to the 51864 mask 82C55A CMOS Programmable Peripheral Interface Circuit.

The Read/Write Logic implementation of the 51864 mask (L7 version) of the 82C55A, while functionally equivalent to previous mask versions, is slightly different. The "Address Stable Before READ", tAR, and "Address Stable Before WRITE", tAW, timing requirements remain specified at 0ns minimum, but on the newer 51864 mask version, a falling edge on the READ or WRITE signal disables further changes on the Address Lines (A0 and A1) during the READ or WRITE operation. This prevents the user from holding the READ or WRITE line asserted low and changing the Address Lines (A0 and A1) to access different ports or registers on the 82C55A. This "disabling of address line change" during READ or WRITE, would not occur on previous mask versions of the 82C55A.

IMPACT - The "disabling of address line change" on the falling edge of READ or WRITE should not affect any application since the READ or WRITE signal generated by the driving device (μP) will always be unasserted prior to changing the address and then be reasserted (READ or WRITE) after the new address has been established. However, some incoming tests may catch this difference and indicate a failure.

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