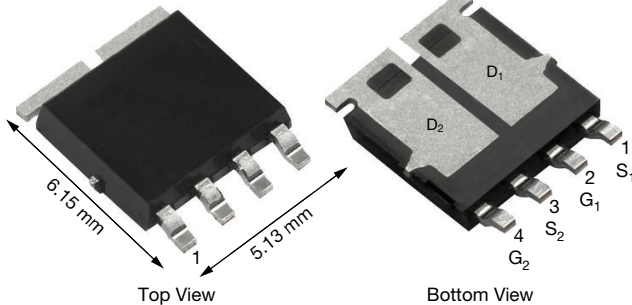


Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET

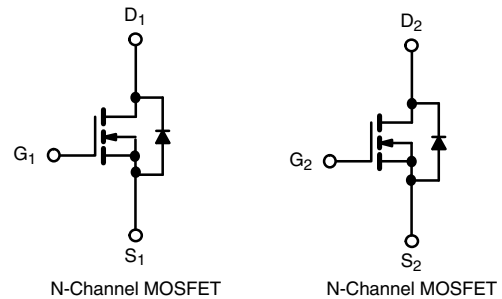
PowerPAK® SO-8L Dual

FEATURES

- TrenchFET® Gen IV Power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE


RoHS
 COMPLIANT
 HALOGEN
FREE

| PRODUCT SUMMARY | |
|---|-------|
| V _{DS} (V) | 40 |
| R _{DS(on)} (Ω) at V _{GS} = 10 V | 0.008 |
| I _D (A) | 30 |
| Configuration | Dual |



| ORDERING INFORMATION | |
|---------------------------------|-----------------|
| Package | PowerPAK SO-8L |
| Lead (Pb)-free and halogen-free | SQJB46EP-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|-------------------------------------|-----------------------------------|-------------|------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-source voltage | | V _{DS} | 40 | V |
| Gate-source voltage | | V _{GS} | ± 20 | |
| Continuous drain current | T _C = 25 °C ^a | I _D | 30 | A |
| | T _C = 125 °C | | 28.5 | |
| Continuous source current (diode conduction) ^a | | I _S | 30 | |
| Pulsed drain current ^b | | I _{DM} | 120 | |
| Single pulse avalanche current | L = 0.1 mH | I _{AS} | 21 | |
| Single pulse avalanche energy | | E _{AS} | 22 | mJ |
| Maximum power dissipation | T _C = 25 °C | P _D | 34 | W |
| | T _C = 125 °C | | 11 | |
| Operating junction and storage temperature range | | T _J , T _{stg} | -55 to +175 | °C |
| Soldering recommendations (peak temperature) ^d | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------|------------------------|-------------------|-------|------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Junction-to-ambient | PCB mount ^c | R _{thJA} | 85 | °C/W |
| Junction-to-case (drain) | | R _{thJC} | 4.3 | |

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leaded package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



| SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------|---|--|------|--------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | | 40 | - | - | V |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | | 2.3 | 2.8 | 3.3 | |
| Gate-source leakage | I_{GSS} | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero gate voltage drain current | I_{DSS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}$ | - | - | 1 | μA |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$ | - | - | 50 | |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$ | - | - | 250 | |
| On-state drain current ^a | $I_{D(on)}$ | $V_{GS} = 10\text{ V}$ | $V_{DS} \geq 5\text{ V}$ | 25 | - | - | A |
| Drain-source on-state resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 8\text{ A}$ | - | 0.0061 | 0.0080 | Ω |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 8\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$ | - | - | 0.0117 | |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 8\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$ | - | - | 0.0136 | |
| Forward transconductance ^b | g_{fs} | $V_{DS} = 15\text{ V}$, $I_D = 8\text{ A}$ | | - | 34 | - | S |
| Dynamic ^b | | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$ | - | 1268 | 1800 | μF |
| Output capacitance | C_{oss} | | | - | 428 | 600 | |
| Reverse transfer capacitance | C_{rss} | | | - | 32 | 45 | |
| Total gate charge ^c | Q_g | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}$, $I_D = 3\text{ A}$ | - | 21 | 32 | nC |
| Gate-source charge ^c | Q_{gs} | | | - | 5.8 | - | |
| Gate-drain charge ^c | Q_{gd} | | | - | 4.5 | - | |
| Gate resistance | R_g | f = 1 MHz | | 1.26 | 2.54 | 3.8 | Ω |
| Turn-on delay time ^c | $t_{d(on)}$ | $V_{DD} = 20\text{ V}$, $R_L = 6.67\text{ }\Omega$ $I_D \cong 3\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ | | - | 12 | 20 | ns |
| Rise time ^c | t_r | | | - | 5 | 10 | |
| Turn-off delay time ^c | $t_{d(off)}$ | | | - | 19 | 30 | |
| Fall time ^c | t_f | | | - | 6 | 12 | |
| Source-Drain Diode Ratings and Characteristics ^b | | | | | | | |
| Pulsed current ^a | I_{SM} | | | - | - | 120 | A |
| Forward voltage | V_{SD} | $I_F = 8\text{ A}$, $V_{GS} = 0\text{ V}$ | | - | 0.8 | 1.2 | V |
| Body diode reverse recovery time | t_{rr} | $I_F = 6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | | - | 26 | 55 | ns |
| Body diode reverse recovery charge | Q_{rr} | | | - | 16 | 35 | nC |
| Reverse recovery fall time | t_a | | | - | 13 | - | ns |
| Reverse recovery rise time | t_b | | | - | 13 | - | |
| Body diode peak reverse recovery current | $I_{RM(REC)}$ | | | - | -1.024 | - | A |

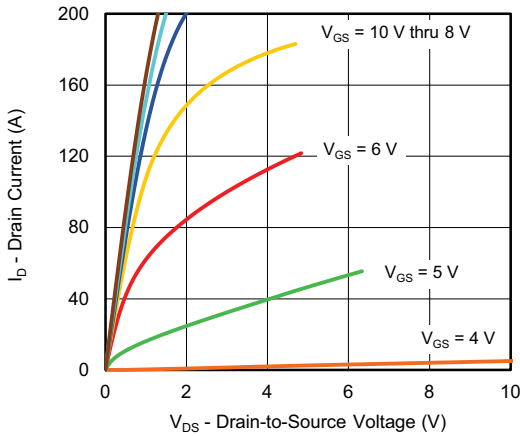
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

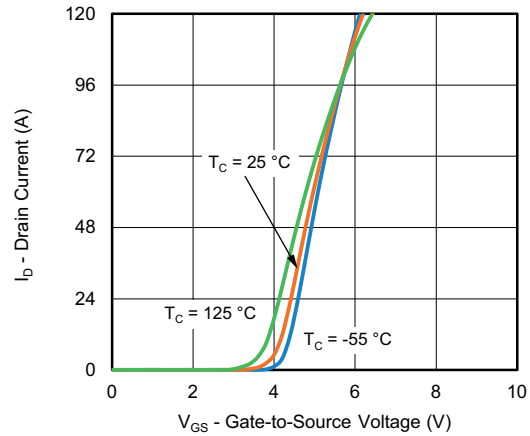
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



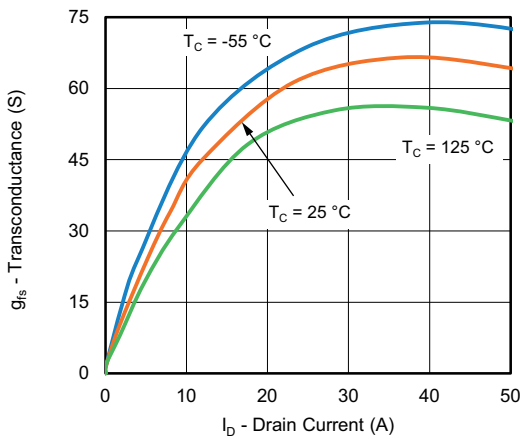
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



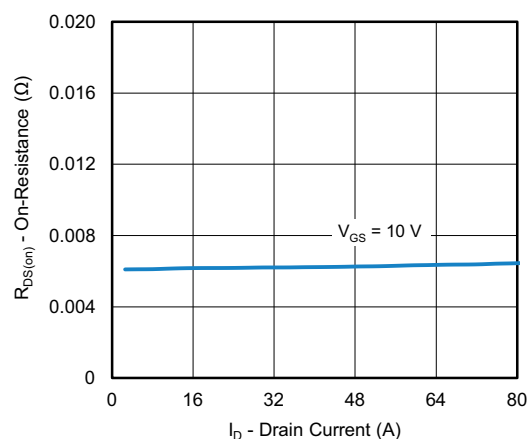
Output Characteristics



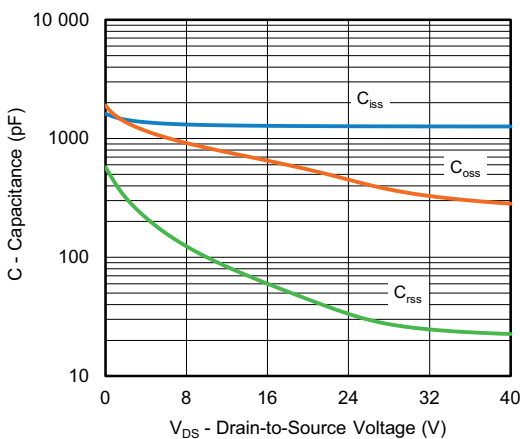
Transfer Characteristics



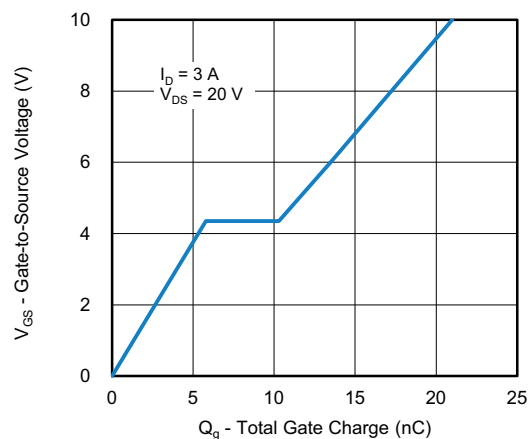
Transconductance



On-Resistance vs. Drain Current

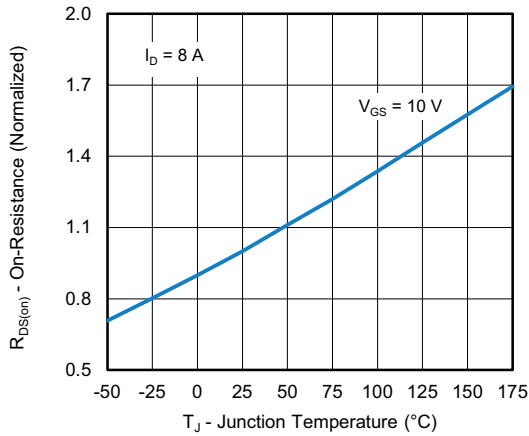


Capacitance

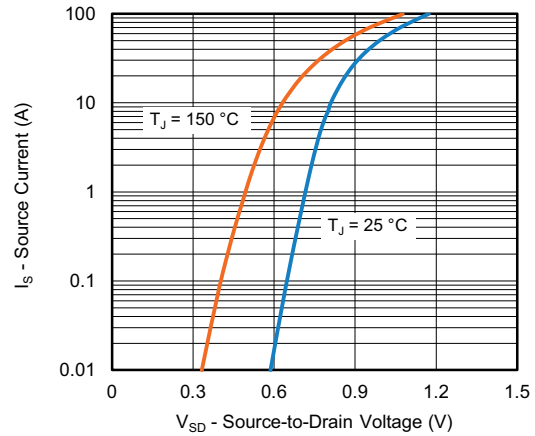


Gate Charge

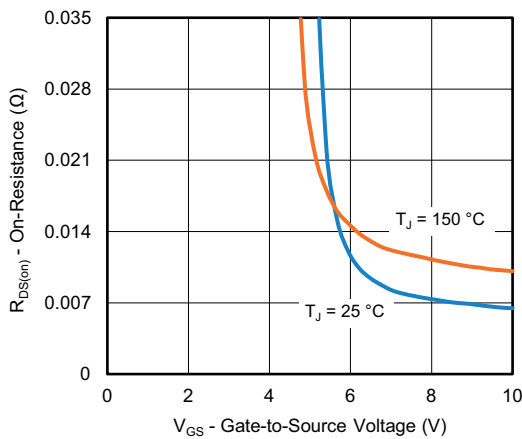
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



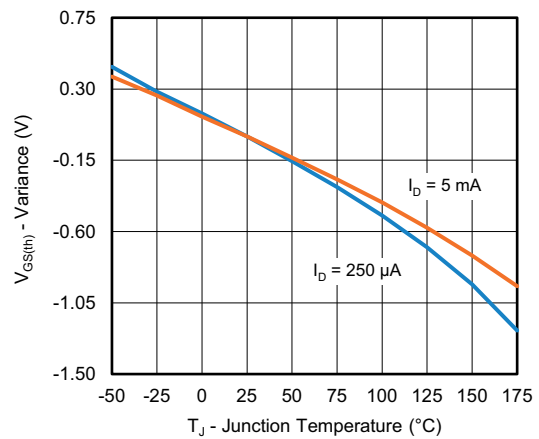
On-Resistance vs. Junction Temperature



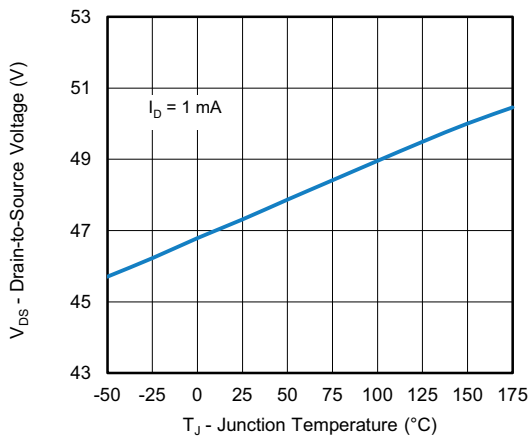
Source Drain Diode Forward Voltage



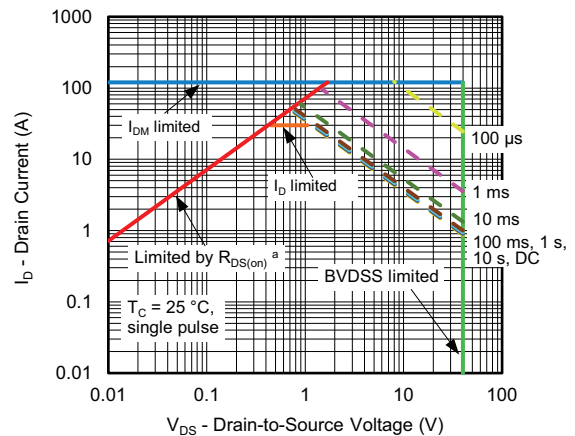
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



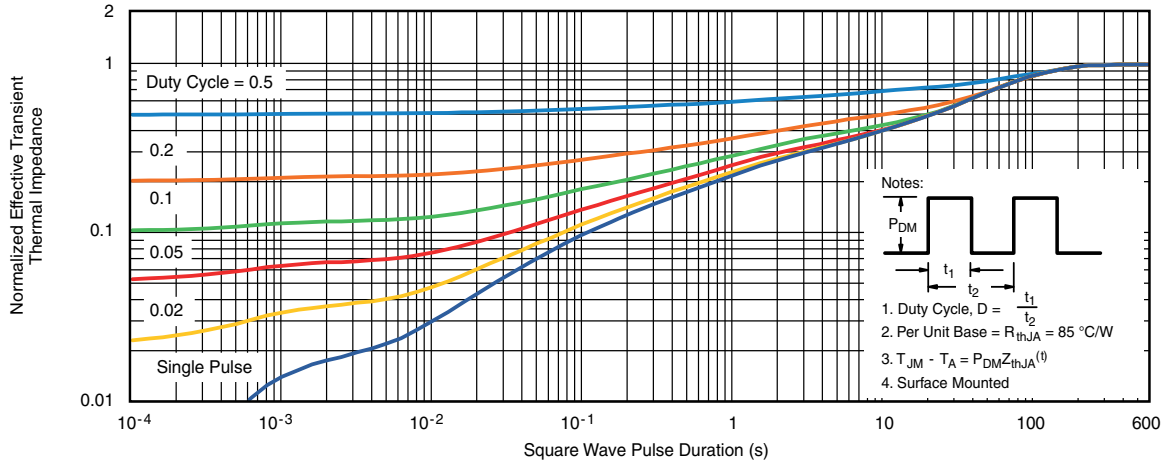
Safe Operating Area

Note

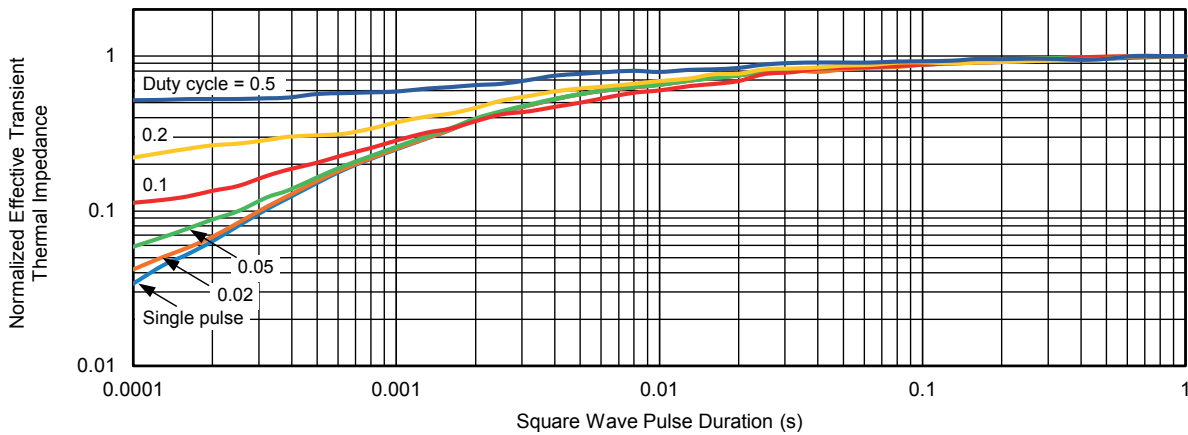
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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