# HI5731

12-Bit, 100MSPS, High Speed D/A Converter

FN4070
Rev 10.00
October 2, 2015

The HI5731 is a 12-bit, 100MSPS, D/A converter which is implemented in the Intersil BiCMOS 10V (HBC-10) process. Operating from +5V and -5.2V, the converter provides -20.48mA of full scale output current and includes an input data register and bandgap voltage reference. Low glitch energy and excellent frequency domain performance are achieved using a segmented architecture. The digital inputs are TTL/CMOS compatible and translated internally to ECL. All internal logic is implemented in ECL to achieve high switching speed with low noise. The addition of laser trimming assures 12-bit linearity is maintained along the entire transfer curve.

## Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| HI5731BIPZ **(No longer available, recommended replacement: HI5731BIBZ)** (See Note) | -40 to 85 | 28 Ld PDIP (Pb-free) | E28.6 |
| HI5731BIBZ (See Note) | -40 to 85 | 28 Ld SOIC (Pb-free) | M28.3 |

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

## Features

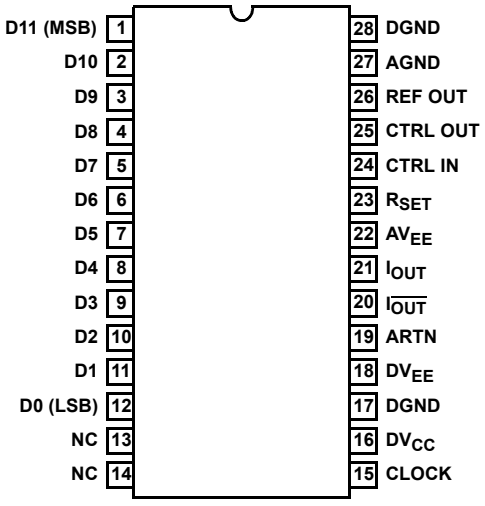
- Pb-free Available as an Option
- Throughput Rate . . . . . 100MSPS
- Low Power . . . . . 650mW
- Integral Linearity Error . . . . . 0.75 LSB
- Low Glitch Energy . . . . . 3.0pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time . . . . . 0.25ns
- Excellent Spurious Free Dynamic Range

## Applications

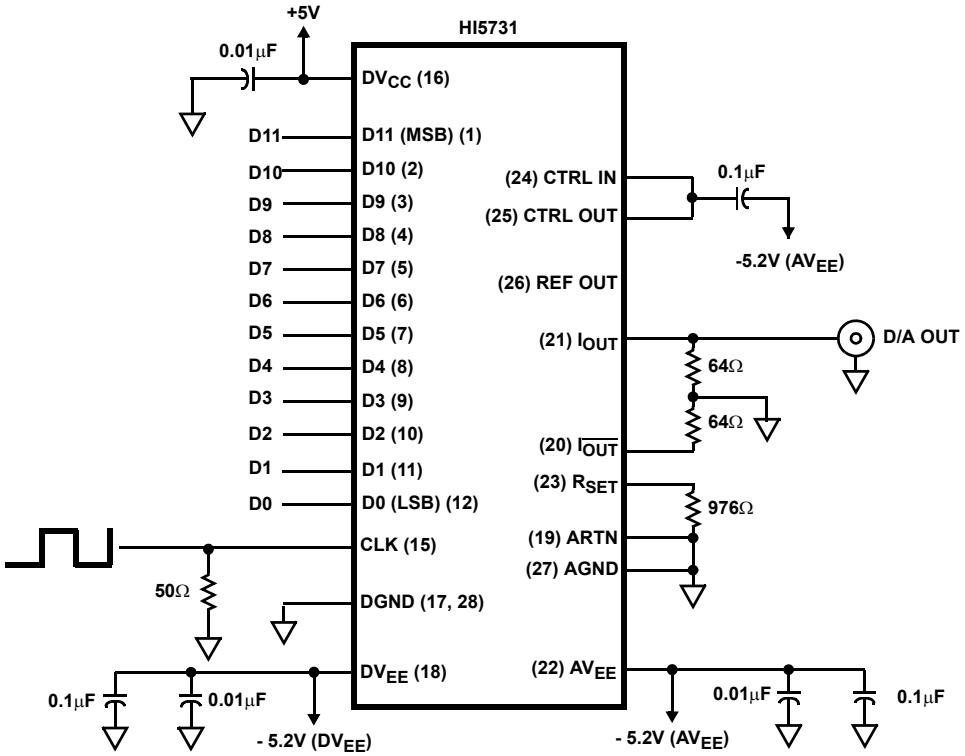
- Cellular Base Stations
- GSM Base Stations
- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

## Pinout

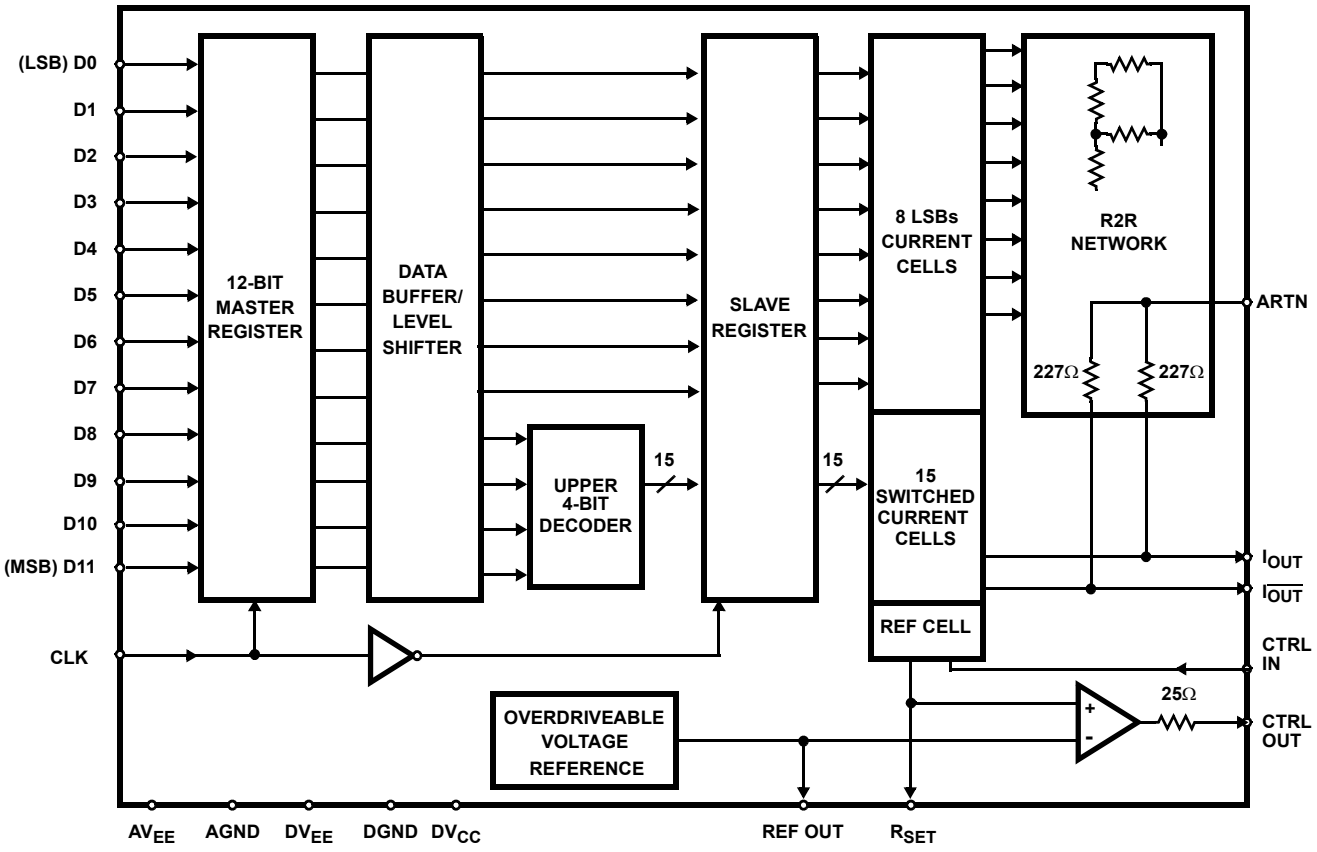
**HI5731**
**(PDIP, SOIC)**
TOP VIEW



## Typical Application Circuit




## Functional Block Diagram



## Absolute Maximum Ratings

Digital Supply Voltage $V_{CC}$ to DGND . . . . . +5.5V
Negative Digital Supply Voltage $DV_{EE}$ to DGND . . . . . -5.5V
Negative Analog Supply Voltage $AV_{EE}$ to AGND, ARTN . . . . -5.5V
Digital Input Voltages (D11-D0, CLK) to DGND. . . . . $DV_{CC}$ to -0.5V
Internal Reference Output Current. . . . . ±2.5mA
Voltage from CTRL IN to $AV_{EE}$ . . . . . 2.5V to 0V
Control Amplifier Output Current . . . . . ±2.5mA
Reference Input Voltage Range. . . . . -3.7V to $AV_{EE}$
Analog Output Current ($I_{OUT}$) . . . . . 30mA

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ ($^{o}$C/W) |
|---|---|
| PDIP Package | 50 |
| SOIC Package | 70 |

Maximum Junction Temperature
HI5731BIx . . . . . 150$^{o}$C
Maximum Storage Temperature Range . . . . . -65$^{o}$C to 150$^{o}$C
Maximum Lead Temperature (Soldering 10s) . . . . . 300$^{o}$C
(SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range. . . . . -40$^{o}$C to 85$^{o}$C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications

$AV_{EE}$, $DV_{EE}$ = -4.94 to -5.46V, $V_{CC}$ = +4.75 to +5.25V, $V_{REF}$ = Internal
$T_A$ = 25$^{o}$C for All Typical Values

| PARAMETER | TEST CONDITIONS | HI5731BI $T_A$ = -40$^{o}$C TO 85$^{o}$C | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **SYSTEM PERFORMANCE** | | | | | |
| Resolution | | 12 | - | - | Bits |
| Integral Linearity Error, INL | (Note 4) ("Best Fit" Straight Line) | - | 0.75 | 1.5 | LSB |
| Differential Linearity Error, DNL | (Note 4) | - | 0.5 | 1.0 | LSB |
| Offset Error, $I_{OS}$ | (Note 4) | - | 20 | 75 | µA |
| Full Scale Gain Error, FSE | (Notes 2, 4) | - | 1 | 10 | % |
| Full Scale Gain Drift | With Internal Reference | - | ±150 | - | ppm FSR/$^{o}$C |
| Offset Drift Coefficient | (Note 3) | - | - | 0.05 | µA/$^{o}$C |
| Full Scale Output Current, $I_{FS}$ | | - | 20.48 | - | mA |
| Output Voltage Compliance Range | (Note 3) | -1.25 | - | 0 | V |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Throughput Rate | (Note 3) | 100 | - | - | MSPS |
| Output Voltage Full Scale Step Settling Time, $t_{SETT}$, Full Scale | To ±0.5 LSB Error Band $R_L$ = 50Ω (Note 3) | - | 20 | - | ns |
| Singlet Glitch Area, GE (Peak) | $R_L$ = 50Ω (Note 3) | - | 5 | - | pV-s |
| Doublet Glitch Area, (Net) | | - | 3 | - | pV-s |
| Output Slew Rate | $R_L$ = 50Ω, DAC Operating in Latched Mode (Note 3) | - | 1,000 | - | V/µs |
| Output Rise Time | $R_L$ = 50Ω, DAC Operating in Latched Mode (Note 3) | - | 675 | - | ps |
| Output Fall Time | $R_L$ = 50Ω, DAC Operating in Latched Mode (Note 3) | - | 470 | - | ps |
| Spurious Free Dynamic Range within a Window (Note 3) | $f_{CLK}$ = 10MSPS, $f_{OUT}$ = 1.23MHz, 2MHz Span | - | 85 | - | dBc |
| | $f_{CLK}$ = 20MSPS, $f_{OUT}$ = 5.055MHz, 2MHz Span | - | 77 | - | dBc |
| | $f_{CLK}$ = 40MSPS, $f_{OUT}$ = 16MHz, 10MHz Span | - | 75 | - | dBc |
| | $f_{CLK}$ = 50MSPS, $f_{OUT}$ = 10.1MHz, 2MHz Span | - | 80 | - | dBc |
| | $f_{CLK}$ = 80MSPS, $f_{OUT}$ = 5.1MHz, 2MHz Span | - | 78 | - | dBc |
| | $f_{CLK}$ = 100MSPS, $f_{OUT}$ = 10.1MHz, 2MHz Span | - | 79 | - | dBc |

**Electrical Specifications** $AV_{EE}$, $DV_{EE}$ = -4.94 to -5.46V, $V_{CC}$ = +4.75 to +5.25V, $V_{REF}$ = Internal $T_A$ = 25°C for All Typical Values **(Continued)**

| PARAMETER | TEST CONDITIONS | HI5731BI $T_A$ = -40°C TO 85°C | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| Spurious Free Dynamic Range to Nyquist (Note 3) | $f_{CLK}$ = 40MSPS, $f_{OUT}$ = 2.02MHz, 20MHz Span | - | 70 | - | dBc |
| | $f_{CLK}$ = 80MSPS, $f_{OUT}$ = 2.02MHz, 40MHz Span | - | 70 | - | dBc |
| | $f_{CLK}$ = 100MSPS, $f_{OUT}$ = 2.02MHz, 50MHz Span | - | 69 | - | dBc |
| **REFERENCE/CONTROL AMPLIFIER** | | | | | |
| Internal Reference Voltage, $V_{REF}$ | (Note 4) | -1.27 | -1.23 | -1.17 | V |
| Internal Reference Voltage Drift | (Note 3) | - | 175 | - | µV/°C |
| Internal Reference Output Current Sink/Source Capability | (Note 3) | -125 | - | +50 | µA |
| Internal Reference Load Regulation | $I_{REF}$ = 0 to $I_{REF}$ = -125µA | - | 50 | - | µV |
| Input Impedance at REF OUT pin | (Note 3) | - | 1.4 | - | kΩ |
| Amplifier Large Signal Bandwidth ($0.6V_{P-P}$) | Sine Wave Input, to Slew Rate Limited (Note 3) | - | 3 | - | MHz |
| Amplifier Small Signal Bandwidth ($0.1V_{P-P}$) | Sine Wave Input, to -3dB Loss (Note 3) | - | 10 | - | MHz |
| Reference Input Impedance | (Note 3) | - | 12 | - | kΩ |
| Reference Input Multiplying Bandwidth (CTL IN) | $R_L$ = 50Ω, 100mV Sine Wave, to -3dB Loss at $I_{OUT}$ (Note 3) | - | 200 | - | MHz |
| **DIGITAL INPUTS (D9-D0, CLK, INVERT)** | | | | | |
| Input Logic High Voltage, $V_{IH}$ | (Note 4) | 2.0 | - | - | V |
| Input Logic Low Voltage, $V_{IL}$ | (Note 4) | - | - | 0.8 | V |
| Input Logic Current, $I_{IH}$ | (Note 4) | - | - | 400 | µA |
| Input Logic Current, $I_{IL}$ | (Note 4) | - | - | 700 | µA |
| Digital Input Capacitance, $C_{IN}$ | (Note 3) | - | 3.0 | - | pF |
| **TIMING CHARACTERISTICS** | | | | | |
| Data Setup Time, $t_{SU}$ | See Figure 1 (Note 3) | 3.0 | 2.0 | - | ns |
| Data Hold Time, $t_{HLD}$ | See Figure 1 (Note 3) | 0.5 | 0.25 | - | ns |
| Propagation Delay Time, $t_{PD}$ | See Figure 1 (Note 3) | - | 4.5 | - | ns |
| CLK Pulse Width, $t_{PW1}$, $t_{PW2}$ | See Figure 1 (Note 3) | 3.0 | - | - | ns |
| **POWER SUPPLY CHARACTERISTICS** | | | | | |
| $I_{EEA}$ | (Note 4) | - | 42 | 50 | mA |
| $I_{EED}$ | (Note 4) | - | 70 | 85 | mA |
| $I_{CCD}$ | (Note 4) | - | 13 | 20 | mA |
| Power Dissipation | (Note 4) | - | 650 | - | mW |
| Power Supply Rejection Ratio | $V_{CC}$ ±5%, $V_{EE}$ ±5% | - | 5 | - | µA/V |

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through $R_{SET}$ (typically 1.28mA). Ideally the ratio should be 16.
3. Parameter guaranteed by design or characterization and not production tested.
4. All devices are 100% tested at 25°C.
5. Dynamic Range must be limited to a 1V swing within the compliance range.

## Timing Diagrams

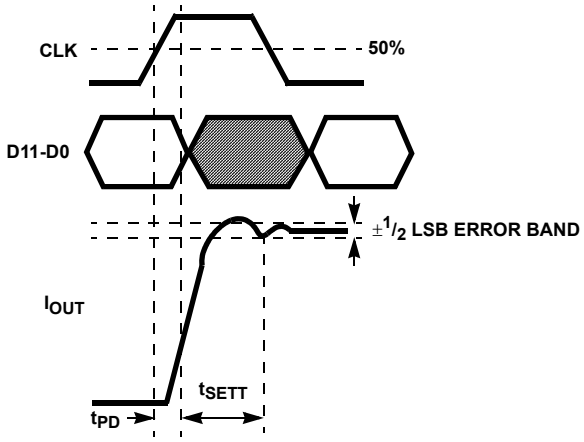



FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

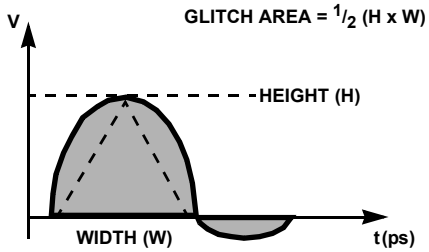



FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

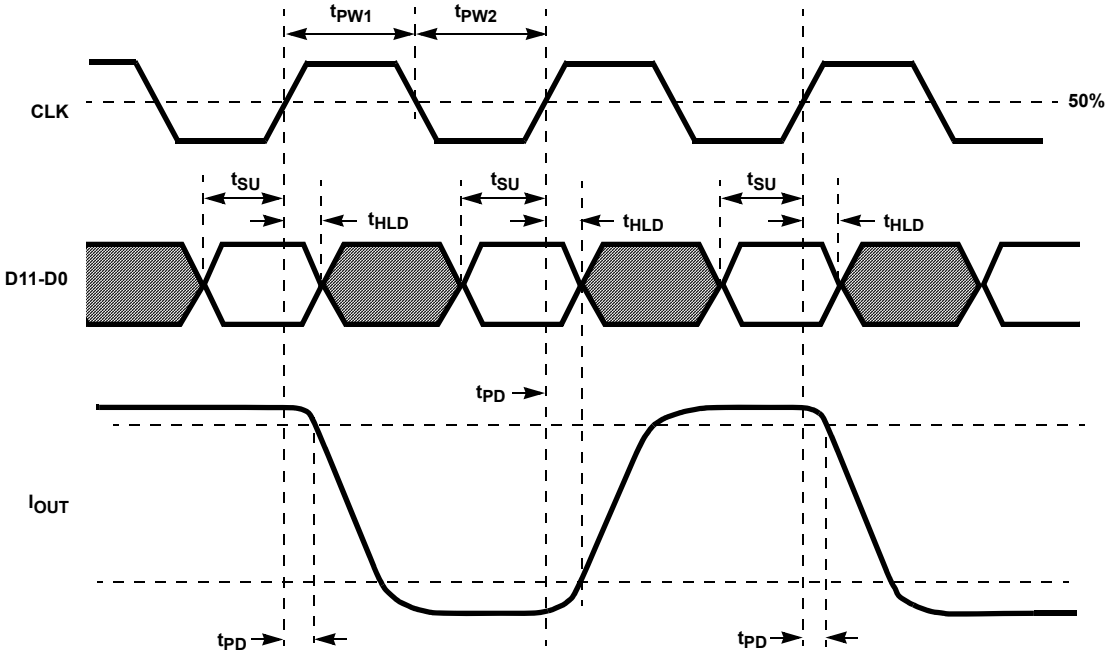



FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

## *Typical Performance Curves*

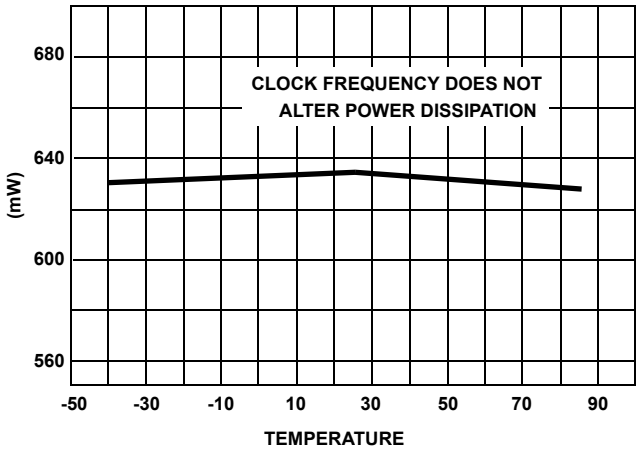



FIGURE 4. TYPICAL POWER DISSIPATION OVER TEMPERATURE

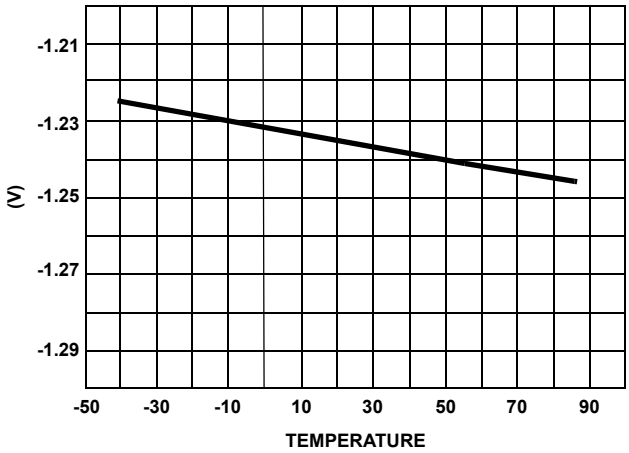



FIGURE 5. TYPICAL REFERENCE VOLTAGE OVER TEMPERATURE

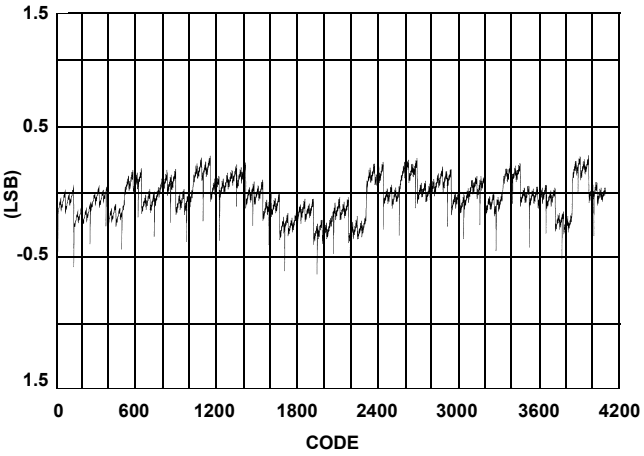



FIGURE 6. TYPICAL INL

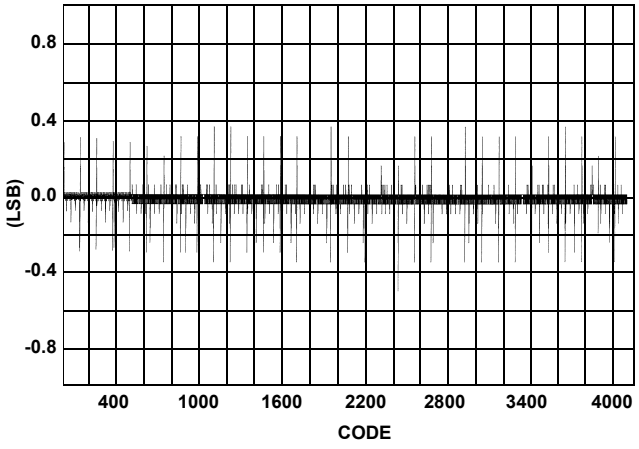



FIGURE 7. TYPICAL DNL

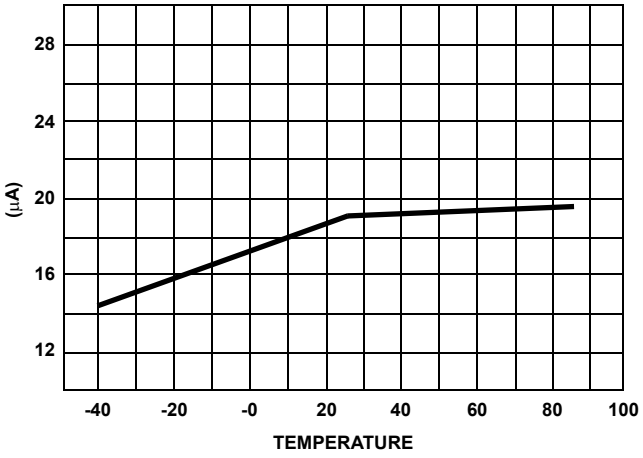



FIGURE 8. OFFSET CURRENT OVER TEMPERATURE

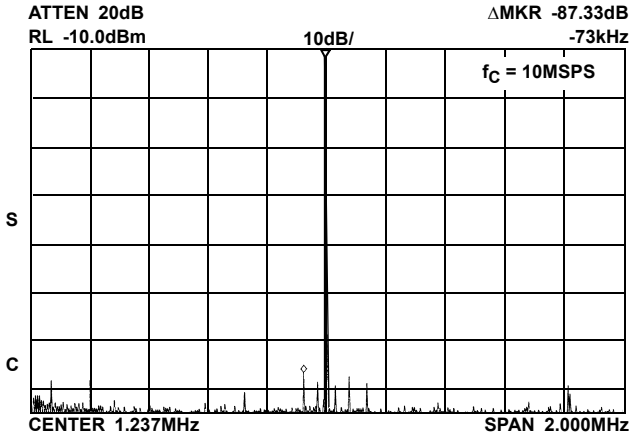



FIGURE 9. SPURIOUS FREE DYNAMIC RANGE = 87.3dBc

## *Typical Performance Curves* (Continued)

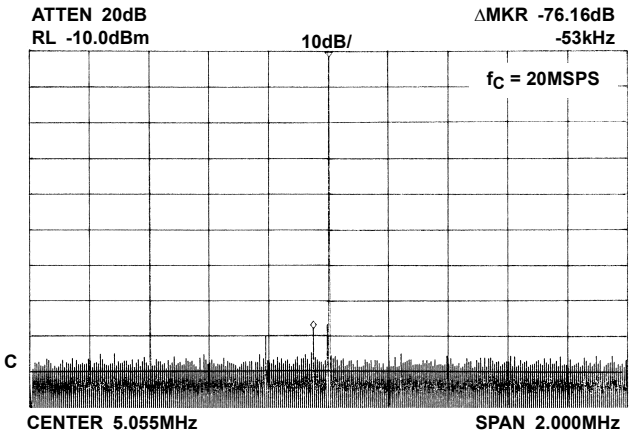



FIGURE 10. SPURIOUS FREE DYNAMIC RANGE = 76.16dBc

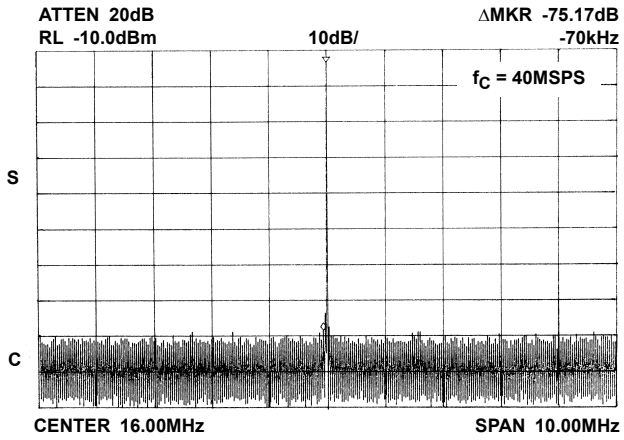



FIGURE 11. SPURIOUS FREE DYNAMIC RANGE = 75.17dBc

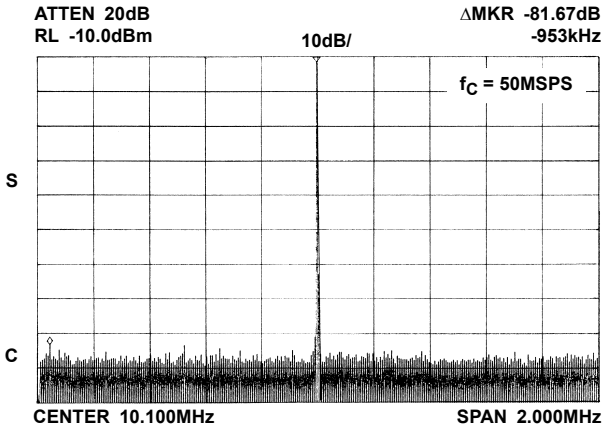



FIGURE 12. SPURIOUS FREE DYNAMIC RANGE = -81.67dBc

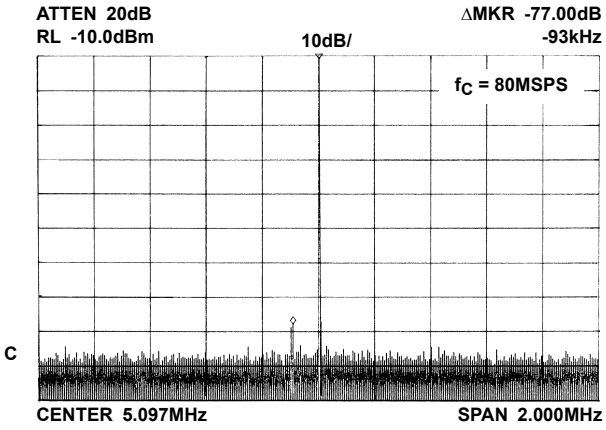



FIGURE 13. SPURIOUS FREE DYNAMIC RANGE = 77dBc

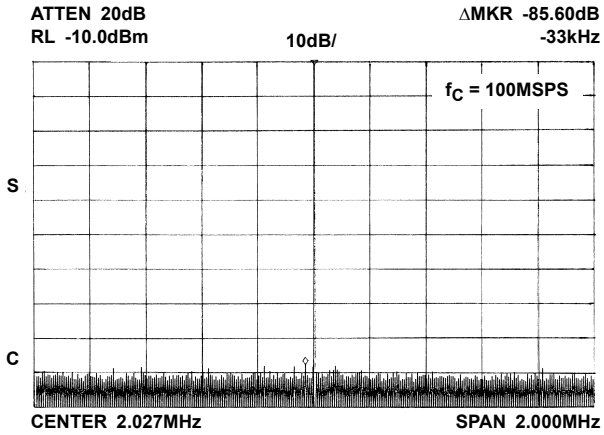



FIGURE 14. SPURIOUS FREE DYNAMIC RANGE = -85.60dBc

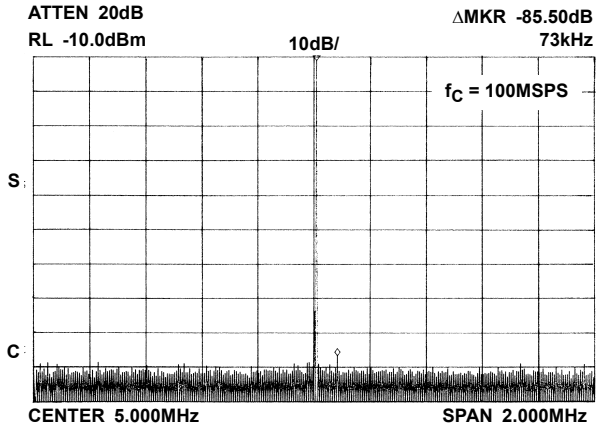



FIGURE 15. SPURIOUS FREE DYNAMIC RANGE = 85.5dBc

## *Typical Performance Curves* (Continued)

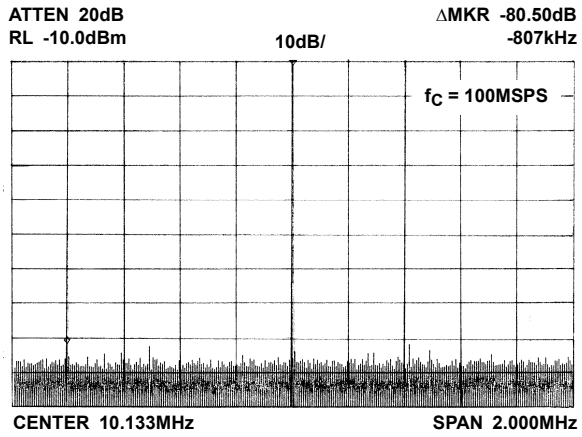



FIGURE 16. SPURIOUS FREE DYNAMIC RANGE = 80.5dBc

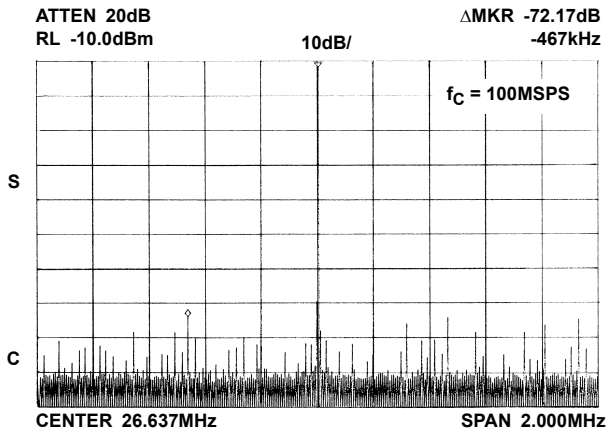



FIGURE 17. SPURIOUS FREE DYNAMIC RANGE = 72.17dBc

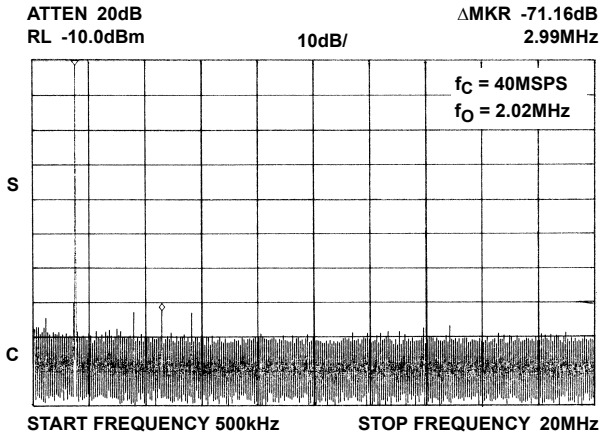



FIGURE 18. SPURIOUS FREE DYNAMIC RANGE = 71.16dBc

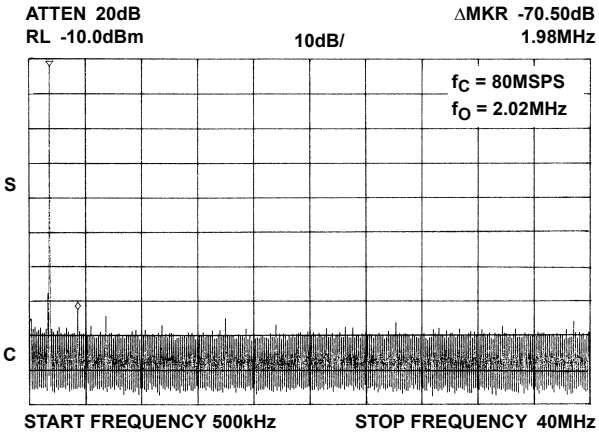



FIGURE 19. SPURIOUS FREE DYNAMIC RANGE = 70.5dBc

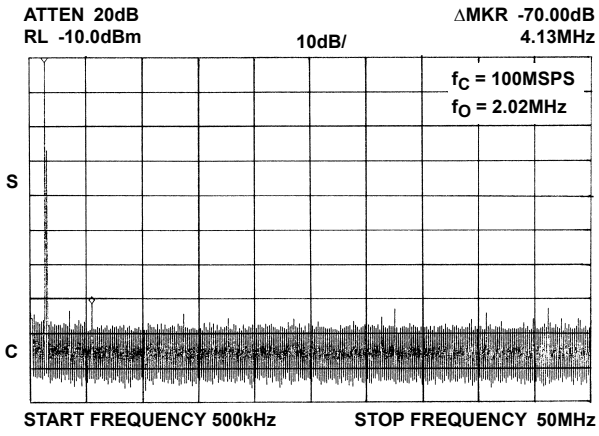



FIGURE 20. SPURIOUS FREE DYNAMIC RANGE = 70dBc

## Pin Descriptions

| PIN NUMBER | PIN NAME | PIN DESCRIPTION |
|---|---|---|
| 1-12 | D11 (MSB) thru D0 (LSB) | Digital Data Bit 11, the Most Significant Bit thru Digital Data Bit 0, the Least Significant Bit. |
| 15 | CLK | Data Clock Pin DC to 100MSPS. |
| 13, 14 | NC | No Connect. |
| 16 | $DV_{CC}$ | Digital Logic Supply +5V. |
| 17, 28 | DGND | Digital Ground. |
| 18 | $DV_{EE}$ | -5.2V Logic supply. |
| 23 | $R_{SET}$ | External resistor to set the full scale output current. $I_{FS}$ = 16 x ($V_{REF\ OUT}$ / $R_{SET}$). Typically 976Ω. |
| 27 | AGND | Analog Ground supply current return pin. |
| 19 | ARTN | Analog Signal Return for the R/2R ladder. |
| 21 | $I_{OUT}$ | Current Output Pin. |
| 20 | $I_{\overline{OUT}}$ | Complementary Current Output Pin. |
| 22 | $AV_{EE}$ | -5.2V Analog Supply. |
| 24 | CTRL IN | Input to the current source base rail. Typically connected to CTRL OUT and a 0.1µF capacitor to $AV_{EE}$. Allows external control of the current sources. |
| 25 | CTRL OUT | Control Amplifier Out. Provides precision control of the current sources when connected to CTRL IN such that $I_{FS}$ = 16 x ($V_{REF\ OUT}$ / $R_{SET}$). |
| 26 | REF OUT | -1.23V (Typ) bandgap reference voltage output. Can sink up to 125µA or be overdriven by an external reference capable of delivering up to 2mA. |

## Detailed Description

The HI5731 is a 12-bit, current out D/A converter. The DAC can convert at 100MSPS and runs on +5V and -5.2V supplies. The architecture is an R/2R and segmented switching current cell arrangement to reduce glitch. Laser trimming is employed to tune linearity to true 12-bit levels. The HI5731 achieves its low power and high speed performance from an advanced BiCMOS process. The HI5731 consumes 650mW (typical) and has an improved hold time of only 0.25ns (typical). The HI5731 is an excellent converter for use in communications applications and high performance instrumentation systems.

### Digital Inputs

The HI5731 is a TTL/CMOS compatible D/A. Data is latched by a Master register. Once latched, data inputs D0 (LSB) thru D11 (MSB) are internally translated from TTL to ECL. The internal latch and switching current source controls are implemented in ECL technology to maintain high switching speeds and low noise characteristics.

### Decoder/Driver

The architecture employs a split R/2R ladder and Segmented Current source arrangement. Bits D0 (LSB) thru D7 directly drive a typical R/2R network to create the binary weighted current sources. Bits D8 thru D11 (MSB) pass thru a “thermometer” decoder that converts the incoming data into 15 individual segmented current source enables. This split architecture helps to improve glitch, thus resulting in a more constant glitch characteristic across the entire output transfer function.

### Clocks and Termination

The internal 12-bit register is updated on the rising edge of the clock. Since the HI5731 clock rate can run to 100MSPS, to minimize reflections and clock noise into the part proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board controlled impedance PCBs should be used with a characteristic line impedance $Z_O$ of 50Ω.

To terminate the clock line, a shunt terminator to ground is the most effective type at a 100MSPS clock rate. A typical value for termination can be determined by the equation:

$R_T = Z_O$,

for the termination resistor. For a controlled impedance board with a $Z_O$ of 50Ω, the $R_T$ = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5731 CLK pin as possible.

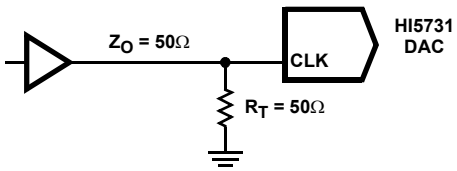



**FIGURE 21. CLOCK LINE TERMINATION**

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator should be connected to DGND.

### Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI5731 as

possible on the analog ($AV_{EE}$) and digital ($DV_{EE}$) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up. The $V_{CC}$ power pin should also be decoupled with a 0.1µF capacitor.

### *Reference*

The internal reference of the HI5731 is a -1.23V (typical) bandgap voltage reference with 175µV/°C of temperature drift (typical). The internal reference is connected to the Control Amplifier which in turn drives the segmented current cells. Reference Out (REF OUT) is internally connected to the Control Amplifier. The Control Amplifier Output (CTRL OUT) should be used to drive the Control Amplifier Input (CTRL IN) and a 0.1µF capacitor to analog $V_{EE}$. This improves settling time by providing an AC ground at the current source base node. The Full Scale Output Current is controlled by the REF OUT pin and the set resistor ($R_{SET}$). The ratio is:

$I_{OUT}$ (Full Scale) = ($V_{REF\ OUT}/R_{SET}$) x 16,

The internal reference (REF OUT) can be overdriven with a more precise external reference to provide better performance over temperature. Figure 22 illustrates a typical external reference configuration.

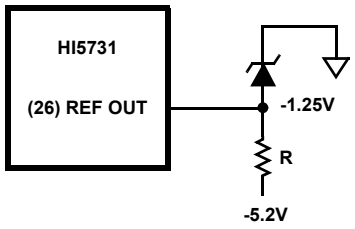



**FIGURE 22. EXTERNAL REFERENCE CONFIGURATION**

### *Multiplying Capability*

The HI5731 can operate in two different multiplying configurations. For frequencies from DC to 100kHz, a signal of up to 0.6$V_{P-P}$ can be applied directly to the REF OUT pin as shown in Figure 23.

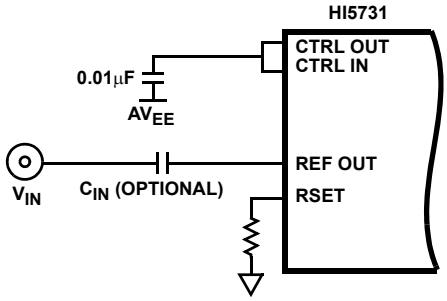



**FIGURE 23. LOW FREQUENCY MULTIPLYING BANDWIDTH CIRCUIT**

The signal must have a DC value such that the peak negative voltage equals -1.25V. Alternately, a capacitor can be placed in series with REF OUT if DC multiplying is not required. The lower input bandwidth can be calculated using the following formula:

$$C_{IN} = \frac{1}{(2\pi)(1400)(f_{IN})}.$$

For multiplying frequencies above 100kHz, the CTRL IN pin can be driven directly as seen in Figure 24.

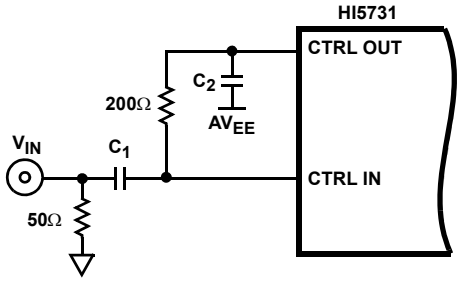



**FIGURE 24. HIGH FREQUENCY MULTIPLYING BANDWIDTH CIRCUIT**

The nominal input/output relationship is defined as:

$$\Delta I_{OUT} = \frac{\Delta V_{IN}}{80\Omega}.$$

In order to prevent the full scale output current from exceeding 20.48mA, the $R_{SET}$ resistor must be adjusted according to the following equation:

$$R_{SET} = \frac{16V_{REF}}{I_{OUT}(\text{FULL SCALE}) - \left(\frac{V_{IN(PEAK)}}{80\Omega}\right)}.$$

The circuit in Figure 24 can be tuned to adjust the lower cutoff frequency by adjusting capacitor values. Table 1 below illustrates the relationship.

**TABLE 1. CAPACITOR SELECTION**

| $f_{IN}$ | C1 | C2 |
|---|---|---|
| 100kHz | 0.01µF | 1µF |
| >1MHz | 0.001µF | 0.1µF |

Also, the input signal must be limited to 1$V_{P-P}$ to avoid distortion in the DAC output current caused by excessive modulation of the internal current sources.

### *Outputs*

The outputs $I_{OUT}$ and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either $I_{OUT}$ or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a load resistor. Both current outputs should have the same load resistor (64Ω typically). By using a 64Ω load on the output, a 50Ω effective output resistance ($R_{OUT}$) is achieved due to the 227Ω (±15%) parallel resistance seen looking back into the output. This is the nominal value of the R2R ladder of the DAC. The 50Ω output is needed for matching the output with a 50Ω line. The load resistor should be chosen so that the effective output

resistance ($R_{OUT}$) matches the line resistance. The output voltage is:

$V_{OUT} = I_{OUT} \times R_{OUT}$.

$I_{OUT}$ is defined in the reference section. $I_{\overline{OUT}}$ is not trimmed to 12 bits, so it is not recommended that it be used in conjunction with $I_{OUT}$ in a differential-to-single-ended application. The compliance range of the output is from -1.25V to 0V, with a $1V_{P-P}$ voltage swing allowed within this range.

**TABLE 2. INPUT CODING vs CURRENT OUTPUT**

| INPUT CODE (D11-D0) | $I_{OUT}$ (mA) | $I_{\overline{OUT}}$ (mA) |
|---|---|---|
| 1111 1111 1111 | -20.48 | 0 |
| 1000 0000 0000 | -10.24 | -10.24 |
| 0000 0000 0000 | 0 | -20.48 |

### *Settling Time*

The settling time of the HI5731 is measured as the time it takes for the output of the DAC to settle to within a $\pm 1/2$ LSB error band of its final value during a full scale (code 0000... to 1111.... or 1111... to 0000...) transition. All claims made by Intersil with respect to the settling time performance of the HI5731 have been fully verified by the National Institute of Standards and Technology (NIST) and are fully traceable.

### *Glitch*

The output glitch of the HI5731 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically, the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. In order to minimize this, the Intersil HI5731 employes an internal register, just prior to the current sources, which is updated on the clock edge. Lastly, the worst case glitch on traditional D/A converters usually occurs at the major transition (i.e., code 2047 to 2048). However, due to the split architecture of the HI5731, the glitch is moved to the 255 to 256 transition (and every subsequent 256 code transitions thereafter). This split R/2R segmented current source architecture, which decreases the amount of current switching at any one time, makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI5731 the output is terminated into a 64Ω load. The glitch is measured at any one of the current cell carry (code 255 to 256 transition or any multiple thereof) throughout the DACs output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 26 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt-seconds (pV-s).

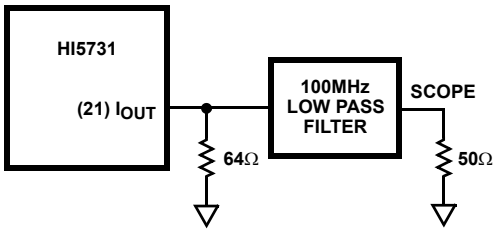



**FIGURE 25. GLITCH TEST CIRCUIT**

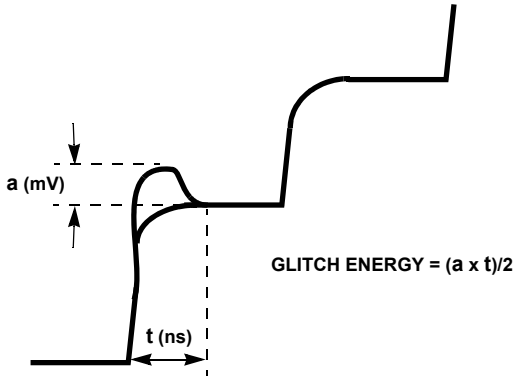



**FIGURE 26. MEASURING GLITCH ENERGY**

## *Applications*

### *Bipolar Applications*

To convert the output of the HI5731 to a bipolar 4V swing, the following applications circuit is recommended. The reference can only provide 125µA of drive, so it must be buffered to create the bipolar offset current needed to generate the -2V output with all bits ‘off’. The output current must be converted to a voltage and then gained up and offset to produce the proper swing. Care must be taken to compensate for the voltage swing and error.

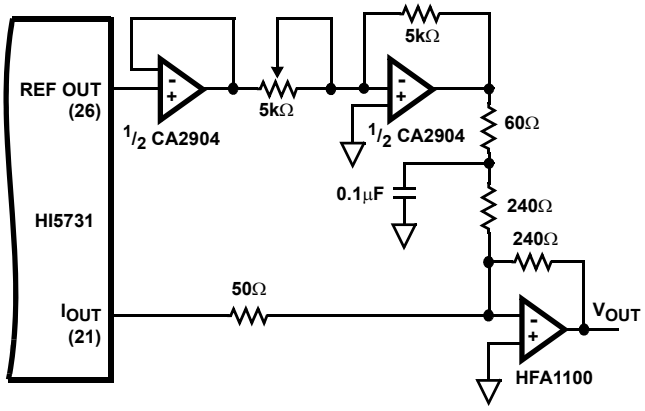



**FIGURE 27. BIPOLAR OUTPUT CONFIGURATION**

### *Interfacing to the HSP45106 NCO-16*

The HSP45106 is a 16-bit, Numerically Controlled Oscillator (NCO). The HSP45106 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 28 shows how to interface an HI5731 to the HSP45106.

### *Interfacing to the HSP45102 NCO-12*

The HSP45102 is a 12-bit, Numerically Controlled Oscillator (NCO). The HSP45102 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 29 shows how to interface an HI5731 to the HSP45102.

This high level block diagram is that of a basic PSK modulator. In this example the encoder generates the PSK waveform by driving the Phase Modulation Inputs (P1, P0) of the HSP45102. The P1-0 inputs impart a phase shift to the carrier wave as defined in Table 2.

**TABLE 3. PHASE MODULATION INPUT CODING**

| P1 | P0 | PHASE SHIFT (DEGREES) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 90 |
| 1 | 0 | 270 |
| 1 | 1 | 180 |

The data port of the HSP45102 drives the 12-bit HI5731 DAC which converts the NCO output into an analog waveform. The output filter connected to the DAC can be tailored to remove unwanted spurs for the desired carrier frequency. The controller is used to load the desired center frequency and control the HSP45102. The HI5731 coupled with the HSP45102 make an inexpensive PSK modulator with Spurious Free performance down to -76dBc.

## *Definition of Specifications*

**Integral Linearity Error, INL,** is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

**Differential Linearity Error, DNL,** is the measure of the error in step size between adjacent codes along the converter's transfer curve. Ideally, the step size is 1 LSB from one code to the next, and the deviation from 1 LSB is known as DNL. A DNL specification of greater than -1 LSB guarantees monotonicity.

**Feedthru,** is the measure of the undesirable switching noise coupled to the output.

**Output Voltage Full Scale Settling Time,** is the time required from the 50% point on the clock input for a full scale step to settle within an $\pm 1/2$ LSB error band.

**Output Voltage Small Scale Settling Time,** is the time required from the 50% point on the clock input for a 100mV step to settle within an $1/2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

**Glitch Area, GE,** is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a picoVolt-time specification (typically pV-s).

**Differential Gain,** $\Delta A_V$, is the gain error from an ideal sine wave with a normalized amplitude.

**Differential Phase,** $\Delta\Phi$, is the phase error from an ideal sine wave.

**Signal to Noise Ratio, SNR,** is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $1/2$ the clock frequency is used to eliminate alias products.

**Total Harmonic Distortion, THD,** is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $1/2$ the clock frequency is used to eliminate alias products.

**Spurious Free Dynamic Range, SFDR**, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $1/2$ the clock frequency to eliminate noise from clocking alias terms.

**Intermodulation Distortion, IMD,** is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD can be calculated using the following equation:

$$IMD = \frac{20\text{Log (RMS of Sum and Difference Distortion Products)}}{\text{(RMS Amplitude of the Fundamental)}}.$$

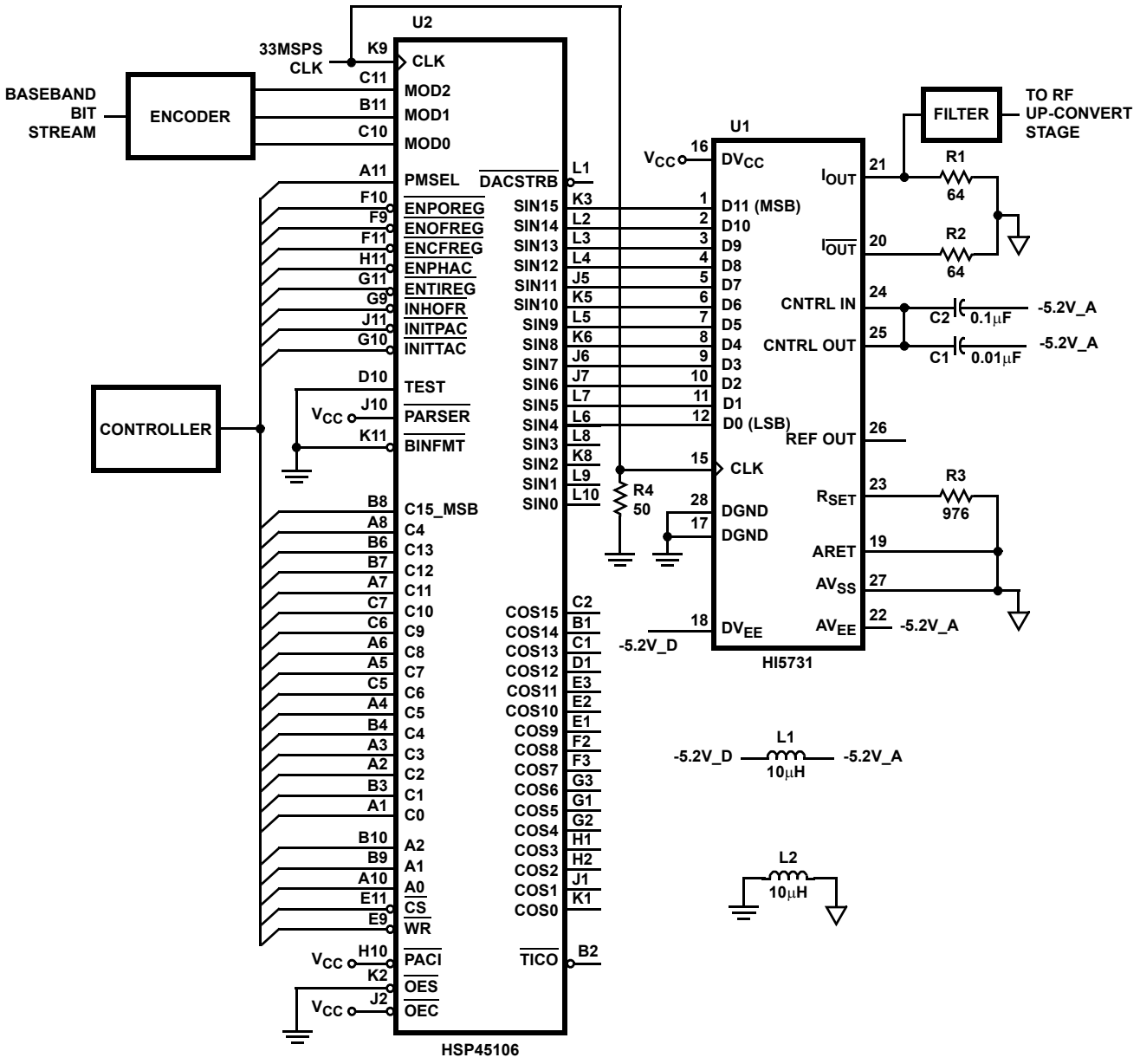



FIGURE 28. MODULATOR USING THE HI5731 AND THE HSP45106 16-BIT NCO

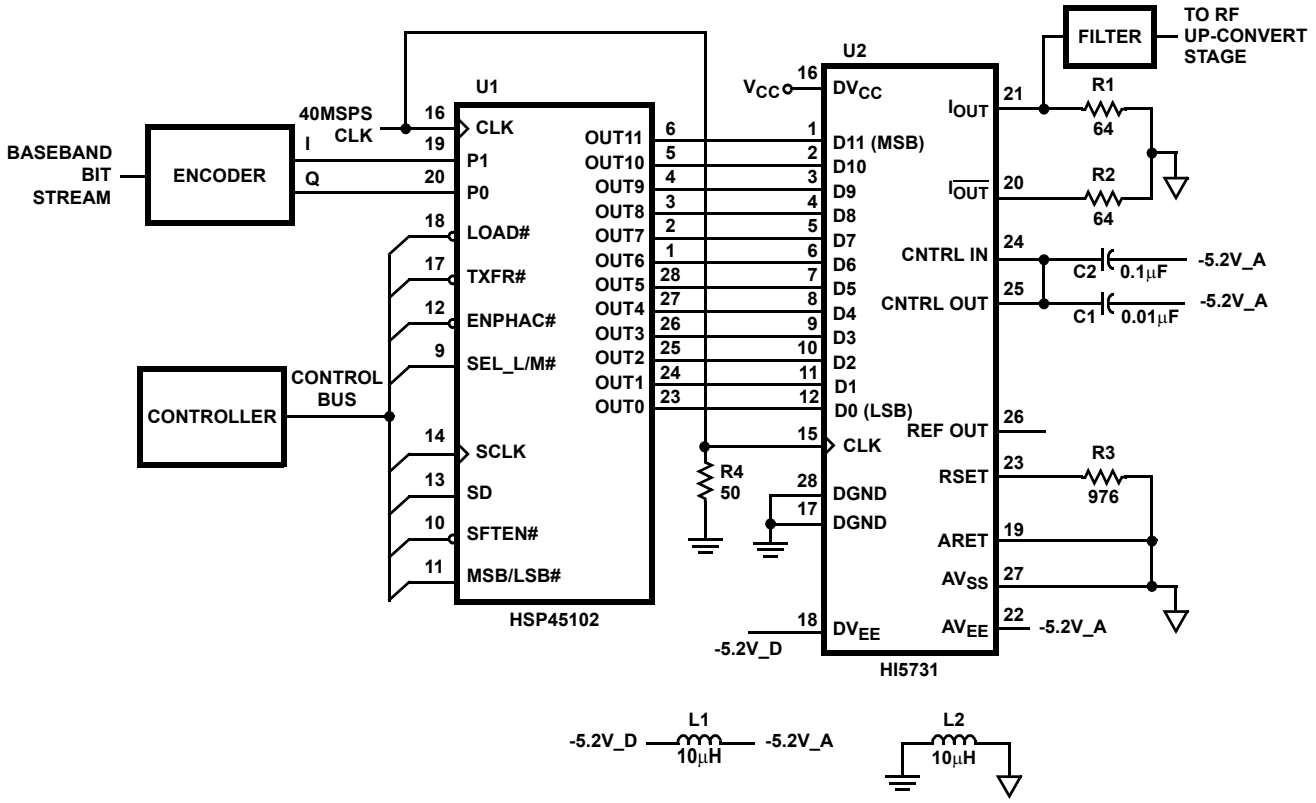



**FIGURE 29. PSK MODULATOR USING THE HI5731 AND THE HSP45102 12-BIT NCO**

## Die Characteristics

**DIE DIMENSIONS**

161.5 mils x 160.7 mils x 19 mils

**METALLIZATION**

Type: AlSiCu
Thickness: M1 - 8kÅ, M2 - 17kÅ

**PASSIVATION**

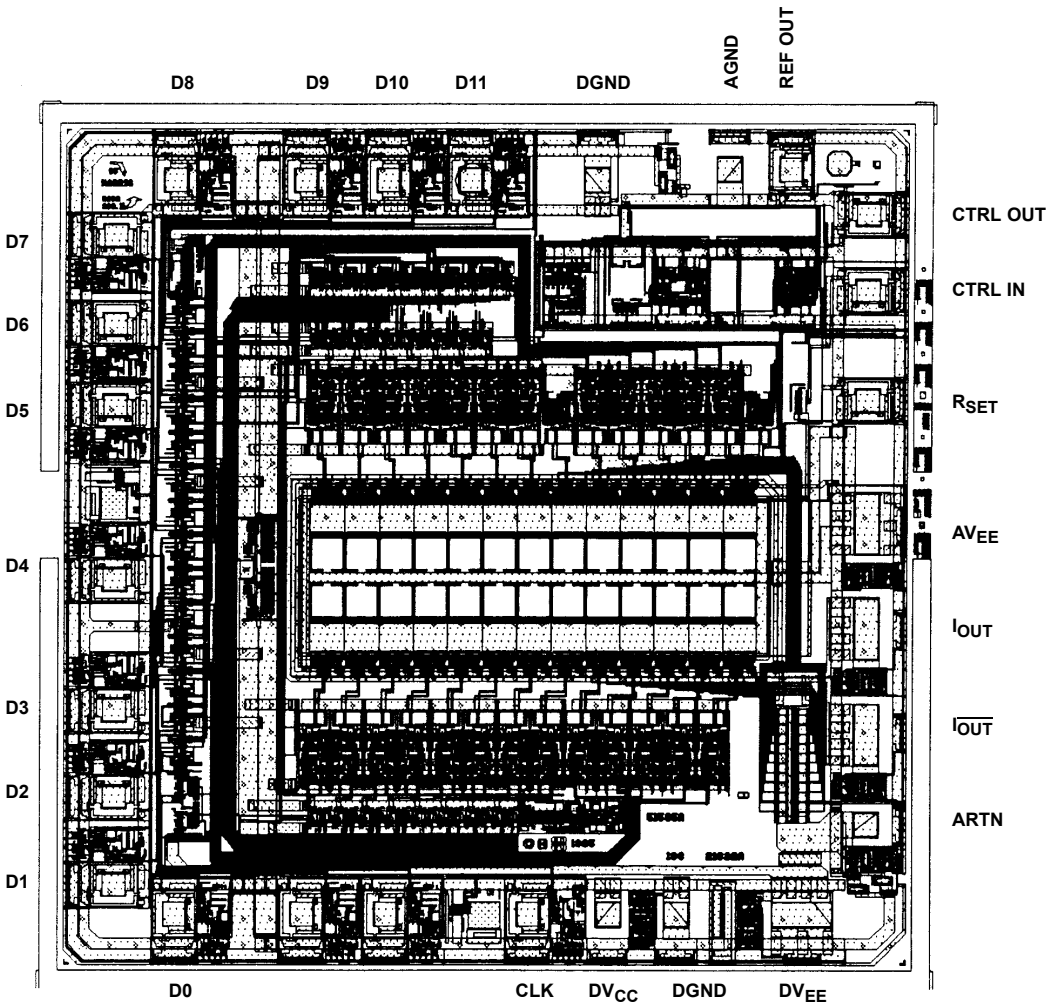
Type: Sandwich Passivation
Undoped Silicon Glass (USG) + Nitride
Thickness: USG - 8kÅ, Nitride - 4.2kÅ
Total 12.2kÅ + 2kÅ

**SUBSTRATE POTENTIAL (POWERED UP)**

$V_{EED}$

## Metallization Mask Layout

**HI5731**



## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| October 2, 2015 | FN4070.10 | - Updated Ordering Information Table on page 1.<br>- Added Revision History.<br>- Added About Intersil Verbiage.<br>- Updated POD M28.3 to latest revision changes are as follow:<br>Added land pattern. |

## About Intersil

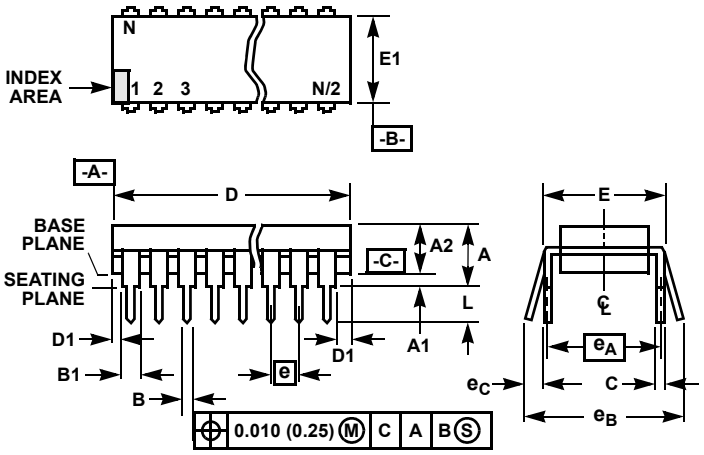
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

## *Dual-In-Line Plastic Packages (PDIP)*




NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $e_A$ are measured with the leads constrained to be perpendicular to datum -C-.
7. $e_B$ and $e_C$ are measured at the lead tips with the leads unconstrained. $e_C$ must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E28.6** (JEDEC MS-011-AB ISSUE B)
**28 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.250 | - | 6.35 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.125 | 0.195 | 3.18 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.030 | 0.070 | 0.77 | 1.77 | 8 |
| C | 0.008 | 0.015 | 0.204 | 0.381 | - |
| D | 1.380 | 1.565 | 35.1 | 39.7 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.600 | 0.625 | 15.24 | 15.87 | 6 |
| E1 | 0.485 | 0.580 | 12.32 | 14.73 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| $e_A$ | 0.600 BSC | | 15.24 BSC | | 6 |
| $e_B$ | - | 0.700 | - | 17.78 | 7 |
| L | 0.115 | 0.200 | 2.93 | 5.08 | 4 |
| N | 28 | | 28 | | 9 |

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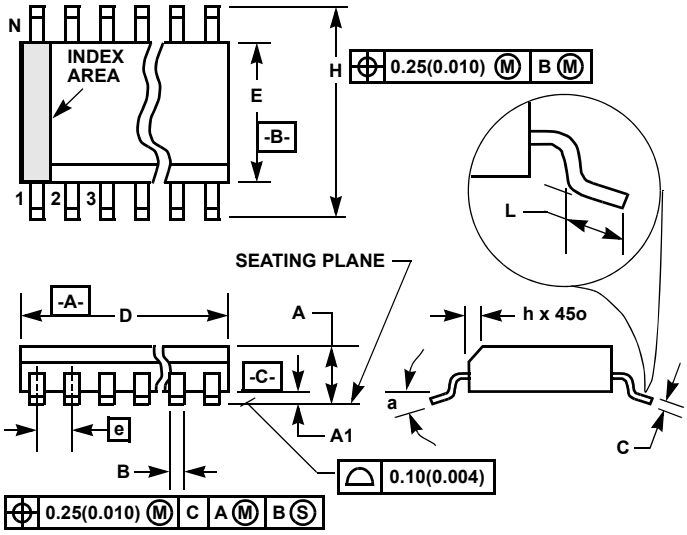
## *Small Outline Plastic Packages (SOIC)*




**M28.3** (JEDEC MS-013-AE ISSUE C)
**28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0926 | 0.1043 | 2.35 | 2.65 | - |
| A1 | 0.0040 | 0.0118 | 0.10 | 0.30 | - |
| B | 0.013 | 0.0200 | 0.33 | 0.51 | 9 |
| C | 0.0091 | 0.0125 | 0.23 | 0.32 | - |
| D | 0.6969 | 0.7125 | 17.70 | 18.10 | 3 |
| E | 0.2914 | 0.2992 | 7.40 | 7.60 | 4 |
| e | 0.05 BSC | | 1.27 BSC | | - |
| H | 0.394 | 0.419 | 10.00 | 10.65 | - |
| h | 0.01 | 0.029 | 0.25 | 0.75 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 28 | | 28 | | 7 |
| $\alpha$ | $0^o$ | $8^o$ | $0^o$ | $8^o$ | - |

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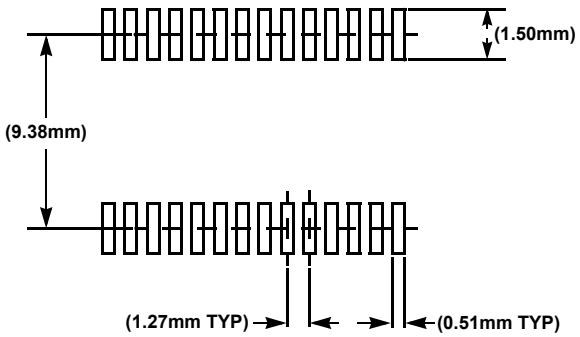
**TYPICAL RECOMMENDED LAND PATTERN**




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.