

Dual/Quad SPST, CMOS Analog Switches

HI-200/HI-201 (dual/quad) are monolithic devices comprising independently selectable SPST switches which feature fast switching speeds (HI-200 240ns, and HI-201 185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltage up to the supply rails and for signal current up to 80mA. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200/HI-201 are ideal components for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and operational amplifier gain switching networks.

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|-----------------------|------------------|--------------------------|-------------|
| HI3-0200-5Z (Note) | 0 to 75 | 14 Ld PDIP* (Pb-free) | E14.3 |
| HI1-0201-2 | -55 to 125 | 16 Ld CERDIP | F16.3 |
| HI1-0201-4 | -25 to 85 | 16 Ld CERDIP | F16.3 |
| HI1-0201-5 | 0 to 75 | 16 Ld CERDIP | F16.3 |
| HI3-0201-5 | 0 to 75 | 16 Ld PDIP | E16.3 |
| HI3-0201-5Z (Note) | 0 to 75 | 16 Ld PDIP* (Pb-free) | E16.3 |
| HI4P0201-5 | 0 to 75 | 20 Ld PLCC | N20.35 |
| HI4P0201-5Z (Note) | 0 to 75 | 20 Ld PLCC (Pb-free) | N20.35 |
| HI9P0201-5 | 0 to 75 | 16 Ld SOIC | M16.15 |
| HI9P0201-5Z (Note) | 0 to 75 | 16 Ld SOIC (Pb-free) | M16.15 |
| HI9P0201-9 | -40 to 85 | 16 Ld SOIC | M16.15 |
| HI9P0201-9Z (Note) | -40 to 85 | 16 Ld SOIC (Pb-free) | M16.15 |

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

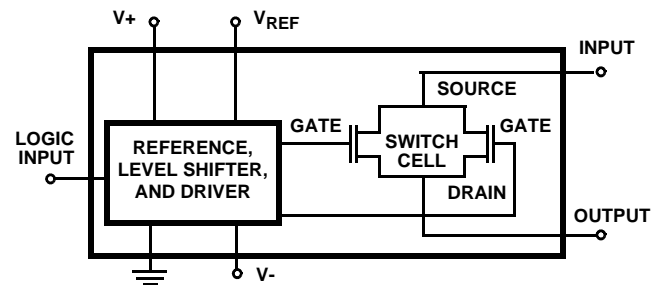
Features

- Pb-Free Available (RoHS Compliant)
- Analog Voltage Range ±15V
- Analog Current Range 80mA
- Turn-On Time 240ns
- Low r_{ON} 55Ω
- Low Power Dissipation 15mW
- TTL/CMOS Compatible

Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks

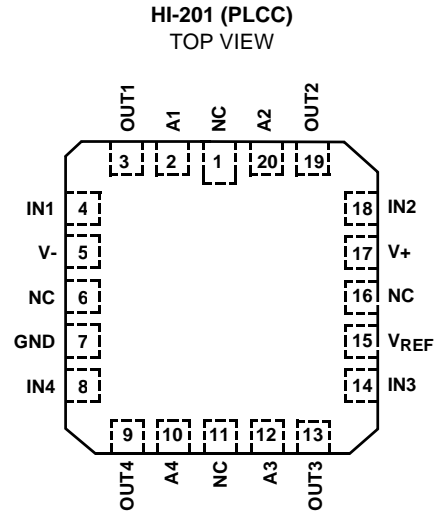
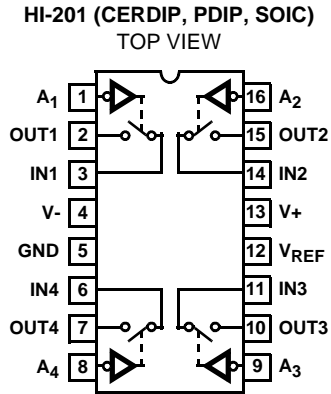
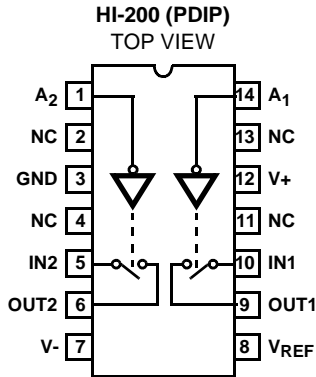
Functional Diagram



TRUTH TABLE

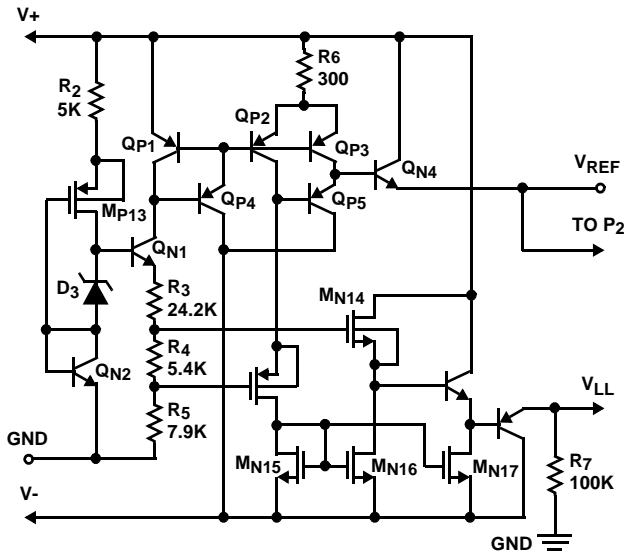
| LOGIC | HI-200 | HI-201 |
|-------|--------|--------|
| 0 | ON | ON |
| 1 | OFF | OFF |

Pinouts (Switches Shown For Logic "1" Input)

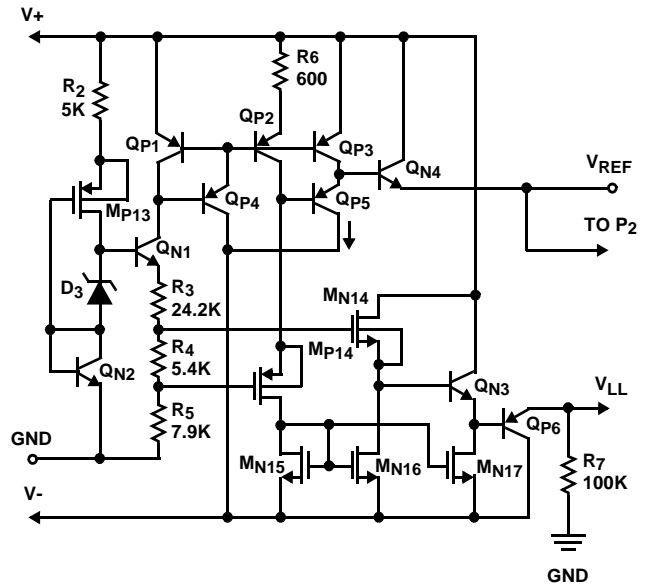


Schematic Diagrams

TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL
HI-200

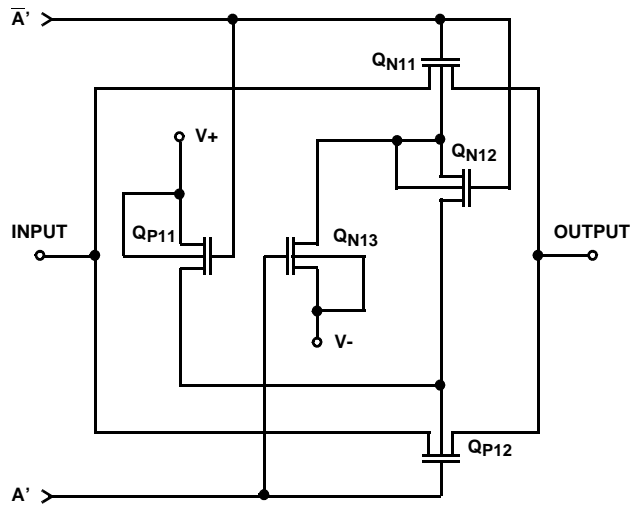


TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL
HI-201

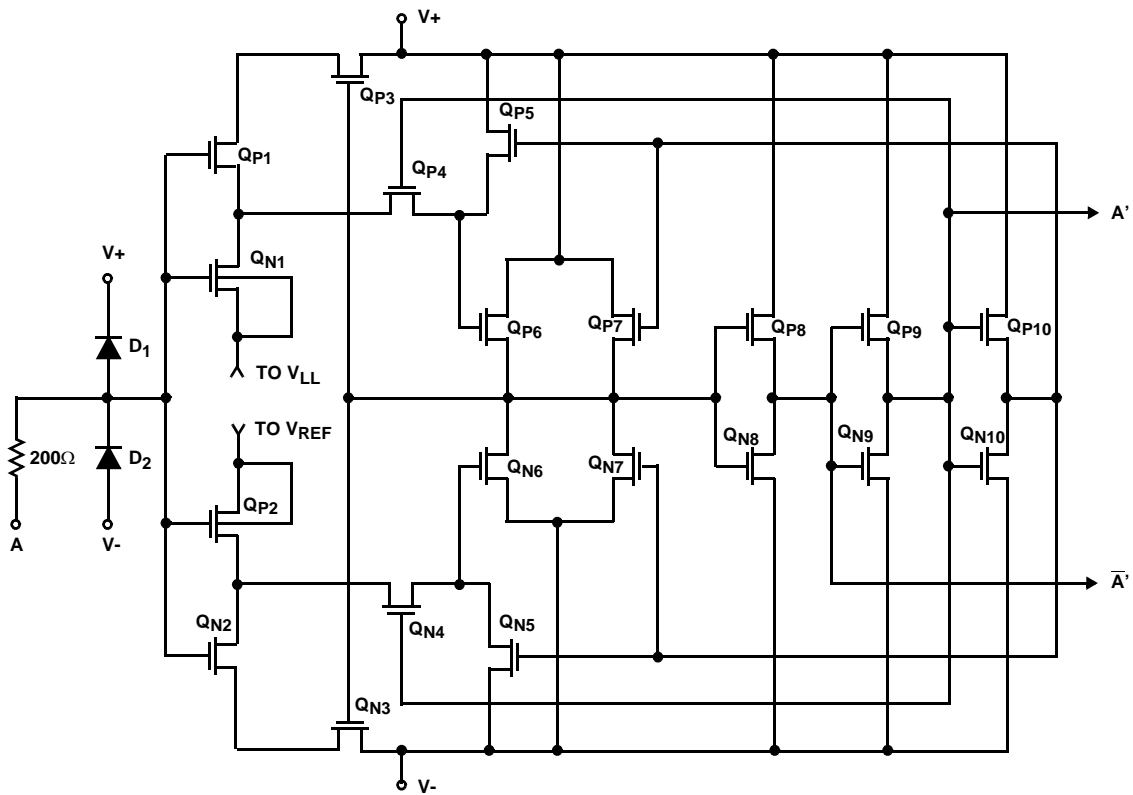


Schematic Diagrams (Continued)

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



HI-200, HI-201

Absolute Maximum Ratings

| | |
|-----------------------------------|----------------------|
| Supply Voltage (V+ to V-) | 44V (±22) |
| V _{REF} to Ground | 20V, -5V |
| Digital Input Voltage | (V+) +4V to (V-) -4V |
| Analog Input Voltage (One Switch) | (V+) +2V to (V-) -2V |

Operating Conditions

| | |
|--------------------|----------------|
| Temperature Ranges | |
| HI-201-2 | -55°C to 125°C |
| HI-201-4 | -25°C to 85°C |
| HI-200-5, HI-201-5 | 0°C to 75°C |
| HI-201-9 | -40°C to 85°C |

Thermal Information

| | | |
|--|---|----------------------|
| Thermal Resistance (Typical, Note 1) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| CERDIP Package | 75 | 20 |
| PLCC Package | 80 | N/A |
| PDIP Package* | 95 | N/A |
| SOIC Package | 110 | N/A |
| Maximum Storage Temperature | -65°C to 150°C | |
| Maximum Junction Temperature (Hermetic Packages) | 175°C | |
| Maximum Junction Temperature (Plastic Packages) | 150°C | |
| Maximum Lead Temperature (Soldering, 10s) | 300°C (PLCC and SOIC - Lead Tips Only) | |

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = 0.8V

| PARAMETER | TEST CONDITIONS | TEMP (°C) | -2 | | | -4, -5, -9 | | | UNITS |
|---|-----------------|-----------|-----|------|-----|------------|------|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| DYNAMIC CHARACTERISTICS | | | | | | | | | |
| Switch ON Time, t _{ON} | | | | | | | | | |
| HI-200 | | 25 | - | 240 | 500 | - | 240 | - | ns |
| HI-201 | | 25 | - | 185 | 500 | - | 185 | - | ns |
| | | Full | - | 1000 | - | - | 1000 | - | ns |
| Switch OFF Time, t _{OFF} | | | | | | | | | |
| HI-200 | | 25 | - | 330 | 500 | - | 500 | - | ns |
| HI-201 | | 25 | - | 220 | 500 | - | 220 | - | ns |
| | | Full | - | 1000 | - | - | 1000 | - | ns |
| Off Isolation | (Note 4) | | | | | | | | |
| HI-200 | | 25 | - | 70 | - | - | 70 | - | dB |
| HI-201 | | 25 | - | 80 | - | - | 80 | - | dB |
| Input Switch Capacitance, C _{S(OFF)} | | 25 | - | 5.5 | - | - | 5.5 | - | pF |
| Output Switch Capacitance, C _{D(OFF)} | | 25 | - | 5.5 | - | - | 5.5 | - | pF |
| Output Switch Capacitance, C _{D(ON)} | | 25 | - | 11 | - | - | 11 | - | pF |
| Digital Input Capacitance, C _A | | 25 | - | 5 | - | - | 5 | - | pF |
| Drain-to-Source Capacitance, C _{DS(OFF)} | | 25 | - | 0.5 | - | - | 0.5 | - | pF |
| DIGITAL INPUT CHARACTERISTICS | | | | | | | | | |
| Input Low Threshold, V _{AL} | | Full | - | - | 0.8 | - | - | 0.8 | V |
| Input High Threshold, V _{AH} | | Full | 2.4 | - | - | 2.4 | - | - | V |
| Input Leakage Current (High or Low), I _A | (Note 3) | Full | - | - | 1.0 | - | - | 1.0 | μA |
| ANALOG SWITCH CHARACTERISTICS | | | | | | | | | |
| Analog Signal Range, V _S | | Full | -15 | - | +15 | -15 | - | +15 | V |
| ON Resistance, r _{ON} | (Note 2) | 25 | - | 55 | 70 | - | 55 | 80 | Ω |
| | | Full | - | 80 | 100 | - | 72 | 100 | Ω |

HI-200, HI-201

Electrical Specifications Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = 0.8V (Continued)

| PARAMETER | TEST CONDITIONS | TEMP (°C) | -2 | | | -4, -5, -9 | | | UNITS |
|---|-----------------|-----------|-----|-----|-----|------------|-----|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| OFF Input Leakage Current, I _{S(OFF)} | (Note 6) | 25 | - | 1 | 5 | - | 1 | 50 | nA |
| | | Full | - | 100 | 500 | - | 10 | 500 | nA |
| | | 25 | - | 2 | 5 | - | 2 | 50 | nA |
| | | Full | - | - | 500 | - | - | 250 | nA |
| OFF Output Leakage Current, I _{D(OFF)} | (Note 6) | 25 | - | 1 | 5 | - | 1 | 50 | nA |
| | | Full | - | 100 | 500 | - | 10 | 500 | nA |
| | | 25 | - | 2 | 5 | - | 2 | 50 | nA |
| | | Full | - | 35 | 500 | - | 35 | 250 | nA |
| ON Leakage Current, I _{D(ON)} | (Note 6) | 25 | - | 1 | 5 | - | 1 | 50 | nA |
| | | Full | - | 100 | 500 | - | 10 | 500 | nA |
| | | 25 | - | 2 | 5 | - | 2 | 50 | nA |
| | | Full | - | - | 500 | - | - | 250 | nA |
| POWER SUPPLY CHARACTERISTICS (Note 5) | | | | | | | | | |
| Power Dissipation, P _D | | 25 | - | 15 | - | - | 15 | - | mW |
| | | Full | - | - | 60 | - | - | 60 | mW |
| Current, I ₊ | | 25 | - | 0.5 | - | - | 0.5 | - | mA |
| | | Full | - | - | 2.0 | - | - | 2.0 | mA |
| Current, I ₋ | | 25 | - | 0.5 | - | - | 0.5 | - | mA |
| | | Full | - | - | 2.0 | - | - | 2.0 | mA |

NOTES:

- V_{OUT} = ±10V, I_{OUT} = 1mA.
- Digital Inputs are MOS gates: typical leakage is < 1nA.
- V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = 3V_{RMS}, f = 100kHz.
- V_A = +3V or V_A = 0V for Both Switches.
- V_A = +3V or V_A = 0V for Both Switches.
- Refer to Leakage Current Measurements (Figure 2).

Test Circuits and Waveforms T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V and V_{REF} = Open

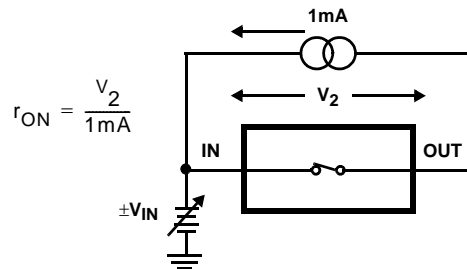


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

Test Circuits and Waveforms $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 2.4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$ and $V_{\text{REF}} = \text{Open}$ (Continued)

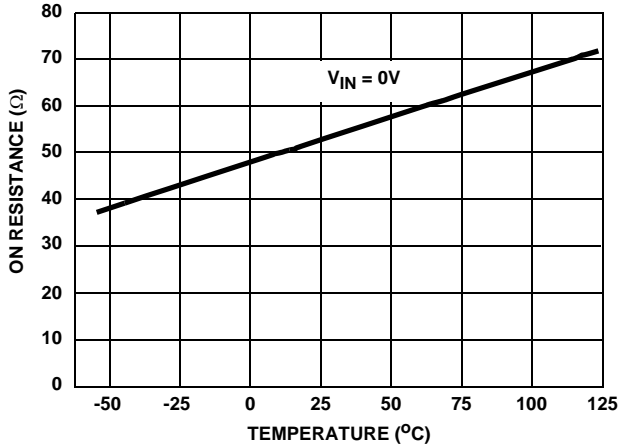


FIGURE 1B. ON RESISTANCE vs TEMPERATURE

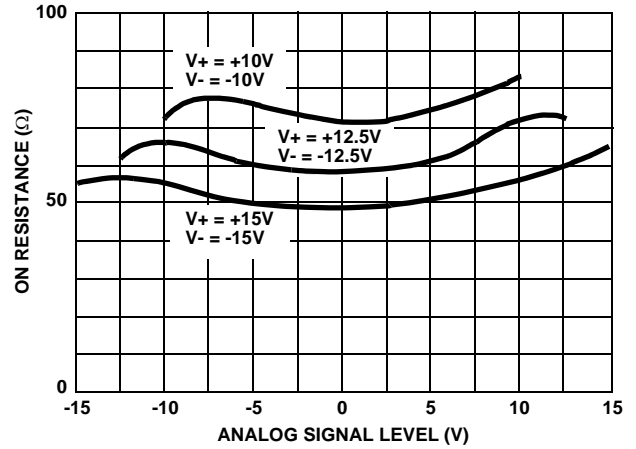


FIGURE 1C. HI-200 ON RESISTANCE vs ANALOG SIGNAL LEVEL

FIGURE 1. ON RESISTANCE

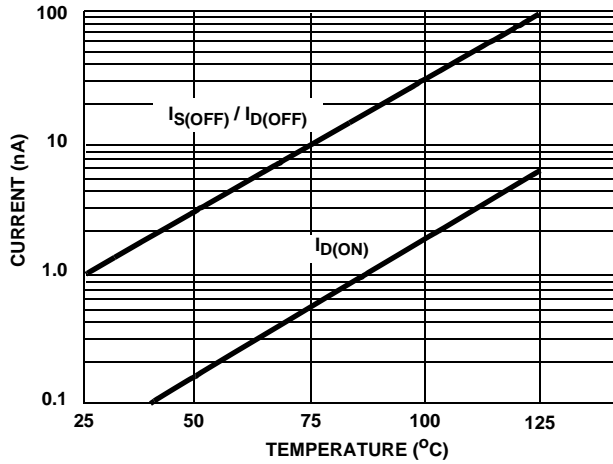


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

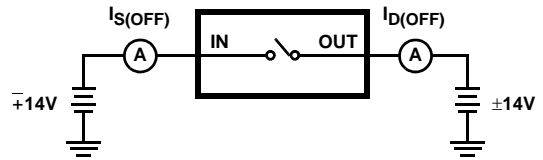


FIGURE 2B. OFF LEAKAGE CURRENT TEST CIRCUIT

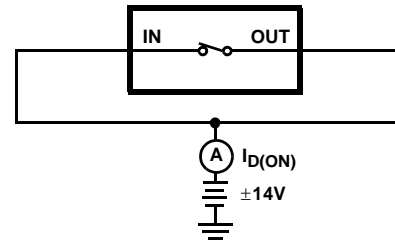


FIGURE 2C. ON LEAKAGE CURRENT TEST CIRCUIT

FIGURE 2. LEAKAGE CURRENTS

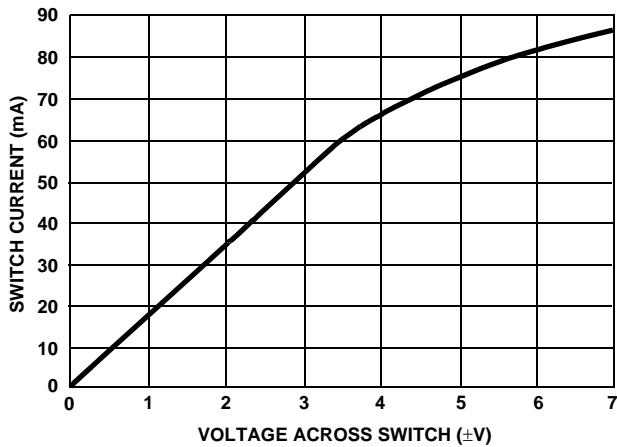


FIGURE 3A. SWITCH CURRENT vs VOLTAGE

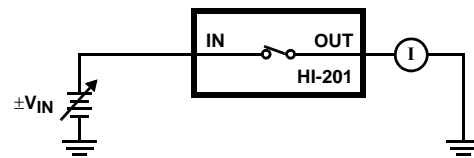


FIGURE 3B. TEST CIRCUIT

FIGURE 3. SWITCH CURRENT

Test Circuits and Waveforms $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 2.4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$ and $V_{\text{REF}} = \text{Open}$ (Continued)

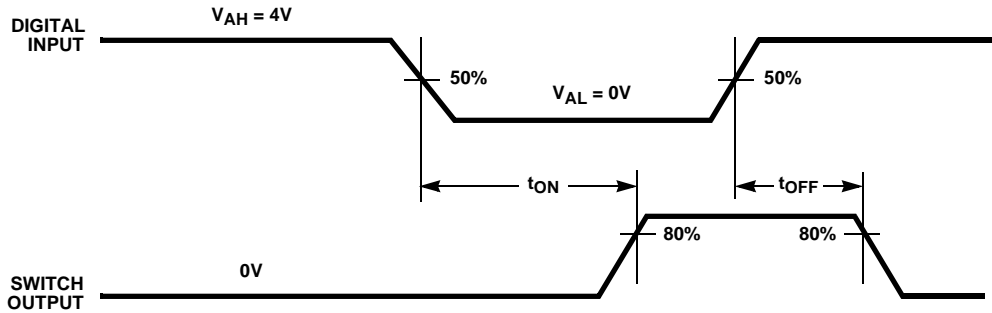


FIGURE 4A. MEASUREMENT POINTS

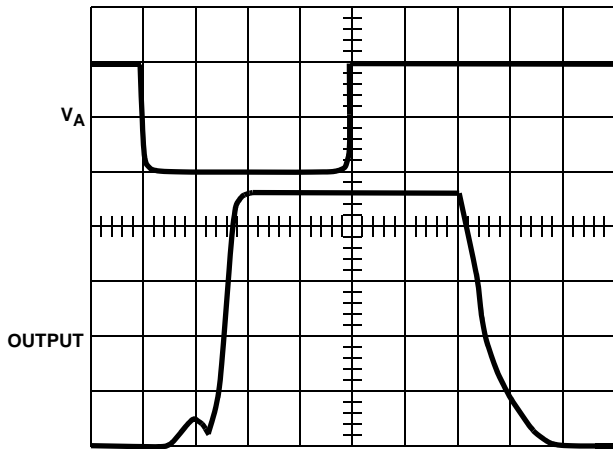


FIGURE 4B. WAVEFORMS WITH TTL COMPATIBLE LOGIC INPUT

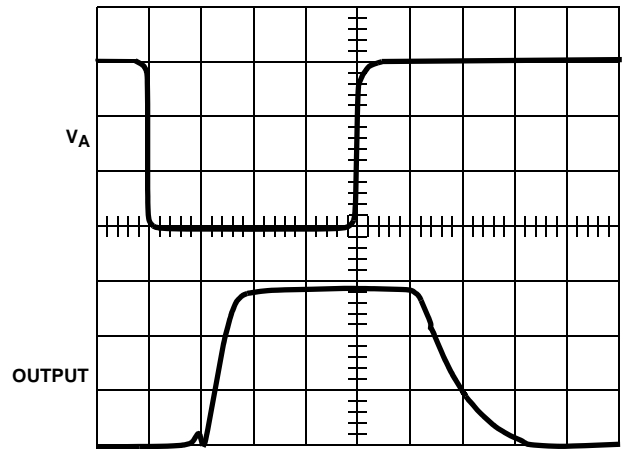


FIGURE 4C. WAVEFORMS WITH CMOS COMPATIBLE LOGIC INPUT

FIGURE 4. SWITCH t_{ON} AND t_{OFF}

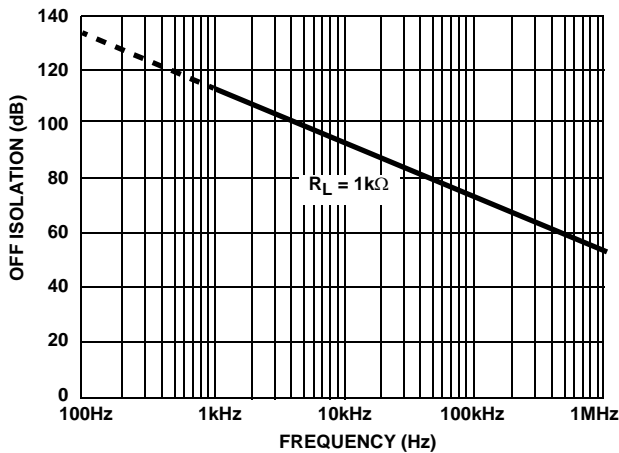


FIGURE 5. HI-201 OFF ISOLATION vs FREQUENCY

For more information see Application Notes AN520, AN521, AN531, AN532 and AN557.

Application Information

Single Supply Operation

The switch operation of the HI-200/201 is dependent upon an internally generated switching threshold voltage optimized for $\pm 15\text{V}$ power supplies. The HI-200/201 does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum $+5\text{V}$ single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels ($\pm 15\text{V}$). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

For further information see Application Notes AN520, AN557, AN1033 and AN1034.

Die Characteristics

METALLIZATION:

Type: CuAl
 Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

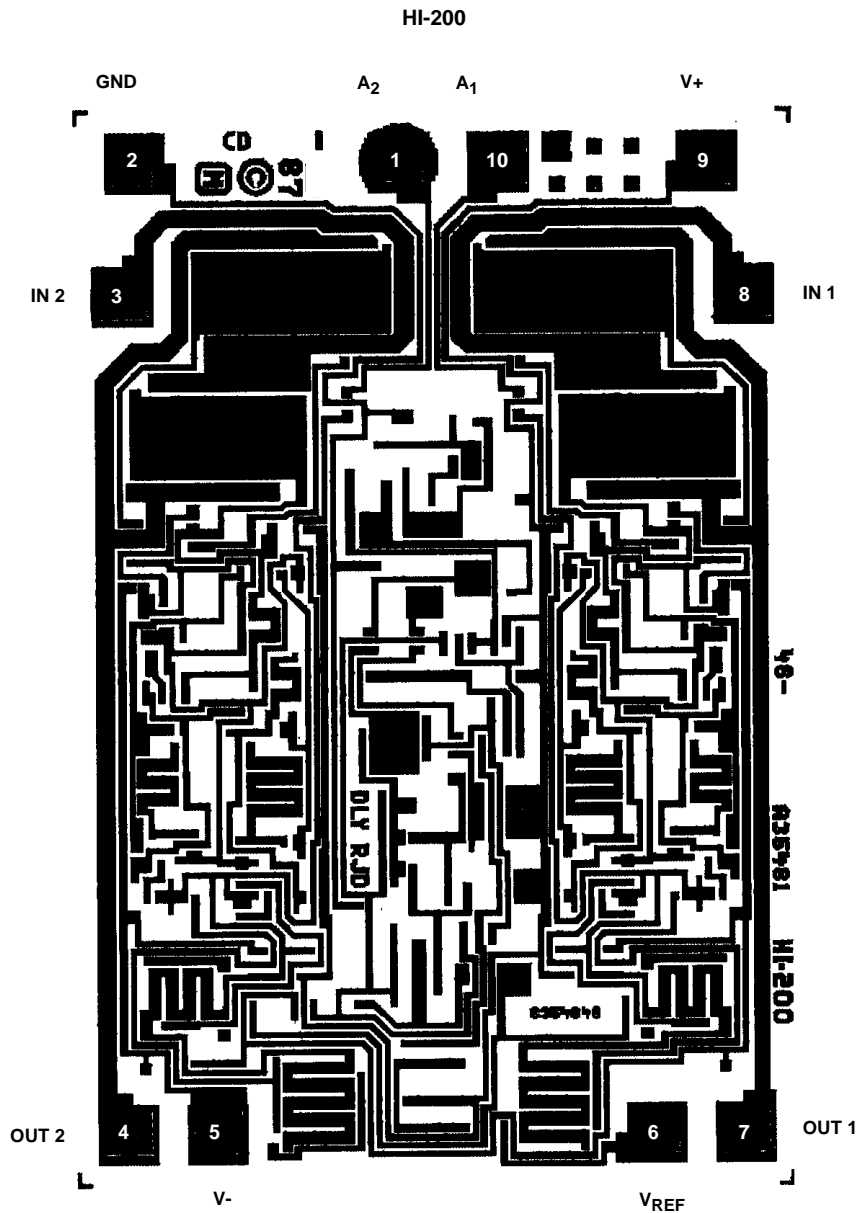
PASSIVATION:

Type: Nitride over Silox
 Nitride Thickness: $3.5\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$
 Silox Thickness: $12\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

$2 \times 10^5 \text{ A/cm}^2$ at 25mA

Metallization Mask Layout



Die Characteristics

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Type: CuAl
 Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

PASSIVATION:

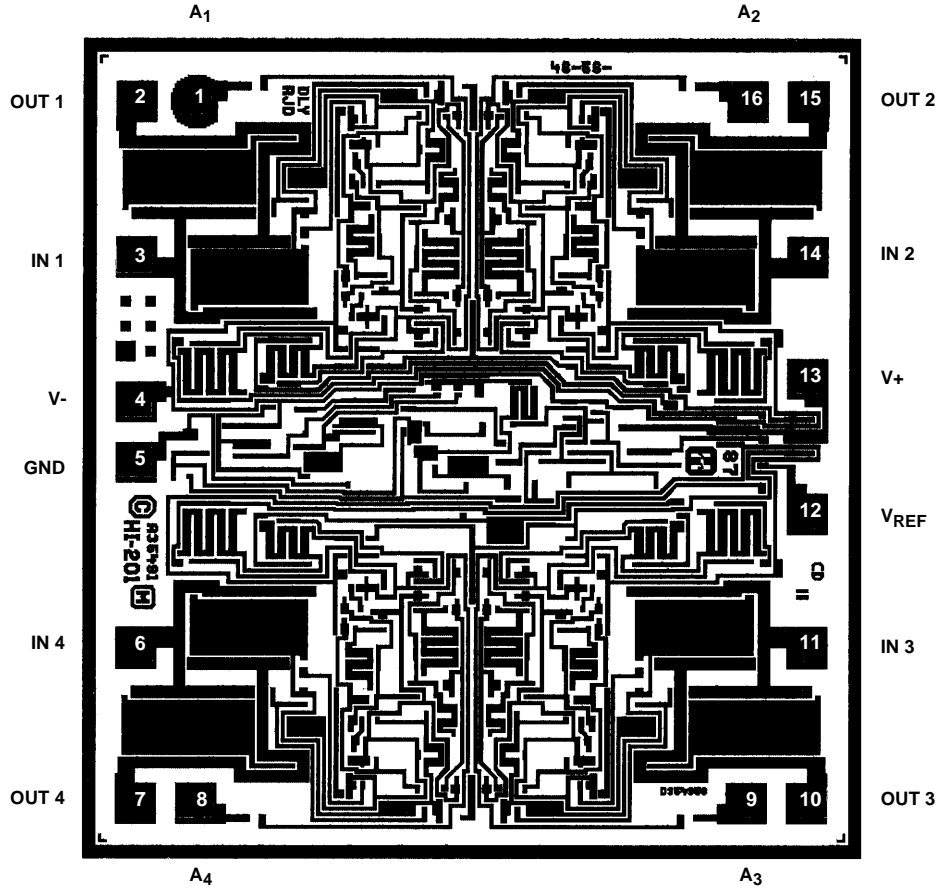
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WORST CASE CURRENT DENSITY:

$2 \times 10^5 \text{ A/cm}^2$ at 25mA

Metallization Mask Layout

HI-201



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