International
IOR Rectifier

Preliminary Data Sheet No. PD-6.045-H

# IR2103

## HIGH AND LOW SIDE DRIVER

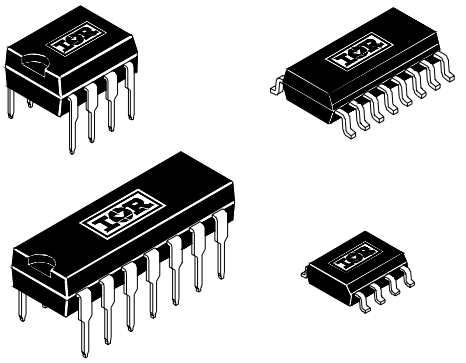
### Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High side output in phase with HIN input
- Low side output out of phase with $\overline{\text{LIN}}$ input

### Product Summary

| | |
|---|---|
| $V_{OFFSET}$ | 600V max. |
| $I_O$+/- | 100 mA / 210 mA |
| $V_{OUT}$ | 10 - 20V |
| $t_{on/off}$ (typ.) | 600 & 90 ns |
| Deadtime (typ.) | 500 ns |

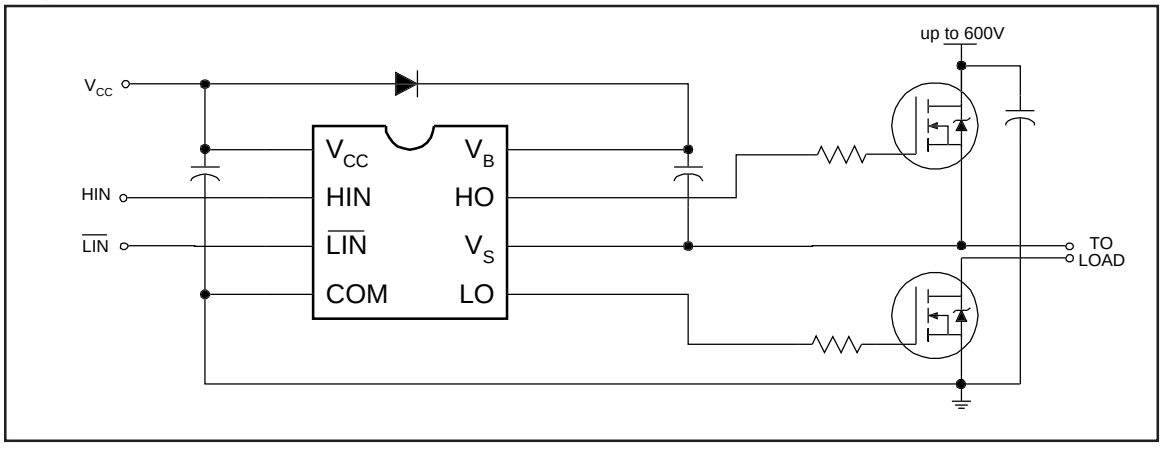
### Packages



### Description

The IR2103 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

### Typical Connection



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Parameter | | Value | | |
|---|---|---|---|---|
| Symbol | Definition | Min. | Max. | Units |
| $V_B$ | High Side Floating Absolute Voltage | -0.3 | 625 | V |
| $V_S$ | High Side Floating Supply Offset Voltage | $V_B$ - 25 | $V_B$ + 0.3 | |
| $V_{HO}$ | High Side Floating Output Voltage | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{CC}$ | Low Side and Logic Fixed Supply Voltage | -0.3 | 25 | |
| $V_{LO}$ | Low Side Output Voltage | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{IN}$ | Logic Input Voltage (HIN & $\overline{LIN}$) | -0.3 | $V_{CC}$ + 0.3 | |
| $dV_S/dt$ | Allowable Offset Supply Voltage Transient | — | 50 | V/ns |
| $P_D$ | Package Power Dissipation @ $T_A \leq +25°C$ (8 Lead DIP) | — | 1.0 | W |
| | (8 Lead SOIC) | — | 0.625 | |
| $Rth_{JA}$ | Thermal Resistance, Junction to Ambient (8 Lead DIP) | — | 125 | °C/W |
| | (8 Lead SOIC) | — | 200 | |
| $T_J$ | Junction Temperature | — | 150 | °C |
| $T_S$ | Storage Temperature | -55 | 150 | |
| $T_L$ | Lead Temperature (Soldering, 10 seconds) | — | 300 | |

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The $V_S$ offset rating is tested with all supplies biased at 15V differential.

| Parameter | | Value | | |
|---|---|---|---|---|
| Symbol | Definition | Min. | Max. | Units |
| $V_B$ | High Side Floating Supply Absolute Voltage | $V_S$ + 10 | $V_S$ + 20 | V |
| $V_S$ | High Side Floating Supply Offset Voltage | Note 1 | 600 | |
| $V_{HO}$ | High Side Floating Output Voltage | $V_S$ | $V_B$ | |
| $V_{CC}$ | Low Side and Logic Fixed Supply Voltage | 10 | 20 | |
| $V_{LO}$ | Low Side Output Voltage | 0 | $V_{CC}$ | |
| $V_{IN}$ | Logic Input Voltage (HIN & $\overline{LIN}$) | 0 | $V_{CC}$ | |
| $T_A$ | Ambient Temperature | -40 | 125 | °C |

Note 1: Logic operational for $V_S$ of -5 to +600V. Logic state held for $V_S$ of -5V to $-V_{BS}$.

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, $C_L$ = 1000 pF and $T_A$ = 25°C unless otherwise specified.

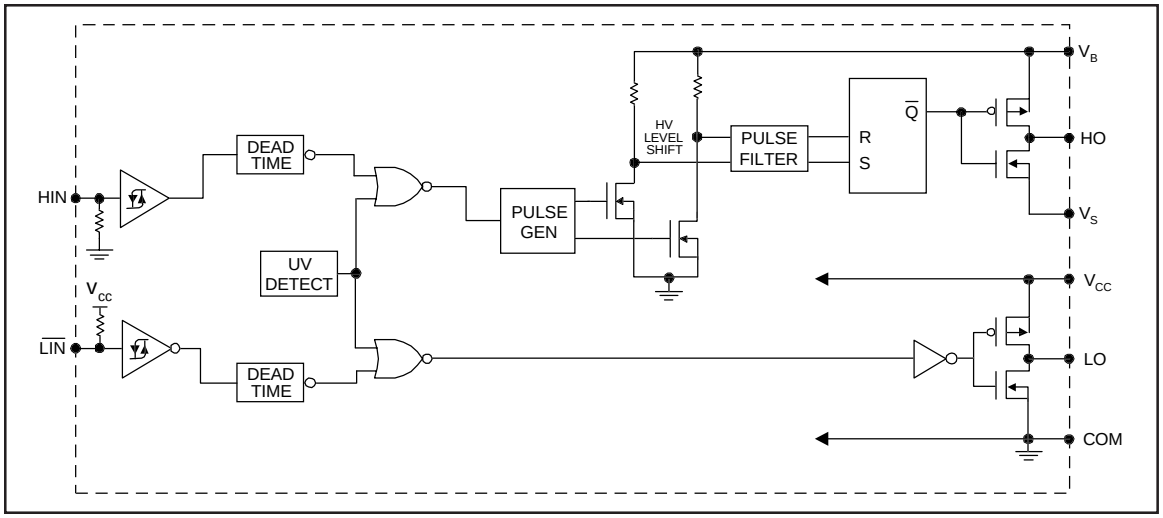
| Symbol | Parameter Definition | Value Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-On Propagation Delay | — | 600 | 720 | ns | $V_S$ = 0V |
| $t_{off}$ | Turn-Off Propagation Delay | — | 90 | 200 | | $V_S$ = 600V |
| $t_r$ | Turn-On Rise Time | — | 100 | 150 | | |
| $t_f$ | Turn-Off Fall Time | — | 50 | 80 | | |
| DT | Deadtime, LS Turn-Off to HS Turn-On & HS Turn-On to LS Turn-Off | — | 500 | 750 | | |
| MT | Delay Matching, HS & LS Turn-On/Off | — | 30 | — | | |

## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V and $T_A$ = 25°C unless otherwise specified. The $V_{IN}$, $V_{TH}$ and $I_{IN}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Parameter Definition | Value Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic “1” Input Voltage for HIN & Logic “0” for $\overline{LIN}$ | 2.7 | — | — | V | $V_{CC}$ = 10V to 20V |
| $V_{IL}$ | Logic “0” Input Voltage for HIN & Logic “1” for $\overline{LIN}$ | — | — | 0.8 | | $V_{CC}$ = 10V to 20V |
| $V_{OH}$ | High Level Output Voltage, $V_{BIAS}$ - $V_O$ | — | — | 100 | mV | $I_O$ = 0A |
| $V_{OL}$ | Low Level Output Voltage, $V_O$ | — | — | 100 | | $I_O$ = 0A |
| $I_{LK}$ | Offset Supply Leakage Current | — | — | 50 | µA | $V_B$ = $V_S$ = 600V |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | — | 20 | 50 | | $V_{IN}$ = 0V or 5V |
| $I_{QCC}$ | Quiescent $V_{CC}$ Supply Current | — | 140 | 240 | | $V_{IN}$ = 0V or 5V |
| $I_{IN+}$ | Logic “1” Input Bias Current | — | 20 | 40 | | HIN = 5V, $\overline{LIN}$ = 0V |
| $I_{IN-}$ | Logic “0” Input Bias Current | — | — | 1.0 | | HIN = 0V, $\overline{LIN}$ = 5V |
| $V_{CCUV+}$ | $V_{CC}$ Supply Undervoltage Positive Going Threshold | 8.3 | 8.9 | 9.5 | V | |
| $V_{CCUV-}$ | $V_{CC}$ Supply Undervoltage Negative Going Threshold | 7.5 | 8.2 | 8.6 | | |
| $I_{O+}$ | Output High Short Circuit Pulsed Current | 100 | 125 | — | mA | $V_O$ = 0V, $V_{IN}$ = $V_{IH}$ PW ≤ 10 µs |
| $I_{O-}$ | Output Low Short Circuit Pulsed Current | 210 | 250 | — | | $V_O$ = 15V, $V_{IN}$ = $V_{IL}$ PW ≤ 10 µs |

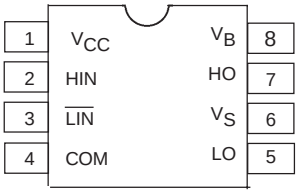
## Functional Block Diagram



## Lead Definitions

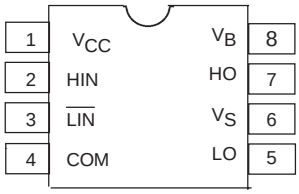
| Lead Symbol | Description |
|---|---|
| HIN | Logic input for high side gate driver output (HO), in phase |
| $\overline{\text{LIN}}$ | Logic input for low side gate driver output (LO), out of phase |
| $V_B$ | High side floating supply |
| HO | High side gate drive output |
| $V_S$ | High side floating supply return |
| $V_{CC}$ | Low side and logic fixed supply |
| LO | Low side gate drive output |
| COM | Low side return |

## Lead Assignments



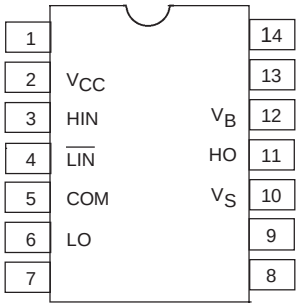

8 Lead DIP

**IR2103**



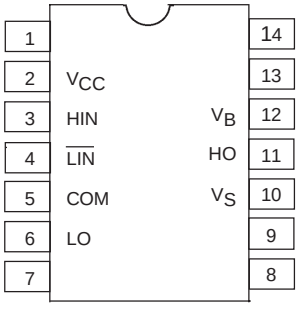

8 Lead SOIC

**IR2103S**




14 Lead DIP

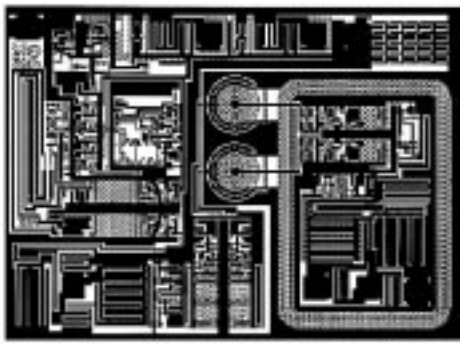
**IR2103P1**

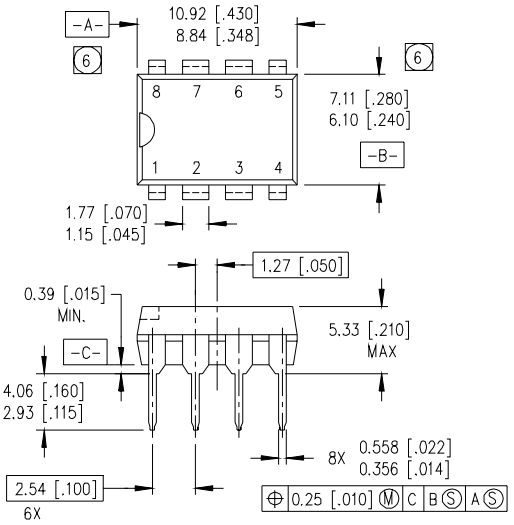



14 Lead SOIC

**IR2103S1**

## Device Information

| | | |
|---|---|---|
| Process & Design Rule | | HVDCMOS 4.0 µm |
| Transistor Count | | 168 |
| Die Size | | 67 X 91 X 26 (mil) |
| Die Outline | |  |
| Thickness of Gate Oxide | | 800Å |
| Connections | Material | Poly Silicon |
| First Layer | Width | 4 µm |
| | Spacing | 6 µm |
| | Thickness | 5000Å |
| | Material | Al - Si (Si: 1.0% ±0.1%) |
| Second Layer | Width | 6 µm |
| | Spacing | 9 µm |
| | Thickness | 20,000Å |
| Contact Hole Dimension | | 5 µm X 5 µm |
| Insulation Layer | Material | PSG ($SiO_2$) |
| | Thickness | 1.5 µm |
| Passivation | Material | PSG ($SiO_2$) |
| | Thickness | 1.5 µm |
| Method of Saw | | Full Cut |
| Method of Die Bond | | Ablebond 84 - 1 |
| Wire Bond | Method | Thermo Sonic |
| | Material | Au (1.0 mil / 1.3 mil) |
| Leadframe | Material | Cu |
| | Die Area | Ag |
| | Lead Plating | Pb : Sn (37 : 63) |
| Package | Types | 8 Lead PDIP / SO-8 |
| | Materials | EME6300 / MP150 / MP190 |
| Remarks: | | |

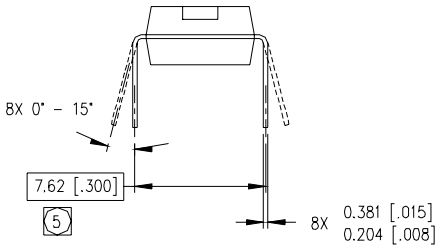



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.

(5) MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

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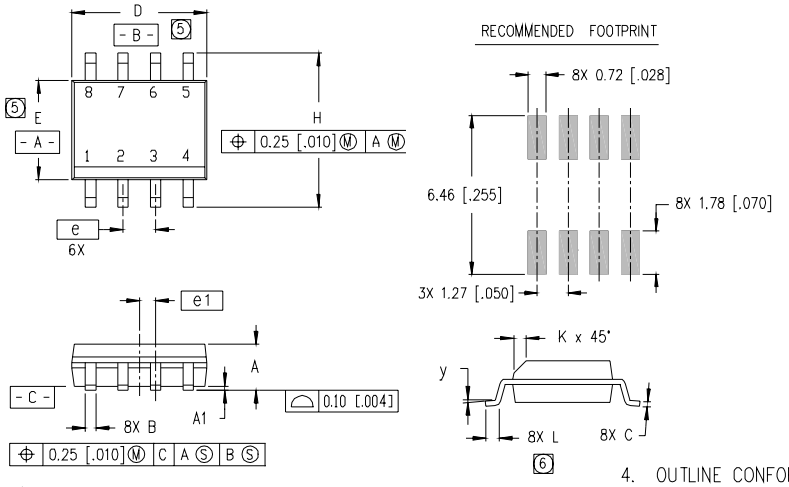
## 8 Lead PDIP




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| B | .014 | .018 | 0.36 | 0.46 |
| C | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .196 | 4.80 | 4.98 |
| E | .150 | .157 | 3.81 | 3.99 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .011 | .019 | 0.28 | 0.48 |
| L | .016 | .050 | 0.41 | 1.27 |
| y | 0° | 8° | 0° | 8° |

NOTES:

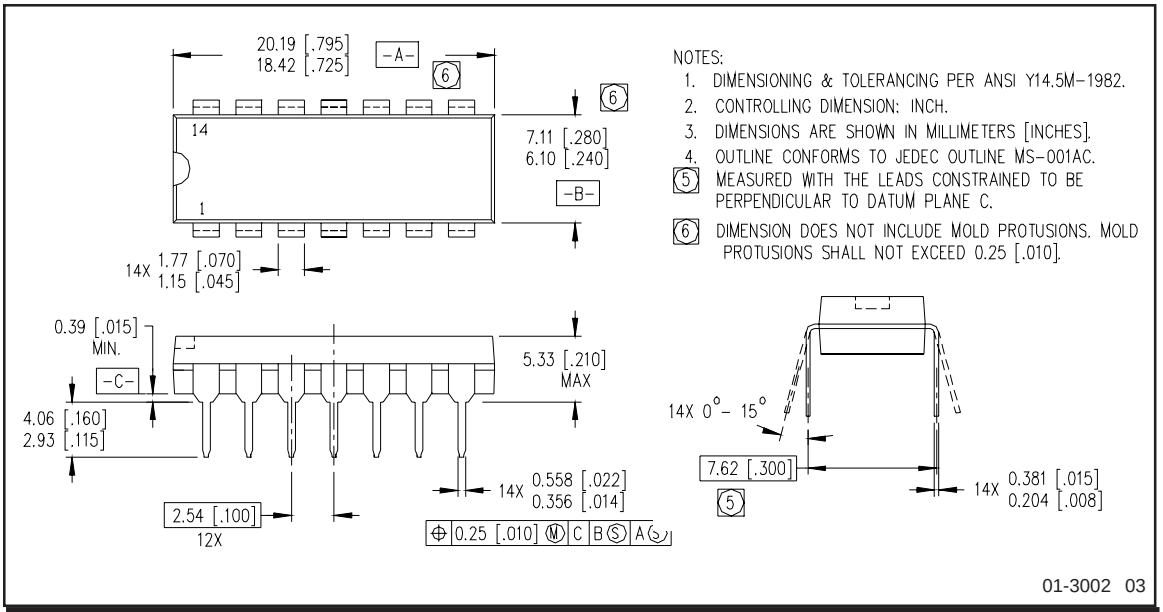
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.

(5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].

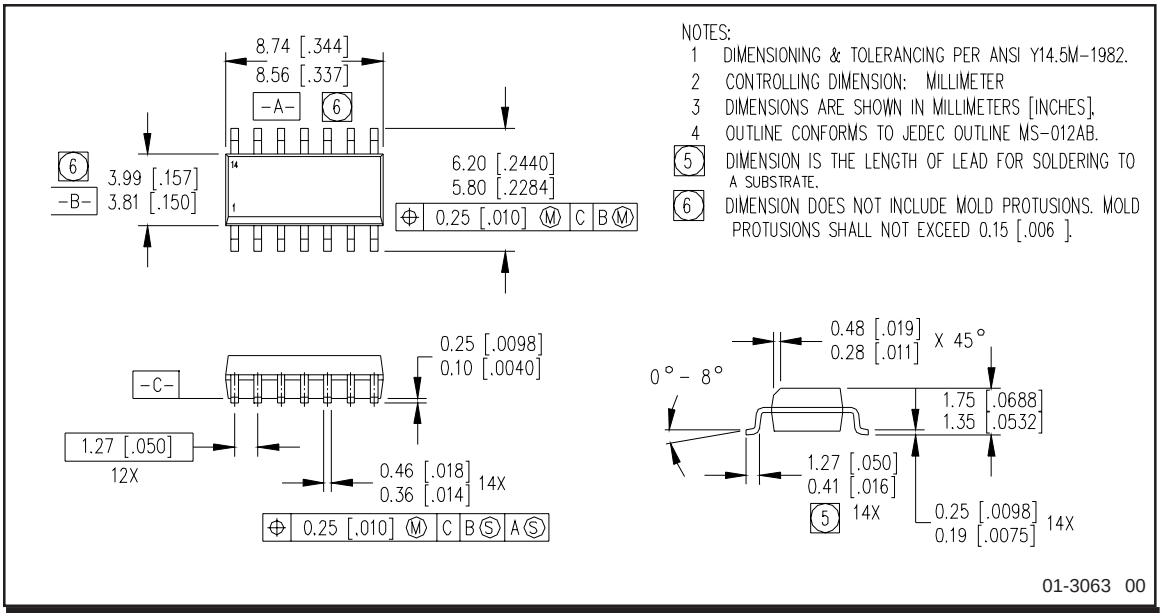
(6) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-0021 08

## 8 Lead SOIC




## 14 Lead PDIP




## 14 Lead SOIC (narrow body)

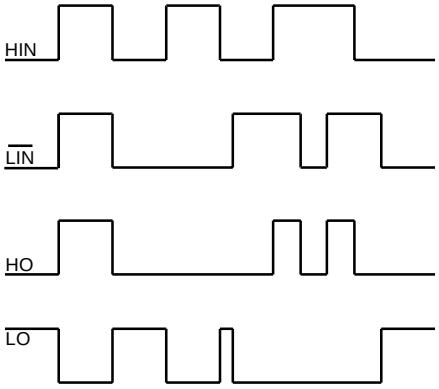



**Figure 1. Input/Output Timing Diagram**

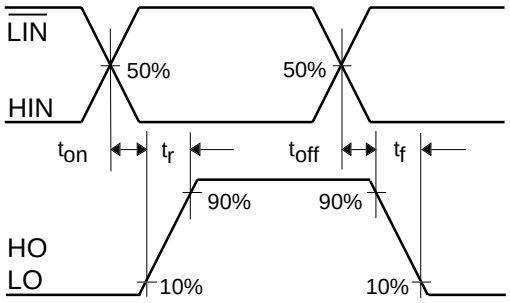



**Figure 2. Switching Time Waveform Definitions**

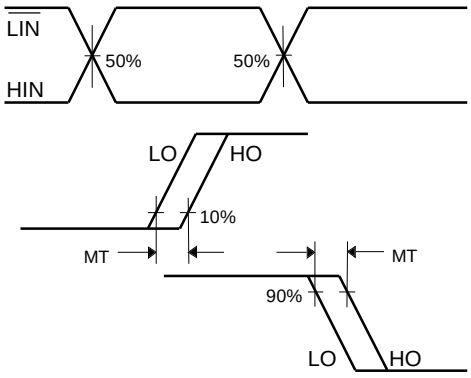



**Figure 3. Delay Matching Waveform Definitions**

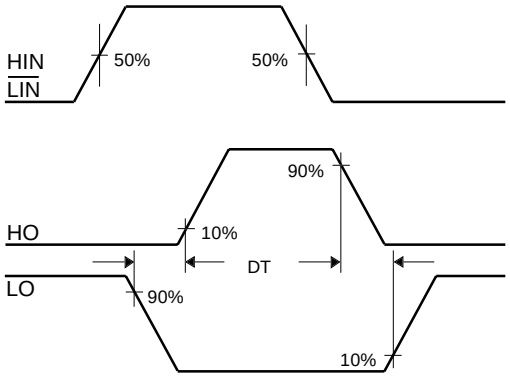



**Figure 4. Deadtime Waveform Definitions**

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**WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
**EUROPEAN HEADQUARTERS:** Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
**IR CANADA:** 15 Lincoln Court, Brampton, Ontario L6T 3Z2 , Tel: (905) 453-2200
**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
**IR FAR EAST:** 171 (K&H Bldg.), 30-4 Nishi-ikebukuro 3-Chome, Toshima-ku, Tokyo Japan Tel: 81 3 3983 0086
**IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371
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