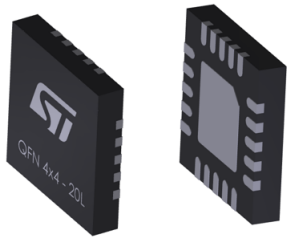
TCPP03-M20

Datasheet

USB-C protection for dual role power (DRP)



QFN-20L 4.0 x 4.0 x 0.75 mm

Product labels

SUSTAINABLE TECHNOLOGY

LONGEVITY 10 YEARS COMMITMENT

Features

- Externally programmable VBUS OVP (over voltage protection) and OCP (over current protection) for provider and consumer power paths with fast turn-off
- Two integrated N-MOSFETs gate drivers for VBUS OVP and OCP
- Very low power in “unattached” state during DRP toggling: 3 µA max. at 125 °C
- Compliant with PPS (programmable power supply) for fast charging, up to 100 W
- Integrated discharge on VBUS and VCONN
- Current sense on VBUS with analog output
- ESD protection for CC1, CC2, compliant with IEC 61000-4-2 Level 4 (±8 kV contact discharge, ±15 kV air discharge)
- V_{CONN} OCP (100 mW max), OVP (6 V max)
- Over voltage protection on CC lines against short-to-V_{BUS}
- Over temperature protection (150 °C typ.)
- Integrated “Dead Battery” management
- I^2C communication, with two I^2C addresses available
- Junction temperature from -40 °C to 125 °C
- Compliant with USB-C power delivery standard 3.1, standard power range (SPR), up to 100 W
- ECOPACK2 compliant

Product status link	
TCPP03-M20	
Order code	TCPP03-M20

Expansion board
X-NUCLEO-DRP1M1

SW expansion for STM32Cube
X-CUBE-TCPP

STM32-UCPD companion chips(1)
STM32G0, STM32G4, STM32L5, STM32U5

1. *Any MCU with USB-C PD SW stack*

I2C address
0110 10x (LSB = ‘x’)

Applications

- USB type-C power delivery used in dual role power (DRP) or dual role data (DRD) configuration
- USB type-C used in Sink configuration requiring current sense on V_{BUS}
- USB type-C sourcing devices

Description

The TCPP03-M20 is an MCU companion chip enabling cost-effective USB-C power delivery dual role power implementation. It provides protections and functionalities to safely comply with the USB-C Power Delivery specification.

TCPP03-M20 drives external N-MOSFETs on VBUS connector pin in the source and sink power path for over voltage and over current protection. It provides an analog current sense output accessible for an MCU ADC, thus minimizing system cost.

The TCPP03-M20 features 24 V tolerant ESD protection as per IEC61000-4-2 level 4 on USB type-C connector communication channel pins (CC). The TCPP03-M20 provides overvoltage protection on CC1 and CC2 pins when these pins are subjected to short circuit with the VBUS pin that may happen when removing the USB type-C cable from its receptacle.

TCPP03-M20 helps to minimize power consumption during DRP toggling states thanks to its three programmable power modes allowing a power consumption as low as 3 µA maximum, up to 125 °C and thanks to enable pin that wake up the MCU.

1 Pinout and functions

Figure 1. **QFN-20L 4.0 x 4.0 x 0.75 mm (top view)**

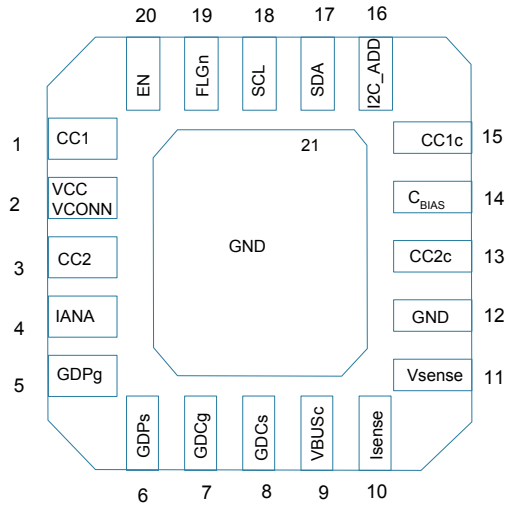


Table 1. **Pinout and functions**

Name	Pin #	Type	Description
CC1	1	Input / Output	Configuration channel 1 pin on power delivery controller side.
VCC_VCONN	2	Power	Power supply for V_{CONN} power pin. Connect to 3.3 V or 5.5 V.
CC2	3	Input / Output	Configuration channel 2 pin on power delivery controller side.
I_{ANA}	4	Output	V_{BUS} current analog measurement.
GDPg	5	Output	Gate driver provider: gate pin of external N-channel MOSFET on source path.
GDPs	6	Input	Gate driver provider: source pin of external N-channel MOSFET on source path.
GDCg	7	Output	Gate driver consumer: gate pin of external N-channel MOSFET on sink path.
GDCs	8	Input	Gate driver consumer: source pin of external N-channel MOSFET on sink path.
VBUSc	9	Input	VBUS connector side.
I_{sense}	10	Input	VBUS current measurement.
V_{sense}	11	Input	VBUS voltage measurement.
GND	12	GND	Ground.
CC2c	13	Input / Output	Configuration channel 2 pin on USB-C connector side.
C_{BIAS}	14	Output	ESD capacitor
CC1c	15	Input / Output	Configuration channel 1 pin on USB-C connector side.
I2C_ADD	16	Input	Least significant bit on I2C address. Connected to GND or 1.8 V / 3.3 V.
SDA	17	Input / Output	Serial data line on I2C bus
SCL	18	Input / Output	Serial clock line on I2C bus
FLGn	19	Output	Open-drain output flag (active low). Floating when not connected.
EN	20	Input	Enable pin.
GND	EP	GND	Ground exposed pad.

2 Block diagram

Figure 2. **Functional block diagram**

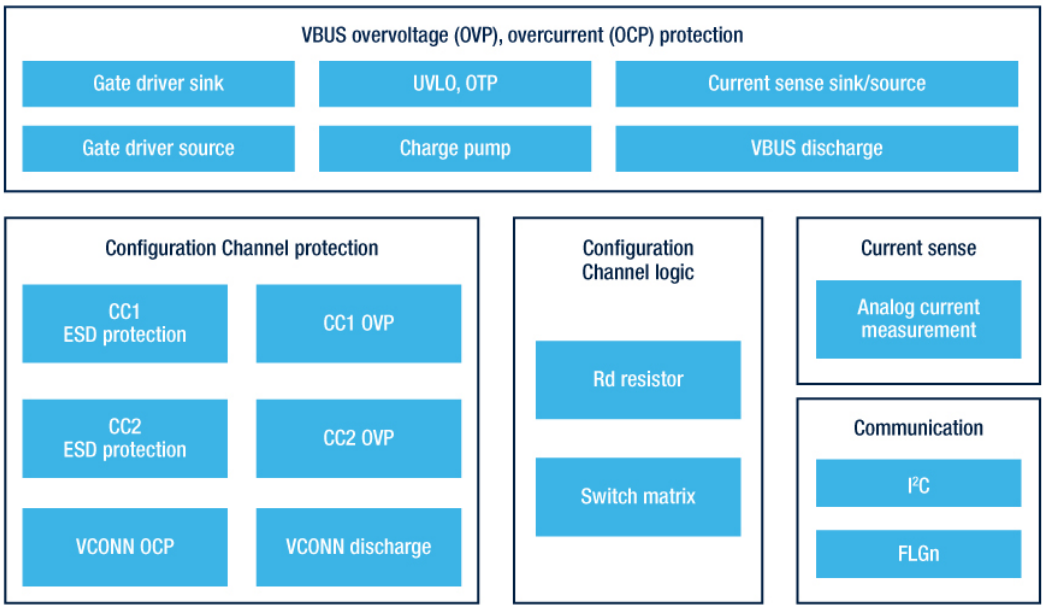
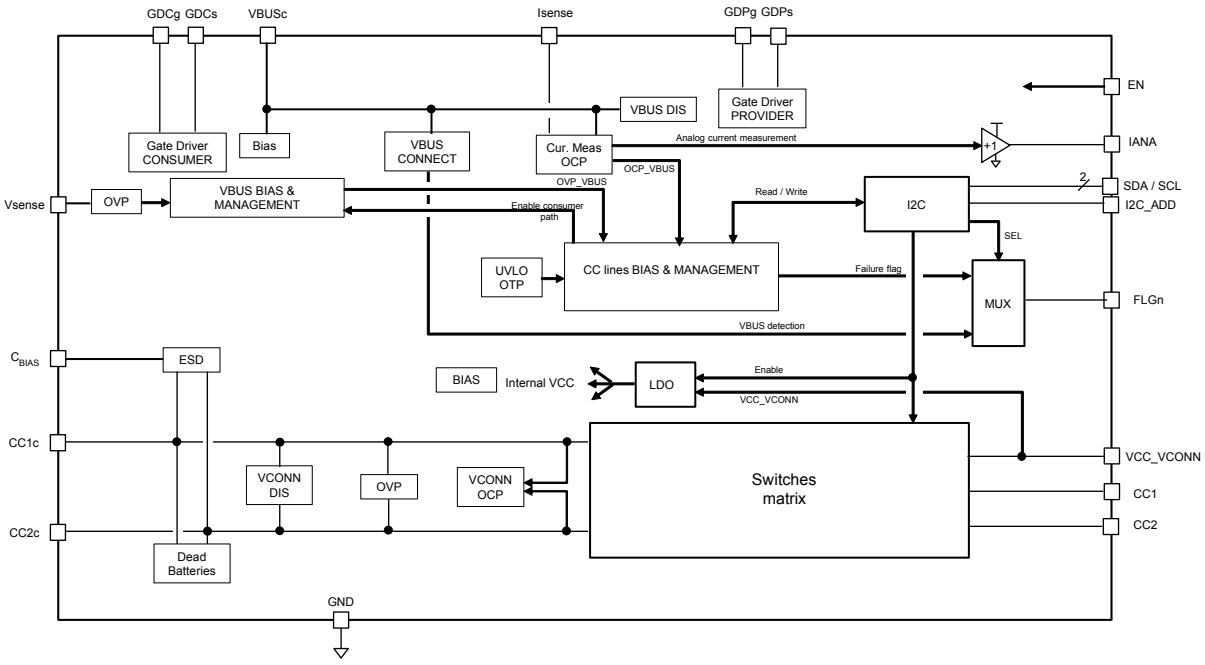
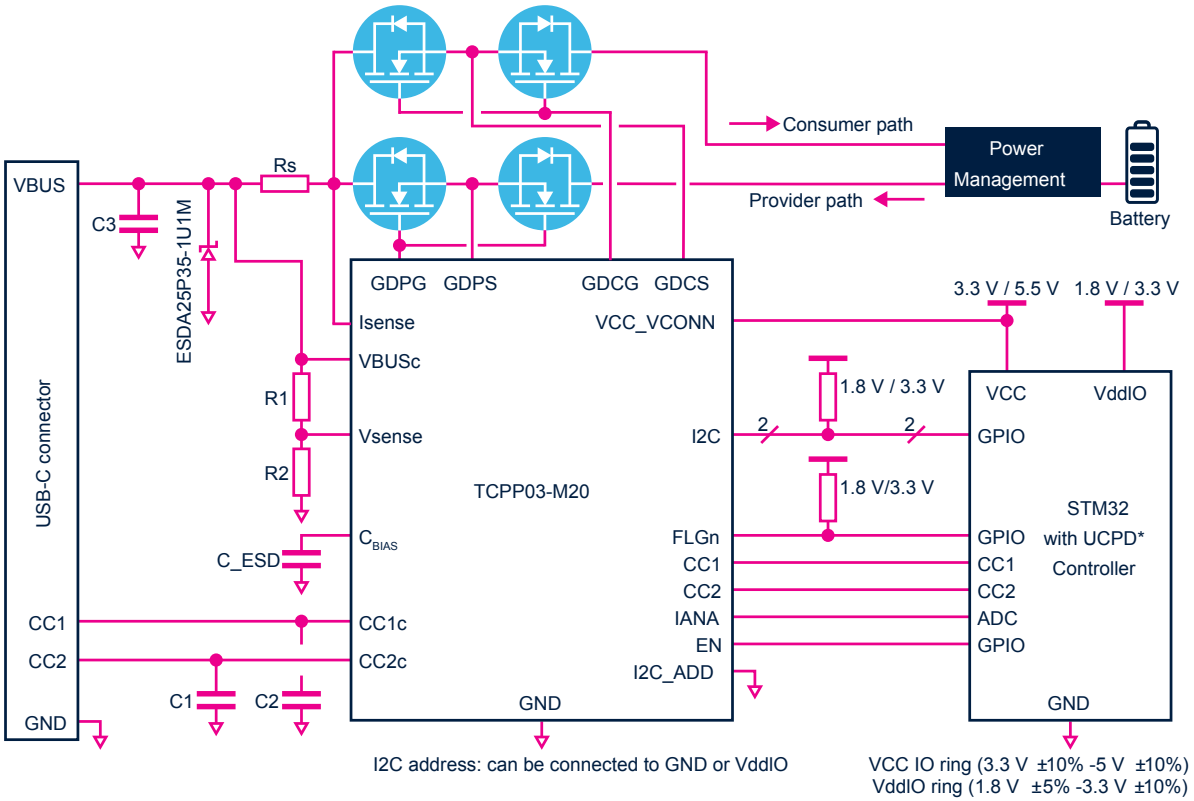


Figure 3. **Internal block diagram**



3 Typical USB-C DRP, DRD application block diagram

Figure 4. Application block diagram example



Note: * UCPD stands for USB Type-C and Power Delivery

Note: UCPD stands for USB type-C and power delivery interface.

External components are described in Section 8.1 External components description.

Please refer to TA0357 for an overview of USB type-C and power delivery technologies.

Please refer to AN5225 for more informations related to USB type-C power delivery using STM32xx Series MCUs and STM32xxx series MPUs.

For more information on EMI filtering and ESD protection of USB datalines, please refer to AN4871: USB type-C protection and filtering.

4 Electrical specification

4.1 Parameter conditions

Unless otherwise specified:

- All voltages are referenced to GND
- The minimum and maximum values are guaranteed in the worst conditions of operating temperature, supply voltage and frequencies, by tests in production on 100 % of the devices
- Typical values are given only as design guidelines and are not tested
- All typical curves are given only as design guidelines and are not tested

4.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings (across junction temperature range)

Symbol	Parameter	Pin name	Value	Unit
V_{POWER}	Voltage for power pins	VCC_VCONN	7	V_{DC}
V_{IN}	Voltage for input pins	EN, V_{sense}, I2C_ADD	7	V_{DC}
		VBUSc, I_{sense}, GDPs, GDCs	24	
V_{OUT}	Voltage for output pins	I_{ANA}, FLGn	7	V_{DC}
		C_{BIAS}, GDPg, GDCg	24	
$V_{I/O}$	Voltage for input, output pins	SDA,SCL, CC1,CC2	7	V_{DC}
		CC1c,CC2c	24	
R_{thj-a}	Junction to ambient thermal resistance		150	°C/W
T_J	Junction temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C

Table 3. ESD ratings (across junction temperature range)

Symbol	Description	Pins	Value	Unit
V_{ESD_c}	System level ESD robustness on USB Type-C connector side(1) IEC61000-4-2 Level 4, contact discharge IEC61000-4-2 Level 4, air discharge	CC1c, CC2c	 8 15	kV
V_{HBM}	V_{ESD} ratings human body model (JESD22-A114D, level 2)	All pins	2	kV

1. *Internal ESD protection functionality is associated with external capacitor connected on pin C_{BIAS}.*

Note: for more information on IEC61000-4-2 standard testing, please refer to AN3353.

4.3 Recommended operating conditions

Table 4. Recommended operating condition, across junction temperature range

Pin name	Min.	Typ.	Max.	Unit
VCC_VCONN, CC1, CC2, V_{SENSE}	2.7		5.5	V
EN, I_{ANA}, I2C_ADD, SDA, SCL, FLGn	1.7		3.6	V
CC1c, CC2c, VBUSc, I_{SENSE}, GDPs, GDCs	0		22	V

4.4 Power supply (VCC_VCONN, VBUSc)

Table 5. Electrical characteristics – Power supply (VCC_VCONN, VBUSc) across T_j

Symbol	Parameter	Test condition across T_{OP}	Value			Unit
			Min.	Typ.	Max.	
ICC_VCONN	V_{cc} supply current	Normal mode		-	2.7	mA
		Low power mode		-	1	µA
I_{enable}	Supply current of EN pin	Low power mode 1,7 V-2,7 V		-	3	µA
		Low power mode 2,7 V-3,6 V		-	10	µA
I_{L_VBUSc}	VBUSc Supply current	V_{BUSc} = 22 V		-	2	mA
		V_{BUSc} = 5 V		-	0.7	
T_{DIS_VBUSc}	VBUSc discharge time			-	220	ms

4.5 VBUS OVP, OCP

Table 6. Electrical characteristics for V_{BUS} (OVP, OCP, gate driver, current monitoring) across T_j

Symbol	Parameter	Test condition across T_{OP}	Value			Unit
			Min.	Typ.	Max.	
VBUS_UVLO	VBUS under voltage lock out		1.9	2.4	2.9	V
V_{GS}	Gate to source voltage consumer VBUSc = 5 V - 20 V		4.5	5	5.5	V
V_{OVP_TH}	OVP V_{BUS} threshold voltage	Vsense pin voltage	1.1	1.16	1.25	V
$T_{OVP\_ON\_VBUS}$	OVP V_{BUS} turn-on time			95	145	ns
$V_{TH\_OCP\_VBUS}$	V_{BUS} OCP threshold voltage	Across sense resistor Rs	35	42	45	mV
$T_{OFF\_OCP\_VBUS}$	V_{BUS} OCP response time			3	8	µs
I_{ana_gain}	Current sensing gain		39	42	45	V/V
V_{IANA}	Output maximum voltage during OCP event on VBUS line				1.7	V
T_{ON}	V_{BUS} turn-on time			1	3	ms

4.6 CC lines OVP and ESD

Table 7. Electrical characteristics: CC lines OVP (CC refers to CC1 and CC2) across T_j

Symbol	Parameter	Test condition across T_{OP}	Value			Unit
			Min.	Typ.	Max.	
R_{ON_CC}	ON resistance of CC OVP FET	Normal mode		0.7	1.5	Ω
		Low power mode	8	17	28	
C_{ON_CC}	Equivalent ON capacitance of CCx line in normal mode	0 - 1.2 V, f = 400 kHz	40	60	100	pF
V_{TH_CC}	CC OVP threshold voltage		5.5	5.75	6	V
V_{MIN}	Minimum voltage on CC1c, CC2c	Current on CC1c or CC2c < 60 µA	0.7			V
R_{DB}	DB resistor	Measured at 400 µA on CC1c / CC2c	4.1	5.1	5.6	kΩ
T_{OVP_CC}	OVP response time on the CC pins			60	100	ns
BW_{CCx}	Bandwidth on CCx pins	at -3dB and 0 - 1.2 V		10		MHz

Table 8. Typical clamping voltage on CC lines after IEC61000-4-2 ±8kV contact discharge

TCPP03-M20 and STM32G071	ESD	First peak	V_{CL} 30 ns
OFF	+8 kV	9.2 V	3.3 V
OFF	-8 kV	-7.7 V	-1.0 V
ON	+8 kV	14.8 V	6.3 V
ON	-8 kV	-11.8 V	-1.5 V

Note: Measurements are performed on X-NUCLEO-DRP1M1 board plugged on top of NUCLEO-G071RB. Ten ESD discharge are applied on connector (CC1c and CC2c) and the voltage measurement is done on MCU side (CC1 and CC2), STM32 still functional after the ESD discharge.

4.7 VCONN OCP, discharge

Table 9. Electrical characteristics V_{CONN} switch (OCP, discharge) across T_j

Symbol	Parameter	Test condition across T_{OP}	Value			Unit
			Min.	Typ.	Max.	
R_{ON_VCONN}	ON resistance of VCONN FET		2.1	3	5.5	Ω
I_{VCONN}	Current thru V_{CONN} FET max operating current	VCONN = 3.0 V - 5.5 V			40	mA
$R_{dis\text{-}vconn}$	V_{CONN} discharge resistor		2.5	4	5	kΩ
OCP_{TH_VCONN}	OCP threshold on V_{CONN}		40	47	55	mA
T_{OCP_VCONN}	V_{CONN} OCP response time			0.9	2	µs

4.8 I2C slave

Table 10. **Electrical characteristics I2C adressing across T_j**

Symbol	Parameter	Test condition across T_{OP}	Value			Unit
			Min.	Typ.	Max.	
I2C speed				-	1	Mbps

5 Typical electrical characteristics curves

Figure 5. VBUS turn-on time (T_{ON})

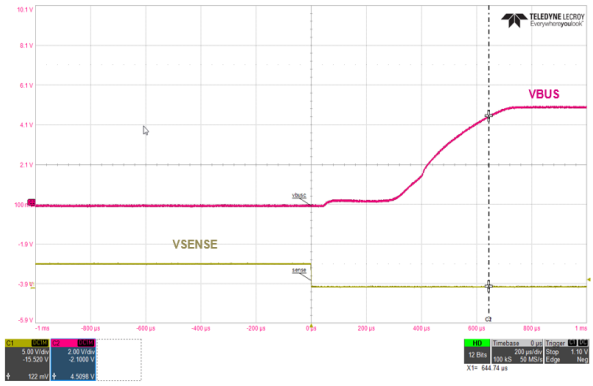
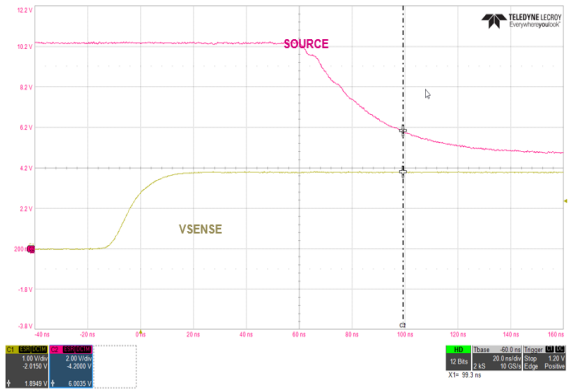
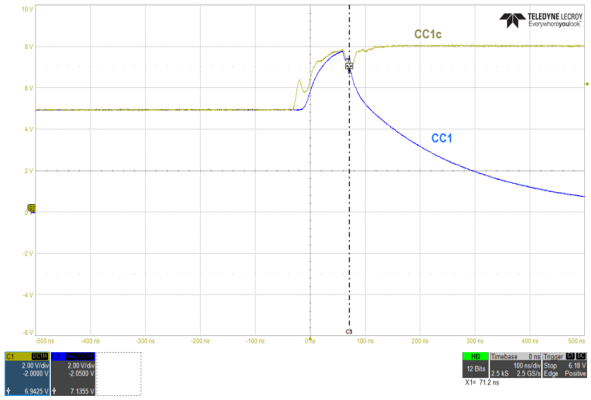


Figure 6. VBUS OVP response time



Note: Test conditions for Figure 5 and Figure 6: TCPP03-M20 is in hibernate mode VCC_VCONN = ENABLE = 0 V, VBUS = 5 V.

Figure 7. CC line (CC1 or CC2) OVP response time



Note: Test conditions for Figure 7: TCPP03-M20 in normal mode VCC_VCONN = +5 V, ENABLE = 3.3 V, VBUS = 0 V.

6 Functional description

6.1 Overview

The TCPP03-M20 is a cost effective solution to protect microcontrollers featuring built-in USB-C power delivery (UCPD) controller or other low voltage power delivery controller. It is especially adapted to dual role power, dual role data applications but also for sink applications requiring a current sense functionality.

Please refer to TA0357 for an overview of USB type-C and power delivery technologies.

Please refer to AN5225 for more informations related to USB type-C power delivery using STM32xx Series MCUs and STM32xxx series MPUs.

6.2 Power modes

The TCPP03-M20 embeds three distinct power modes controlled by the UCPD controller via the I2C bus.

Figure 8. Power modes process

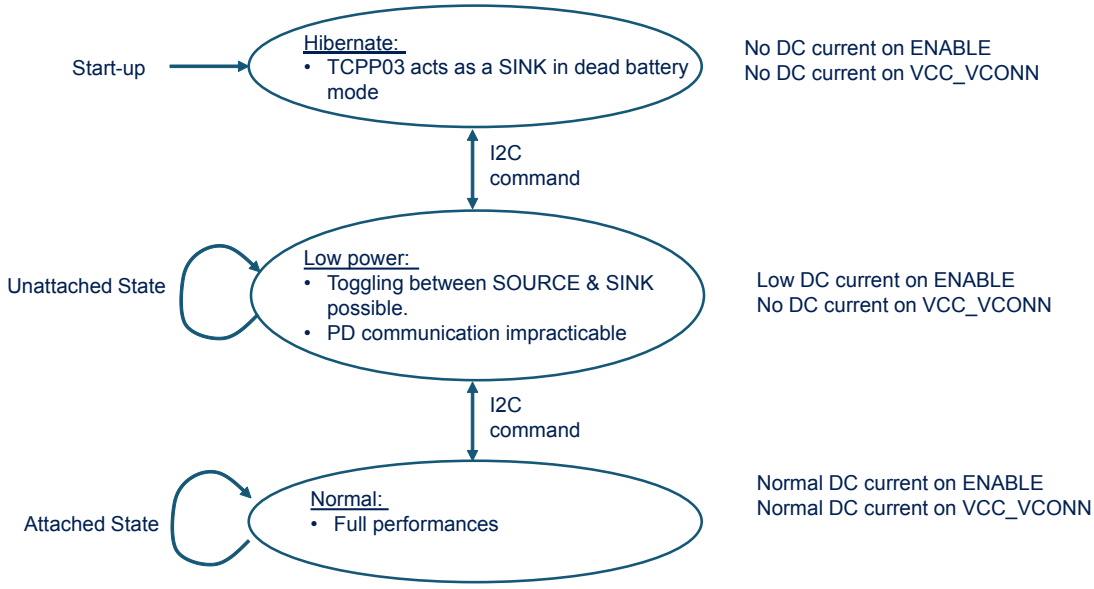


Table 11. Power mode versus power supply

VCC_VCONN	ENABLE	I_{DC} VCC_VCONN	I_{DC} ENABLE	Mode	Comments
X	0 V	0 µA(2)	0 µA(1)(2)	OFF (reset)	Dead batteries enabled FLGn indicates VBUS voltage I2C inactive / I2C registers reset
X	1.8 V ±5% 3.3 V ±10%	0 µA(2)	0(1) µA(2)	Hibernate	Dead batteries enabled FLGn indicates VBUS voltage I2C active Default state at start-up
X	1.8 V ±5% 3.3 V ±10%	0 µA(2)	< 10 µA(1)(2)(3)	Low power	Dead batteries disabled High ohmic CC => No PD communication possible OVP protection by clamping FLGn indicates VBUS voltage I2C active
3.3 V ±10% 5 V ±10%	1.8 V ±5% 3.3 V ±10%	2.7 mA	< 30 µA(1)(2)	Normal	Dead batteries disabled Full performance mode I2C active FLGn indicates failures

1. *Dynamic current of I2C interface have to be added to the values indicated when the I2C bus is used.*
2. *ESD leakage current have to be added to the values indicated.*
3. *For pin EN voltage between 1.7 V and 3.6 V.*

Table 12. TCPP03-M20 states versus power modes

Power mode	CC switches	OVP CC	Dead batteries	Gate driver consumer	Gate driver provider	OVP VBUS	FLGn	I2C	I_{ANA}	OCP VBUS	V_{CONN} VBUS Dis.	Comment
OFF	OFF	NA	ON	ON(1)	OFF	ON	VBUS connect	OFF	OFF	OFF	OFF	TCPP not powered
Hibernate	OFF	NA	ON	Controlled by I2C	OFF	ON	VBUS connect	ON	OFF	OFF	OFF	Default state at start-up
Low power	High ohmic	5 V clamp	OFF	Controlled by I2C	OFF	ON	VBUS connect	ON	OFF	OFF	OFF	Signaling only
Normal	Full perf.	Active OVP	OFF	Controlled by I2C		ON	Failure flags	ON	ON	ON	Controlled by I2C	PD communication active

1. *Consumer (sink) gate driver is self biased with VBUSc voltage*

6.3 I2C registers

The I2C address used by TCPP03-M20 is 0110 10x, with LSB = ‘x’.

The LSB bit of the I2C address is set when connecting TCPP03-M20 pin I2C_ADD to GND (for LSB = ‘0’) or to 1.8 V or 3.3 V (for LSB = ’1’).

Figure 9. I2C registers

I2C address : 0110 10x, x=LSB

VCONND=1:
- VCONN discharge ON

VCONND=0:
- VCONN discharge OFF

VBUSD=1:
- VBUS discharge ON

VBUSD=0:
- VBUS discharge OFF

PM2	PM1	Power Mode
0	0	Hibernate
1	0	Low power
0	1	Normal
1	1	Not Used

GDC=1:
- Switch load opened

GDC=0:
- Switch load closed

GDP=1:
- Switch load closed

GDP=0:
- Switch load opened

V2	V1	VCONN switch	
		VC2	VC1
0	0	Open	Open
1	0	Close	Open
0	1	Open	Close
1	1	Open	Open

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Writing register (address = 0)	VCONN DISCHARGE (VCONND)	VBUS DISCHARGE (VBUSD)	PM2 Power Mode 2	PM1 Power Mode 1	Gate Driver Consumer (GDC)	Gate Driver Provider (GDP)	V2	V1
Reading register n°1 (address = 1) Flags are set to '1' when active	VCONN DISCHARGE Acknowledge	VBUS DISCHARGE Acknowledge	PM2 Acknowledge	PM1 Acknowledge	Gate Driver Consumer Acknowledge	Gate Driver Provider Acknowledge	VCONN2 Acknowledge	VCONN1 Acknowledge
Reading register n°2 (address = 2) Flags are set to '1' when active	0 => TCPP03 1 => TCPP02	0	FLGn VBUS_OK	FLGn OVP_CC	FLGn OTP	FLGn OVP_VBUS	FLGn OCP_VBUS	FLGn OCP_VCONN

7 Protection features

TCPP03-M20 embeds protection features for dual role power (DRP), dual role data (DRD) applications, as required by:

- USB-C specification
- USB power delivery specification 3.1
- International electrotechnical commission (IEC)

7.1 FLGn pin description

FLGn pin is an open-drain output flag in steady state, it must be left floating when not connected.

In hibernate and low power modes FLGn indicates voltage presence on VBUS.

In normal mode, FLGn indicates an error (OVP, OCP or OTP): I2C registers must be read to identify the error. Recovery for each error type is described in each section of below paragraphs.

7.2 How to protect against ESD (electrostatic discharge) applied on the USB-C connector ?

Electrostatic discharges can be conducted by the USB Type-C connector and damage the electronic circuitry of the application.

The ESD surge waveform is modelized by the international electrotechnical commission in the specification IEC61000-4-2.

The TCPP03-M20 integrates ESD protection for CC1 and CC2 lines up to +8 kV contact discharge , associated with an external 100 nF - 50 V capacitor on C_{BIAS} pin.

Please refer to AN4871 USB type-C protection and filtering to apply required protections to comply with the IEC61000-4-2 specification.

For more information on IEC61000-4-2 standard testing, please refer to STMicroelectronics application note AN3353.

7.3 VBUS management

An overvoltage protection is required on VBUS when the absolute maximum ratings of your power management integrated circuit is below the maximum voltage that can be applied on VBUS.

Until now, it was common to find the protection circuit inside a controller dedicated to USB-C power delivery. However, by supporting USB-C PD with an embedded module inside an MCU and a companion Type-C port protection device, you can lower your bill of material and facilitate the transition , without requiring an expensive USB-C PD ASIC controller. One of the reasons the MCU and TCPP03-M20 bundle is such a compelling financial proposition is that the latter device integrates the VBUS gate drivers, which enables the use of cheaper and smaller N-MOSFETs, instead of the P-MOSFETs usually used by ASIC controllers.

This is an added value of TCPP03-M20, specially when VBUS line is compromised if a defective charger is stuck at a higher voltage than negociated or a defective cable is inserted.

Overvoltage protection is always required on the VBUS line to prevent a voltage higher than negociated is applied on the VBUS.

This use case can occur even when power delivery is not used i.e when VBUS voltage is 5 V.

7.3.1 VBUS turn-on

VBUS turn-on time after I2C command is achieved in T_{ON} = 1 ms typical (see Figure 5).

7.3.2 VBUS UVLO (under voltage lock out)

This block continuously monitors VBUS voltage. It acts as:

- An UVLO (under voltage lock out) for the VBUS circuitry: OVP_VBUS and consumer gate driver are enabled once the VBUS voltage reaches VBUS_UVLO voltage level (2.4 V typ.)
- It signals to the I2C block the presence of a voltage on VBUS when the VBUS voltage reach VBUS_UVLO voltage level (2.4 V typ.)

7.3.3 VBUS OVP turn-on and turn-off

When V_{SENSE} pin voltage goes above V_{OVP_TH}, OVP is turned ON in less than 95 ns ($T_{OVP\_ON\_VBUS}$ typical value), and FLGn pin goes to 'low-Z' state.

Fast shut-down is enabled by TCPP03-M20 gate driver by shorting the MOSFET gate and source pin. As a result, source pin goes safely to 0 V and I2C register is updated with relevant value.

OVP recovery is ensured after a typical delay of 64 µs: the external power mosfet is turned-on and Flag pin FLGn goes back to Hi-Z state after the end of the ovp condition.

7.3.4 How to set TCPP03-M20 OVP threshold according to VBUS maximum voltage allowed by the application

As shown in Figure 4, R1 / R2 bridge gives an image of VBUS voltage to set TCPP03-M20 OVP threshold.

With fixed R1 value (10 kΩ), the table provides R2 values for various TCPP03-M20 OVP threshold according to VBUS maximum voltage allowed by the application.

Table 13. R2 values versus VBUS OVP threshold when R1 = 10 kΩ

R2	VBUS max.	P max.
2.4 kΩ	6 V	15 W
1.3 kΩ	10 V	27 W
976 Ω	13 V	36 W
732 Ω	17 V	45 W
560 Ω	22 V	100 W

Note: R2 selected in accordance with input AMR on consumer path.

7.4 VBUS current sense (I_{ANA} pin)

The I_{ANA} output pin is active only in normal mode.

The I_{ANA} output can be connected directly to the STM32 ADC input because it is internally biased by EN pin.

The I_{ANA} output voltage level is about 1.7 V at the OCP tripping level allowing connection to 1.8 V MCU I/O pin.

7.5 V_{BUS} analog current measurement and bidirectional OCP

The over current protection on VBUS is bidirectional i.e active for both consumer (i.e sink or UFP application) and provider (i.e source or DFP application) power path.

VBUS OCP threshold is set by external serial resistor on VBUS. The gain for the analog reading is set to 42 V/V.

The OCP threshold is set to 0.042 V across Rs.

The OCP VBUS is biased by VCC_VCONN and works only in normal mode.

Equivalent block diagram in TCPP03-M20 for V_{BUS} analog current measurement and OCP is given here after:

Figure 10. Equivalent block diagram in TCPP03-M20

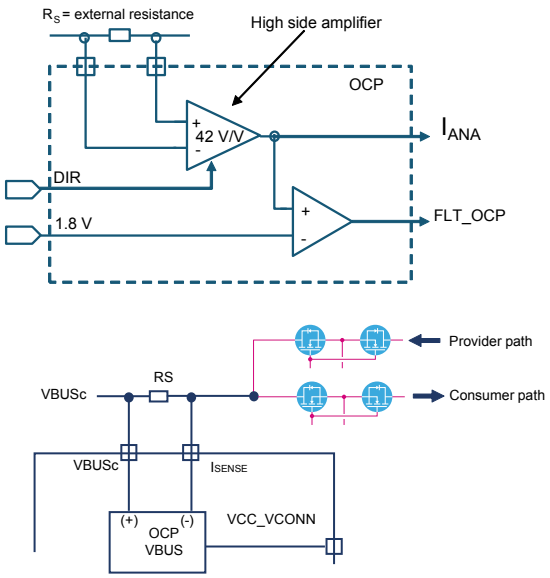


Table 14. Recommended values

Typical current	VBUS OCP threshold	Rs - Sense resistor (normalized values)
0.5 A	0.9 A	47 mΩ
1.5 A	1.9 A	22 mΩ
3.0 A	4.2 A	10 mΩ
5.0 A	6.0 A	7 mΩ

The OCP is biased continuously: inrush current magnitude is controlled by the user through an external capacitor.

Please refer to the X-NUCLEO-DRP1M1 user manual for more informations on external capacitor to control the insrush current magnitude.

If an OCP event occurs:

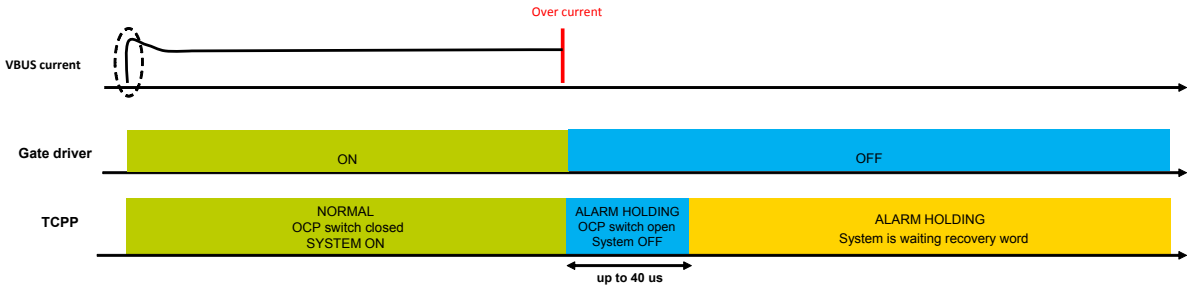
- V_{CONN} switches, CC switches and gate drivers are shutting down
- During up to 40 µs typ., this OCP alarm is held (no recovery is possible)
- After this delay, CC switches are turned ON but V_{CONN} switches and gate drivers are held OFF

The system can be restarted only with a recovery word send by the MCU via the I2C bus.

- The FLGn signal stays low while the recovery word has not been sent

The recovery word is described in next paragraph

Figure 11. Typical chronograms of TCPP03-M20 VBUS OCP



Note:

- *In case of VBUS OCP event, the TCPP03-M20 switches OFF all active functions except CC switches:*
  - *V_{CONN} switches*
  - *VBUS gate driver (provider and consumer)*
  - *V_{CONN} and V_{BUS} discharge paths are activated*
- *It is signaled to the user by several ways:*
  - *I2C corresponding state bits are cleared (i.e. VCONN1_ACK = 0, VCONN2_ACK = 0…)*
  - *I2C relevant OCP flag is set (FLGn_OCP_VBUS is the OCP event coming from VBUS switch for example)*
  - *Failure flag pin (FLGn) is active (i.e. in LowZ state)*
- *After a delay of up to 40 µs, to recover, the below bit sequence has to be written and after recovery, the user can resume a start-up procedure:*

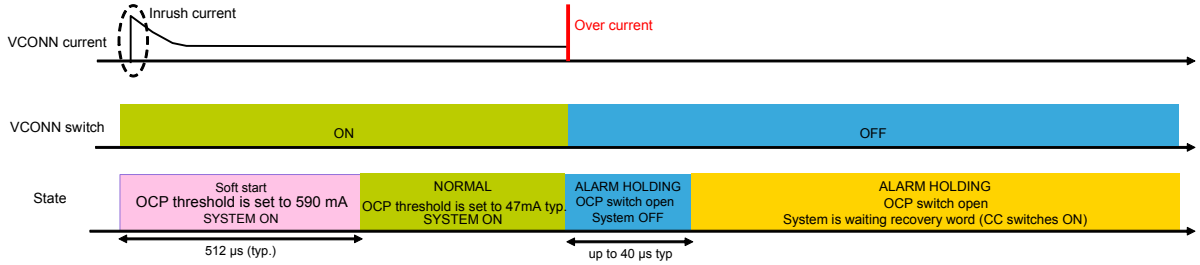
Table 15. VBUS OCP recovery bit sequence table

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	PM2	PM1	1	0	0	0

7.6 V_{CONN} OCP

- At start-up, a soft start sets the tripping current to about 590 mA during 512 µs min. (1ms max.)
- After this delay, the soft start is ended and the normal OCP threshold occurs (50 mA).
- If an OCP event occurs:
  - V_{CONN} switches, CC switches and gate drivers are shutting down
  - During up to 40 µs typical, this OCP alarm is held (no recovery is possible)
  - After this delay, CC switches are turned ON but V_{CONN} switches and gate drivers are held OFF. The system can be restarted only with a recovery word send by the MCU via the I2C bus.
  - The FLGn signal stays low as long as the recovery word has not been sent

Figure 12. V_{CONN} OCP chronograms



To recover, the below bit sequence has to be written and after recovery, the user can resume a start-up procedure:

Table 16. VBUS OCP recovery bit sequence table

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	PM2	PM1	1	0	0	0

7.7 V_{CONN} CC line OVP

7.7.1 CC lines short to VBUS

This happens when VBUS high voltage short circuit to the CC lines when hot unplug is done with a poor mechanical quality connector. Over voltage protection is needed on the CC lines because VBUS typical voltage can be as high as 20 V when CC pins are usually 5 V tolerant I/Os on low voltage USB-PHY controllers.

TCPP03-M20 integrate this protection against CC lines short to VBUS thanks to an overvoltage protection (integrated FET).

When the voltage on CC line goes above V_{TH_CC}, the OVP on CC line turns-on in less than 60ns (T_{OVP_CC} typical value) and FLGn pin goes to '0' state.

When the OVP event disappear, OVP on CC line is turned-off and the FLGn pin goes back to 'Hi-Z' state.

7.8 VBUS discharge

VBUS discharge is activated via I2C bus and controlled via firmware by the USB-C power delivery controller.

The VBUS discharge feature integrated in TCPP03-M20 allows to discharge 10 µF in less than 220 ms (T_{DIS_VBUS}).

This discharge time is in line with USB-C specification, extracted below for VBUS discharge:

Table 17. Common source / sink electrical parameters from USB-C specification

Parameter	Description	Min.	Typ.	Max.	Units
tSafe0V	Time to reach vSafe0V max.	-	-	650	ms
tSafe0V	Time to reach vSafe0V max.	-	-	275	ms

Note: To avoid short-circuit, the VBUS discharge cannot be activated if the consumer or the provider gate driver is active.

7.9 V_{CONN} discharge

V_{CONN} discharge is activated via I2C bus and controlled via firmware by the USB-C power delivery controller.

The V_{CONN} discharge feature integrated in TCPP03-M20 allows to discharge V_{CONN} in R_{DIS_VCONN} < 5.5 kΩ, as per USB-C specification table extracted below:

Table 18. V_{CONN} source characteristics from USB-C power delivery specification

	Minimum	Maximum	Notes
R_{dch}	30 Ω	6120 Ω	Discharge resistance applied in UnattachedWait.SRC between the CC pin being discharged and GND.

Note:

- *V_{CONN} discharge is activated and stopped via I2C commands from USB-PD controller*
- *To avoid short-circuit, V_{CONN} discharge cannot be activated if V_{CONN} switch are closed*
- *The CCxc pin discharged is the last one acting as V_{CONN}*

7.10 OTP (over temperature protection)

Above 150°C typ., the OTP triggers the FLGn pin.

OVP and OCP on VCONN, CC lines, VBUS are shut down.

Auto recovery is ensured when the temperature goes back below OTP threshold.

8 USB-C dual role power schematic example

Figure 13. **Partial schematic extract of nucleo expansion board X-NUCLEO-DRP1M1 using TCPP03-M20**

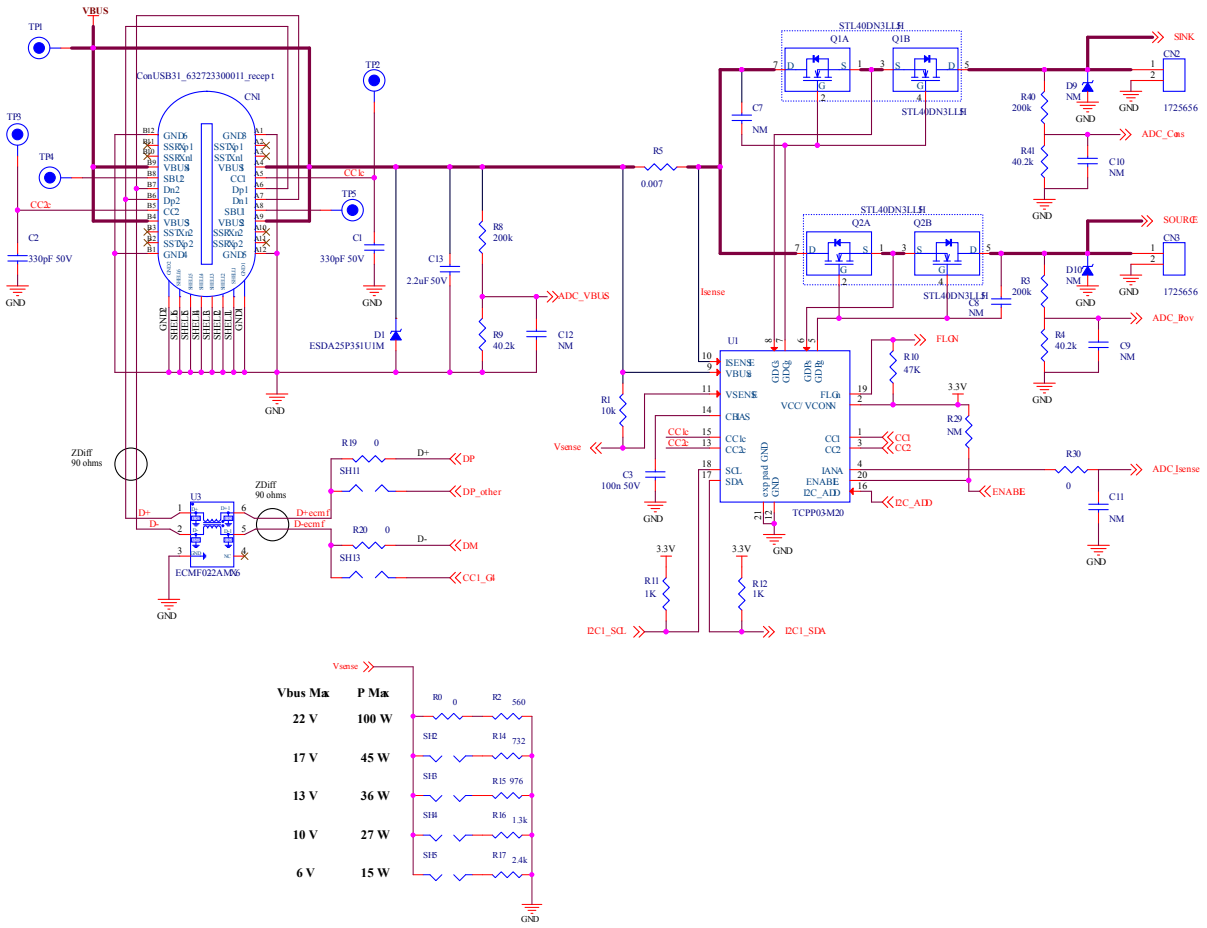
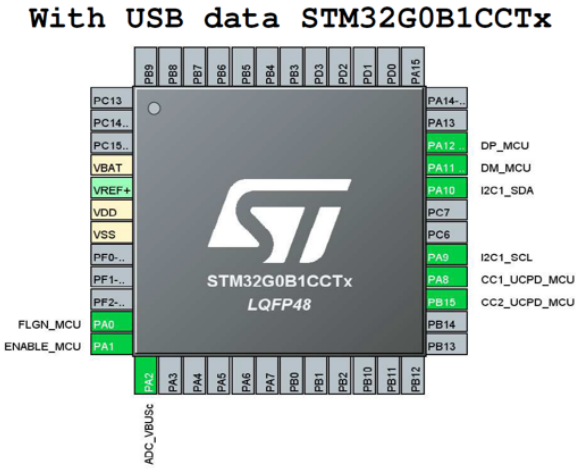


Figure 14. **STM32 configuration with CubeMX**



8.1 External components description

Table 19. Schematic description

Component reference	Component name or value	Description
D1	ESDA25P35-1U1M	TVS protecting against 25 A 8/20 µs surge waveforms and ESD transients(1) (see Section 8.2 Transient Voltage suppressor on VBUS).
C1, C2	330 pF typ., 25 V	EMI capacitor, required to comply with USB-C specification.
C3	100 nF, 50 V	X7R ESD protection capacitance with low ESL required to comply with USB-C specification.
C13	2,2 µF, 50 V	VBUSc bulk capacitance, required in the USB-C power delivery specification.
R5	0.007 Ω	Serial resistor which value sets the VBUS OCP threshold.
R1 and R2 or R14, or R15, or R16, or R17	See Table 13	Resistor bridge to set VBUS OVP threshold.

1. *For more informations on USB type-C protection and filtering, cf AN4871, and AN3353 for informations related to IEC 61000-4-2 standard testing.*

8.2 Transient Voltage suppressor on VBUS

The D1 diode ESDA25P35-1U1M is used to comply with the international electrotechnical commission specification IEC61000-4-5 on the VBUS power line when it is subjected to switching and lightning transients.These surges are defined in 8/20 µs waveform. For more information, please refer to AN4275: IEC61000-4-5 standard overview.

8.3 Configuration channel: line capacitance on CC1c and CC2c

USB-C PD has a specification for the total amount of capacitance for proper operation on CC lines. This specification is given here after.

Table 20. USB-C PD specification

Description	Minimum	Maximum
CC receiver capacitance	200 pF	600 pF

Therefore, the capacitance added by the TCPP03-M20 and by the MCU or LV controller must fall within limits. The next table shows the analysis involved in choosing the correct external capacitor for the system.

Table 21. Table analysis

CC capacitance	Min.	Max.	Comment
CC line target capacitor	200 pF	600 pF	From *USB PD Specification* section 5.8.6
TCPP03-M20 capacitance	40 pF	100 pF	
MCU or low voltage capacitance	60 pF	90 pF	Typical value. To be adapted following the exact reference used.
Proposed capacitance for C1, C2	120 pF	390 pF	25 VDC min. of rated voltage. 0402 or smaller recommended.

C1 and C2 must be placed as close as possible to the USB-C connector to optimize the electromagnetic immunity.

8.4 Bulk capacitance

USB-C power delivery specification defines cSnkBulk and cSrcBulk capacitances as the sum of bulk capacitances on both sides of the ohmic path of VBUSc.

To insure compliance with the standard and TCPP03-M20 protection performances, it is mandatory to place this capacitance on VBUSc, as close as possible to the USB-C connector with a value of 2,2 µF - 50 V.

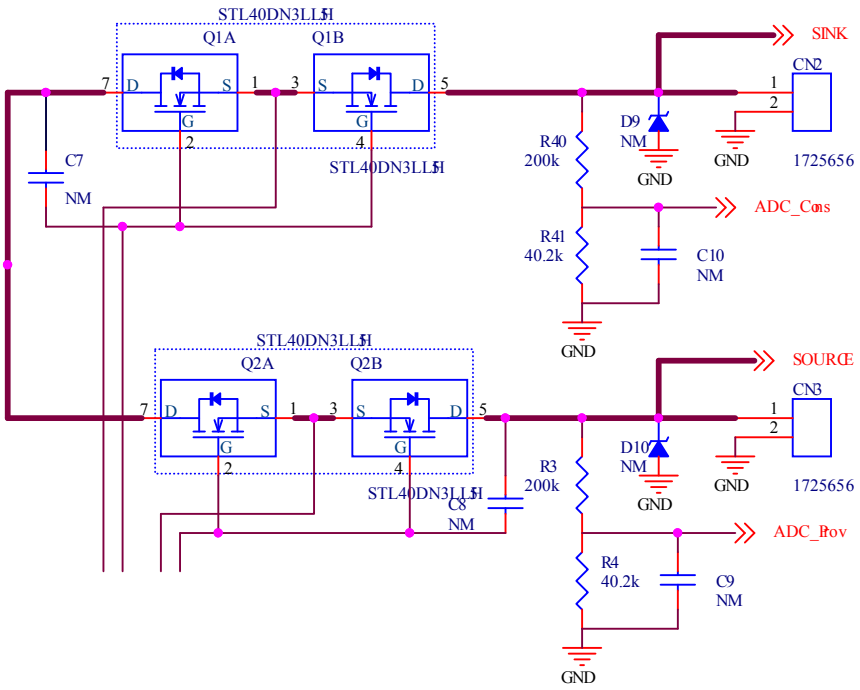
8.5 N-channel MOSFET

The TCPP03-M20 ensures a V_{GS} voltage between 5 V and 6 V when the N-channel MOSFET is ON.

The user must choose a N-channel MOSFET fully specified (for example: STL40DN3LLH5 in source to source configuration) with 5 V of V_{GS}. Maximum current in USB-PD applications can raises up to I_{DS} = 5 A.

As shown in Figure 15, C7 and C8 external capacitor may be associated to other N-channel MOSFET reference to avoid OCP trigger due to inrush current on VBUS pin.

Figure 15. Schematic example from X-NUCLEO-DRP1M1



8.6 Complementary products for USB dataline ESD protection for pins DP, DM, SSRX, SSTX

For applications requiring USB dataline protection, STMicroelectronics recommends the implementation shown in picture below:

Figure 16. USB dataline ESD protection for pins DP, DM, SSRX, SSTX

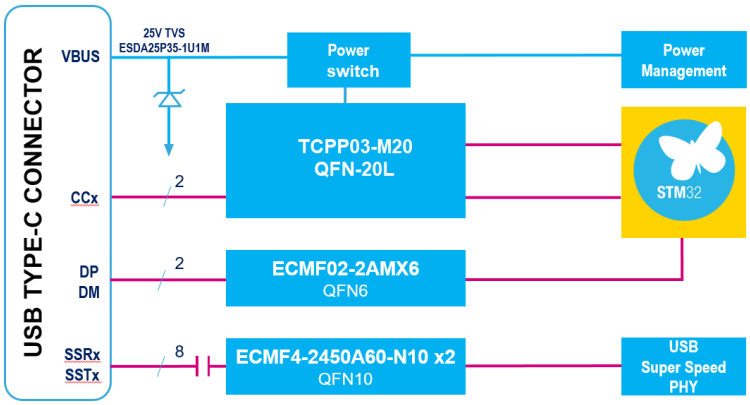


Table 22. Product recommendations

Part Number	Description	USB-C connector pin	Protection features
TCPP03-M20	Type-C port protection	VBUS, CC1, CC2, V_{CONN}	ESD protection as per IEC61000-4-2 Level 4 Overvoltage, overcurrent and discharge on VBUS Overvoltage, overcurrent and discharge on CC1/CC2, V_{CONN}
ESDA25P35-1U1M	Power line transient voltage suppressor (TVS)	VBUS	ESD protection as per IEC61000-4-2 Level 4 IEC61000-4-5 (8/20µs surge waveform)
ECMF02-2AMX6	Common mode filter with integrated ESD protection	D+, D-	ESD protection as per IEC61000-4-2 Level 4 RF antenna desense due to high speed differential link EMI radiation
ECMF4-2450A60N10 (x2)	Common mode filter with integrated ESD protection	TX1+, TX1-, RX1+, RX1- TX2+, TX2-, RX2+, RX2-	ESD protection as per IEC61000-4-2 Level 4 RF antenna desense due to high speed differential link EMI radiation

For more information on USB Type-C protection for datalines, please refer to AN4871, USB Type-C protection and filtering.

For more information on RF antenna desense due to high speed differential link EMI radiation, please refer to AN4356, Antenna desense on handheld equipment.

9 PCB design recommendation

9.1 PCB routing

When routing the TCPP03-M20, please respect the following recommendation:

- Place the circuit as close as possible to the USB-C connector in order to maximize the efficiency of the ESD protection for CC lines
- Place the ESD capacitor as close as possible to the TCPP03-M20

10 USB type-C port protection (TCPP) comparison table

Table 23. **Device comparison table**

Part number	Expansion board	SW expansion board	USB type-C application	Package
TCPP01-M12	X-NUCLEO-SNK1M1	X-CUBE-TCPP	Sink, UFP, consumer	µQFN-12L
TCPP02-M18	X-NUCLEO-SRC1M1		Source, DFP, provider	µQFN-18L
TCPP03-M20	X-NUCLEO-DRP1M1		DRP, dual role power DRD, dual role data Sink requiring current sense and OCP	µQFN-20L

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 QFN-20L 4.0 x 4.0 x 0.75 mm package information

Figure 17. **QFN-20L 4.0 x 4.0 x 0.75 mm package outline**

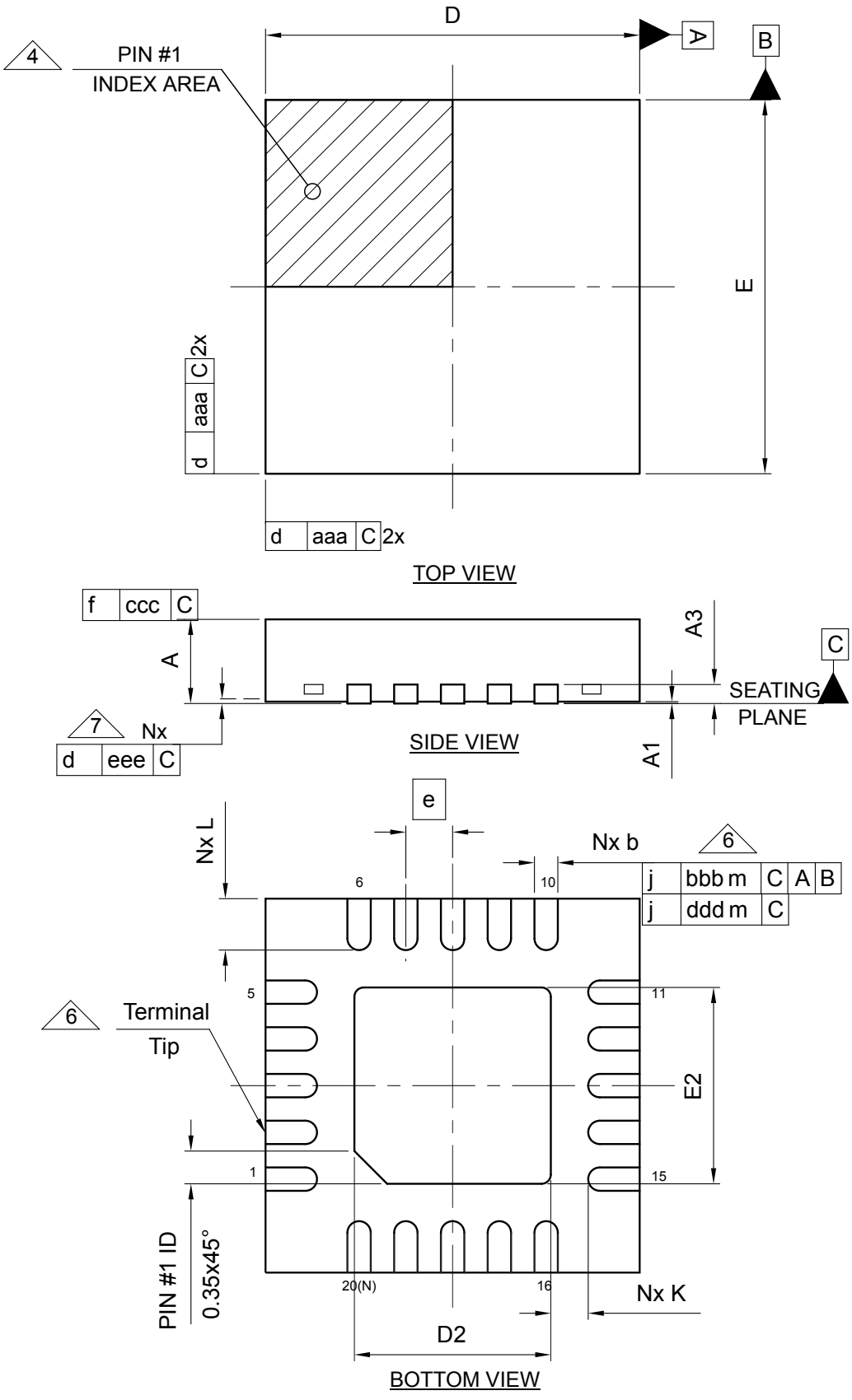


Table 24. **QFN-20L 4.0 x 4.0 x 0.75 mm package mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1		0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D	3.95	4.00	4.05
D2	1.95	2.10	2.20
E	3.95	4.00	4.05
E2	1.95	2.10	2.20
e		0.50 BSC	
L	0.50	0.55	0.60
K	0.20		
N		20	
ND		5	
NE		5	
aaa		0.05	
bbb		0.10	
bbb		0.10	
ddd		0.05	
eee		0.08	

Figure 18. **recommended footprint (dimensions are in mm)**

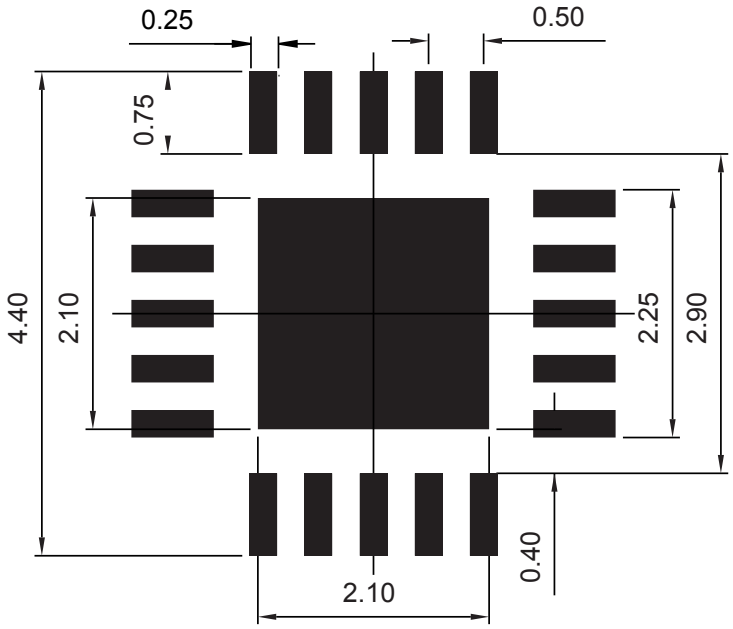


Figure 19. **Tape and reel outline**

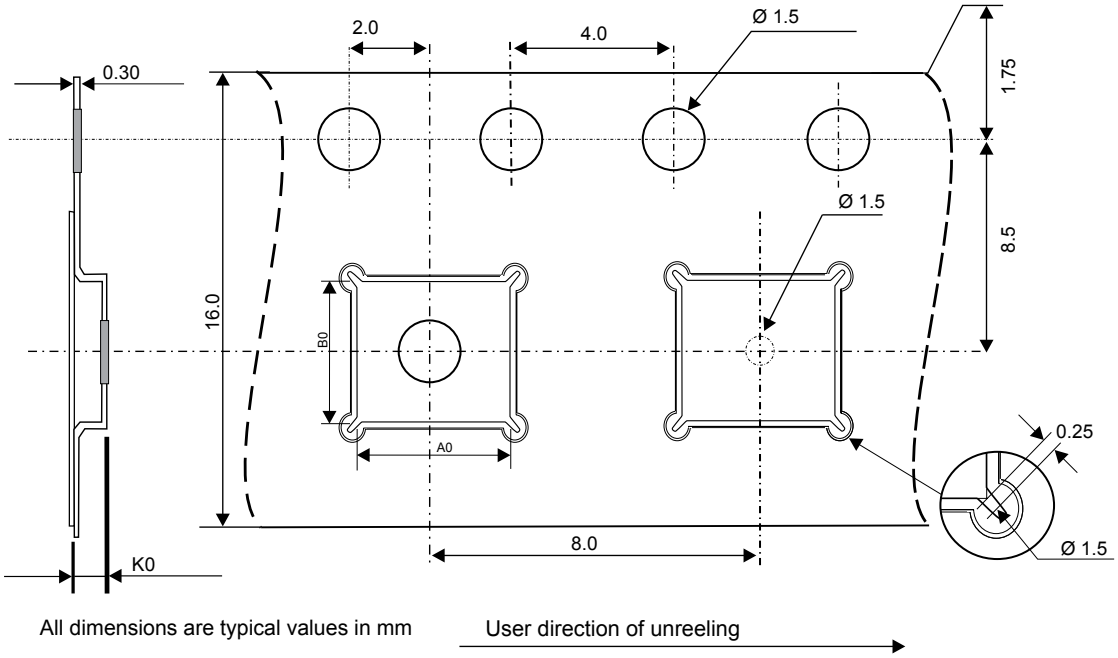
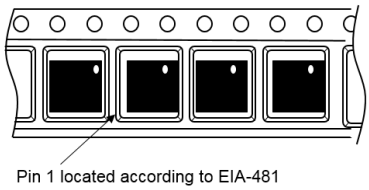


Table 25. **Tape and reel mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A0	4.25	4.35	4.45
B0	4.25	4.35	4.45
K0	1.00	1.10	1.20

Figure 20. **Package orientation in reel**



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Figure 21. **Tape and reel orientation**

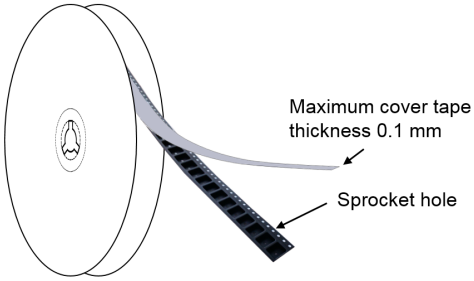


Figure 22. **Reel dimensions (mm)**

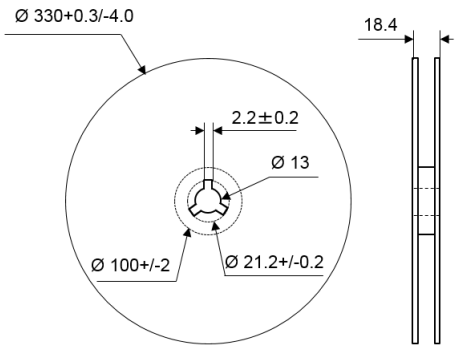
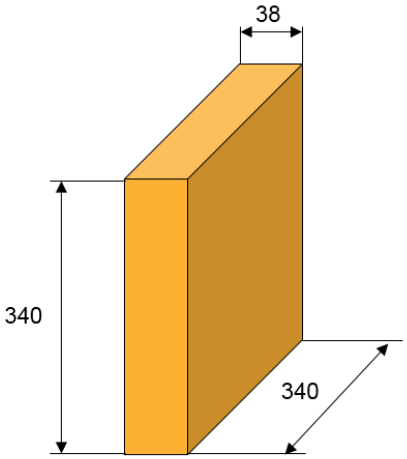


Figure 23. **Inner box dimensions (mm)**



12 Ordering information

Table 26. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TCPP03-M20	TCPP03	QFN-20L 4.0 x 4.0 x 0.75 mm	44 mg	3000	Tape and reel

Revision history

Table 27. **Document revision history**

Date	Revision	Changes
21-Jun-2021	1	Initial release.

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