LAN9360

AVB Audio Endpoint

Highlights

- Supports the implementation of an Automotive Ethernet Audio Device (AED-A) to transmit and/or receive uncompressed audio over an Ethernet Audio Video Bridging (AVB) network

Target Applications

- Automotive in-vehicle networking
- Infotainment
- Telematics

Features

- generalized Precision Time Protocol (gPTP)
  - Grandmaster
  - Slave
  - Precise time synchronization
  - 1PPS measurement support
- Audio Video Transport Protocol (AVTP)
  - AVTP Audio Format (AAF) Listener or Talker
  - AVTP Clock Reference Format (CRF) Listener or Talker
- Real-time Transport Protocol (RTP)
  - Extended with AVB RTCP support
  - Configurable Payload Type Id for fitting to custom RTP profile specifications
- Stream routing
  - Up to 8 streams in parallel
  - Processing of up to 40 audio channels
  - Parallel processing of incoming and outgoing streams
  - PDM to PCM decimation
- Media Clock recovery, from an:
  - AVTP AAF stream
  - AVTP CRF stream
  - RTP stream
- Media Clock generation, based on:
  - Local crystal
  - External FSY signal
- Configuration
  - Avnu entity model based
  - Tool assisted by MPLAB® Network Creator
- Bootloader
  - Remote firmware update over Ethernet
  - Remote configuration update over Ethernet
- External MCU connectivity
  - MCU connected as Layer 2 device
  - Ethernet frame pass through on SPI
- Secure element (optional)
  - High-bandwidth Digital Content Protection (HDCP) receiver
  - Secure boot
  - Secure update
- Ethernet MAC 10/100 Mbps in Reduced Media Independent Interface (RMII) mode
- Two I²C Ports
  - PLL, TA100 and EEPROM control
  - User-specific external modules
- Serial Peripheral Interface (SPI) Port
- Two Audio Interfaces supporting:
  - Inter-IC Sound (I^2S)
  - Time-Division Multiplexing (TDM)
  - Pulse-Density Modulation (PDM)
- System
  - Embedded voltage regulator for single-supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD)
  - AEC-Q100 Grade 2 qualified
- Package
  - 100-ball TFBGA, 9x9 mm, pitch 0.8 mm

Conformity

- Automotive Ethernet AVB Functional and Interoperability Specification
- IEEE 1722™-2016 (AVTP)
- RFC 3550-2003 (RTP/RTP Control Protocol (RTCP))
- IEEE 1733™-2011 (AVB RTCP packet extension)
- IEEE 802.1AS™-2011 (gPTP)

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Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

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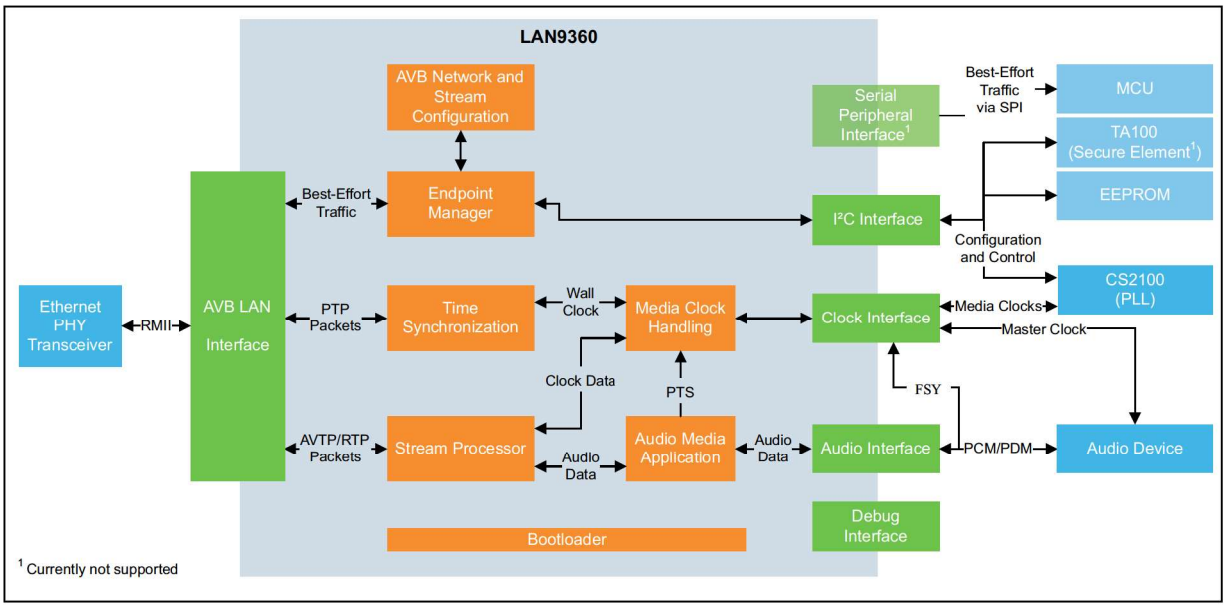
1.0 INTRODUCTION

The LAN9360 supports the implementation of an Automotive Ethernet Audio Device enabling uncompressed audio data transfers over an Ethernet Audio Video Bridging network. Hence, it is designed to route audio data between an AVB/TSN Media Stream on the Ethernet network and an Audio Interface that connects to digital audio sources and sinks.

The LAN9360 provides an implementation of an AVB/TSN protocol stack. By connection to an external Ethernet PHY Transceiver, it can be used with several Ethernet physical layers.

Figure 1-1 depicts the block diagram of the LAN9360.

FIGURE 1-1: LAN9360 BLOCK DIAGRAM



As outlined in Figure 1-1, the LAN9360 consists of functional blocks. Each functional block contains one or multiple components that provide specific functionality.

1.1 LAN9360 Functional Blocks

The LAN9360 functional blocks are described in the LAN9360 data sheet.

Functional blocks, which interfere with external devices via physical pins are called interfaces.

1.2 External Devices

Ethernet PHY Transceiver

100BASE-T1 or 100BASE-TX may be selected by configuration. 10BASE-T1S is supported for evaluation.

PLL

The LAN9360 requires an external PLL of type CS2100 to generate the Bit-Clock for the Audio Interface.

Audio Device

An external audio device, e.g., a DSP or a CODEC, is connected to the Audio Interface to transfer digital audio data. It is used as sink and/or source of Pulse-Code Modulation/Pulse-Density Modulation (PCM/PDM) coded audio data.

Secure Element (Optional)

A TA100 is used for HDCP, secure boot and secure update.

EEPROM (Optional)

The I^2C Serial EEPROM is used to read a pre-programmed globally unique EUI-48 node identity for MAC address configuration. The LAN9360 can operate with EEPROMs that are compatible to the storage format as used with Microchip's 24AA025E48.

MCU (Optional)

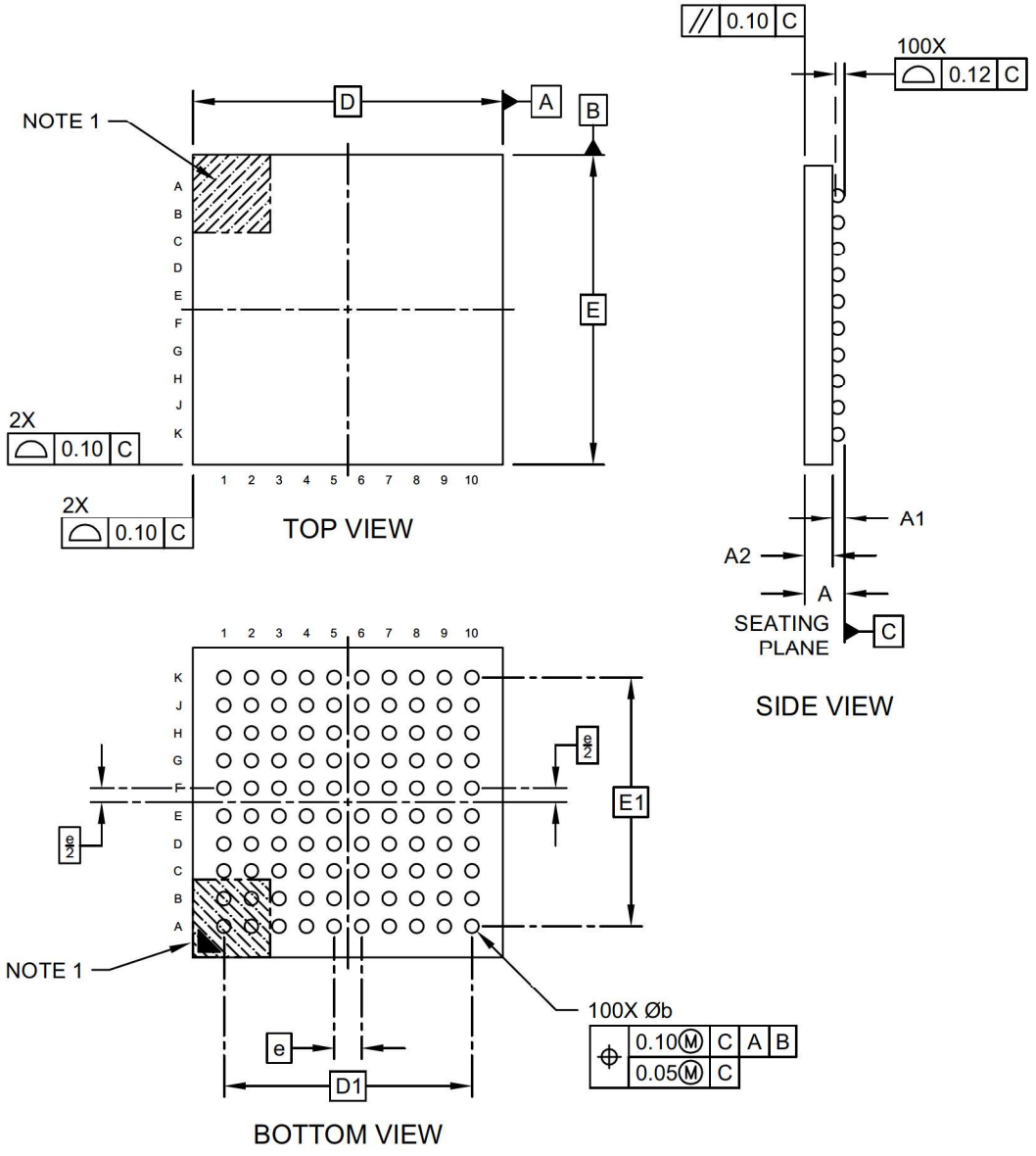
An external MCU may be connected to the SPI to send and receive Ethernet frames.

2.0 PACKAGE AND PINOUT

2.1 100-Ball TFBGA Package Outline

100-Ball Ceramic Ball Grid Array Package (CQB) - 9x9 mm Body [TFBGA]
Atmel Legacy Global Package Code CPR

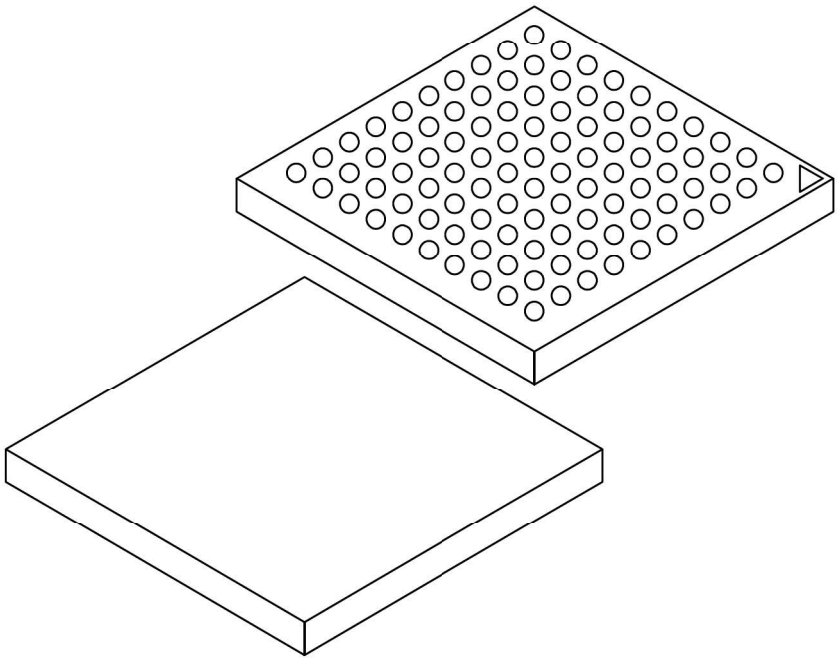
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21503-CQB Rev B Sheet 1 of 2

100-Ball Ceramic Ball Grid Array Package (CQB) - 9x9 mm Body [TFBGA]
Atmel Legacy Global Package Code CPR

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.80 BSC	
Overall Height	A	1.10	-	1.20
Ball Height	A1	0.20	-	-
Molded Package Height	A2	0.65	-	-
Overall Length	D		9.00 BSC	
Overall Pitch	D1		7.20 BSC	
Overall Width	E		9.00 BSC	
Overall Pitch	E1		7.20 BSC	
Terminal Diameter	b	0.40	0.45	0.50

Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21503-CQB Rev B Sheet 2 of 2

100-Ball Ceramic Ball Grid Array Package (CQB) - 9x9 mm Body [TFBGA]
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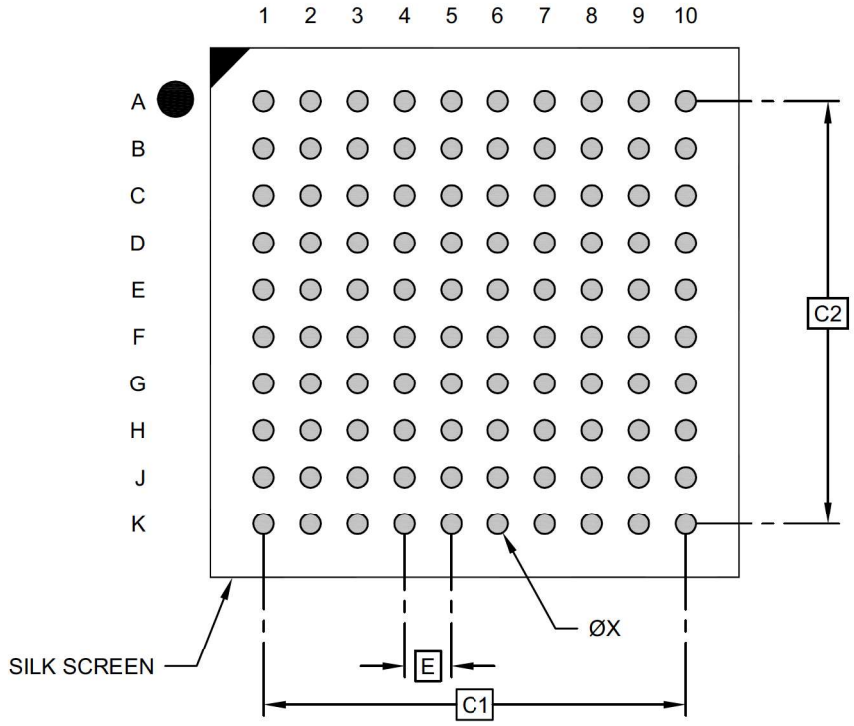

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Overall Pitch	C1		7.20 BSC	
Contact Pad Spacing	C2		7.20 BSC	
Contact Pad Diameter (X100)	X1			0.35

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23503-CQB Rev B

2.2 100-Lead Package Pinout

TFBGA Ball	Signal	Conditions/ I/O Type	Pin Description	Type	Note
Audio Interface					
E2	SCKA	GPIO	Serial Clock	Input/Output	—
E1	FSYA		Word Select	Input/Output	
K9	SRA	GPIO_AD	Serial Data Input	Input	
G3	SXA	GPIO	Serial Data Output	Output	
C10	SCKB	GPIO_AD	Serial Clock	Input/Output	—
J6	FSYB		Word Select	Input/Output	
J5	SRB		Serial Data Input	Input	
C7	SXB	GPIO	Serial Data Output	Output	
B1	CLKEN	GPIO_AD	Bit-Clock and Word-Clock enable		Assigned, when PLL clock output is stable
Serial Peripheral Interface					
H1	$\overline{\text{PCS}}$	GPIO	Peripheral Chip Select	Master: Output, Slave: Input	—
K3	MISO		Master In Slave Out	Master: Input, Slave: Output	
H5	MOSI	GPIO_AD	Master Out Slave In	Master: Output, Slave: Input	
J4	SPCK		Serial Clock	Master: Output, Slave: Input	
G1	IRQ		Interrupt Request	Output	
K1	FC		Flow Control		
Clock Interface					
F8	REFCLK0	GPIO	Reference Clock 0	Output	Reference clock output to be connected to REFCLKIN. Used for internal clock management
	ERASE		—	Input	—
K8	REFCLK1		Reference Clock 1	Output	Signal is used to drive the clock reference of the external PLL for the audio clock.
			1PPS Measurement Signal		1PPS method for clock accuracy measurement
G2	MCLK	GPIO_AD	Master Clock		—
J1	PLLDIVSEL		PLL Divider Select		
J3	PLLIN		Reference Clock Input	Input	
A9	EVIN	GPIO	Event Input for Timestamping		
H7	UNLOCK	GPIO_AD	Media Clock Unlock	Output	Signals media clock synchronization failures
H8	REFCLKIN		Reference Clock Input	Input	—

TFBGA Ball	Signal	Conditions/ I/O Type	Pin Description	Type	Note
Crystal 12 MHz					
A2	XOUT	CLOCK	—	Output	—
A1	XIN			Input	
AVB LAN Interface					
C1	GTXCK	GPIO_AD	Transmit Clock	Input	Input only. GTXCK must be provided with a 50 MHz external oscillator.
D2	GTXEN	GPIO	Transmit Enable	Output	—
E3	GTX0		Transmit Data	Output	
B5	GTX1				
A5	GRXDV	GPIO_CLK	Receive Data Valid	Input	
D5	GRX0		Receive Data	Input	
B6	GRX1				
A6	GRXER		Receive Error	Input	
B7	GMDC		Management Data Clock	Output	
B8	GMDIO		Management Data Input/Output	Input/Output	
F1	$\overline{\text{GINT}}$	GPIO_AD	LAN interrupt	Input	From LAN PHY
J8	$\overline{\text{GRST}}$		LAN reset	Output	To LAN PHY
I²C Interface					
H4	SDA0	GPIO_AD	Serial Data	Input/Output	Interface to host
J7	SCK0		Serial Clock	Output	
F9	SDA1	GPIO_AD	Serial Data	Input/Output	Interface to connect a PLL and an optional Secure Element
H10	SCK1	GPIO	Serial Clock	Output	
H6	TA100RST	GPIO_CLK	TA100 reset		—
Debug Interface					
C8	SWO	GPIO	Serial Wire Output	Output	—
G8	SWDIO		Serial Wire Debug Input/Output	Input	
E9	SWCLK	GPIO	Serial Wire Debug Clock	Input	
Miscellaneous					
G10	RST	RST	—	Input	—

TFBGA Ball	Signal	Conditions/ I/O Type	Pin Description	Type	Note
Power and Ground					
C5, F3, G7	VDDIO	POWER	Power	—	—
C6, D6, G6	VDDCORE				
D7	VDDPLL				
E5	VDDUTMII				
B3	VDDUTMIC				
E6	VDDPLLUSB				
C3	VDDOUT				
C2	VDDIN				
D1	VREFP				
D3	VREFN	GROUND			
A8, C4, D4, E4, E7, F4, F5, F6	GND		Ground		
Not Connected					
A3, A4, A7, A10	Not connected	—	—	—	—
B2, B4, B9, B10					
C9					
D8, D9, D10					
E8, E10					
F2, F7, F10					
G4, G5, G9					
H2, H3, H9					
J2, J9, J10					
K2, K4, K5, K6, K7, K10					

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	-	X	/	XX	[X](1)	-	[XXX]	-	XXX
	Device Family		Device Variant		Operating Temperature Range	Package Type		Tape and Reel Option		Automotive Code Option		Revision Code

Device Family:	LAN9360	
Device Variant:	A	= Basis feature set
Operating Temperature Range:	V I	= -40°C to +105°C (AEC-Q100 Grade 2) = -40°C to +85°C (Industrial)
Package Type:	CQB	= TFBGA (100-ball)
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel(1)
Automotive Code Option:	Blank VXX	= Industrial grade = Automotive grade
Revision Code:	100 CXX	= Standard revision code = Custom revision code, contact Microchip support if needed.

Examples:

a) LAN9360A-V/CQBT-VAO-100,
Basis feature set,
TFBGA (100 ball),
-40°C to +105°C,
Tape and Reel,
Automotive grade
Standard revision code 100

b) LAN9360A-I/CQBT-CXX,
Basis feature set,
TFBGA (100 ball),
-40°C to +85°C,
Tape and Reel,
Industrial grade
Custom revision code CXX

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. Reel size is 5,000.

APPENDIX A: REVISION HISTORY

Revision	Date	Comment
DS60001577D	Jan. 2021	Initial release of this document
DS60001577C	July 2020	Updated draft document. For details refer to the respective document revision.
DS60001577B	Nov. 2019	
DS60001577A	July 2019	Initial version of draft document

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