swissbit®

Product Data Sheet

Industrial microSD/SDHC Memory Card

S-455u Series

UHS-I Interface, SLC

made in germany

Contents

S-455u Series – Industrial microSD/SDHC Memory Card, SLC

1. Product Summary

- **Capacities:** 512 MBytes, 1 GBytes, 2 GBytes, 4 GBytes, 8 GBytes
- **Form Factor:** Standard microSD Memory Card form factor - 15.0 x 11.0 x 0.7mm (1.0mm)
- **Compliance:** Fully compliant with SD Memory Card specification 3.0
  - SD ultra high speed mode, speed class 1
  - SD high speed mode, up to speed class 10
  - SD2.0 SDHC backward compliant, default speed and high speed mode
- **Performance:**
  - SD burst up to 50MB/s
  - SD Normal speed 0...25MHz clock rate
  - SD High speed 0...50MHz clock rate
  - SD UHS-I speed 0...50MHz (DDR) and 0...100MHz (SDR)
  - Up to 37MByte/sec sequential data rate
- **Operating Temperature Range:** Extended: -25 °C to 85 °C; Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** Extended: -25 °C to 100 °C; Industrial: -40 °C to 100 °C
- **Operating Voltage:** 2.7...3.6V (Low-power CMOS technology)
- **Power consumption (Max Capacity):** 90mA
- **Data Retention:** 10 Years @ Life Begin / 1 Year @ Life End
- **Shock/Vibration:** 1,500 g/50 g
  Electromagnetic Compatibility Tests: Radiated Emission; Radiated Immunity; Electrostatic Discharge

2. Product Features

- Optimized FW algorithms especially for high read access and long data retention applications
  - Patented power-off reliability technology
  - Wear Leveling technology
  - Write Endurance technology
  - Read Disturb Management
  - Data Care Management
  - Near Miss ECC technology
  - Diagnostic features with Life Time Monitoring tool support
- High reliability
  - Designed for industrial market - especially read intensive application like navigation, infotainment, POS/POI, medical and general boot medium use case
  - The product is optimized for a long life cycle that requires good data retention because of high temperature mission profile
  - Number of card insertions/removals up to 20,000
  - SIP (System In Package) process for extreme dust, water and ESD resistance
  - Selected AEC-Q100 qualification
- Manufactured in a TS 16949 certified factory
- Customization options like CID registers, CPRM keys, firmware incl. settings and product marking based on your requirements
- In-field firmware update
  Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)

3. Ordering Information

Table 1: Standard Product List

Capacity	Extended Temperature	Industrial Temperature
	Part Number	Part Number
512 MBytes	SFSD0512NxBM1T0-E-ME-2y1-STD	SFSD0512NxBM1T0-I-ME-2y1-STD
1 GBytes	SFSD1024NxBM1T0-E-DF-2y1-STD	SFSD1024NxBM1T0-I-DF-2y1-STD
2 GBytes	SFSD2048NxBM1MT-E-ME-2y1-STD	SFSD2048NxBM1MT-I-ME-2y1-STD
4 GBytes	SFSD4096NxBM1MT-E-DF-2y1-STD	SFSD4096NxBM1MT-I-DF-2y1-STD
8 GBytes	SFSD8192NxBM1MT-E-QG-2y1-STD	SFSD8192NxBM1MT-I-QG-2y1-STD

x = product generation and y = firmware revision (A, B, ...)

Table 2: Available Part Numbers, SLC NAND Flash 24nm/25nm

Capacity	Extended Temperature	Industrial Temperature
	Part Number	Part Number
512 MBytes	SFSD0512N1BM1T0-E-ME-2A1-STD	SFSD0512N1BM1T0-I-ME-2A1-STD
1 GBytes	SFSD1024N1BM1T0-E-DF-2A1-STD	SFSD1024N1BM1T0-I-DF-2A1-STD
2 GBytes	SFSD2048N1BM1MT-E-ME-2A1-STD	SFSD2048N1BM1MT-I-ME-2A1-STD
4 GBytes	SFSD4096N1BM1MT-E-DF-2A1-STD	SFSD4096N1BM1MT-I-DF-2A1-STD
8 GBytes	SFSD8192N1BM1MT-E-QG-2A1-STD	SFSD8192N1BM1MT-I-QG-2A1-STD

4. Product Description

The microSD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The card operates in two basic modes:

- SD/SDHC and UHS-I card modes
- SPI mode

The microSD Memory Card also supports SD Default and High Speed mode with up to 50MHz clock frequency as well as UHS-I modes DDR50, SDR12/25/50 with up to 100MHz clock frequency.

The cards are compliant with

- SD Memory card Specification Part 1, Physical layer Specification V3.01
- SD Memory card Specification Part 2, File System Specification V3.00
- SD Memory card Specification Part 3, Security Specification V3.00
- MICRO SD Memory Card Addendum V4.00

Simplified specifications are available at https://www.sdcard.org/

The Card has an internal intelligent controller, which manages interface protocols, data storage and retrieval as well as hardware BCH Error Correction Code (ECC), defect handling, diagnostics and clock control.
The advanced wear leveling mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware BCH-code ECC allows to detect and correct up to 40 defect bits per 1kByte.
The controller performs control read operations and checks the consistence of the data. If an error of some bits is detected, the card refreshes all data in the flash cells to prevent data retention problems.

The card has a power-loss management feature to prevent data corruption after power-down.
The cards are RoHS compliant and lead-free.

4.1 Performance Specifications

Table 3: Read/Write Performance

System Performance		Typ[1] [2]	Max[1] [3]	Unit
Burst Data transfer Rate (max SD clock 100MHz)			50	MB/s
Sustained Sequential Read	512MB	22	25	MB/s
	1GB-8GB	31-37	40	MB/s
Sustained Sequential Write	512MB	12	15	MB/s
	1GB-2GB	15-18	21	
	4GB-8GB	25-26	28	MB/s
Sustained Random Read 4k	512MB-8GB	3.1-4.4	5.0	MB/s
Sustained Random Write 4k	512MB	5.1	6.0	MB/s
	1GB-8GB	3.3-3.6	4.0	MB/s

4.2 Environmental Specifications

4.2.1 Recommended operating conditions

The recommended operating conditions for the S-455u microSD Memory Card are provided in Table 4 below.

Table 4: microSD Memory Card recommended operating conditions

Parameter	Min	Typ	Max[4]	Unit
Extended Operating Temperature	-25	25	85	°C
Industrial Operating Temperature	-40	25	85	°C

[1] All values refer to Toshiba Flash 4Gb or Micron Flash 16Gb

[2] Sustained Speed measured with USB-SD Memory Card reader with crystal disk test tool.

[3] Target values

[4] High Temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected

4.2.2 Recommended storage conditions

The recommended storage conditions are listed below in Table 5.

Table 5: microSD Memory Card recommended storage conditions

Parameter	Min	Typ	Max[5]	Unit
Extended Storage Temperature	-25	25	100	°C
Industrial Operating Temperature	-40	25	100	°C

4.2.3 Humidity and EMC

The humidity and EMC conditions are listed below in Table 6.

Table 6: Humidity & EMC

Parameter	Condition
Humidity (non-condensing)	85% RH @85°C 1000h
ESD	up to ±4 kV (contact discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, on each contact pad, non-operating up to ±15 kV, (air discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, isolated contact pad area, non-operating

4.2.4 Environmental conditions

The Environmental conditions are listed below in Table 7.

Table 7: Environmental conditions

Parameter	Condition
UV light exposure	UV: 254nm, 15Ws/cm2 according to ISO7816-1
X-Ray	0.1 Gy 70keV to 140KeV (ISO7816-1) according SDA
Durability	20,000 mating cycles
Drop Test	1.5m free fall
Bending / Torque	10N / 0.15Nm ±2.5° max
Mechanical Shock	1500G, 0.5ms, half sine wave ±xyz-axis, 4 pulses each non-operating, JESD22B110 Condition B
Vibration	50G, p-p, 20..2000Hz, sweep xyz-axis, 4 pulses each, non-operating, MIL-STD-883 M2007.3 Condition B

[5] High Temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected

4.3 Physical dimensions

The physical dimensions of the S-455u microSD Memory Card are listed in the following table.

Table 8: Physical dimensions

Outer physical dimensions	Value	Unit
Length	15.0±0.1	mm
Width	11.0±0.1	mm
Thickness	0.7 (1.0)±0.1	mm
Weight (typ.)	0.4	g

4.4 Reliability

Table 9: Reliability

Parameter	Value[6]
Data Retention at beginning @ 40°C	10 years
Data Retention at life end (60k-100k PE cycles) @ 40°C	1 year

4.5 Geometry Specification

Table 10: microSD Memory Card capacity specification

Capacity	Sector	Total Addressable Bytes
512MB	967,680	495,452,160
1GB	1,953,792	1,000,341,504
2GB	3,938,304	2,016,411,648
4GB	7,774,208	3,980,394,496
8GB	15,802,368	8,090,812,416

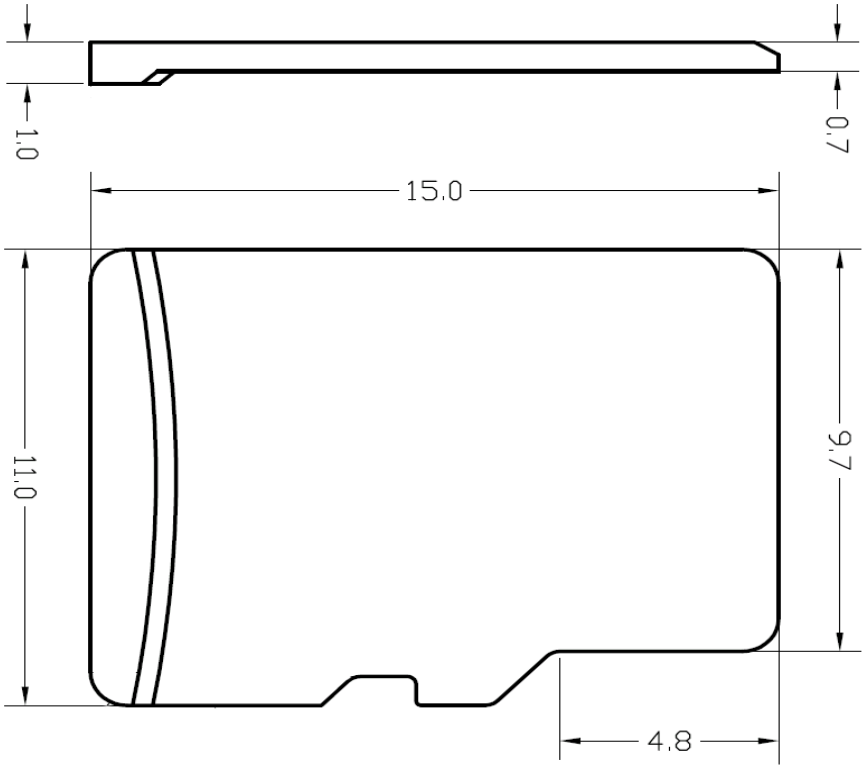
[6] After every power on the card reads the whole flash and performs a data refresh if necessary. So, the data retention can be much longer in most use cases.

5. Card physical

5.1 Physical description

The microSD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).

Figure 1: Simplified mechanical dimensions microSD Memory Card



The dimensions and tolerances are according to the SD specification.

6. Electrical Interface

6.1 Electrical description

Figure 2: microSD Memory Card shape and Interface (Bottom view)

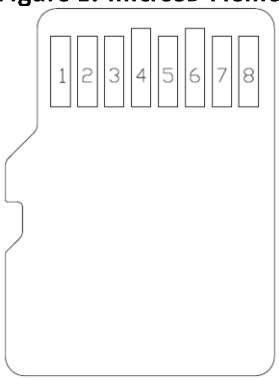


Table 11: Pad Assignment – SD Mode

Pin	SD Mode		
	Name	Type[7]	Description
1	DAT2[8]	I/O/PP	Data Line [Bit 2]
2	CD/DAT3[9]	I/O/PP[10]	Card Detect/ Data Line [Bit 3]
3	CMD	PP	Command/Response
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]
3	DAT1[11]	I/O/PP	Data Line [Bit 1]

Table 12: Pad Assignment – SPI Mode

Pin	SPI Mode		
	Name	Type[7]	Description
1	RSV		
2	CS	I[10]	Chip Select (neg true)
3	DI	I	Data In
4	VDD	S	Supply voltage
5	SCLK	I	Clock
6	VSS	S	Supply voltage ground
7	DO	O/PP	Data Out
8	RSV		

[7] S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers

[8] DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

[9] The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.

[10] At power up this line has a 50kOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

[11] DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).

6.2 Power up / Power down behavior and reset

6.2.1 Power up

When the voltage is ramped up the controller is ready (internal reset pin released) if the voltage reaches 1.65V. The host can start with communication 1ms after 2.7V is reached according the SDA specification.
That should perform 74 clock cycles and start with the sequence CMD0, CMD8, ACMD41 until card is ready as described in the SD specification 3.01.

6.2.2 Power down

When the power falls below 2.6V the controller stops the communication to the flash, but enables the flash to finish a started flash program operation (if voltage drop is not fast).

After next initialization the controller checks the last written data for consistency and refreshes the data. Either the new or the old data (if the write operation could not be finished) are available.

6.2.3 Power drop

If the voltage drops below 2.6V and rises again, the card preforms a reset. The card must be initialized like after a power on.

6.2.4 Operation below minimum voltage

If the card initialization is performed below the specified voltage of 2.7V, the card may be detected as 1MB card with no useful data. In this case the host should power off and on the card and start initialization above 2.7V.

6.3 DC characteristics

Measurements are not recommended operation conditions unless otherwise specified.

Table 13: DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{DD}	Operating Current Read		50	80	mA	@ 25°C
I_{DD}	Operating Current Write		60	80	mA	@ 25°C
I_{DD}	Background read and refresh[12]		80	110	mA	@ 25°C
I_{DD}	Pre-initialization Standby Current		5	15	mA	@ 25°C
I_{DD}	Post-initialization Standby Current[13]		2	10	mA	@ 25°C
I_{DD}	Post-initialization Standby Current[13]		5	15	mA	@ 85°C
I_{LI}	Input Leakage Current	-2		2	µA	without pull up R
I_{LO}	Output Leakage Current	-2		2	µA	without pull up R

Table 14: microSD Memory Card recommended operation conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply voltage	Normal operating status	2.7	3.3	3.6	V
-	Power Up Time (from 0V to V_{DD} min)				250	ms

6.4 Signal loading

According to SD specification

[12] The card can perform auto data read of the whole card to check for ECC errors and performs data refresh

[13] Before auto read the idle current is larger than the typical idle current after auto read

6.5 AC characteristics

6.5.1 Default speed mode (0-25MHz)

According to SD specification

6.5.2 High speed mode (0-50MHz)

According to SD specification

6.5.3 UHS modes

UHS modes were driven with a signal level of 1.8V.
The cards support following UHS-I modes:

Table 15: Supported UHS-I modes

Mode	Max. Burst MB/s	Max. Clock frequency MHz
SDR12	12.5	25
SDR25	25	50
SDR50	50	100
DDR50	50	50 (rising and falling edge)

7. Host access specification

The following chapters summarize how the host accesses the card:

- Chapter 7.1 summarizes the SD and SPI buses.
- Chapter 7.2 summarizes the registers.

7.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

7.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

7.1.2 SPI Bus Mode Protocol

The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional dataIn and dataOut signals.

Table 16: SPI Bus signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

7.1.3 Mode Selection

The microSD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in idle_state. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.
During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should restart the card as Multimedia Card using CMD0 and CMD1.

7.2 Card registers

The microSD Memory Card has the following registers.

Table 17: microSD Memory Card registers

Register name	Bit width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA[14]	16	Relative Card Address	This register carries the card address is SD Card mode.
SSR	512	SD Status	information about the card proprietary features and vendor specific life time information

Table 18: CID register

Register name	Bit width	Description	Function
MID	8	Manufacture ID	0x5d
OID	16	OEM/Application ID	0x5342
PNM	40	Product Name	("0008G") density
PRV	8	Product Revision	0xgg
PSN	32	Product Serial Number	xxxxxxxx
–	4	Reserved	0x0
MDT	12	Manufacture Date	0xyym
CRC	7	Check sum of CID contents	chksum
–	1	Not used; always=1	1

[14] RCA register is not available in SPI mode

Table 19: OCR register

OCR bit positon	VDD voltage windows	Typ. value	OCR bit position	VDD voltage window	Typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24	Switching to 1.8V accepted	1
13	2.5-2.6	0	25-29	Reserved	
14	2.6-2.7	0	30	Card Capacity Status (CCS)	*[15]
			31	0=busy; 1=ready	*[16]

[15] This bit is valid only when the card power up status bit is set

[16] This bit is set to LOW if the card has not finished the power up routine

Table 20: CSD register

Register name	Bits	Bit width	Description	Typ. value (max. 2GB)	Typ. value (>2GB)
CSD_STRUCTURE	127:126	2	CSD structure	00	01
–	125:120	6	Reserved	00000	00000
TAAC	119:112	8	Data read access time 1	00101111	00001110
NSAC	111:104	8	Data read access time 2 (CLK cycle)	00000000	00000000
TRAN_SPEED	103:96	8	Data transfer rate	00110010 Default speed 00001011 SDR 50 or other values	00110010 Default speed 00001011 SDR 50 or other values
CCC	95:84	12	Card command classes	010111110101	010110110101
READ_BL_LEN	83:80	4	Read data block length	1001	1001
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	1	0
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0	0
DSR_IMP	76	1	DSR implemented	0	0
–	75:74	2	Reserved	00	–
C_SIZE	73:62	12	Device size	xxx[17]	–
VDD_R_CURR_MIN	61:59	3	VDD min read current	111	–
VDD_R_CURR_MAX	58:56	3	VDD max read current	111	–
VDD_W_CURR_MIN	55:53	3	VDD min write current	111	–
VDD_W_CURR_MAX	52:50	3	VDD max write current	111	–
C_SIZE_MULT	49:47	3	Device size multiplier	111[17]	–
–	75:70	6	Reserved	–	000000
C_SIZE	69:48	22	Device size	–	xxx[17]
–	47	1	Reserved	–	0
ERASE_BLK_EN	46	1	Erase single block enable	1	1
SECTOR_SIZE	45:39	7	Erase sector size	1111111	1111111
WP_GRP_SIZE	38:32	7	Write protect group size	0000000	0000000
WP_GRP_ENABLE	31	1	Write protect group enable	1	0
–	30:29	2	Reserved	00	00
R2W_FACTOR	28:26	3	Write speed factor	010	010
WRITE_BL_LEN	25:22	4	Write data block length	1001[17]	1001[17]
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0	0

[17] Drive size and block sizes vary with card capacity

–	20:16	5	Reserved	00000	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(1)	0 W(1)
COPY	14	1	Copy flag	0 W(1)	0 W(1)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(1)	0 W(1)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W	0 W
FILE_FORMAT	11:10	2	File format	00 W(1)	00 W(1)
–	9:8	2	Reserved	00 W	00 W
CRC	7:1	7	Checksum of CSD contents	xxxxxxx W	xxxxxxx W
–	0	1	Always=1	1	1

≤2GB
memory capacity = BLOCKNR * BLOCK_LEN
Where
BLOCKNR = (C_SIZE+1) * MULT
MULT = $2^{C\_SIZE\_MULT+2}$ (C_SIZE_MULT < 8)
BLOCK_LEN = $2^{READ\_BL\_LEN}$, (READ_BL_LEN < 12)

>2GB
memory capacity = (C_SIZE+1) * 512kByte

W value can be changed with CMD27 (PROGRAM_CSD)
W(1) value can be changed ONCE with CMD27 (PROGRAM_CSD)

Table 21: SCR register

Field	Bits	Bit width	Typ. value	Remark
SCR_STRUCTURE	63:60	4	0000	SCR 1.01…2.00
SD_SPEC	59:56	4	0010	SD 2.0 or 3.0
DATA_STAT_AFTER_ERASE	55	1	1	data are oxFF after erase
SD_SECURITY	54:52	3	010 011	1.01 (SDSC) 2.00 (SDHC)
SD_BUS_WIDTHS	51:48	4	0101	1 or 4 bit
SD_SPEC3	47	1	1	yes→ SD3.0
EX_SECURITY	46:43	4	0000	no extended security
Reserved	42:34	9	0	0
CMD_SUPPORT	33:32	2	00 11	CMD23 / CMD20 not supported CMD23 / CMD20 supported
Reserved	31:0	32	0	0

Table 22: RCA register

Field	Bits	Bit width
RCA	16	0x0000[18]

[18] After initialization the card can change the RCA register

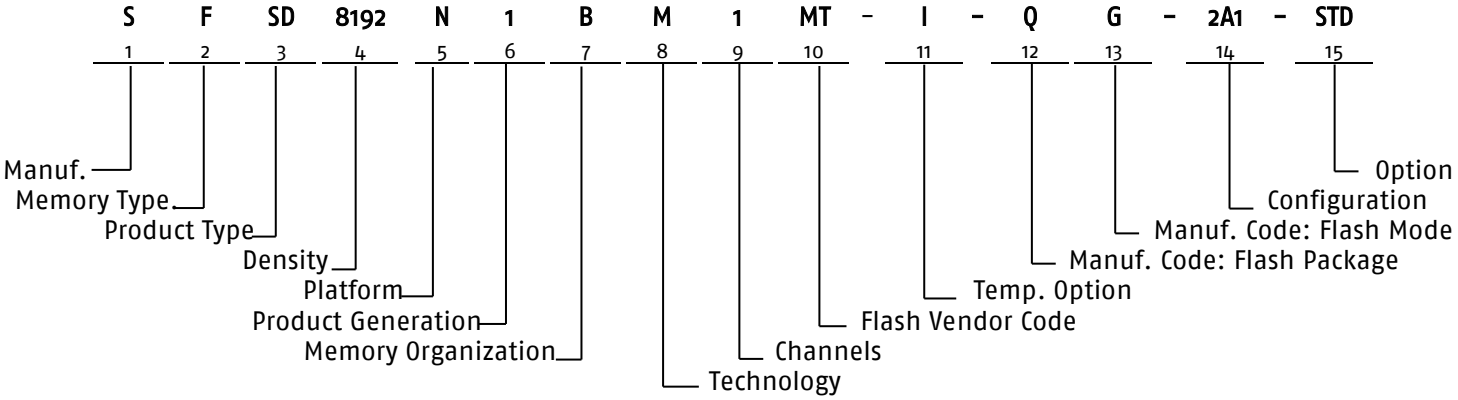
Table 23: SSR register

Field	Bits	Bit width	Typ. value	Remark
Data bus width	511:510	2	0x2[19]	4 bit width
Secured mode	509:509	1	0x0	not secured
Reserved for security	508:502	7	0x00	-
Reserved	501:496	6	0x00	-
SD card type	495:480	16	0x0000	Regular SD
Size protected area	479:448	32	0x03000000 0x04000000	48MB 64MB
Speed class	447:440	8	0x04	Class 10
Move performance	439:432	8	0x05 0x00	5 MB/s sequential write
Allocation unit size	431:428	4	0x7 0x9	1 MiB 4 MiB
Reserved	427:424	4	0x0	
Erase unit size	423:408	16	0x0001	1 AU
Erase unit timeout	407:402	6	0x01	1 second
Erase unit offset	401:400	2	0x1	1 seconds
UHS mode Speed Grade	399:396	4	0x1	10MB/s
Allocation unit size in UHS mode	395:392	4	0x7 0x9	1 MiB 4 MiB
Reserved	391:312	80		
Data structure version identifier, currently 1	311:304	8	0x01	version 1
Number of manufacturer marked defect blocks	303:288	16	0x0008	8 initial BB
Number of initial spare blocks (worst chip)	287:272	16	0x00bf	191 spare blocks
Number of initial spare blocks (sum over all chips)	271:256	16	0x017e	382 spare blocks
Percentage of remaining spare blocks (worst chip)	255:248	8	0x64[19]	100%
Percentage of remaining spare blocks (all chips)	247:240	8	0x64[19]	100%
Number of uncorrectable ECC errors (not including ECC errors during startup)	239:224	16	0x0000[19]	0 uncorrectable errors
Number of correctable ECC errors (not including ECC errors during startup)	223:192	32	0x0045074b[19]	4523851 correctable ECC errors
Lowest wear level class	191:176	16	0x0000[19]	0
Highest wear level class	175:160	16	0x0000[19]	0
Wear level threshold	159:144	16	0x01ff	512 block erases per WL class
Total number of block erases	143:96	48	0x00...1ff0[19]	8176 block erase commands
Number of flash blocks, in units of 256 blocks	95:80	16	0x0020	8192 flash blocks
Maximum flash block erase count target, in wear level class units	79:64	16	0x0075	Flash endurance 117 WL classes (59904 erases)
Power on count	63:32	32	0x00000003[19]	3x power on
Firmware version	31:0	32	0xYYMMDDXX	Firmware version

Bit 311:0 are vendor specific, example values in the table

[19] Value change in operation

8. Part Number Decoder



8.1 Manufacturer

Swissbit code	S

8.2 Memory Type

Flash	F

8.3 Product Type

SATA Interface	SD

8.4 Density

512 MByte	0512
1 GByte	1024
2 GByte	2048
4 GByte	4096
8 GByte	8192

8.5 Platform

microSD Memory Card	N

8.6 Product Generation

Generation	1
	2
	3

8.7 Memory Organization

x8	B

8.8 Technology

SD Memory Card controller (S-4xx platform)	M

8.9 Channels

1 Flash channel	1

8.10 Flash Code

Toshiba	T0
Micron	MT

8.11 Temperature Option

Extended Temperature Range: -25 °C to 85°C	E
Industrial Temperature Range: -40 °C to 85 °C	I

8.12 Die Classification

	S-4x MLC	S-4xx SLC
MONO (single die package)	G	M
DDP (dual die package)	L	D
QDP (quad die package)	H	Q
ODP (octal die package)	M	N

8.13 Pin Mode

Single nCE and Single R/nB	E
Dual nCE and Dual R/nB	F
Quad nCE and Quad R/nB	G

8.14 Configuration XYZ

X = Configuration

Configuration	X
Default, non UHS	1
UHS-I	2

Y = Firmware Revision

FW Revision	Y
Version 1	A
Version 2	B

Z = Optional

Optional	Z
Optional	1

8.15 Option

Swissbit/Standard	STD

9. Swissbit marking specification

9.1 Front side marking

Swissbit

Density

Micro SDHC Memory Card logo

9.2 Back side marking

Part Number

Calendar week and year
Lot code

10. Revision History

Table 24: Document Revision History

Date	Revision	Description	Revision Details
May 01, 2018	1.00	Initial release	Doc. req. no. 2180