

## MAX40080

## Precision, Fast Sample-Rate, Digital Current-Sense Amplifier

### General Description

The MAX40080 is a high-precision, fast-response, bi-directional current-sense amplifier with digital output and a very wide input common-mode range from -0.1V (ground sensing) to 36V.

The device features an ultra-low 5 $\mu$ V input offset voltage and a very low 0.2% gain error. The low input offset voltage is especially important because it allows using a small sense resistor, thus saving power dissipation, but at the same time not compromising the measurement accuracy. The device also features a programmable input sensing range between  $\pm 10$ mV and  $\pm 50$ mV (or programmable input gain between 125V/V and 25V/V) which is very useful to enhance accuracy at low current.

The device includes an analog-to-digital converter with a programmable sample rate and 12-bit resolution (13-bit including sign bit for current measurement) and features an I<sup>2</sup>C compliant and SMBus compatible interface.

The device features a wake-up current threshold and auto-shutdown mode when the I<sup>2</sup>C is inactive. Both these features are designed to minimize power consumption.

The device is available in a small 12-pin WLP (and also a 12-pin TDFN) and is specified over the -40°C to +125°C extended operating temperature range.

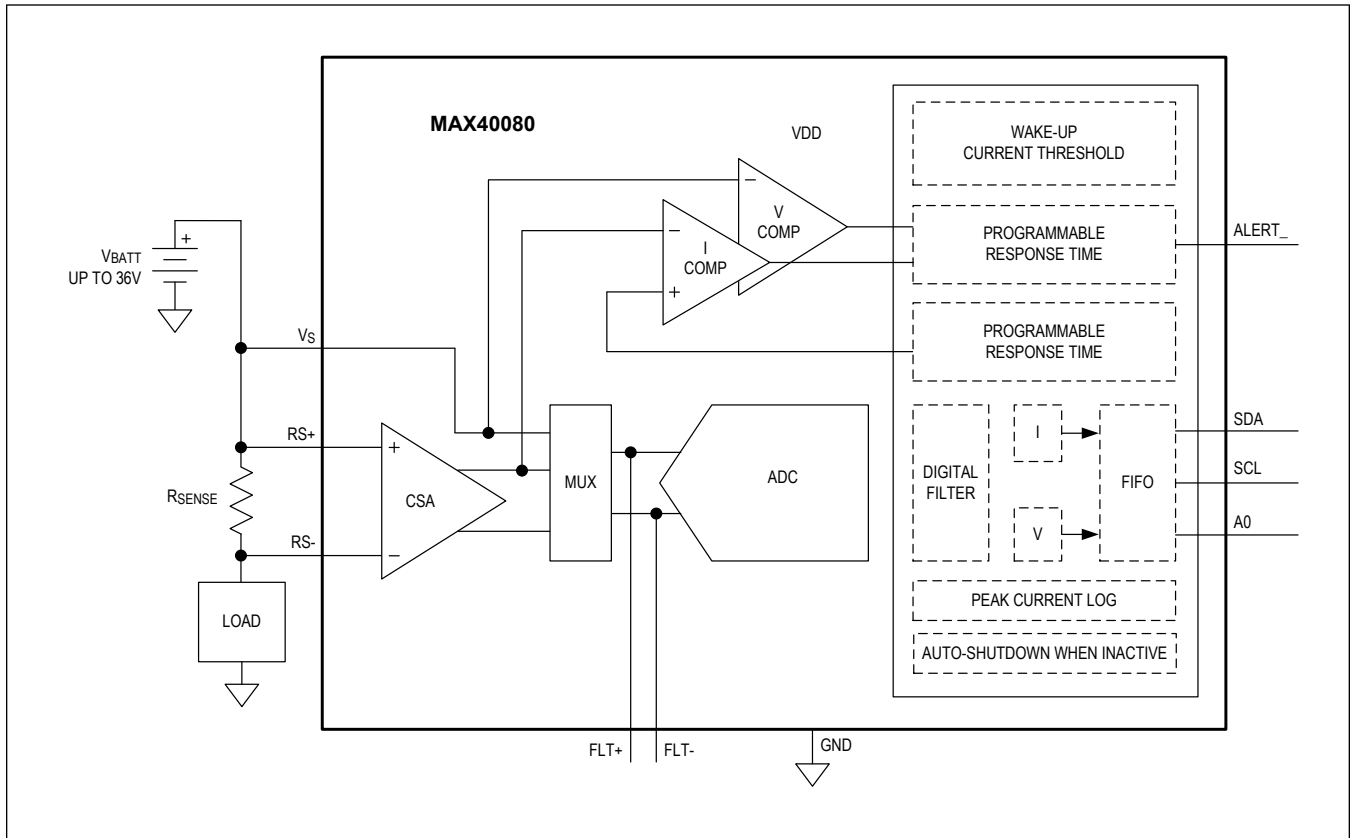
### Applications

- Server Backplanes
- Base-Station PA Control
- Telecom Equipment
- Battery Operated Devices
- Industrial Control and Automation

### Benefits and Features

- Programmable Sample Rate up to 1MSPS
- Wide Input Common-Mode range from -0.1V (ground sensing) to 36V
- Programmable Input Sense Range ( $\pm 10$ mV and  $\pm 50$ mV)
- Very low 5 $\mu$ V Input Offset Voltage allows using a small sense resistor
- I<sup>2</sup>C compliant and SMBus compatible interface with smart modes to save power:
  - Wake-up current threshold
  - Low 4 measurements/s rate
  - Auto-shutdown when I<sup>2</sup>C is inactive
- Bi-directional current sensing
- Common-Mode Voltage monitoring up to 36V
- Space-saving 12-bump WLP (0.4mm pitch) and 12-pin TDFN
- Peak current Log
- Programmable over-current/voltage thresholds and under-voltage threshold
- Alert output with programmable response time
- 64-cell deep FIFO

Block Diagram



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**Absolute Maximum Ratings**

$V_{DD}$ to GND.....	-0.3V to +2V	Continuous Power Dissipation (Multilayer Board) ( $T_A = +70^\circ\text{C}$ , derate 13.73mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ .) .....	1098.60mW
RS+ to RS- .....	$\pm 2\text{V}$	Operating Temperature Range .....	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
$V_S$ , RS+, RS- to GND.....	-0.3V to +40V	Junction Temperature .....	$+150^\circ\text{C}$
All other pins to GND .....	-0.3V to $V_{DD} + 0.3\text{V}$	Storage Temperature Range .....	$-40^\circ\text{C}$ to $+150^\circ\text{C}$
Continuous current into any input pin .....	10mA	Soldering Temperature (reflow) .....	$+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	N121D1+1S
Outline Number	<a href="#">21-100492</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction-to-Ambient ( $\theta_{JA}$ )	72.82°C/W
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ )	17.90°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

The drawing includes the following views and dimensions:

- TOP VIEW:** Shows a square package with a Pin 1 Indicator (+) at the top-left corner. Dimensions include E (width), D (height), and a marking 'AAAA'.
- FRONT VIEW:** Shows the package profile with dimensions A, A1, A2, A3, and A1. It includes a detail of a bump with a diameter of 0.05 mm and a shape 'S'.
- BOTTOM VIEW:** Shows a 2x2 grid of bumps. Dimensions include E1, SE, e, SD, D1, and  $\phi b$ . It includes a detail of a bump with a diameter of 0.05 mm and a shape 'AB'.
- SIDE VIEW:** Shows the package height with a reference to Note 7.
- COMMON DIMENSIONS TABLE:**

COMMON DIMENSIONS	
A	0.50 MAX
A1	0.19 ±0.03
A2	0.28 REF
A3	0.025 BASIC
b	∅0.27 ±0.03
D	1.268 ±0.025
E	1.698 ±0.025
D1	0.80 BASIC
E1	1.20 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

**NOTES:**

- Terminal pitch is defined by terminal center to center value.
- Outer dimension is defined by center lines between scribe lines.
- All dimensions in millimeter.
- Marking shown is for package orientation reference only.
- Tolerance is ± 0.02 unless specified otherwise.
- All dimensions apply to PbFree (+) package codes only.
- Front - side finish can be either Black or Clear.

**TITLE:** PACKAGE OUTLINE 12 BUMPS THIN WLP PKG. 0.4 mm PITCH, N121D1+1S

**APPROVAL:** [Signature] **DOCUMENT CONTROL NO.:** 21-100492 **REV.:** C

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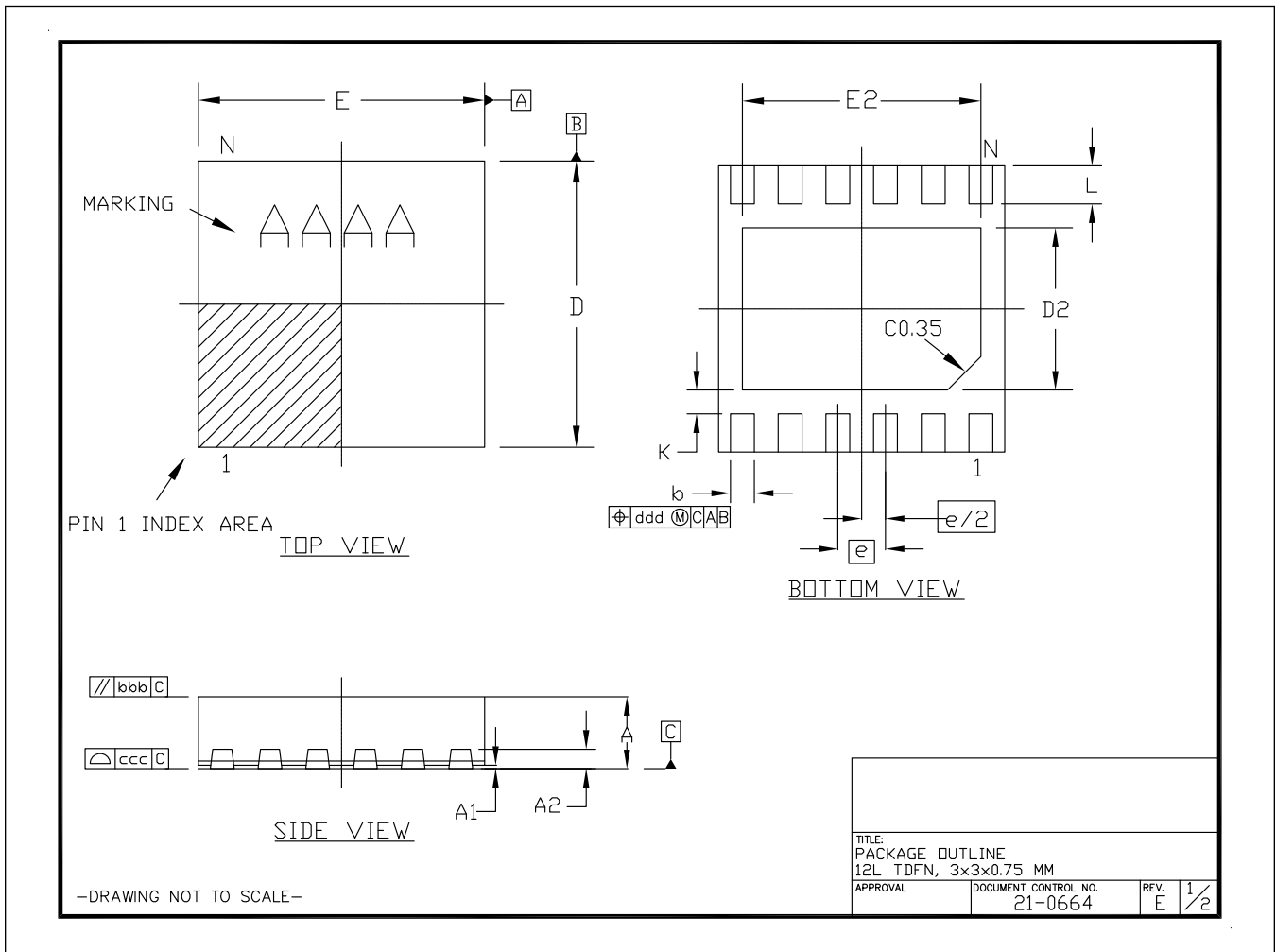


**TDFN\***

Package Code	TD1233+1C
Outline Number	<a href="#">21-0664</a>
Land Pattern Number	<a href="#">90-0397</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction-to-Ambient ( $\theta_{JA}$ )	63 °C/W
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ )	8.5 °C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction-to-Ambient ( $\theta_{JA}$ )	41 °C/W
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ )	8.5 °C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).



DIMENSIONAL REFERENCES							
	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8	0.7	0.75	0.8
STAND OFF	A1	0	0.035	0.05	0	0.035	0.05
L/F THICKNESS	A2	0.203 REF			0.203 REF		
LEAD WIDTH	b	0.2	0.25	0.3	0.2	0.25	0.3
BODY SIZE	D	2.9	3.0	3.1	2.95	3.00	3.05
	E	2.9	3.0	3.1	2.95	3.00	3.05
LEAD PITCH	e	0.5 BSC			0.5 BSC		
EP SIZE	D2	1.6	1.7	1.8	1.45	1.55	1.65
	E2	2.4	2.5	2.6	2.4	2.50	2.6
LEAD LENGTH	L	0.35	0.4	0.45	0.30	0.4	0.50
PACKAGE EDGE TOLERANCE	aaa	0.1			0.1		
MOLD FLATNESS	bbb	0.1			0.1		
COPLANARITY	ccc	0.08			0.08		
LEAD OFFSET	dld	0.1			0.1		
EXP PAD TO LEAD EDGE	K	0.25 min			0.25 min		
LEAD COUNT	N	12			12		
PKG CODE:		TD1233+1, TD1233+1C			TD1233+2, TD1233+2C,		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. WARPAGE SHALL NOT EXCEED 0.10 mm.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. COPLANARITY SHALL NOT EXCEED 0.08 mm.
5. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
6. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODES ONLY.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE 12L TDFN, 3x3x0.75 MM		
APPROVAL	DOCUMENT CONTROL NO. 21-0664	REV. E 2/2

## Electrical Characteristics

( $V_{DD} = 1.8V$ ,  $V_{RS+} = V_{RS-} = +12V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $V_S = +12V$ ,  $T_A = +25^\circ C$ , minimum and maximum limits are from  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CURRENT MEASUREMENT</b>						
Input Common Mode Range	$V_{CM}$		-0.1		36	V
Input Voltage Sense	$V_{SENSE}$	(RS+ - RS-), Option #1 programmable with I <sup>2</sup> C		±50		mV
		(RS+ - RS-), Option #2 programmable with I <sup>2</sup> C		±10		
CSA Gain	G	$V_{SENSE} = \pm 10mV$ , Option #1 programmable with I <sup>2</sup> C		125		V/V
		$V_{SENSE} = \pm 10mV$ , Option #1 programmable with I <sup>2</sup> C		25		
Input Offset Voltage (CSA only)	$V_{OS}$	$T_A = +25^\circ C$		5	20	µV
		$-40^\circ C \leq T_A \leq +125^\circ C$		5	45	
Input Offset Voltage (CSA + ADC)	$V_{OS}$	$T_A = +25^\circ C$		5	25	µV
		$-40^\circ C \leq T_A \leq +125^\circ C$		5	55	µV
Input Offset Drift	$TCV_{OS}$			50		nV/°C
Input Bias Current	$I_B$	$-40^\circ C \leq T_A \leq +125^\circ C$		1	20	nA
Gain Error (CSA only)	GE	$T_A = +25^\circ C$		0.2	0.55	%
		$-40^\circ C \leq T_A \leq +125^\circ C$		0.2	0.75	
Gain Error (CSA + ADC)	GE	$T_A = +25^\circ C$		0.05	0.5	%
		$-40^\circ C \leq T_A \leq +125^\circ C$		0.05	1.05	
Common Mode Rejection Ratio (CSA only)	CMRR		123	140		dB
Common Mode Rejection Ratio (CSA + ADC)	CMRR		119	140		dB
Power Supply Rejection Ratio (CSA only)	PSRR		76	110		dB
Power Supply Rejection Ratio (CSA + ADC)	PSRR		76	110		dB
Input Voltage-Noise Density	$V_N$	$V_{SENSE} = (V_{RS+} - V_{RS-}) = 50mV$ $f = 1kHz$		47		nV/√Hz
Small Signal Bandwidth	BW	$V_{SENSE} = (V_{RS+} - V_{RS-}) = \pm 50mV$		50		kHz
		$V_{SENSE} = (V_{RS+} - V_{RS-}) = \pm 10mV$		10		
Wake-up and Over-Current Thresholds Resolution		$V_{SENSE} = \pm 50mV$		0.78		mV
Wake-up Response Time		Sampling Rate = 15ksps		32.7		ms
Over-Current Response Time		Unfiltered (D4 = 0)		31		µs
		Filtered (D4 = 1), Sample Rate = 15ksps		294		
		Filtered (D4 = 1), Sample Rate = 60ksps		88		
		Filtered (D4 = 1), Sample Rate = 1Msps		35		

**Electrical Characteristics (continued)**

( $V_{DD} = 1.8V$ ,  $V_{RS+} = V_{RS-} = +12V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $V_S = +12V$ ,  $T_A = +25^\circ C$ , minimum and maximum limits are from  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT VOLTAGE MEASUREMENT</b>						
Input Voltage Range	$V_S$		0		36	V
Voltage Buffer Gain	G			1/30		V/V
Input Offset Voltage (Voltage Buffer only)	$V_{OS}$	Referred to $V_S$ , $V_S = 1.2V$		1.5	21	mV
Input Offset Voltage (Voltage Buffer + ADC)	$V_{OS}$	Referred to $V_S$ , $V_S = 1.2V$		1.5	35	mV
Gain Error (Voltage Buffer only)	GE			0.05	0.4	%
Gain Error (Voltage Buffer + ADC)	GE			0.2	1.2	%
Input Voltage Signal Bandwidth	BW			1		kHz
Over/Under-Voltage Thresholds Resolution		Referred to $V_S$		0.586		V
Input Impedance	$Z_{IN}$			6.5		M $\Omega$
Over/Under-Voltage Response Time		Unfiltered (D4 = 0) Filtered (D4 = 1), Sample Rate = 15ksps Filtered (D4 = 1), Sample Rate = 60ksps Filtered (D4 = 1), Sample Rate = 1Msps		31 294 88 35		$\mu s$
<b>ADC CHARACTERISTICS</b>						
Sample Frequency	$f_S$	Programmable through I <sup>2</sup> C	15		1,000	Ksps
Resolution		(Note 2)		12		bits
Internal Reference Voltage	$V_{REF}$			1.25		V
Switching Time	$t_S$	From current to voltage measurement or vice-versa		1		ms
<b>I<sup>2</sup>C TIMING (UP TO 1MHz) (Note 3)</b>						
Serial Clock Frequency	$f_{SCL}$				1	MHz
Bus Free Time Between Start and Stop Conditions	$t_{BUF}$		0.5			$\mu s$
START Condition Hold Time	$t_{HD:STA}$		0.26			$\mu s$
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA	0.26			$\mu s$
Clock Low Period	$t_{LOW}$		0.5			$\mu s$
Clock High Period	$t_{HIGH}$		0.26			$\mu s$
START Condition Setup Time	$t_{SU:STA}$	90% of SCL to 90% of SDA	0.26			$\mu s$
Data Setup Time	$t_{SU:DAT}$	10% of SDA to 10% of SCL	50			ns
Data In Hold Time	$t_{HD:DAT}$	10% of SCL to 10% of SDA	0			$\mu s$

**Electrical Characteristics (continued)**

( $V_{DD} = 1.8V$ ,  $V_{RS+} = V_{RS-} = +12V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $V_S = +12V$ ,  $T_A = +25^\circ C$ , minimum and maximum limits are from  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Receive SCL/ SDA Rise Time	$t_R$	(Note 3)		20 + 0.1 $C_B$		ns
Maximum Receive SCL/ SDA Rise Time	$t_R$	(Note 3)		120		ns
Minimum Receive SCL/ SDA Fall Time	$t_F$	(Note 3)		20 + 0.1 $C_B$		ns
Maximum Receive SCL/ SDA Fall Time	$t_F$	(Note 3)		120		ns
Transmit SDA Fall Time	$t_F$	Bus capacitance = 550pF.			120	ns
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter				50		ns
Capacitive Load for Each Bus Line	$C_B$			550		pF
<b>I<sup>2</sup>C TIMING (HS MODE UP TO 3.4MHz) (Note 3)</b>						
Serial Clock Frequency	$f_{SCL}$				3.4	MHz
START Condition Hold Time	$t_{HD:STA}$		160			ns
START Condition Setup Time	$t_{SU:STA}$	90% of SCL to 90% of SDA	160			ns
Clock Low Period	$t_{LOW}$		160			ns
Clock High Period	$t_{HIGH}$		60			ns
Data Setup Time	$t_{SU:DAT}$	10% of SDA to 10% of SCL	10			ns
Data In Hold Time	$t_{HD:DAT}$	10% of SCL to 10% of SDA		35		ns
Minimum Receive SCL/ SDA Rise Time	$t_R$	(Note 3)		20 + 0.1 $C_B$		ns
Maximum Receive SCL/ SDA Rise Time	$t_R$	(Note 3)		120		ns
Minimum Receive SCL/ SDA Fall Time	$t_F$	(Note 3)		20 + 0.1 $C_B$		ns
Maximum Receive SCL/ SDA Fall Time	$t_F$	(Note 3)		120		ns
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA	160			ns
Capacitive Load for Each Bus Line	$C_B$			100		pF
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter				10		ns
<b>LOGIC (SDA, SCL, A0, ALERT_) DC CHARACTERISTICS</b>						
Input High Voltage	$V_{IH}$		0.7 x $V_{DD}$		$V_{DD} +$ 0.3	V

**Electrical Characteristics (continued)**

( $V_{DD} = 1.8V$ ,  $V_{RS+} = V_{RS-} = +12V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $V_S = +12V$ ,  $T_A = +25^\circ C$ , minimum and maximum limits are from  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Low Voltage	$V_{IL}$			-0.3		$0.3 \times V_{DD}$	V
Input High Leakage Current	$I_{IH}$	Logic Input to $DV_{DD}$		-1	$\pm 0.005$	+1	$\mu A$
Input Low Leakage Current	$I_{IL}$	Logic Input to 0V		-1	$\pm 0.005$	+1	$\mu A$
Input Capacitance	$C_{IN}$				5		pF
Output Low Voltage	$V_{OL}$	$I_{OL} = 3mA$		0		0.3	V
Output High Leakage Current		$V_{OUT} = V_{DD}$			$\pm 0.005$	1	$\mu A$
<b>POWER SUPPLY</b>							
Supply Voltage Range	$V_{DD}$	Guaranteed by PSRR		1.71		1.98	V
Active Power Supply Current	$I_{ACTIVE}$	Active mode, I <sup>2</sup> C inactive	$-40^\circ C \leq T_A \leq +125^\circ C$		2700	3500	$\mu A$
Low-Power Mode Supply Current	$I_{LP}$	I <sup>2</sup> C inactive, ADC is shutdown, current-sense takes one measurement every 50ms	$-40^\circ C \leq T_A \leq +125^\circ C$		52	85	$\mu A$
Average Supply Current in Selected Active Mode	$I_{AVE}$	I <sup>2</sup> C inactive, 4 conversions/s	$-40^\circ C \leq T_A \leq +125^\circ C$		41	65	$\mu A$
		I <sup>2</sup> C inactive, 1 conversions/s	$-40^\circ C \leq T_A \leq +125^\circ C$ (Note 3)		18	38	
		I <sup>2</sup> C inactive, 0.25 conversions/s	$-40^\circ C \leq T_A \leq +125^\circ C$ (Note 3)		14	27	
		I <sup>2</sup> C inactive, 0.0625 conversions/s	$-40^\circ C \leq T_A \leq +125^\circ C$ (Note 3)		13	23	
Standby Supply Current	$I_{SDBY}$	In Standby and between conversions, I <sup>2</sup> C bus inactive	$-40^\circ C \leq T_A \leq +125^\circ C$		2.7	15	$\mu A$
Turn-On Time	$t_{EN}$	In Low-Power Mode, analog current-sense wakes up every 50ms. Measured current is below programmed value in "Wakeup Current" register			300		$\mu s$
		From Low-Power Mode to Active Mode. From Standby to either Active Mode or Selected Active Mode or Single Measurement Mode			500		
Power-On Time	$t_{ON}$	$V_{DD} = 0V$ to 1.8V			100		ms

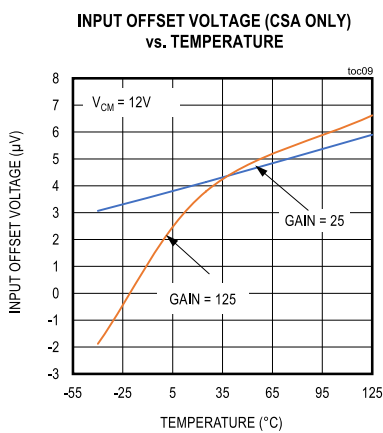
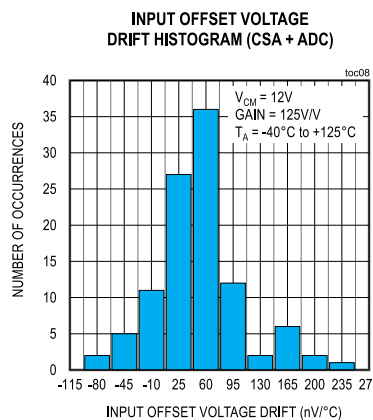
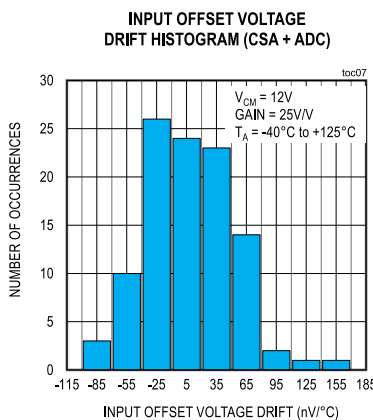
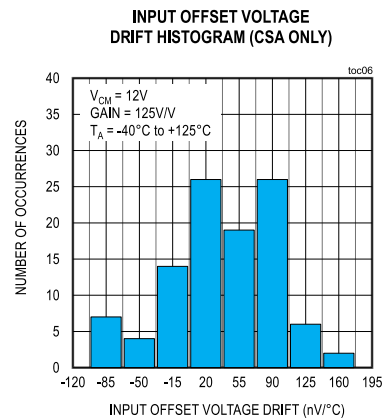
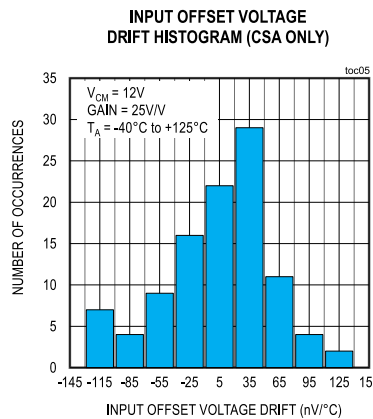
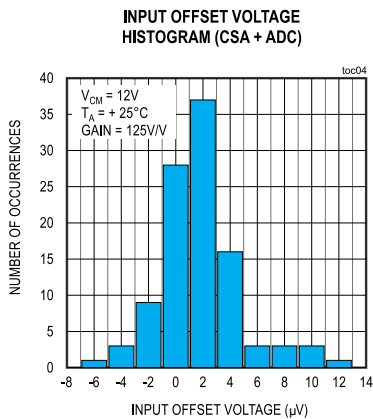
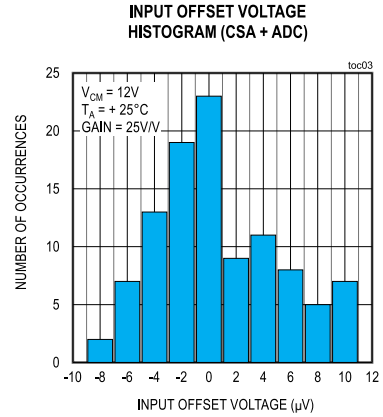
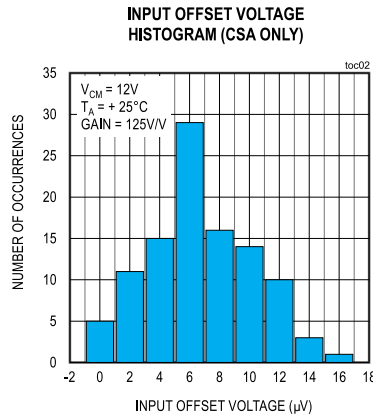
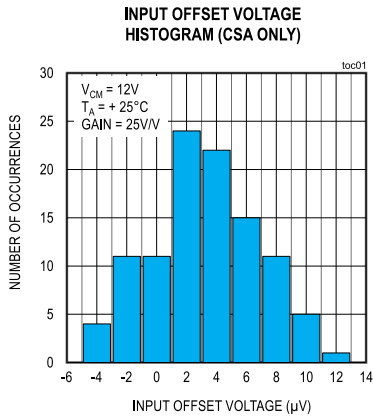
**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Specifications over temperature limits are guaranteed by design and characterization.

**Note 2:** 12 bit data + 1bit sign bit for current measurement.

**Note 3:** Guaranteed by design.

Typical Operating Characteristics

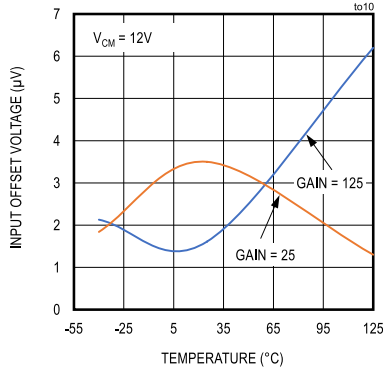
( $V_{DD} = 1.8V$ ,  $V_{RS+} = V_{RS-} = +12V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $V_S = +12V$ ,  $T_A = +25^\circ C$ , minimum and maximum limits are from  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted.)



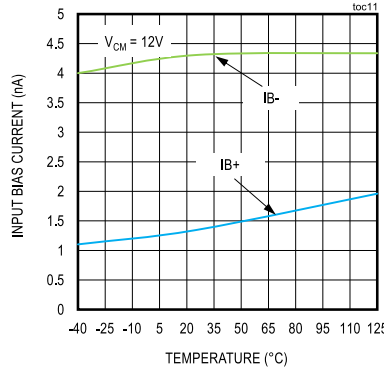
Typical Operating Characteristics (continued)

( $V_{DD} = 1.8V$ ,  $V_{RS+} = V_{RS-} = +12V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $V_S = +12V$ ,  $T_A = +25^\circ C$ , minimum and maximum limits are from  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted.)

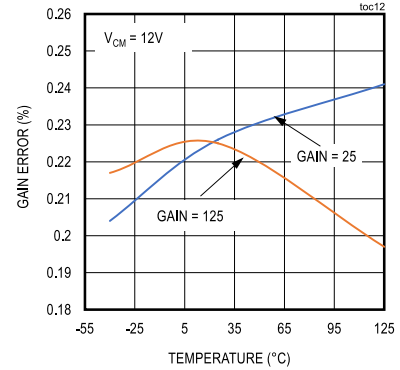
INPUT OFFSET VOLTAGE (CSA + ADC) vs. TEMPERATURE



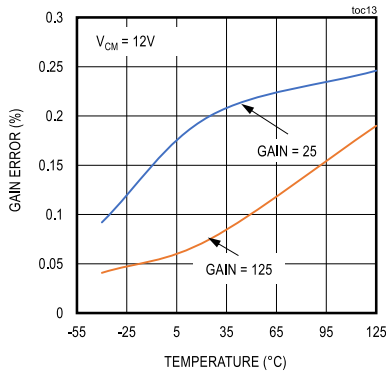
INPUT BIAS CURRENT vs. TEMPERATURE



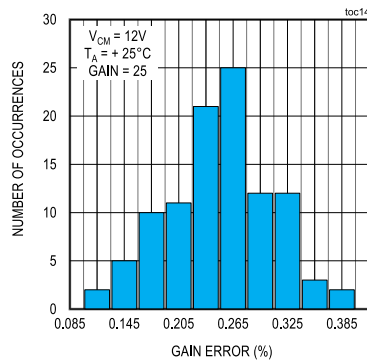
GAIN ERROR (CSA ONLY) vs. TEMPERATURE



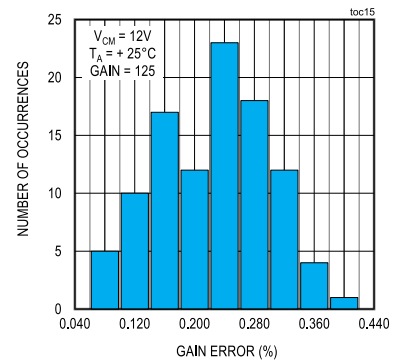
GAIN ERROR (CSA + ADC) vs. TEMPERATURE



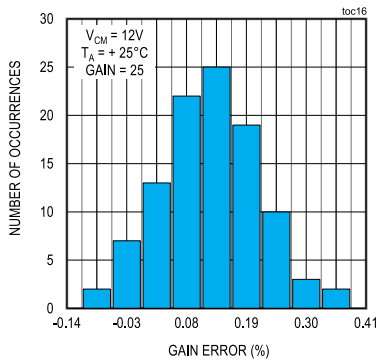
GAIN ERROR HISTOGRAM (CSA ONLY)



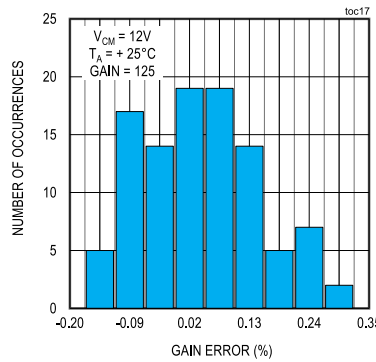
GAIN ERROR HISTOGRAM (CSA ONLY)



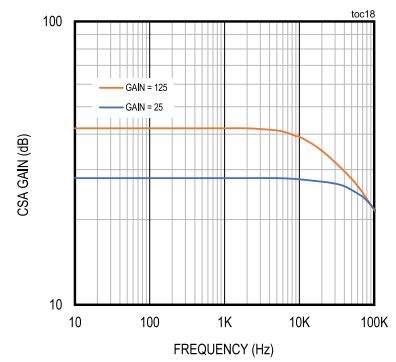
GAIN ERROR HISTOGRAM (CSA + ADC)



GAIN ERROR HISTOGRAM (CSA + ADC)



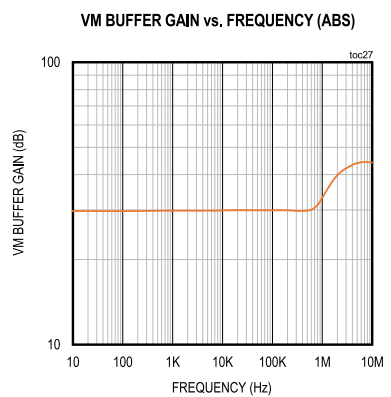
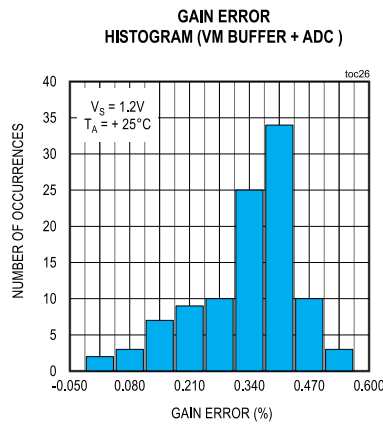
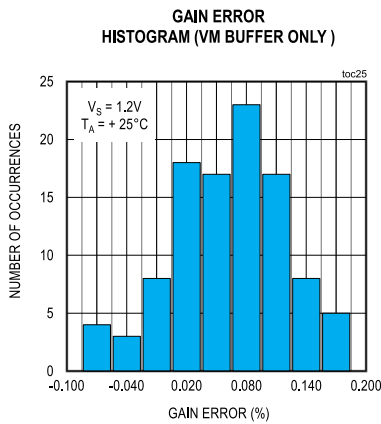
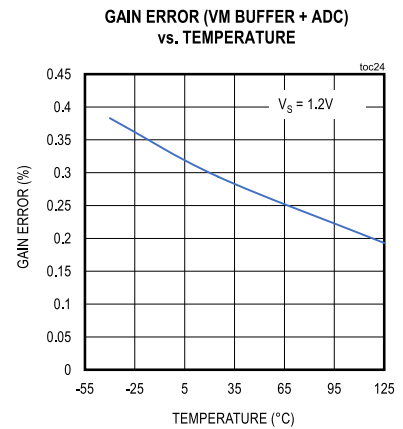
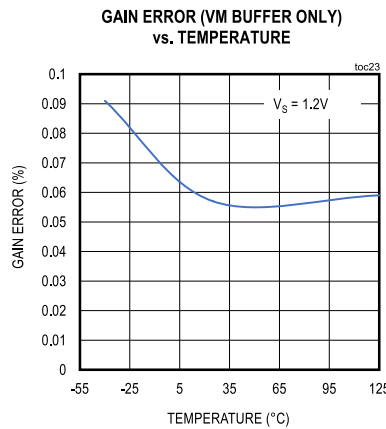
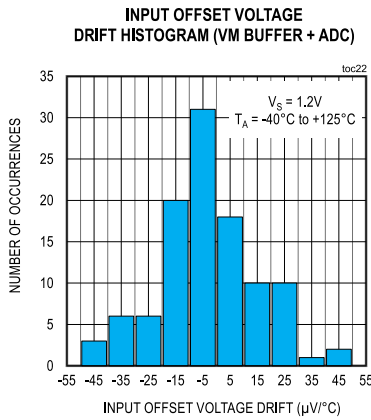
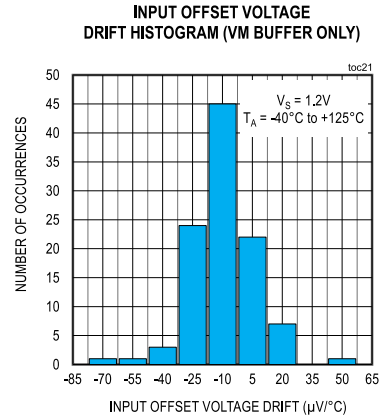
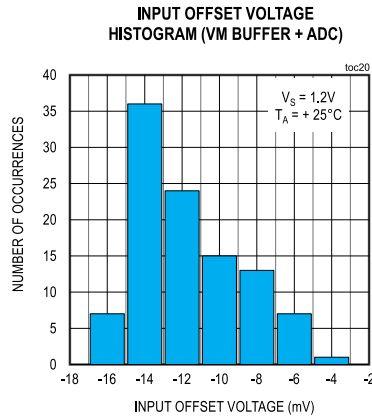
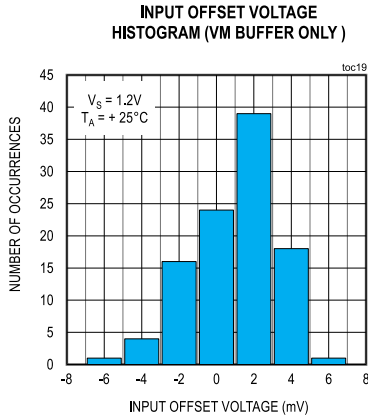
CSA GAIN vs. FREQUENCY





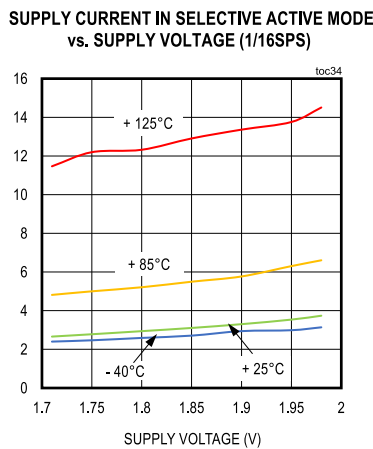
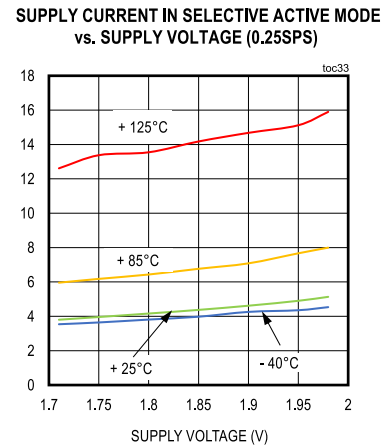
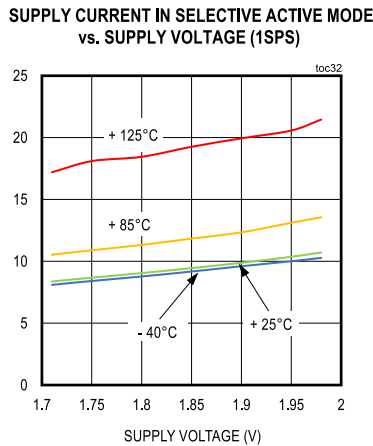
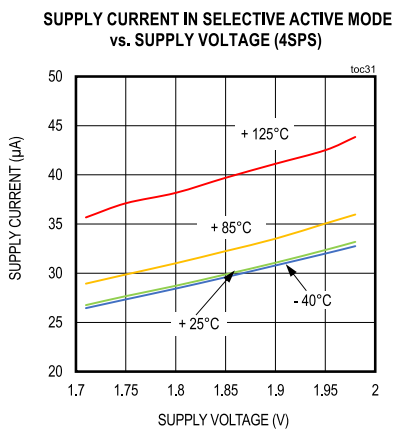
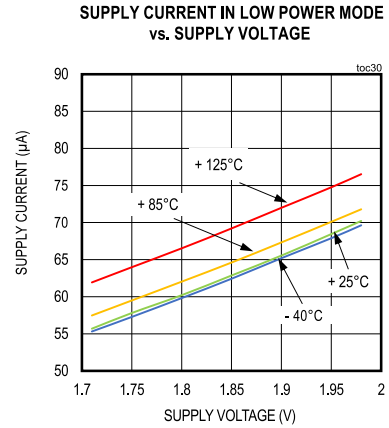
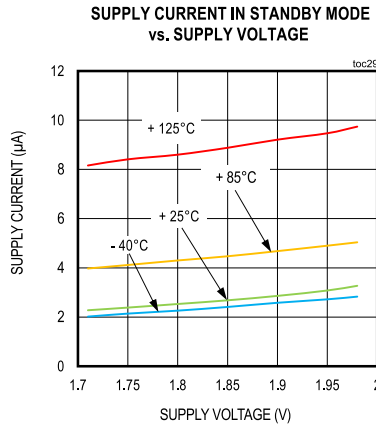
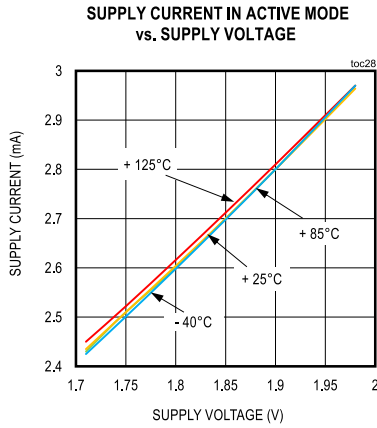
Typical Operating Characteristics (continued)

( $V_{DD} = 1.8V$ ,  $V_{RS+} = V_{RS-} = +12V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $V_S = +12V$ ,  $T_A = +25^\circ C$ , minimum and maximum limits are from  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted.)



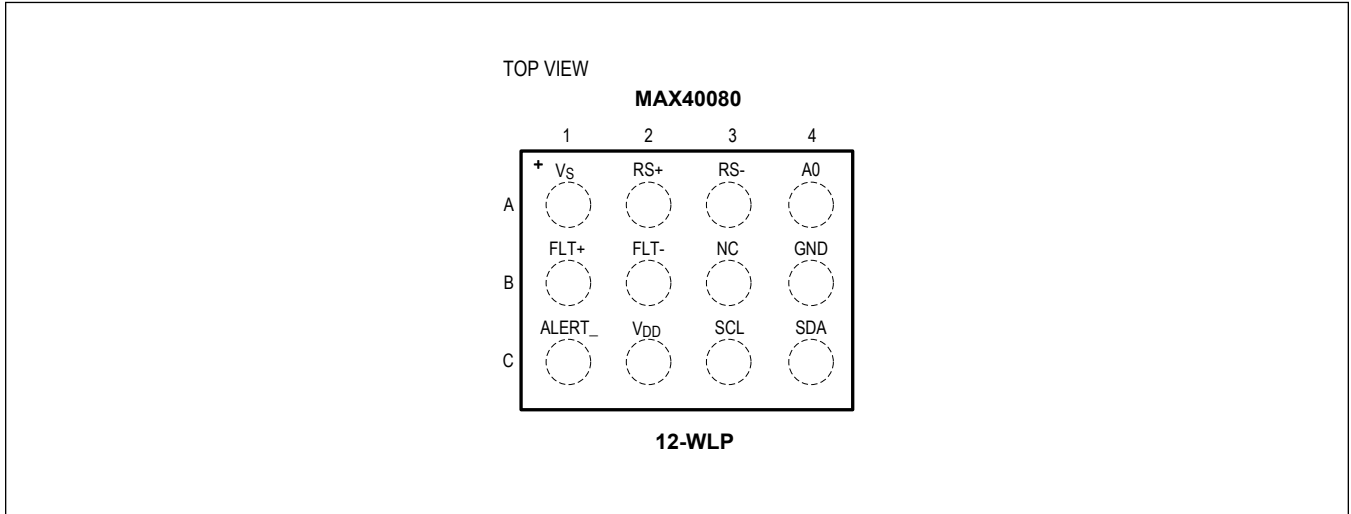
Typical Operating Characteristics (continued)

( $V_{DD} = 1.8V$ ,  $V_{RS+} = V_{RS-} = +12V$ ,  $V_{SENSE} = (V_{RS+} - V_{RS-}) = 0V$ ,  $V_S = +12V$ ,  $T_A = +25^\circ C$ , minimum and maximum limits are from  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted.)

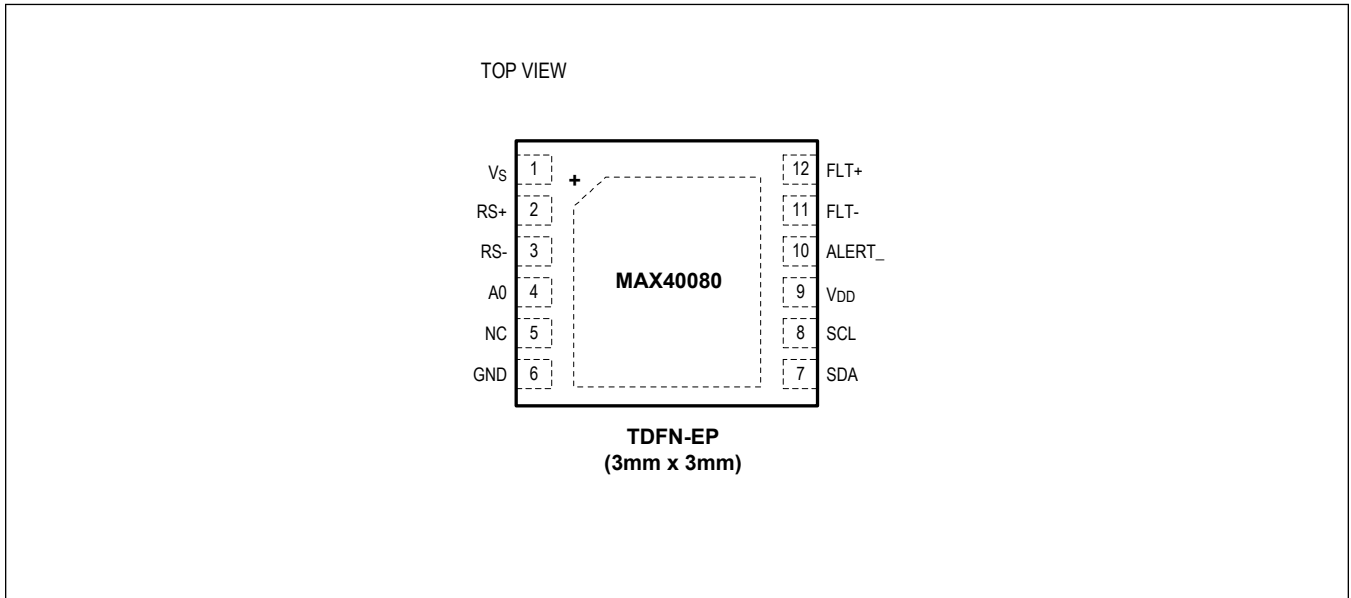


Pin Configurations

WLP-12



TDFN



## Pin Description

PIN		NAME	FUNCTION
WLP-12	TDFN		
A1	1	V <sub>S</sub>	Input Voltage Sense
A2	2	RS+	Positive Current-Sensing Input
A3	3	RS-	Negative Current-Sensing Input
A4	4	A0	Address Input. Connect to the external resistor
B1	12	FLT+	Connect a capacitor between FLT+ and FLT- to limit the input signal bandwidth.
B2	11	FLT-	Connect a capacitor between FLT+ and FLT- to limit the input signal bandwidth
B3	5	NC	Do Not Connect
B4	6	GND	Ground
C1	10	ALERT_	I <sup>2</sup> C Interrupt/Alert Output (active low)
C2	9	V <sub>DD</sub>	Analog Positive Supply Voltage
C3	8	SCL	I <sup>2</sup> C Clock
C4	7	SDA	I <sup>2</sup> C Data

### Detailed Description

The MAX40080 measures current and common-mode voltage and converts the data into digital form. It is an I<sup>2</sup>C-compatible two-wire serial interface that allows access to conversion results. Standard I<sup>2</sup>C commands allow reading the data and configuring other operating characteristics. While reading the current/voltage registers, any changes in measured current and voltage are ignored until the read is completed. The current/voltage register is updated for the new measurement upon completion of the read operation.

### I<sup>2</sup>C-Compliant and SMBus-Compatible Bus Interface

A standard I<sup>2</sup>C-compliant 2-wire serial interface reads current/voltage data from the current and voltage registers. It also reads and writes control bits to/from the configuration registers. In addition, the interface supports useful SMBus functions, including selectable Packet Error Checking (PEC). SMBus timeout is not supported which makes this SMBus interface, compatible but not fully compliant.

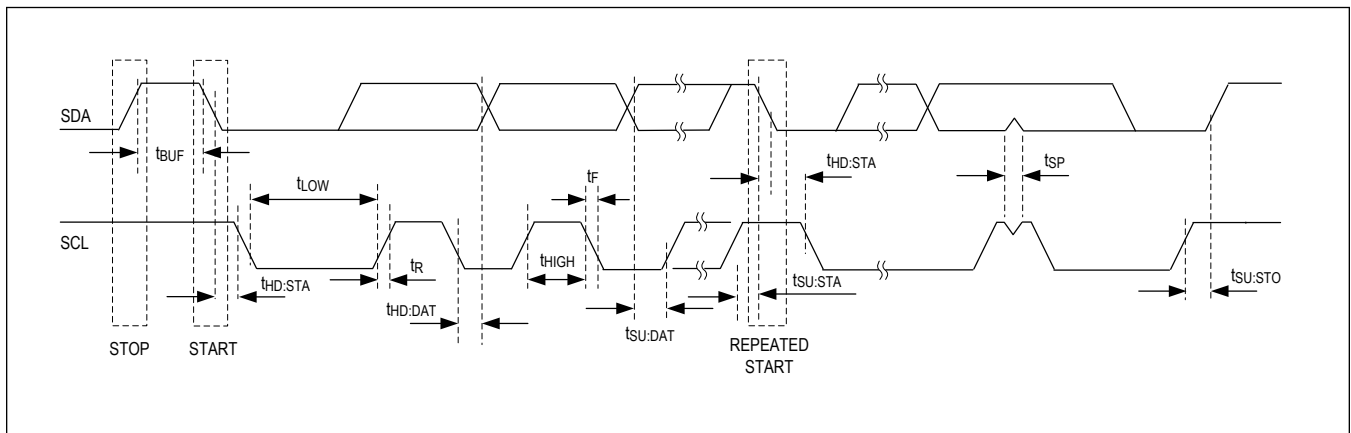


Figure 1. I<sup>2</sup>C/SMBus Timing Diagram

Normal transactions consist of 2-byte writes and reads. However, some registers are single-byte read and one register is 4-byte read. An additional byte will be appended when PEC is enabled. Attempting longer transactions is not recommended. A transaction always begins with a START (S) condition followed by the slave address and the Write/Read bit.

A 2-byte write transaction (Write Word) begins with the master generating a START condition and then transmitting the MAX40080's slave address followed by the Write bit. The device acknowledges with an ACK (A) bit, and the master transmits the target register, followed by another ACK from the MAX40080. The master then writes the two data bytes, and the MAX40080 ACKs each. The master ends the transaction by generating a STOP (P) condition. Writing more bytes (not recommended) will simply overwrite the register (e.g., DATA LOW - DATA HIGH - DATA LOW - DATA HIGH for a 4-byte write).

DIRECTION	M → S	M → S	M → S	S → M	M → S	S → M	M → S	S → M	M → S	S → M	M → S
BITS	1	7	1	1	8	1	8	1	8	1	1
CONTENT	S	SLAVE ADDRESS	WR	A	REGISTER SELECT	A	DATA BYTE [7:0]	A	DATA BYTE [15:8]	A	P

Figure 2. 2-Byte Write (Write Word)

When Packet Error Checking (PEC) is enabled, the write transaction is similar, except that the PEC byte (calculated using SLAVE ADDRESS, REGISTER ADDRESS, DATA LOW, and DATA HIGH) is appended by the master after the

ACK bit that follows the second data byte. Any attempted write that is not a multiple of three bytes will be ignored. If more than one set of three bytes is written, the PEC byte is calculated using the bytes listed above, plus the first PEC byte and the second DATA LOW and DATA HIGH bytes. Again, writing more than three bytes with PEC enabled is not recommended.

DIRECTION	M → S	M → S	M → S	S → M	M → S	S → M	M → S	S → M	M → S	S → M	M → S	S → M	M → S
BITS	1	7	1	1	8	1	8	1	8	1	8	1	1
CONTENT	S	SLAVE ADDRESS	WR	A	REGISTER SELECT	A	DATA BYTE [7:0]	A	DATA BYTE [15:8]	A	PEC BYTE	A	P

Figure 3. 2-Byte Write with PEC Byte

A 2-byte read (Read Word) is slightly more complex than a write. After transmitting the register byte and receiving an ACK from the device, the master generates a REPEAT START (Sr) and writes the address and a Read bit. The device then ACKs the address/read a byte and transmits the two data bytes. The master ACKs the first and NACKs the second, signaling that the transaction is complete, and then generates the STOP condition.

DIRECTION	M → S	M → S	M → S	S → M	M → S	S → M						
BITS	1	7	1	1	8	1						
CONTENT	S	SLAVE ADDRESS	WR	A	REGISTER SELECT	A						

...

M → S	M → S	M → S	S → M	S → M	M → S	S → M	M → S	M → S
1	7	1	1	8	1	8	1	1
Sr	SLAVE ADDRESS	Rd	A	DATA BYTE [7:0]	A	DATA BYTE [15:8]	N	P

Figure 4. 2-Byte Read (Read Word)

When Packet Error Checking (PEC) is enabled, the read transaction is similar, except that the PEC byte is appended by the device after the ACK bit that follows the second data byte.

DIRECTION	M → S	M → S	M → S	S → M	M → S	S → M						
BITS	1	7	1	1	8	1						
CONTENT	S	SLAVE ADDRESS	WR	A	REGISTER SELECT	A						

...

M → S	M → S	M → S	S → M	S → M	M → S	S → M	M → S	S → M	M → S	M → S
1	7	1	1	8	1	8	1	8	1	1
Sr	SLAVE ADDRESS	Rd	A	DATA BYTE [7:0]	A	DATA BYTE [15:8]	A	PEC BYTE	N	P

Figure 5. 2-Byte Read with PEC Byte

A one-byte read without and with PEC is similar to the Read Word above, but only one byte is read, as shown in [Figure 6](#) and [Figure 7](#).

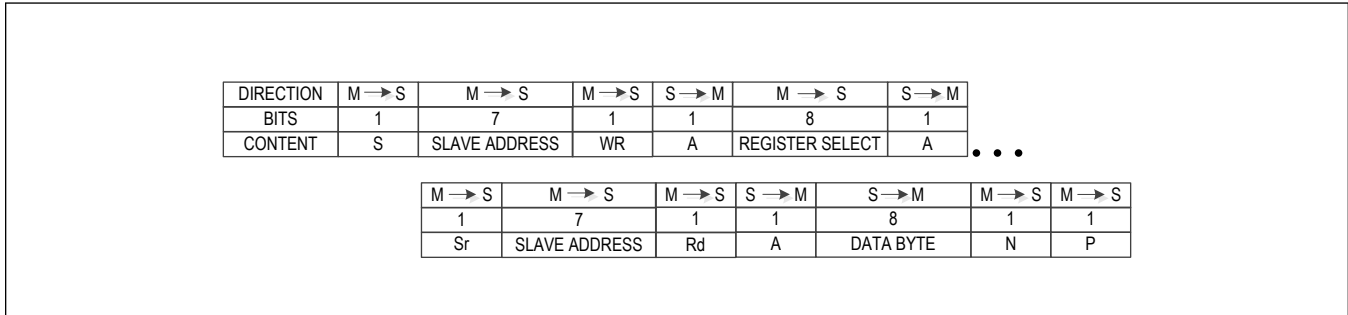


Figure 6. One-Byte Read

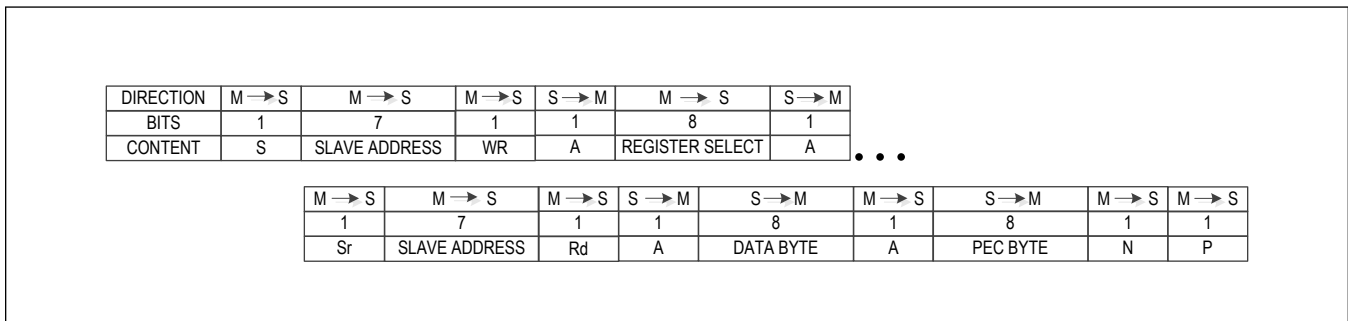


Figure 7. One-Byte Read with PEC

**Read 32 Protocol:** The Read 32 protocol is used with commands that require reading up to 32 bits (4 bytes) of data from a slave device. For MAX40080 this only applies to register Current\_Voltage\_Measurement. This protocol can be used to read less than 32 bits, but the packet must be padded to fill 32 bits. Data or meaningful bits are packed into the lower order bits and unused higher-order bits are filled with zeros. For example, a 20-bit value is transmitted in bits [19:0] with the most significant bit in bit [19]. Bits [31:20] are all zeros.

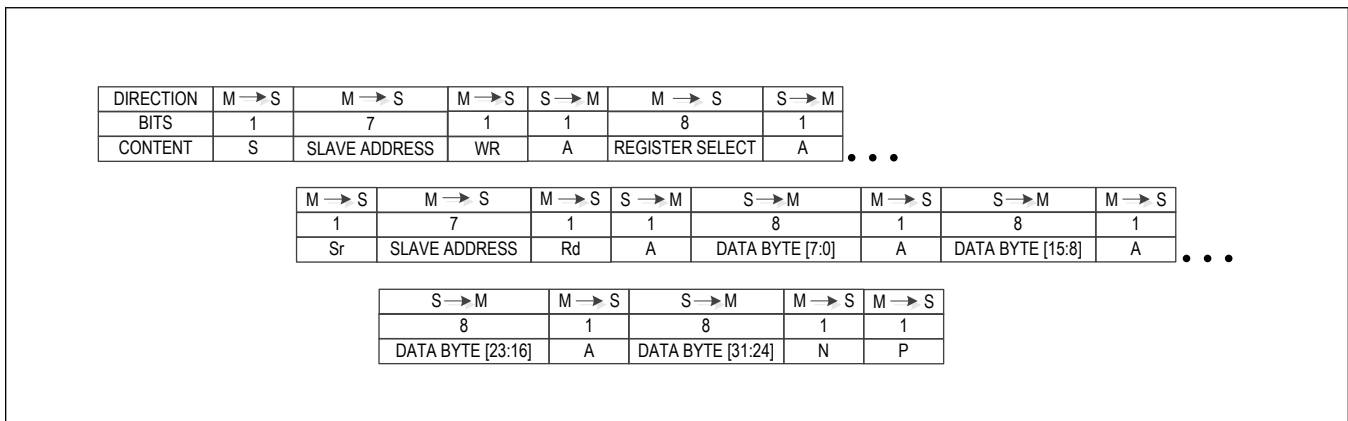


Figure 8. Read 32

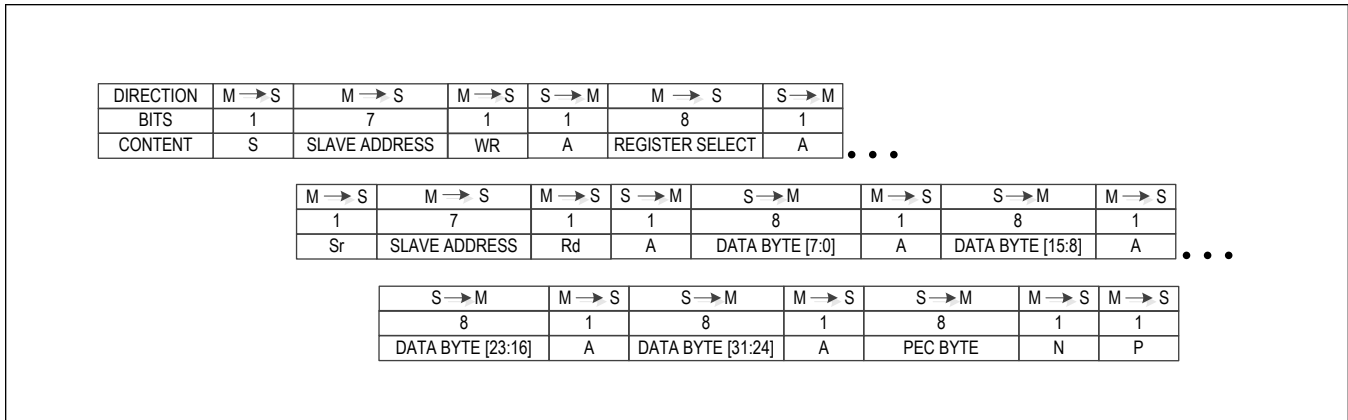


Figure 9. Read 32 with PEC

### I<sup>2</sup>C Slave Address

The MAX40080 has a unique I<sup>2</sup>C slave address selection method based on a single resistor connected to the A0 input pin. Such a resistor-based method has many benefits, including lower cost and smaller size, as well as allowing the users to stock just one part in their inventory system and use it in multiple projects with different I<sup>2</sup>C addresses just by changing a single standard 1% resistor. Select the resistor value by choosing the desired I<sup>2</sup>C address. See [Table 1](#).

32 different resistor values that correspond to 32 addresses, which are encoded by the 5 least significant bits. The two most significant bits of the address word (A<sub>6</sub>, A<sub>5</sub>) are fixed, two options A<sub>6</sub> = 0, A<sub>5</sub> = 1 or A<sub>6</sub> = 1, A<sub>5</sub> = 0 are available to be chosen at factory final test via OTP. Default value is A<sub>6</sub> = 0, A<sub>5</sub> = 1. Note that the part will monitor the resistor value at A0 pin continuously, if the resistor value changes after the part are powered up, the I<sup>2</sup>C slave address will be changed.

**Table 1. I<sup>2</sup>C Slave Addresses**

RESISTOR VALUE [Ω], 1%	SLAVE ADDRESS
115,000	A <sub>6</sub> , A <sub>5</sub> , 0_0000
100,000	A <sub>6</sub> , A <sub>5</sub> , 0_0001
86,600	A <sub>6</sub> , A <sub>5</sub> , 0_0010
75,000	A <sub>6</sub> , A <sub>5</sub> , 0_0011
64,900	A <sub>6</sub> , A <sub>5</sub> , 0_0100
56,200	A <sub>6</sub> , A <sub>5</sub> , 0_0101
48,700	A <sub>6</sub> , A <sub>5</sub> , 0_0110
42,200	A <sub>6</sub> , A <sub>5</sub> , 0_0111
36,500	A <sub>6</sub> , A <sub>5</sub> , 0_1000
30,900	A <sub>6</sub> , A <sub>5</sub> , 0_1001
26,100	A <sub>6</sub> , A <sub>5</sub> , 0_1010
21,500	A <sub>6</sub> , A <sub>5</sub> , 0_1011
16,900	A <sub>6</sub> , A <sub>5</sub> , 0_1100
12,400	A <sub>6</sub> , A <sub>5</sub> , 0_1101
8,060	A <sub>6</sub> , A <sub>5</sub> , 0_1110
3,740	A <sub>6</sub> , A <sub>5</sub> , 0_1111
2,870	A <sub>6</sub> , A <sub>5</sub> , 1_0000
2,490	A <sub>6</sub> , A <sub>5</sub> , 1_0001
2,150	A <sub>6</sub> , A <sub>5</sub> , 1_0010
1,870	A <sub>6</sub> , A <sub>5</sub> , 1_0011



**Table 1. I<sup>2</sup>C Slave Addresses (continued)**

1,620	A <sub>6</sub> , A <sub>5</sub> , 1_0100
1,400	A <sub>6</sub> , A <sub>5</sub> , 1_0101
1,210	A <sub>6</sub> , A <sub>5</sub> , 1_0110
1,050	A <sub>6</sub> , A <sub>5</sub> , 1_0111
909	A <sub>6</sub> , A <sub>5</sub> , 1_1000
768	A <sub>6</sub> , A <sub>5</sub> , 1_1001
649	A <sub>6</sub> , A <sub>5</sub> , 1_1010
536	A <sub>6</sub> , A <sub>5</sub> , 1_1011
422	A <sub>6</sub> , A <sub>5</sub> , 1_1100
309	A <sub>6</sub> , A <sub>5</sub> , 1_1101
200	A <sub>6</sub> , A <sub>5</sub> , 1_1110
95.3	A <sub>6</sub> , A <sub>5</sub> , 1_1111

### I<sup>2</sup>C Communication Speed

The MAX40080 provides a revision 3.0 I<sup>2</sup>C-compatible (3.4MHz) serial interface. Revision 3.0 I<sup>2</sup>C-compatible serial communications channel:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)
- 0Hz to 3.4MHz (high-speed mode or HS mode)
- Does not utilize I<sup>2</sup>C clock stretching

Operating in standard mode, fast mode and fast mode plus do not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance ( $C \times R$ ) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing section of the I<sup>2</sup>C revision 3.0 specification* for detailed guidance on the pullup resistor selection. In general, for bus capacitance of 200pF, a 100kHz bus needs 5.6k $\Omega$  pullup resistors, a 400kHz bus needs about 1.5k $\Omega$  pullup resistors, and a 1MHz bus needs 680 $\Omega$  pullup resistors. Note that the pullup resistor dissipates power when the open drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation is ( $V^2/R$ ).

Operating high-speed mode requires some considerations. For the full list of considerations, refer to the I<sup>2</sup>C 3.0 specification. The major considerations with respect to MAX40080 are:

- The I<sup>2</sup>C bus master uses current source pull-ups to shorten the signal rise time.
- The I<sup>2</sup>C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high speed master code.

At power-up and after each STOP condition, the MAX40080 input filters are set to standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz), unless bit 7 in the Configuration Register is set high. In that case, once entering the HS-mode, the device will stay into such a mode until this bit remains set, thus ignoring the STOP condition.

Once the bit is reset, at the next STOP condition the MAX40080 will exit from HS mode.

### Engaging HS-Mode for Operation up to 3.4MHz

[Figure 10](#) shows the protocol for engaging HS mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz. The engaging HS-mode protocol is as follows:

1. Begin the protocol, while operating at a bus speed of 1MHz or lower.
2. The master sends a START command (S).
3. The master sends the 8-bit master code of 00001xxx<sub>b</sub> where xxx<sub>b</sub> are don't care bits.
4. The addressed slave issues a NOT ACKNOWLEDGE (NA).

5. The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.
6. The master may continue to issue high-speed read/write operations until a STOP (P) is issued. Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. After a STOP has been issued, steps 1 to 6 in the above algorithm may be skipped.

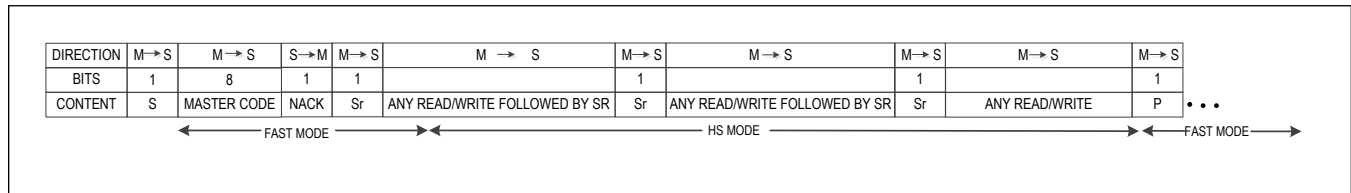


Figure 10. Engaging HS Mode

Note that the I<sup>2</sup>C HS Mode is only available when the device operates in Active Mode. See the [Configuration Register](#) section for more details about Active Mode and the other modes of operation.

### Modes of Operation

The device operates in one of the following five modes that can be programmed through the "Configuration" register:

1. **Standby Mode:** The device is not active, except for the I<sup>2</sup>C interface which can receive commands.
2. **Low-Power Mode:** The ADC is disabled, but the current sense is partially active, taking one current measurement every 50ms. The measured current is below the threshold set in the "Wake Up Current" register. Once the measured current reaches the threshold the device will enter into "Active Mode". No voltage measurement is taken as long as the device stays in low-power mode. For this reason, it is recommended that only current is stored into the FIFO (See the *FIFO configuration register* to determine what to store into the FIFO). But once the device wakes up from low-power mode to active mode, it will take either current or voltage measurement according to the Store V<sub>I</sub> setting in the FIFO configuration register.
3. **Single-Measurement Mode:** The device is basically in Standby mode, but when it responds to the SM BUS "Quick Command", it wakes up and takes one current and voltage measurement, then it enters into Standby again until the next "Quick Command".
4. **Active Mode:** The device is active in all its functionality and measurement is continuously taken.
5. **Selected Active Mode:** The device automatically takes several measurements per second (according to the sample rate setting) and stays on standby in between each measurement.

When operating in either "Active Mode" or "Selected Active Mode" if the I<sup>2</sup>C bus is inactive for as long as 1 minute the device will automatically go in the Standby Mode.

#### Quick Command:

In the Quick Command, the R/W# bit of the slave address denotes the command. The R/W# bit is used only when in Single-Measurement Mode to make the measurement. There are no data sent or received.

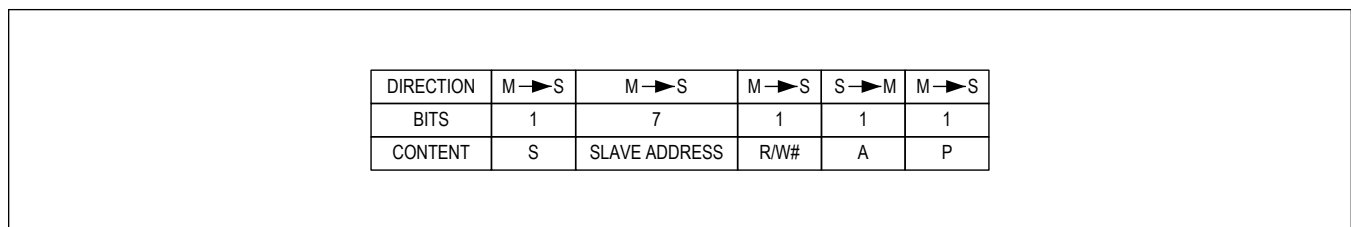


Figure 11. Quick Command

### Alert Management

The MAX40080 features an open-drain ALERT<sub>o</sub> output that reports when any of the following situations occur:

- Overcurrent
- Overvoltage
- Under voltage
- FIFO overflow warning (programmable threshold)
- FIFO full (64 data on it)
- Conversion ready (single-measurement mode only)
- Wake-up current threshold reached
- One minute timeout on the I<sup>2</sup>C bus (when inactive) expired

Any of the conditions above are also reported in the Status Register.

The ALERT\_ output is latched and is de-asserted only after the relevant flag has been cleared in the Status Register. Such a flag is cleared by writing into the Status Register. See the *Status Register description* for more details.

The ALERT\_ interrupt output (also called SMBALERT#) is a wired-AND signal that is used in conjunction with the SMBus Alert Response Address (ARA).

A slave-only device can signal the host through SMBALERT# that it wants to talk. The host processes the interrupt and simultaneously accesses all SMBALERT# devices through the Alert Response Address. Only the device(s) which pulled SMBALERT# low will acknowledge the Alert Response Address. The host performs a modified Receive Byte operation. The 7-bit device address provided by the slave transmits device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

If more than one device pulls SMBALERT# low, the highest priority (lowest address) device will win communication rights via standard arbitration during the slave address transfer.

After receiving an acknowledge (ACK) from the master in response to its address, that device must stop pulling down on the SMBALERT# signal. If the host still sees SMBALERT# low when the message transfer is complete, it knows to read the ARA again.

## Internal Registers

The pointer register selects between the registers as shown in [Table 2](#). The pointer register must be written for each I<sup>2</sup>C transaction.

Register addresses are not auto-incremented during reads and write. The max peak current register resets upon reading.

Write to the configuration register by writing the slave address byte, the pointer register byte to value 00h, and the data bytes. All other registers require the slave address byte, pointer register byte (04h or 05h, etc.), and 2 data bytes. If only 1 data byte is written, it is saved in bits D[15:8] of the respective register. If more than 2 data bytes are written, the additional data writes to the same register.

Perform a read operation by issuing the slave address byte (write), pointer byte, repeat START, another slave address byte (read), and then reading the data byte. If more than 2 data bytes are read, the additional reads are from the same register. See [Figure 4](#).

**Table 2. Register Functions and POR States**

REGISTER NAME	R/W	ADDRESS(HEX)	NUMBER OF BITS	POR STATE(HEX)	I <sup>2</sup> C READ TYPE
Configuration	R/W	00h	16	0060h	Read Word
Status	R	02h	14	0000h	Read Word
Threshold_Over_Current	R/W	04h	7	30h	Read Byte
Threshold_Over_Voltage	R/W	05h	6	30h	Read Byte
Threshold_Under_Voltage	R/W	06h	6	00h	Read Byte
Wake_Up_Current	R/W	07h	7	08h	Read Byte
Max_Peak_Current	R	08h	14	0000h	Read Word
FIFO_Configuration	R/W	0Ah	16	3400h	Read Word
Current_Measurement	R	0Ch	16	0000h	Read Word
Voltage_Measurement	R	0Eh	16	0000h	Read Word

**Table 2. Register Functions and POR States (continued)**

Current_Voltage Measurement	R	10h	32	0000 0000h	Read 32
INT_EN	R/W	14h	8	FFh	Read Byte

**Configuration Register**

The configuration register contains 16 bits of data:

D15	D14 D13 D12	D11 D10 D9 D8	D7	D6	D5	D4	D3	D2 D1 D0
Reserved	Digital Filter	ADC Sample Rate	Stay HS Mode	Input Range	PEC	Alert	I2C Timeout	Modes

**Operation Modes**

Set bits D2, D1 and D0 to select one of the following device operation modes:

**Table 3. Operation Mode**

OPERATION MODE	D2	D1	D0	COMMENT
Standby Mode	0	0	0	Default mode at device power up
Low-Power Mode	0	0	1	
Single-Conversion Mode	0	1	0	
Active Mode	0	1	1	Continuous measurement
Selected Active Mode	1	0	0	Fixed sample rate at 4sps
	1	0	1	Fixed sample rate at 1sps
	1	1	0	Fixed sample rate at 0.25sps
	1	1	1	Fixed sample rate at 0.0625sps

If a mode of operation is changed when a conversion is taking place, the conversion completes and then change occurs. While in standby, the I<sup>2</sup>C interface remains active and all registers remain accessible to the master.

When operating in either "**Active Mode**" or "**Selected Active Mode**" if the I<sup>2</sup>C bus is inactive for as long as 1 minute the device will automatically go into Standby Mode.

**I<sup>2</sup>C Timeout**

Write 1 to D3 to disable I<sup>2</sup>C timeout.

Write 0 to D3 to enable I<sup>2</sup>C timeout (default condition at reset and power-up). When operating in either "**Active Mode**" or "**Selected Active Mode**" if the I<sup>2</sup>C bus is inactive for as long as 1 minute the device will automatically go into Standby Mode. When such a condition happens the ALERT\_ is pulled low and a bit is set in the Status Register.

**Alert Response Time**

Bit D4 selects the alert interrupt response time:

- D4 = 0: Unfiltered. The alert is issued as soon as it is detected.
- D4 = 1: The alert is issued after being detected in four consecutive ADC clock samples (delay time varies from 4μs to 266.4μs depending on the ADC sample frequency).

**PEC**

Write 1 to enable Packet Error Checking (Default).

Write 0 to disable Packet Error Checking.

Set PEC bit to enable Packet Error Checking (PEC). When enabled, a PEC byte is appended to the end of each message transfer. This is a CRC-8 byte that is calculated on all the message bytes (including the address/read/write byte). The last device to transmit a data byte, also transmits the PEC byte, so the master transmits the PEC byte after a Write transaction and the device transmits the PEC byte after a Read transaction.

**Input Range**

Write 0 to D6 to select a range of 50mV (default).

Write 1 to D6 to select a range of 10mV.

**Stay HS Mode**

Set D7 to 1 to make the device stay in HS mode. Set D7 to 0 to exit from the HS mode (default). When this bit is set to 1, if device I<sup>2</sup>C speed is set to HS mode (up to 3.4MHz) the device will stay in HS mode, thus ignoring the STOP condition. Once the bit is reset to 0, at the next STOP condition the device will exit from HS mode.

**ADC Sample Rate**

[Table 4](#) shows all the available ADC sampling rates, please note column "Data read from FIFO" is only valid for active mode. In single measurement and selected active mode, data read from FIFO can be "Both Current and Voltage" at any sample rate.

**Table 4. Sample Rate Selection**

D11	D10	D9	D8	SAMPLE RATE (ksps)	DATA READ FROM FIFO
0	0	0	0	15	Either Current or Voltage
0	0	1	0	23.45	Either Current or Voltage
0	0	1	1	30	Either Current or Voltage
0	1	0	0	37.5	Either Current or Voltage
0	1	0	1	47.1	Either Current or Voltage
0	1	1	0	60	Either Current or Voltage
0	1	1	1	93.5	Either Current or Voltage
1	0	0	0	120	Either Current or Voltage
1	0	0	1	150	Either Current or Voltage
1	0	1	0	234.5	Either Current or Voltage
1	0	1	1	375	Either Current or Voltage
1	1	0	0	468.5	Either Current or Voltage
1	1	0	1	750	Either Current or Voltage
1	1	1	0	1,000	Either Current or Voltage
1	1	1	1	0.5	Both Current and Voltage

The I<sup>2</sup>C interface reads data at a maximum speed of 3.4MHz. Therefore, not all the ADC sample rates can be continuously pulled out from the device without overflowing the FIFO.

The main purpose of the high ADC sample rate is for over-sampling with digital filtering. It is the responsibility of the user to ensure that the I<sup>2</sup>C can read data without overflowing the FIFO.

See the Application Section "[FIFO Reading Data Rate](#)" for details.

See also FIFO Configuration register to determine whether the MAX40080 should store either current or voltage or both current and voltage. When MAX40080 is in active mode and FIFO is configured to store both current and voltage, only the slowest sample rate of 0.5ksps can be used. Note that when the part is in a single measurement and selected active state, both current and voltage can be read at any sample rate.

**Digital Filter**

This option calculates the average among samples. See [Table 5](#). Such an average is applied to the following modes of operation:

- Active mode
- Selected active mode
- Single Measurement mode

In each of these modes there is also the option of not using any filter.

**Table 5. Digital Filter Selection**

D14	D13	D12	FUNCTION
0	0	0	No Average
0	0	1	Average among 8 samples
0	1	0	Average among 16 samples
0	1	1	Average among 32 samples
1	0	0	Average among 64 samples
1	0	1	Average among 128 samples

Table 6 shows the output rate depending on the selected sample frequency and filter option.

**Table 6. Output Data Rate vs. Sample Rate**

Sample Rate [ksps]	Output Data Rate [ksps]					
	No Filter	x8	x16	x32	x64	x128
15	15	1.875	0.9375	0.46875	0.234375	0.1171875
18.75	19	2.34375	1.171875	0.5859375	0.29296875	0.146484375
23.45	23	2.93125	1.465625	0.7328125	0.36640625	0.183203125
30	30	3.75	1.875	0.9375	0.46875	0.234375
37.5	38	4.6875	2.34375	1.171875	0.5859375	0.29296875
47.1	47	5.8875	2.94375	1.471875	0.7359375	0.36796875
60	60	7.5	3.75	1.875	0.9375	0.46875
93.5	94	11.6875	5.84375	2.921875	1.4609375	0.73046875
120	120	15	7.5	3.75	1.875	0.9375
150	150	18.75	9.375	4.6875	2.34375	1.171875
234.5	235	29.3125	14.65625	7.328125	3.6640625	1.83203125
375	375	46.875	23.4375	11.71875	5.859375	2.9296875
468.5	469	58.5625	29.28125	14.640625	7.3203125	3.66015625
750	750	93.75	46.875	23.4375	11.71875	5.859375
1000	1000	125	62.5	31.25	15.625	7.8125

### Status Register

The status register contains 6 flags plus 6 bits of FIFO data count:

D13-8	D7	D6	D5	D4	D3	D2	D1	D0
FIFO Data Count	FIFO Overflow	FIFO Alarm	I <sup>2</sup> C Timeout	Underflow_V	Overflow_V	Overflow_I	Conversion Ready	Wake-Up

In order to clear each of the flags in bits D7–D0, a write to this register with the same word that was read is required. When doing this flag clearing, what is written in the upper byte is meaningless and will not affect this register.

For instance, suppose that the over the current flag is set because an overcurrent condition occurred. Suppose the FIFO has 4 data on it.

A read to this register will yield the data 0x0404.

To clear the overcurrent flag, a write to this register with the data 0xXXX4 must happen where the X in the upper byte indicates that any value is allowed.

### Wake-Up Current

D0 is a read-only status bit indicating that the measured current has exceeded the value programmed in the register

**"Wake\_up\_Current"**. This only applies when the device is set in Low-Power Mode. An interrupt is also generated.

### Conversion Ready

D1 is a read-only status bit indicating that the ADC conversion is completed. This bit is only used in Single-Measurement Mode and in such a mode an interrupt is also generated.

### Overflow Current

D2 is a read-only bit that indicates that the measured current has exceeded the value programmed in the register **"Threshold Over-Current"**. Such a condition also generates an interrupt. This bit is used in single conversion mode, selective active mode, and active mode, this bit not applies when FIFO store voltage only. In active mode when FIFO stores both current and voltage, the bit only applies when the ADC sampling rate is 0.5Ksps.

### Overflow or Underflow Voltage

D3 is a read-only bit that indicates that the measured voltage has exceeded the value programmed in the register **"Threshold Over-Voltage"**. Such a condition also generates an interrupt.

D4 is a read-only bit that indicates that the measured voltage has gone below the value programmed in the register **"Threshold Under-Voltage"**. Such a condition also generates an interrupt.

Both D3 and D4 can be used in single conversion mode, selective active mode, and active mode. These two bits do not apply when FIFO only store current measurement. In active mode, when FIFO stores both current and voltage measurement, these two bits only apply when the ADC sampling rate is 0.5Ksps.

### I<sup>2</sup>C Timeout

D5 is a read-only bit that indicates that when operating in either **"Active Mode"** or **"Selected Active Mode"** if the I<sup>2</sup>C bus is inactive for one minute the device will automatically go into Standby Mode. Such a condition also generates an interrupt.

### FIFO Alarm

D6 is a read-only status bit indicating that the ADC FIFO is about to overflow. When such a condition happens an interrupt is also generated.

FIFO is 64 deep, the overflow warning is issued when N locations have been written and none has been read yet. The number N is determined by the field Overflow\_Threshold in the FIFO Configuration register.

### FIFO Overflow

When set to 1 it indicates that the FIFO is full with 64 data on it. An interrupt is also issued. In any other situations where the number of data is less or equal to 63 this bit will be 0.

### FIFO Data Count

6-bit counter that indicates the number of data that are currently inside the FIFO. Range is from 0 to 63.

If the FIFO is full, meaning there are 64 data on it, then this counter will be 0, but the Overflow bit will be set to 1

### Thresholds and Wake-Up Current registers

[Table 7](#) shows the data format for the threshold\_over\_current, threshold over/under\_voltage and wake-up current registers

**Table 7. Thresholds and Wake-Up Current registers**

REGISTER NAME	REGISTER ADDRESS	BIT 6	BITS 5-0
Threshold_Over_Current	0x04	sign	Over-current threshold. When the measured current is higher than this value an alert is issued on ALERT_ and one status register bit is set
Threshold_Over_Voltage	0x05	n/a	Over-voltage threshold. When the measured voltage is higher than this value an alert is issued on ALERT_ and one status register bit is set



**Table 7. Thresholds and Wake-Up Current registers (continued)**

Threshold_Under_Voltage	0x06	n/a	Under-voltage threshold. When the measured voltage is lower than this value an alert is issued on ALERT_ and one status register bit is set
Wake_up_Current	0x07	sign	Wake-up current threshold when in Low-Power Mode. When the measured current is higher than this value the device will switch on to Active Mode. Additionally, an alert is issued on ALERT_ and one status register bit is set

**MAX\_Peak\_Current**

Display the maximum current value FIFO stored.

**FIFO Configuration**

BIT	D15	D14	D13-8	D7-2	D1-0
BIT NAME	Flush	RO	Overflow_Warning	Not_Used	Store_IV
DEFAULT	0	0	110100	000000	00

**Store IV**

These two bits determine whether the device measures and stores into the FIFO either current or voltage or both current and voltage.

- 2'b00: Current Only
- 2'b01: Voltage Only
- 2'b10: Current and Voltage
- 2'b11: Not Used

The FIFO is 64 deep and 32 bits wide. Regardless of the selection made with these two bits, current and voltage information always occupies the data format as shown in the following table.

D31–D16	D15–D0
Voltage	Current

In Current Only mode (2'b00) the ADC only measures current and the voltage bits (D31–D16) are always empty and meaningless.

In Voltage Only mode (2'b01) the ADC only measures voltage and the current bits (D15–D0) are always empty and meaningless.

In Current and Voltage mode (10) the ADC continuously alternates between 10 current measurements and one voltage measurement. All the bits (D31–D0) are written. The voltage bits are repeated for 10 contiguous current bits. In this mode, the actual sample rate for either current or voltage is less than what is specified in the Configuration Register, ADC Sample Rate.

Current and Voltage data are retrieved from the FIFO through the registers Current\_Measurement (0x0C), Voltage Measurement (0x0E), and Current\_Voltage Measurement (0x10). It is the user's responsibility to keep track of the mode of operation. For instance, if these bits are set to Current Only (2'b00) only the register Current\_Measurement (0x0C) will provide meaningful data.

All data are two's complement.

**Overflow\_Threshold**

This is a 6-bit programmable threshold that allows the user to set at what data count in the FIFO the overflow warning interrupt should be issued.

The range is from 0x00 to 0x3F.

The default value is 0x34 (80% of FIFO is filled)

**RO**

**RO (Roll-Over):**



It defines the rollover behavior when the FIFO is full. If RO is set to low, then a new data sample does not write to the FIFO and is lost when the FIFO is full. If RO is set to high, then the FIFO rolls over to the first location, and a new data sample writes to the FIFO, overwriting the old data sample.

### Flush

When set to 1 it resets the entire data content in the FIFO.

### Read Current and Voltage from the FIFO

Current and Voltage data are retrieved from the FIFO through the following registers.

The FIFO Configuration Register (bits Store V<sub>I</sub>) specifies whether the user wants to read either Current Only or Voltage Only or Current and Voltage. The read pointer is incremented after each reading.

All data are two's complement.

Registers that allow reading from the FIFO:

FIFO Configuration Register: bits Store IV:

- 2'b00: Current Only (2 bytes - Read Only)

REGISTER NAME	REGISTER ADDRESS	D15	D14–D13	D12	D11–D0
Current_Measurement	0x0C	Data Valid	Current Sign Extension	Current Sign	Current Magnitude

- 2'b01: Voltage Only (2 bytes - Read Only)

REGISTER NAME	REGISTER ADDRESS	D15	D14–D13	D12	D11–D0
Voltage_Measurement	0x0E	Data Valid	Voltage Sign Extension	Voltage Sign	Voltage Magnitude

- 2'b10: Current and Voltage (4 bytes - Read Only)

REGISTER NAME	REGISTER ADDRESS	D31	D30–D28	D27–D16	D15	D14–D12	D11–D0
Current_Voltage_Measurement	0x10	Data Valid	Voltage Sign (repeated 3x)	Voltage Magnitude	Reserved	Current Sign (repeated 3x)	Current Magnitude

- 11: Not Used

Data Valid = 0: FIFO is empty and the data is meaningless.

Data Valid = 1: FIFO is not empty and the data is valid.

Voltage Sign is expected to be always 0 since the voltage measurement is always positive.

### INT\_EN

This register is a mask for the status register, meaning that each bit enables/disables the interrupt generation from the status register. Bits are in the same order as they are reported in the status register.

1 = Interrupt generation is enabled (default)

0 = Interrupt generation is disabled

BIT	D7	D6	D5	D4	D3	D2	D1	D0
<b>BIT NAME</b>	Overflow Mask Enable	Alarm Mask Enable	I <sup>2</sup> C Timeout Mask Enable	Underflow_V Mask Enable	Overflow_V Mask Enable	Overflow_I Mask Enable	Conversion Ready Mask Enable	Wake-up Mask Enable
<b>DEFAULT</b>	1	1	1	1	1	1	1	1

## Applications Information

### Filter Selection

The MAX40080 offers two programmable input ranges ( $\pm 10\text{mV}$  or  $\pm 50\text{mV}$ ) with different bandwidth specifications (10kHz or 50kHz). Additional capacitor can be added at filter pins (FLT $\pm$ ), which will limit the input bandwidth of the ADC. At  $\pm 50\text{mV}$  range, input bandwidth of different values of filter cap and typical settling time. See [Table 8](#). Typically, a 4.7nF cap is recommended across filter pins (FLT $\pm$ ).

**Table 8. Filter Cap Selection**

FILTER CAP	-3dB FREQUENCY	TYPICAL SETTling TIME FOR A 1.25V STEP TO 0.5 LSB (12 bit)
4.7nF	45.6 kHz	25 $\mu\text{s}$
100nF	2.3 kHz	450 $\mu\text{s}$

### FIFO Reading Data Rate

The I<sup>2</sup>C interface reads data at a maximum speed of 3.4MHz. Therefore, not all the ADC sample rates can be continuously pulled out from the device without overflowing the FIFO.

[Table 9](#) explains this situation. The main purpose of the high ADC sample rate is for over-sampling with digital filtering. It is the responsibility of the user to ensure that the I<sup>2</sup>C can read data without overflowing the FIFO.

**Table 9. FIFO Reading Data Rate vs. I<sup>2</sup>C Interface Speed**

FIFO_READ [BITS]	I <sup>2</sup> C_READ [BITS]	READ MODE	SAMPLE FREQUENCY [Ksps]	I <sup>2</sup> C INTERFACE SPEED [MHz]
27	66	Current and Voltage	0.5	0.033
14	48	Either Current or Voltage	15	0.72
14	48	Either Current or Voltage	18.75	0.9
14	48	Either Current or Voltage	23.45	1.1256
14	48	Either Current or Voltage	30	1.44
14	48	Either Current or Voltage	37.5	1.8
14	48	Either Current or Voltage	47.1	2.2608
14	48	Either Current or Voltage	60	2.88
14	48	Either Current or Voltage	93.5	4.488
14	48	Either Current or Voltage	120	5.76
14	48	Either Current or Voltage	150	7.2
14	48	Either Current or Voltage	234.5	11.256
14	48	Either Current or Voltage	375	18
14	48	Either Current or Voltage	468.5	22.488

**Table 9. FIFO Reading Data Rate vs. I<sup>2</sup>C Interface Speed (continued)**

14	48	Either Current or Voltage	750	36
14	48	Either Current or Voltage	1000	48

Reading both current and voltage requires 4 bytes, while reading either of the two requires only 2 bytes. Table 10 and Table 11 show the number of transactions and bits involved in both types of reads.

**Table 10. Read 2 Bytes**

TRANSACTION	READ 2 BYTES
1	START
2	SLAVE_ADDRESS + WR
3	ACK
4	REG_ADDRESS
5	ACK
6	RPT_START
7	SLAVE_ADDRESS + RD
8	ACK
9	DATA (1st Byte)
10	ACK
11	DATA (2nd Byte)
12	NACK
13	STOP
<b>Total Bits</b>	<b>48</b>

**Table 11. Read 4 Bytes**

TRANSACTION	READ 4 BYTES
1	START
2	SLAVE_ADDRESS + WR
3	ACK
4	REG_ADDRESS
5	ACK
6	RPT_START
7	SLAVE_ADDRESS + RD
8	ACK
9	DATA (1st Byte)
10	ACK
11	DATA (2nd Byte)
12	ACK
13	DATA (3rd Byte)
14	ACK
15	DATA (4th Byte)
16	NACK
17	STOP
<b>Total Bits</b>	<b>66</b>

MAX40080

Precision, Fast Sample-Rate,  
Digital Current-Sense Amplifier

### Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX40080ANC+	-40°C to +125°C	12 WLP	+AAS
MAX40080ANC+T	-40°C to +125°C	12 WLP	+AAS
MAX40080ATC+T*	-40°C to +125°C	12 TDFN	+AIO

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

\* Denotes future product.

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/21	Release for Market Intro	—