HARRIS SEMICONDUCTOR

HV400

HV400CP

May 1992

High Current MOSFET Driver

Features

- Fast Fall Times .....16ns at 10,000pF
- No Supply Current in Quiescent State
- Peak Source Current 6A
- Peak Sink Current 30A
- High Frequency Operation 300kHz

Applications

- Switch Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Uninterruptible Power Supplies

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HV400CP	0°C to +75°C	8 Pin Plastic Mini-DIP
HV400CB	0°C to +75°C	8 Pin Plastic SOIC
HV400IP	-40°C to +85°C	8 Pin Plastic Mini-DIP
HV400IB	-40°C to +85°C	8 Pin Plastic SOIC
HV400MJ/883*	-55°C to +125°C	8 Pin CerDIP
HV400Y	+25°C	DICE

* Contact Harris for availability date.

Description

The HV400 is a single monolithic, non-inverting high current driver designed to drive large capacitive loads at high slew rates. The device is optimized for driving single or parallel connected N-channel power MOSFETs with total gate charge from 5nC to >1000nC. It features two output stages pinned out separately allowing independent control of the MOSFET gate rise and fall times. The current sourcing output stage is an NPN capable of 6A. An SCR provides over 30A of current sinking. The HV400 achieves rise and fall times of 54ns and 16ns respectively driving a 10,000pF load.

Special features are included in this part to provide a simple, high speed gate drive circuit for power MOSFETs. The HV400 requires no quiescent supply current, however, the input current is approximately 15mA while in the high state. With the internal current steering diodes (pin 7) and an external capacitor, both the timing and MOSFET gate power come from the same pulse transformer; no special external supply is required for high side switches. No high voltage diode is required to charge the bootstrap capacitor.

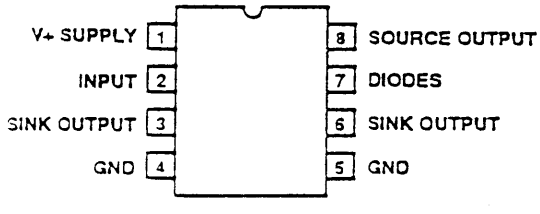
The HV400 in combination with the MOSFET and pulse transformer makes an isolated power switch building block for applications such as high side switches, secondary side regulation and synchronous rectification. The HV400 is also suitable for driving IGBTs, MCTs, BJTs and small GTOs.

The HV400 is a type of buffer; it does not have input logic level switching threshold voltages. This single stage design achieves propagation delays of 20ns. The output NPN begins to source current when the voltage on pin 2 is approximately 2V more positive than the voltage at pin 8.

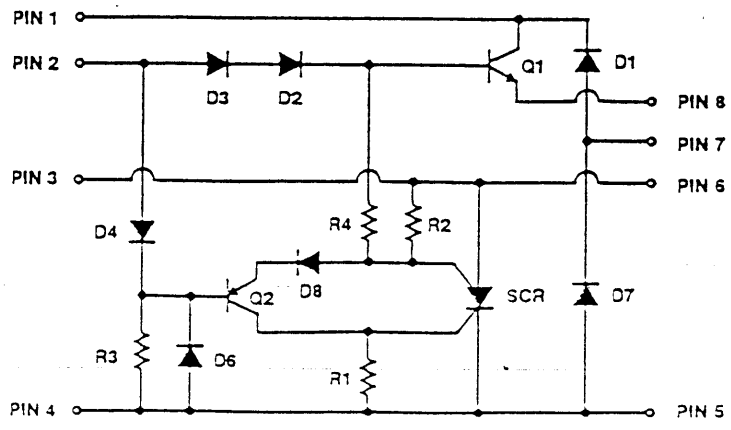
The output SCR switches on when the input pin 2 voltage is 1V more negative than the voltage at pins 3/6. Due to the use of the SCR for current sinking, once the output switches low, the input must not go high again until all the internal SCR charge has dissipated, 0.5µs - 1.5µs later.

Pinout

HV400 (PLASTIC MINI-DIP AND SOIC)
TOP VIEW



Schematic



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Absolute Maximum Ratings

Voltage Between Pin1 and Pin 4/5 ..... 35V
Input Voltage Pin 7 (Max) ..... Pin 1 + 1.5V
Input Voltage Pin 7 (Min) ..... Pin 4/5 -1.5V
Input Voltage Pin 2 to Pin 4/5 ..... +/- 35V
Input Voltage Pin 2 to Pin 6 ..... -35V
Maximum Clamp Current (Pin 7) ..... ±300mA
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C < T_A < +150°C

Thermal Resistance	θ_{ja}	θ_{jc}
PDIP	93.8°C/W	31.5°C/W
SOIC	157.1°C/W	42.8°C/W

Power Dissipation at T_A = +25°C ..... 1.33W Mini-DIP
Power Dissipation at T_A = +25°C ..... 0.8W SOIC
Operating Temperature Range
HV400CP/CB ..... 0°C < T_A < +70°C
HV400IP/IB ..... -40°C < T_A < +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{SUPPLY} = 15V

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INPUT (PIN 2)							
Input High Differential Voltage (Pin 2 - Pin 8)	V_{IH}	V_{OUT} = 0V, I_{OUT} HI = 10mA	+25°C	0.6	1.7	2.8	V
			Full	0.5	-	3.5	V
Input Low Differential Voltage (Pin 2 - Pin 3/6)	V_{IL}	V_{OUT} = 12V, I_{OUT} LO = -3mA	+25°C	-1.1	-0.9	-0.8	V
			Full	-1.26	-	-0.65	V
Input High Current	I_{IH}	$V_{PIN\ 1,2}$ = 30V, I_{SOURCE} = 0	+25°C	15	18	20	mA
			Full	15		22	mA
Input High Current Peak	I_{IHP}	I_{SOURCE} = 6A, 1µs pulse, V_{IN} = 9V, V_{OUT} = 0V	+25°C		700		mA
Input Low Current	I_{IL}	$V_{PIN\ 2}$ = -30V	+25°C	-80	-50		µA
			Full	-120			µA
SOURCE OUTPUT (PIN 8)							
High Output Voltage	V_{OH}	V_{IN} = +V, I_{OUT} = 150mA	+25°C	12.1	12.8	13.4	V
			Full	12.0		13.5	V
Peak Output Current	I_{OPS}	V_{IN} = 9V, 1µs Pulse, V_{OUT} = 0V	+25°C		6		A
Output Low Leakage	I_{OL}	V_{OUT} = 0V, V_{IN} = 0V	+25°C	0	10	50	µA
			Full			55	µA
SINK OUTPUT (PIN 3/6)							
Low Output Voltage	V_{OL}	V_{IN} = 0V, I_{OUT} = -150mA	+25°C	0.8	0.89	1.0	V
			Full	0.8		1.05	V
Peak Output Current	I_{OPS}	V_{IN} = 0V, 5µs Pulse, V_{OUT} = 4V	+25°C		30		A
Output High Leakage	I_{OH}	V_{IN} = 15V	+25°C	0	0.3	2	µA
			Full	0		13.5	µA
DIODES D1 AND D7 (PIN 7)							
Forward Voltage	V_F	I_D = 100mA	+25°C	0.9	1.03	1.1	V
			Full	0.8		1.4	V
Reverse Leakage Current	I_R	V_R = 30V	+25°C	0	0.1	1	µA
			Full	0		1	µA
Diode (Pin 7) Stored Charge	Q_{RR}	I_D = 100mA	+25°C		6.5		nC

NOTE: Limits are 100% tested at +25°C; limits over the full temperature range are guaranteed but not tested.

Pin Descriptions

SYMBOL	DESCRIPTION
DC INPUT PARAMETERS	
V_{IH}	The differential voltage between the input (Pin 2) to the output (Pin 8) required to source 10mA
V_{IL}	The differential voltage between the input (Pin 2) to the output (Pins 3, 6) required to sink 3mA
I_{IH}	The current required to maintain the input (Pin 2) high with I_{OUT} = 0A
I_{IHP}	The input (Pin 2) current for a given pulsed output current
I_{IL}	The current require to maintain the input (Pin 2) low
DC OUTPUT PARAMETERS	
V_{OH}	The output (Pin 8) voltage with input (Pin 2) = V+
I_{OP8}	The pulsed peak source current form output (Pin 8)
I_{OL}	The output (Pin 8) leakage current with the input (Pin 2) = Ground
V_{OL}	The output (Pins 3, 6) voltage with the input (Pin 2) = Ground
I_{OP6}	The pulsed peak sink current into output (Pins 3, 6)
I_{OH}	The output (Pins 3, 6) leakage current with the input (Pin 2) = V+
V_F	The forward voltage of diode D1 or D7
I_R	The reverse leakage current of diode D1 or D7
Q_{RR}	The time integral of the reverse current at turn off
AC PARAMETERS (See Switching Time Specifications)	
T_R	The low to high transition of the output
T_F	The high to low transition of the output
T_{OR}	The output propagation delay from the input (Pin 2) rising edge
T_{OF}	The output propagation delay from the input (Pin 2) falling edge
T_{OR}	The minimum time required after an output high to low transition before the next input low to high transition

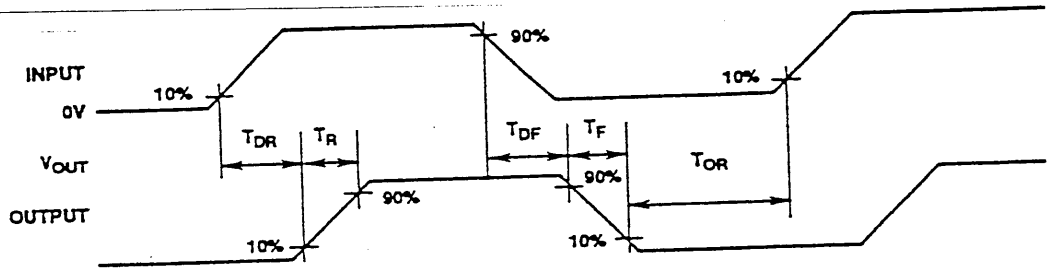
Switching Time Specifications V_{SUPPLY} = 15V

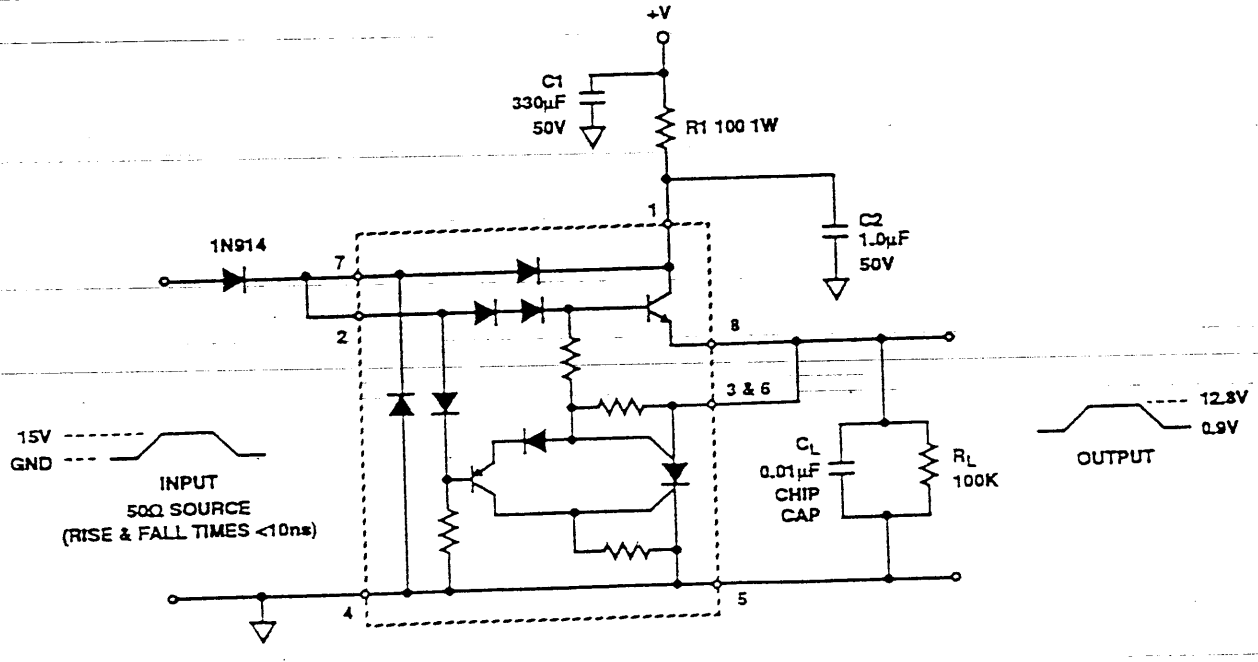
PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS			UNITS
				MIN	TYP	MAX	
Rise Time	T_R	See Switching Test Circuit	Full		50	66	ns
Fall Time	T_F	See Switching Test Circuit	Full		15	24	ns
Delay Time (Lo to Hi)	T_{DR}	See Switching Test Circuit	Full		20	25	ns
Delay Time (Hi to Lo)	T_{DF}	See Switching Test Circuit	Full		17	28	ns
Minimum Off Time	T_{OR}	See Switching Test Circuit	Full		900	1500	ns

NOTES:

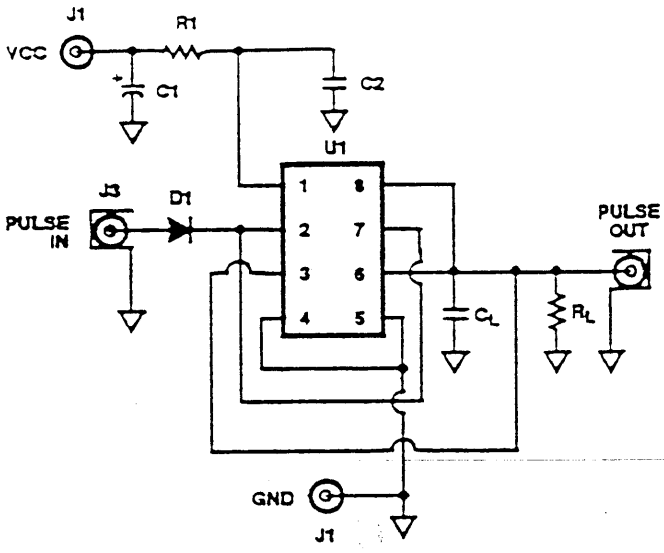
1. Switching times are guaranteed but not tested
2. Typical values are for +25°C

Switching Diagram and Test Circuit



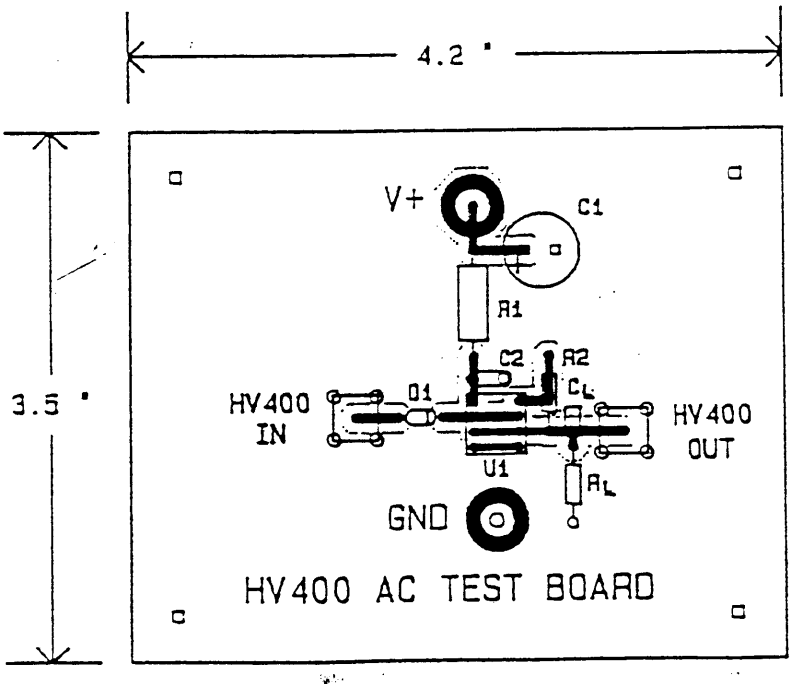


HV400 Switching Test Circuit



Parts List

R1 100Ω, 1W Carbon Resistor
R2 Wire
R_L 100KΩ, 1/8W Carbon Resistor
C1 330µF, 50V Capacitor
C2 1µF, 50V Capacitor
C_L 0.01µF, 50V Chip Capacitor
D1 1N914 Diode
J1, J2 PC Mount Banana Jack Johnson 108-0740-001
J3, J4 PC Mount SMA Connector Johnson EFJ142
U1 Harris HV400 I.C.



Application Information

Circuit Operation

The HV400's operation is easily explained by referring to the schematic. The control signal is applied to pin 2. If the control signal is about 2V above pin 8, the output NPN Q1 turns on charging the MOSFET gate from a capacitor connected to pin 1. Resistor R4 helps keep the SCR off by applying a reverse bias to the SCR anode gate.

When the control input drops about 1V below pin 3/6, PNP Q2 turns on which triggers the SCR by driving both the anode and cathode gates. The SCR discharges the MOSFET gate and when its current becomes less than 10mA, it turns off. Transistor Q2 conducts any gate leakage currents, through resistors R1 and R2, once the SCR turns off. Figure 7 shows the output characteristics before the SCR turns on and after it turns off. When the SCR turns on, resistor R4 provides a path to remove Q1 base charge. Resistor R3 provides the base current for Q2 to reduce the turn off delay time. Resistors R1 and R2 reduce the SCR recovery time.

The two diodes connected to the diode input pin 7 provide some operation flexibility. With pins 2 and 7 connected together, diode D1 provides a path to recharge the storage capacitor once the MOSFET gate is pulled high and, along with diodes D2 and D3, keeps Q1 from going into hard saturation which would increase delay times. Diode D7 would clamp the input near ground and provide a current path if an input DC blocking capacitor is used.

Alternatively, pin 7 can be connected to pin 6 so that the SCR and NPN Q1 don't have to pass reverse current if the output "rings" above the supply or below ground. When high performance diodes are required, pin 7 can be left disconnected and external diodes substituted.

The diodes in series with pin 2 decouple the input from the output during negative going transitions. The absence of input current turns off Q1 and allows Q2 to trigger the SCR. Diode D8 turns off Q2 once the SCR turns on pulling the output low, otherwise Q2 would saturate and slow down circuit operation. In addition, the diodes D2, D3 and D8 improve noise immunity by adding about 2.5V of input hysteresis.

The HV400 is capable of large output currents but only for brief durations due to power dissipation.

Circuit Board Layout

PC board layout is very important. Pins 3 and 6 should be connected together as should pins 4 and 5. Otherwise the internal interconnect impedance is doubled and only half of the bond wires are used which would degrade the reliability.

The bootstrap capacitor should hold at least 10x the charge of the MOSFET and should be connected between pins 1 and 4/5 with minimum lead lengths and spacings. Likewise, the HV400 should be as close to the MOSFET as possible. Any long PC traces (parasitic inductances) between the MOSFET gate and pins 8 or 3/6 or between the source and pins 4/5 should be avoided. Inductance between the HV400 and the MOSFET limit the MOSFET switching time. If they are too large, the HV400 may operate erratically as discussed below.

Cross Conduction Faults

It is possible to have both Q1 and the SCR on at the same time resulting in very large cross conduction currents. The SCR has larger current capacity so the output goes low and the storage capacitor is discharged. The conditions that cause cross conduction and precautions are discussed below.

Minimum Off Time

The SCR requires a recovery time before voltage can be reapplied without it switching back on. Figure 13 shows how this SCR recovery time, called "minimum off time" (T_{OR}), is a function of the load capacitance. If the input voltage goes high before this recovery time is complete, the SCR will switch back on.

Note that reverse current flowing through the SCR, for example due to load inductance ringing, extends the minimum off time. Since the minimum off time is really dependent upon how much stored charge remains in the SCR when the anode (pin 3/6) is taken positive, it may vary for different applications. Figure 13 indirectly shows that the minimum off time increases with larger currents. It also increases at elevated temperatures as shown in Figure 14. Excessive ringing increases the minimum off time since the stored charge doesn't begin to dissipate until the current drops below 10mA for the last time. Rising anode voltage acts on the internal SCR capacitance to generate its own triggering current. The excess stored charge increases this capacitance. Faster rise times and/or higher voltages also increase the amount of internal trigger current from the internal capacitance so applications with larger dV/dt require longer minimum off times.

The minimum off time must be considered for all occurrences of SCR current. For example, in a half bridge switch mode power supply, there are two MOSFET's connected to the transformer primary. Assume that the high side MOSFET switch is off. When the low side MOSFET switch is turned on, the HV400 driving the high side MOSFET will have to sink gate current from C_{gd} and will have to source gate current when the low side MOSFET switches back off. Both of these current pulses will try to flow through pin 3/6 since the pin 8 output is turned off. Sourcing current from pins 3/6 through the SCR is possible, the pin 3/6 voltage becoming negative with respect to pins 4/5 (See Figure 8). But a better practice would be to connect a Schottky diode between pins 4/5 (anode) and 3/6 (cathode) so reverse current does not flow through the SCR.

False SCR Triggering

The SCR may be triggered inadvertently. The output may overshoot the input due to inductive loading or over driving the output NPN (allowing it to saturate). Whenever pin 6 is more positive than pin 2 by 1V, the SCR is triggered on. Also,

apidly, greater than 0.5V/nS, the SCR
issues are resolved by minimizing the
inserting sufficient resistance, usually
een pin 8 and the load.

e going input voltage can result in
about 2.5µs. If the output can not keep
out, the stored charge of diode D4 is
base of Q2. This excess charge in Q2
issipate. Otherwise, when pin 3/6 goes
on and trigger the SCR. An external
pin 2, as shown in Figure 1, will prevent
into the base of Q2 but that will also
voltage by the forward voltage of that

connected to pin 7 are provided for
ay not be suitable for large currents.
rt of the integrated circuit, they are
erate at high current densities, and have
s. Figure 15 shows that their forward
ade above 100mA. In addition, Figure 16
recovery charge as a function of forward
ct of this charge, the applied reverse
uency is the additional power dissipation
For stored charge calculations, use the
nt within 100ns of the application of
dition to the extra power dissipation, the
e diodes may extend the switching delay

n Calculations

to drive the MOSFET is the product of
times the gate supply voltage (maximum
pin 1, 2 or 7) times the frequency.
MOSFET gate resistance is negligible,
ated within the HV400. If resistors are
HV400 and the MOSFET, then some of
ated in the resistors, the percentage
e ratio of resistors to HV400 output

er sources of power dissipation to
is the power in R3 which is the product
ent and voltage (with no output current)
Second is the product of the pin 7 diode
is dependent upon the forward current,
de reverse voltage times the frequency.
vailable from figures 3 and 16 in this

uits

gned to interface a pulse transformer to
There must be some means to balance
-second product over a cycle. The
n Figure 1 lets the core magnetization
e primary and secondary voltages. The
mary side limits this voltage and must
be capable of dissipating the energy stored in the transformer. The load may be connected to either the power MOSFET drain or source.

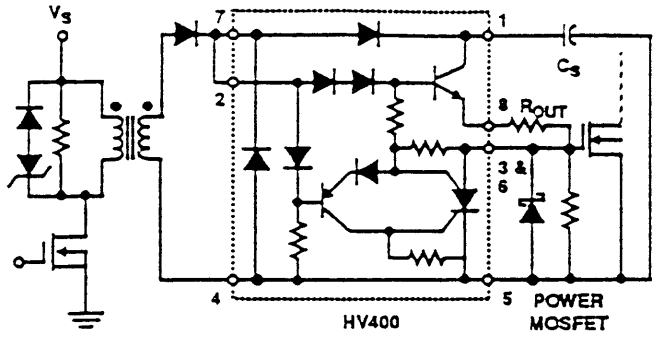


FIGURE 1. UNIPOLAR DRIVE

A diode is added in series with pins 2 and 7 to allow the transformer secondary to go negative. The charge storage of the pin 7 diode may cause the turn off delay time to be too long. Alternatively, pin 7 could be left disconnected and a second external diode connected between the transformer (anode) and pin 1 (cathode). In some applications the diode in series with pin 2 may be unnecessary but the -35V input to output or ground maximum rating should be observed.

Sometimes the volt-second balance is achieved by a push-pull drive on the pulse transformer primary. This is especially useful if there are two secondary windings driving two HV400's out of phase such as in a half-bridge configuration

Other times it is more convenient to achieve volt-second balance by using capacitors to block DC in the primary and secondary windings as shown in Figure 2. The pin 7 diodes provide a path for discharging the secondary side DC blocking capacitor. Both capacitors, C_{IN} and C_S, should be at least 10 times the equivalent MOSFET gate capacitance.

The HV400 can be used as a current booster for low side switches by connecting directly to the PWM output. The circuit would be similar to the switching time test circuit.

It is worth restating that some consideration (and experimentation) should be given to the choice of external components, i.e. resistors, capacitors and diodes, to optimize performance in a given application.

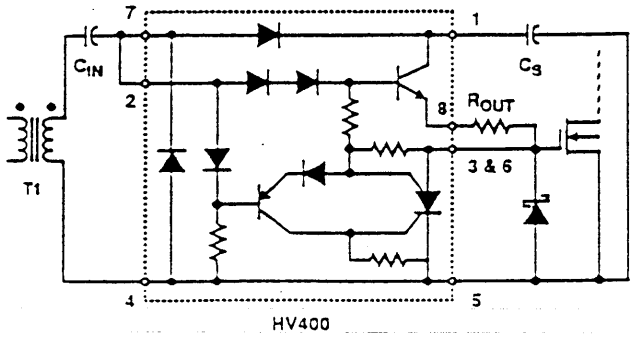


FIGURE 2. BIPOLAR DRIVE WITH DC BLOCKING CAPACITOR

Typical Performance Curves T_A = +25°C Unless Otherwise Specified

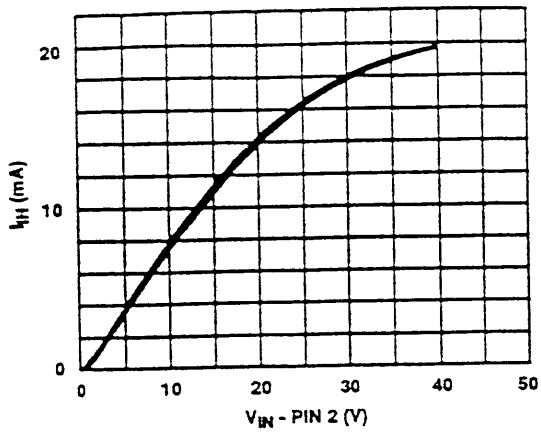


FIGURE 3. PIN 2 INPUT CURRENT vs INPUT VOLTAGE WITH ZERO OUTPUT CURRENT

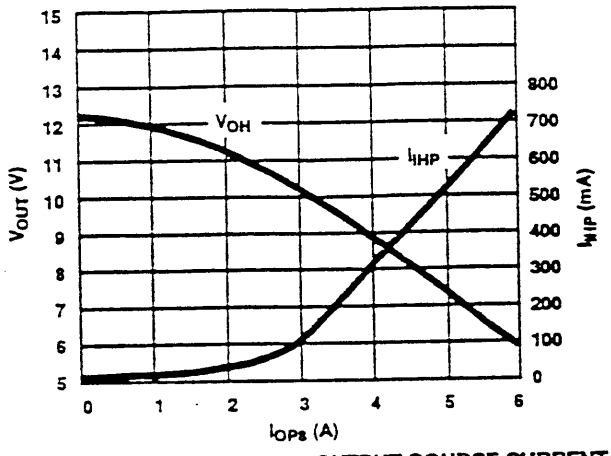


FIGURE 4. PIN 2 I_{IHP} & V_{OH} vs OUTPUT SOURCE CURRENT

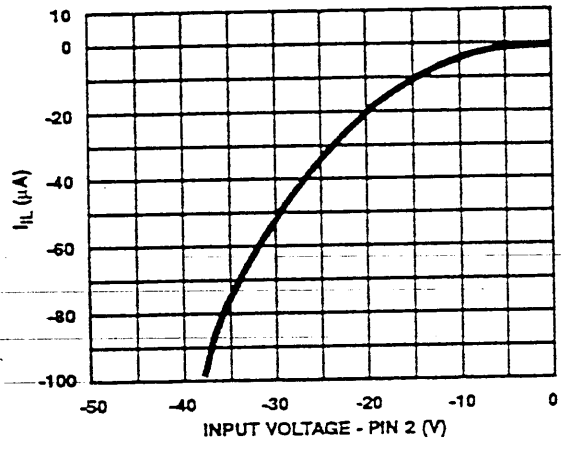


FIGURE 5. PIN 2 I_{IL} vs INPUT VOLTAGE

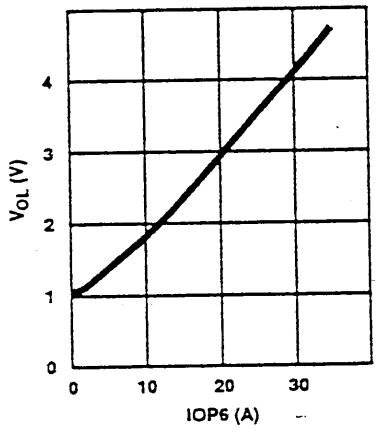


FIGURE 6. V_{OL} vs I_{OP6} (5µs PULSES)

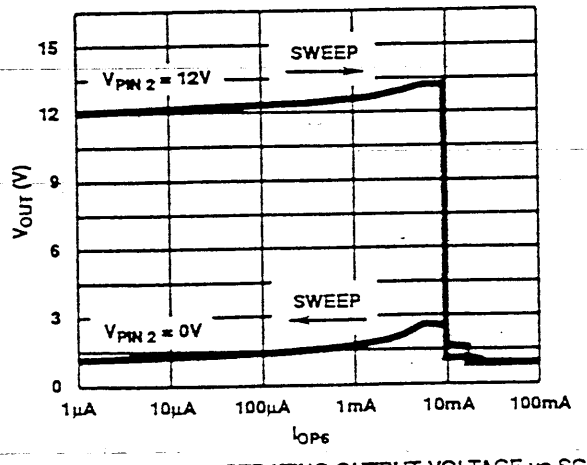


FIGURE 7. PIN 3/6 ILLUSTRATING OUTPUT VOLTAGE vs SCR OUTPUT SINK LATCHING AND HOLDING CURRENT

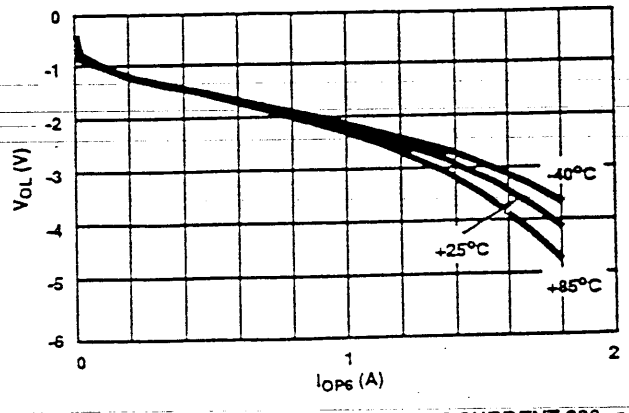


FIGURE 8. PIN 3/6 VOLTAGE vs REVERSE CURRENT 300µs PULSES

Typical Performance Curves T_A = +25°C Unless Otherwise Specified (Continued)

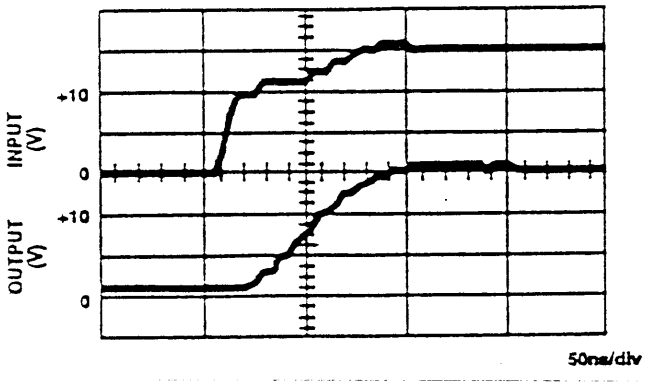


FIGURE 9. LOW TO HIGH TRANSIENT RESPONSE WAVEFORMS (C_L = 10nF)

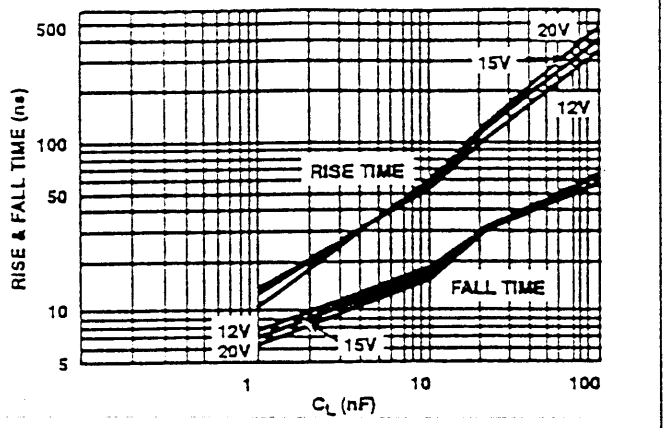


FIGURE 10. RISE & FALL TIMES vs C_L(V+ = 12V, 15V, 20V)

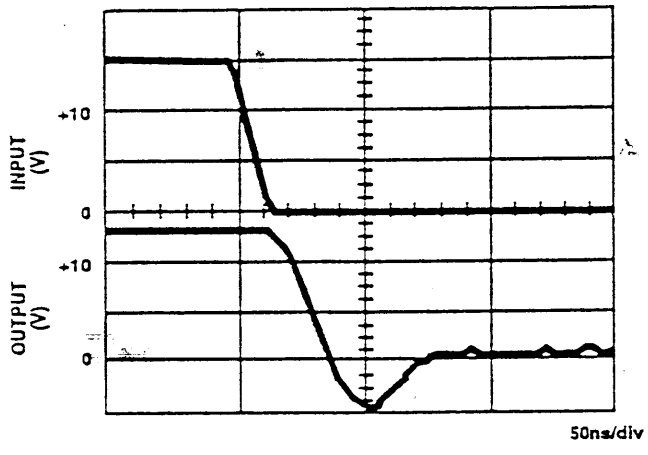


FIGURE 11. HIGH TO LOW TRANSIENT RESPONSE WAVEFORMS (C_L = 10nF)

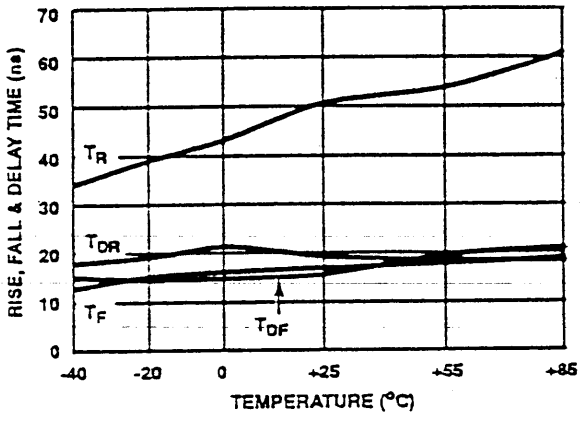


FIGURE 12. RISE, FALL & DELAY TIMES vs TEMPERATURE

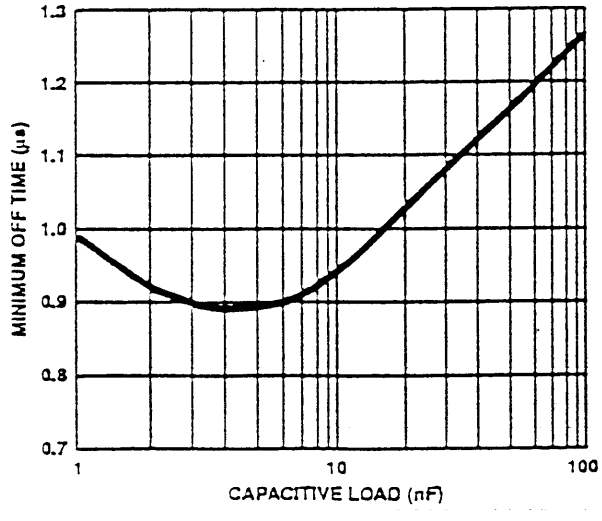


FIGURE 13. MINIMUM OFF TIME (T_{OR}) vs C_L AT +25°C

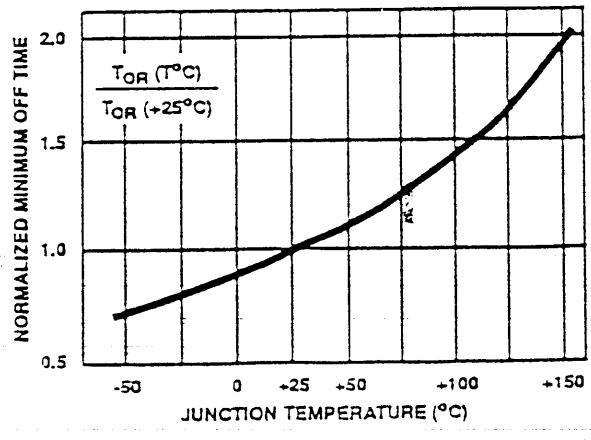


FIGURE 14. NORMALIZED MINIMUM OFF TIME (T_{OR}) vs TEMPERATURE (C_L = 10nF)

Typical Performance Curves T_A = -25°C Unless Otherwise Specified (Continued)

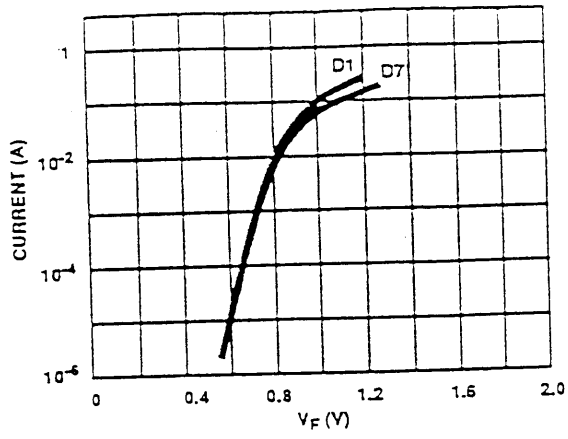


FIGURE 15. DIODE D1 & D7 CURRENT vs V_F

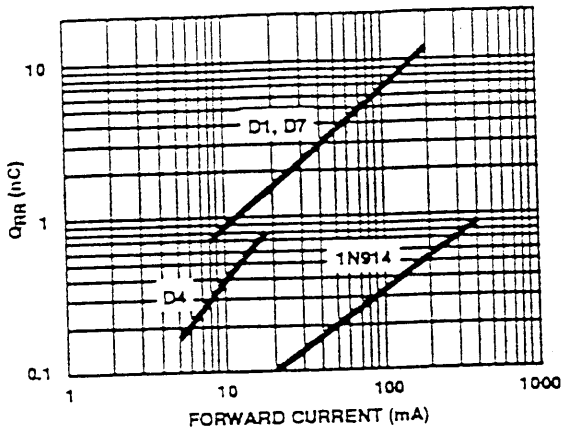
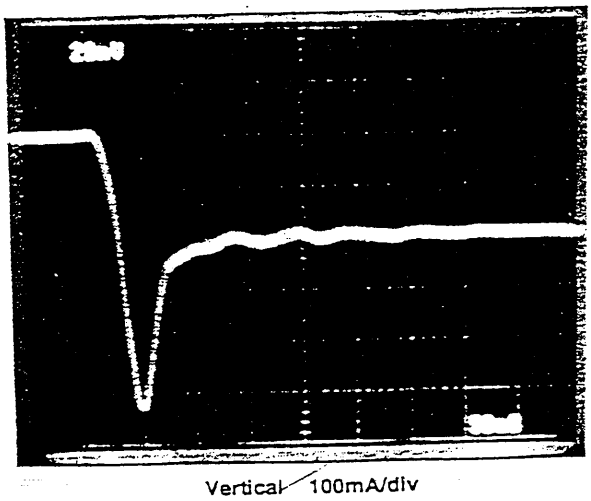


FIGURE 16. DIODE Q_{RR} vs FORWARD CURRENT



Vertical 100mA/div
Horizontal 50ns/div

FIGURE 17. DIODE D1 REVERSE RECOVERY WAVEFORM
I_F = 200mA, 20V REVERSE BIAS

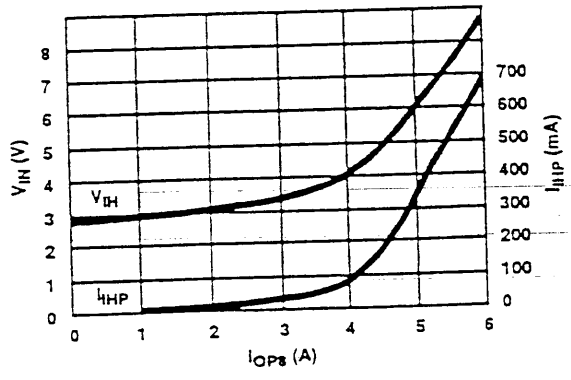


FIGURE 18. V_{IH} & I_{IHP} vs I_{OPS} [V_{OUT} (PIN 8) = 0, V+ = 15V, 1µs PULSE]

Metallization Topology

DIE DIMENSIONS:
66.9 x 71.65 x 19 mils
(1700 x 1820 x 483µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

SUBSTRATE POTENTIAL (POWERED UP):
Unbiased

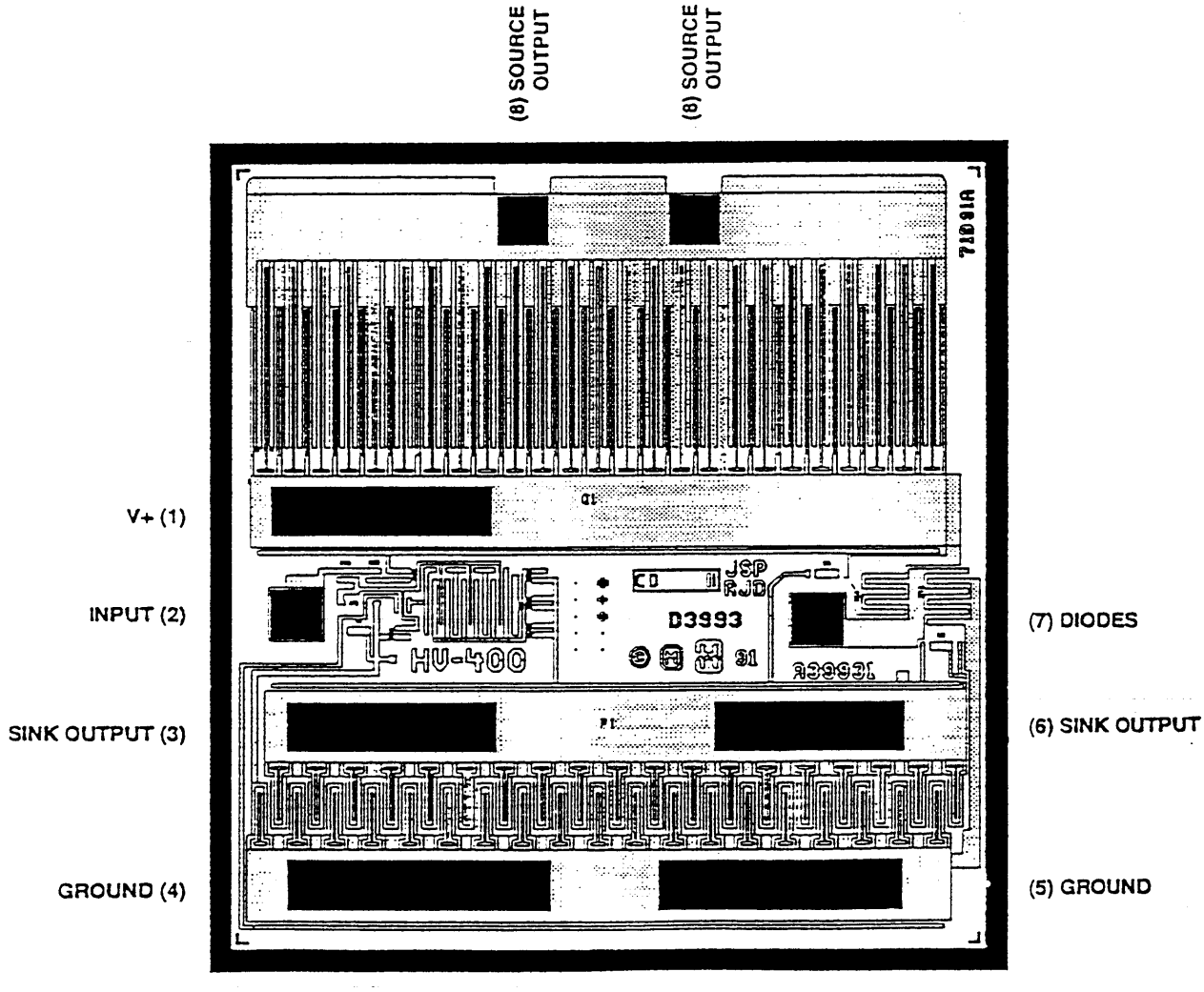
GLASSIVATION:
Type: Silox
Thickness: 12kÅ ± 2kÅ
Type: Nitride
Thickness: 3.5kÅ ± 2.5kÅ

TRANSISTOR COUNT: 3

PROCESS: HFSB Linear Dielectric Isolation

Metallization Mask Layout

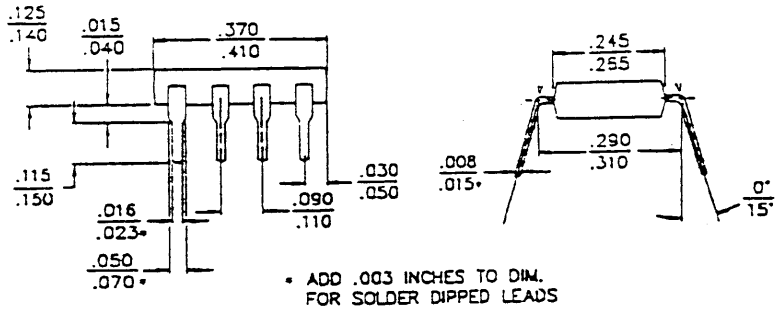
HV400Y



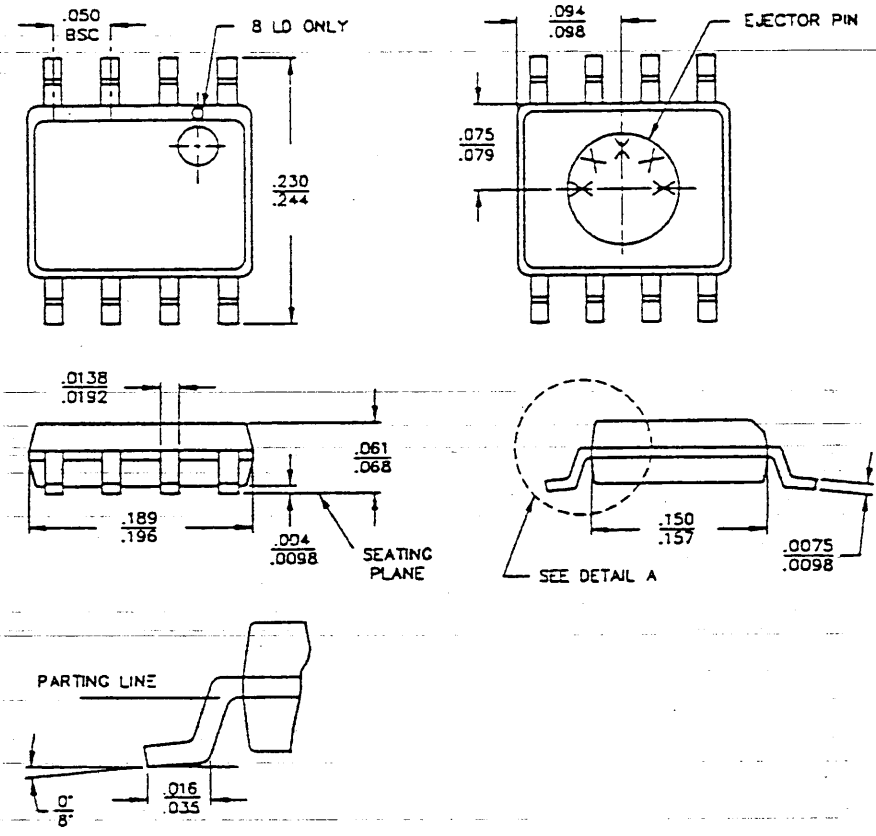
NOTE: Pin Numbers Correspond to Mini-DIP and SOIC Packages Only.

Packaging

8 PIN PLASTIC MINIDIP



8 PIN PLASTIC SOIC



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