MICROCHIP

FPGA and SoC Product Families

Lowest Power, Proven Security and Exceptional Reliability

Rethink FPGAs

Our unique, low-power, non-volatile technology sets Microchip's Field Programmable Gate Arrays (FPGAs) apart from traditional SRAM-based devices. With an extensive heritage of reliability, Microchip's FPGAs and SoCs meet demands for low power, and security in a variety of applications.

In wired and wireless communications, defense and aviation, and industrial embedded applications, Microchip FPGAs deliver ample resources at the lowest power, highest reliability and greatest security. Microchip FPGAs demonstrate value in applications such as hardware acceleration, artificial intelligence, image processing and edge computing with robust DSP and memory resources.

Broad Range FPGA Supplier (1-500K LE)

Features	SmartFusion® ProASIC3®, IGLOO®	SmartFusion2 IGLOO2	PolarFire™
Logic Elements	100–30K	5K–150K	100–480K
Transceiver Rate	–	1–5 Gbps	250 Mbps–12.7 Gbps
I/O Speeds	400 Mbps LVDS	667 Mbps DDR3 750 Mbps LVDS	1600 Mbps DDR4 1.6 Gbps LVDS
DSP (18x18 Multipliers)	–	240	1480
Max RAM	144 Kb	5 Mb	33 Mb
Processor Option	Hard 100 MHz Arm® Cortex®-M3	Hard 166 MHz Arm Cortex-M3 Soft RISC-V	Soft RISC-V Hard Crypto Processor
On-Board Flash	Up to 512 KB code store	Up To 512 KB code store	56 KB secure NVM
Family Type	CPLD Replacements Smallest Packages	Low Density FPGAs with more resources and lowest power	Mid-Range Density FPGAs Lowest Power, Cost Optimized

PolarFire™ Cost-Optimized to Deliver the Lowest Power at Mid-Range Densities

The PolarFire family extends Microchip's non-volatile FPGA leadership by offering up to 50% lower power than equivalent SRAM FPGAs. The devices are ideal for a wide range of implementations within wireline access networks and cellular infrastructure, defense and commercial aviation markets, as well as industrial automation and IoT markets. The devices offer unprecedented capabilities while maintaining all the advantages traditionally associated with non-volatile FPGAs such as the lowest static power, the best security and FPGA configuration cell Single Event Upset (SEU) immunity.

The PolarFire family is cost-optimized to give designers a mid-range portfolio of FPGAs with the SERDES and DSP resources needed for a range of high-speed and compute intensive applications constrained by low-power and small formfactor.

As a true broad-range FPGA supplier, Microchip offers FPGA product families spanning 1K to 500K Logic Elements (LEs).

The devices offer unprecedented capabilities while maintaining all the advantages traditionally associated with non-volatile FPGAs such as the lowest static power, security and Single Event Upset (SEU) immunity.

Cost-Optimized Architecture

- Transceiver performance optimized for 12.7 Gbps, which yields smaller size
- Architecture and process optimizations for specific band-widths (10 Gbps–40 Gbps) at specific densities
- 1.6 Gbps I/Os—best-in-class hardened I/O gearing logic with CDR (supports SGMII/GbE links on these GPIOs)
- High-performance, best-in-class hardened security IP in mid-range devices

Power Optimization

- The lowest static power—28 nm non-volatile process yields very-low static power
- Optimized for 12.7 Gbps, which yields the lowest power
- Integrated hard IP—DDR PHY, PCIe endpoint/root port, crypto processor
- Total power (static and dynamic)—up to 50% lower power

Solving Key Market Issues

Communications

- Low-cost 10G SERDES with built-in burst mode receiver for small form factor PON applications
- Built-in CDR on GPIO enables use of smaller devices when using GbE
- Hardened pre-adders ideal for low/mid-bandwidth DFE 4 × 4 × 60 MHz and baseband processing
- Ultra-low power transceiver for 10G CPRI, bridging, and fronthaul/back-haul transport

Defense

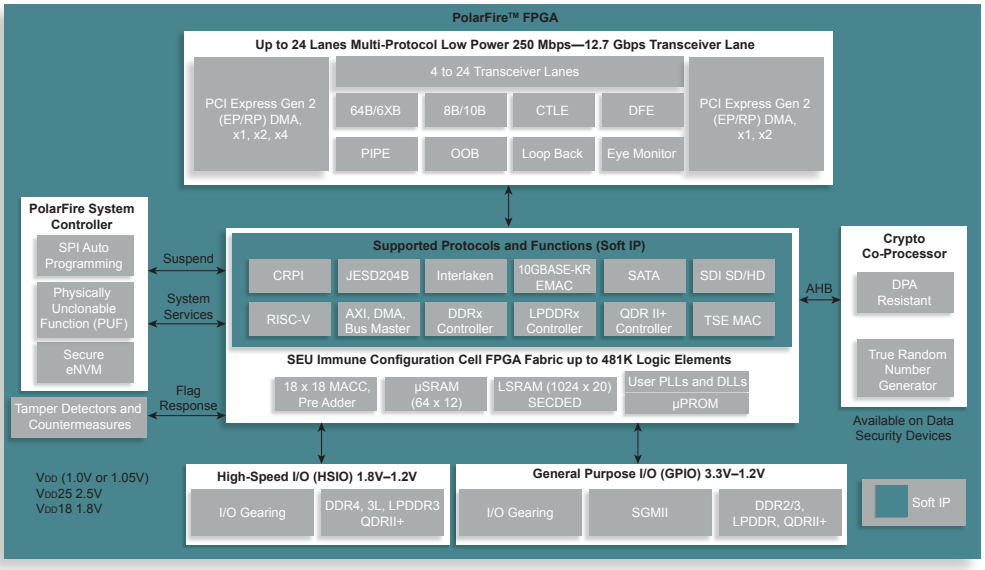
- Anti-tamper for Foreign Military Sales (FMS)
- Increasing automation in vehicles and weaponry
- Enhancing operator situational awareness
- Battlefield portability and increased mission life
- Increased cybersecurity
- Supply chain security

Industrial

- Integration of imaging and AI for smart embedded systems
- Increased networking of factory automation
- M2M—growth of additional sensors and nodes
- Rise of cloud services requiring decentralized, secure computing
- Portability becoming more prevalent
- Cyber security threats
- Functional safety

Delivering 50% Lower Power With Up to 500K Logic Elements, 12.7G Transceivers

- High-speed serial connectivity with built-in multi-gigabit/multi-protocol transceivers from 250 Mbps to 12.7 Gbps
- Up to 481K logic elements consisting of a 4-input Look-Up Table (LUT) with a fractureable D-type flip-flop
- Up to 33 Mbits of RAM
- Up to 1480 18 × 18 multiply accumulate blocks with hardened pre-adders
- Integrated dual PCIe for up to ×4 Gen 2 Endpoint (EP) and Root Port (RP) designs
- High-Speed I/O (HSIO) supporting up to 1600 Mbps DDR4, 1333 Mbps DDR3L and 1333 Mbps LPDDR3/DDR3 memories with integrated I/O gearing
- General Purpose I/O (GPIO) supporting 3.3V built-in CDR to support SGMII for serial gigabit Ethernet, 1067 Mbps DDR3, and 1600 Mbps LVDS I/O speed with integrated I/O gearing logic



Reliability Features

- SEU immune FPGA configuration cells
- Built-in SECDED and memory interleaving on LSRAMs
- System controller suspend mode for safety-critical designs

Security Features

- Integrated Physically Unclonable Function (PUF)
- Built-in tamper detectors and countermeasures
- Integrated Athena TeraFire EX-P5200B Crypto Co-processor
- True random number generator
- CRI DPA countermeasures and pass through license

Smart Embedded Vision

- Small form factors
- MIPI sensor interface
- Soft core imaging and video IP
- Machine learning inferencing IP
- CoaXPress®

Cyber Security is the #1 Concern for Connected Devices on the Network Edge

It is not enough for today's demanding applications to meet the functional requirements of their design—they must do so in a secured way. Security starts during silicon manufacturing and continues through system deployment and operations. Our PolarFire FPGAs represent the industry's most advanced secure programmable FPGAs.

Security Leadership

Security Advantage	Low Density		Mid-Range	
	Microchip	Competition	Microchip	Competition
Prevent overbuilding and cloning	Best Low-density Security	N/A	Best Security in the Industry	N/A
Full design IP protection		N/A		Weak
Root of trust		N/A		N/A
Secure data communications		N/A		Weak
Anti-tamper		N/A		N/A

"The number of IoT sensors is expected to approach 30 billion in 5 years – and each unit is a potential entry point for cyber-criminals" – The Economist Intelligence Unit, April, 2016

"Some call cybercrime the greatest transfer of wealth in human history" – The Center of Strategic and International Studies, The Economic Impact of Cybercrime, July 2013

Feature and Packaging Overview of the PolarFire FPGA Family

		PolarFire™ FPGAs			
Features		**MPF100T**	**MPF200T**	**MPF300T**	**MPF500T**
FPGA fabric	Logic elements (4 LUT + DFF)	109	192	300	481
	Math blocks (18 × 18 MACC)	336	588	924	1480
	LSRAM blocks (20 kbits)	352	616	952	1520
	µSRAM blocks (64 × 12)	1008	1764	2772	4440
	Total RAM (Mbits)	7.6	13.3	20.6	33
	µPROM (Kbits, 9-bit bus)	297	297	459	513
	User DLLs/PLLs	8	8	8	8
High-speed I/O	250 Mbps to 12.7 Gbps transceiver lanes	8	16	16	24
	PCIe Gen2 endpoints/root ports	2	2	2	2
Total I/Os	Total user I/Os	284	368	512	584
Packaging	Type/size/pitch	Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs			
	FCSG325 (11 × 11, 11 × 14.5*, 0.5 mm)	170(84/86) 8/4	170(84/86) 8/4*		
	FCSG536 (16 × 16, 0.5 mm)		300(120/180) 15/4	300(120/180) 15/4	
	FCVG484 (19 × 19, 0.8 mm)	284(120/164) 14/4	284(120/164) 14/4	284(120/164) 14/4	
	FCG484 (23 × 23, 1.0 mm)	244(96/148) 13/8	244(96/148) 13/8	244(96/148) 13/8	
	FCG784 (29 × 29, 1.0 mm)		364(132/232) 20/16	388(156/232) 20/16	388(156/232) 20/16
	FCG1152 (35 × 35, 1.0 mm)			512(276/236) 24/16	584(324/260) 24/24

Devices in the same package and family type are pin-compatible.
*Wider package dimension applies to the MPF200 device only.

More Resources in Low-Density Devices with Arm® Cortex®-M3 Processor

SmartFusion®2 SoC FPGAs deliver more resources in low-density devices with low-power requirements, proven security and exceptional reliability. These devices are ideal for general purpose functions such as Gigabit Ethernet or dual-PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. Our SoC FPGAs are used in communications, industrial, medical, defense and aviation markets.

- Embedded Arm Cortex-M3 Microcontroller Subsystem (MSS)
- PCIe Gen2 endpoints starting at 10K logic elements
- Embedded DDR3 memory controllers
- Small packages
- 1 mW in Flash*Freeze mode
- Instant-on
- Zero FIT FPGA configuration cells
- SECDED memory protection
- NRBG, AES-256, SHA-256, ECC cryptographic engine
- User Physically Unclonable Function (PUF)
- CRI DPA pass-through license

SmartFusion2 Devices

SmartFusion®2 Devices	Features	M2S005	M2S010	M2S025	M2S050	M2S060	M2S090	M2S150
Logic/DSP	Maximum logic elements (4LUT + DFF)	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 × 18)	11	22	34	72	72	84	240
	Fabric Interface Controllers (FICs)	1			2	1		2
	PLLs and CCCs	2		6				8
	Security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
MSS	Cortex-M3 + instruction cache	Yes						
	eNVM (KB)	128	256				512	
	eSRAM (KB)	64						
	eSRAM (KB) non-SECDED	80						
	CAN, 10/100/1000 Ethernet, HS USB	1 each						
	Multi-mode UART, SPI, I²C, timer	2 each						
Fabric Memory	LSRAM 18K blocks	10	21	31	69		109	236
	uSRAM 1K blocks	11	22	34	72		112	240
	Total RAM (kbits)	191	400	592	1,314		2,074	4,488
High-Speed	DDR controllers (count × width)	1 × 18			2 × 36	1 × 18		2 x 36
	SERDES lanes	0	4		8	4		16
	PCIe endpoints	0	1		2			4
User I/O	MSIO (3.3 V)	115	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40		62	40		106
	DDRIO (2.5 V)	66	70		176	76		176
	Total user I/Os	209	233	267	377	387	425	574

Low-Density Devices with High-Performance Memory Subsystem

IGLOO2 FPGAs deliver more resources in low-density devices with low-power requirements, proven security and exceptional reliability than any FPGAs in their class. These devices are ideal for general purpose functions such as Gigabit Ethernet or dual-PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. FPGAs are used in communications, industrial, medical, defense and aviation markets.

- High-performance memory subsystem
- PCIe Gen2 endpoints starting at 10K logic elements
- Embedded DDR3 memory controllers
- SECDED memory protection
- 1 mW in Flash*Freeze mode
- Instant-on
- Zero FIT FPGA configuration cells
- CRI DPA pass-through license
- Small packages
- NRBG, AES-256, SHA-256, ECC cryptographic engine
- User Physically Unclonable Function (PUF)

IGLOO2 Devices

IGLOO®2 Devices	Features	M2GL005	M2GL010	M2GL025	M2GL050	M2GL060	M2GL090	M2GL150
Logic/ DSP	Maximum logic elements (4LUT + DFF)	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 × 18)	11	22	34	72	72	84	240
	PLLs and CCCs	2		6				8
	SPI/HPDMA/PDMA	1 each						
	Fabric interface controllers (FICs)	1			2	1		2
	Data security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
Memory	eNVM (KB)	128	256				512	
	LSRAM 18K blocks	10	21	31	69		109	236
	uSRAM 1K blocks	11	21	34	72		112	240
	eSRAM (KB)	64						
	Total RAM (kbits)	703	912	1104	1826		2586	5000
High-speed	DDR controllers (count × width)	1 × 18			2 × 36	1 × 18		2 × 36
	SERDES lanes	0	4		8	4		16
	PCIe endpoints	0	1		2			4
User I/O	MSIO (3.3 V)	115	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40		62	40		106
	DDRIO (2.5 V)	66	70		176	76		176
	Total user I/Os	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M)	C, I	C, I, M					

Notes: 1. Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 and SmartFusion2 Fabric User Guide for details. 2. Feature availability is package dependent.

The Ideal Low-Power, Programmable Solution for CPLD Replacement

The IGLOO family of reprogrammable and full-featured Flash FPGAs is designed to meet the low-power and area requirements of today's portable electronics. Based on nonvolatile Flash technology, the 1.2V to 1.5V operating voltage family offers the industry's lowest-power consumption—as low as 5 µW. The IGLOO family supports up to 35K logic elements with up to 504 kbits of true dual-port SRAM, up to six embedded PLLs, and up to 620 user I/Os. Low-power applications that require 32-bit processing can use the Arm Cortex-M1 processor without license fees or royalties in M1 IGLOO devices. Developed specifically for implementation in FPGAs, Cortex-M1 devices offer an optimal balance between performance and size to minimize power consumption.

- Low-power FPGAs
- Flash*Freeze technology for low-power consumption
- 1.2V core and I/O voltage
- Instant-on
- AES-protected In-System Programming (ISP)
- User nonvolatile FlashROM

IGLOO/e Devices

IGLOO® Devices	Features	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
Arm®-Enabled IGLOO[1] devices					M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
Logic	Logic elements (approximate)	330	700	1,500	3,000	5,000	7,000	11,000	7,000	35,000
	System gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	3,000,000
	VersaNet globals[3]	6	18	18	18	18	18	18	18	18
	Flash*Freeze mode (typical, µW)	5	10	16	24	32	36	53	49	137
	AES-protected ISP[1]		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Integrated PLLs with CCC[2]		1	1	1	1	1	1	6	6
Fabric memory	RAM (1,024 bits)		18	36	36	54	108	144	108	504
	RAM blocks (4,608 bits)		4	8	8	12	24	32	24	112
	FlashROM kbits (1,024 bits)	1	1	1	1	1	1	1	1	1
User I/O	I/O banks	2	2	2	4	4	4	4	8	8
	Maximum user I/Os	81	96	133	143	194	235	300	270	620

Notes: 1. AES is not available for Cortex-M1 IGLOO devices. 2. AGL060 in CS121 does not support the PLL. 3. Six chip (main) and twelve quadrant global networks are available for AGL060 devices and above.

The Industry's Lowest-Power, Smallest-Size Solution

IGLOO nano products offer groundbreaking possibilities in power, size, lead-times, operating temperature ranges and cost. Available in logic densities from 100–3K logic elements, 1.2V to 1.5V IGLOO nano devices have been designed for high-volume applications where power and size are the key decision criteria. IGLOO nano devices are perfect ASIC or ASSP replacements, yet retain the historical FPGA advantages of flexibility and quick time-to-market in low-power and small footprint profiles.

- Ultra-low power in Flash*Freeze mode, as low as 2 µW
- Small footprint packages from 14 mm × 14 mm to 3 mm × 3 mm
- Enhanced commercial temperature
- 1.2V to 1.5V single voltage operation
- Enhanced I/O features
- Embedded SRAM and non-volatile memory (NVM)
- ISP and security
- Instant-on

IGLOO nano Devices

IGLOO® nano Devices	Features	AGLN010	AGLN020	AGLN060	AGLN125	AGLN250
Logic	Logic elements (approximate)	100	200	700	1,500	3,000
	System gates	10,000	20,000	60,000	125,000	250,000
	VersaNet globals	4	4	18	18	18
	Flash*Freeze mode (typical, µW)	2	4	10	16	24
	AES-protected ISP			Yes	Yes	Yes
	Integrated PLL in CCCs[1]			1	1	1
Fabric Memory	RAM kbits (1,024 bits)			18	36	36
	4,608-bit blocks			4	8	8
	FlashROM kbits (1,024 bits)	1	1	1	1	1
User I/O	I/O banks	2	3	2	2	4
	Maximum user I/Os (packaged device)	34	52	71	71	68

Notes: 1.AGLN060, AGLN125 and AGLN250 in the CS(G)81 package do not support PLLs.

Low-Power FPGA with Enhanced I/O Capabilities

IGLOO PLUS products deliver low-power consumption and enhanced I/Os in a feature-rich programmable device, offering more I/Os per logic element than IGLOO devices and supporting independent Schmitt trigger inputs, hot-swapping, and Flash*Freeze bus hold. Ranging from 330–1.5K logic elements, 1.2V to 1.5V IGLOO PLUS devices have been optimized to meet the needs of I/O-intensive, power-conscious applications that require exceptional features.

- I/O-optimized FPGA
- Low power in Flash*Freeze mode, as low as 5 µW
- Small footprint and low-cost packages
- Reprogrammable Flash technology
- 1.2V to 1.5V single voltage operation
- Embedded SRAM NVM
- AES-protected ISP
- Instant-on

IGLOO PLUS Devices

IGLOO® PLUS Devices	Features	AGLP030	AGLP060	AGLP125
Logic	Logic elements (approximate)	330	7,000	1,500
	System gates	30,000	60,000	125,000
	VersaNet globals	6	18	18
	Flash*Freeze mode (typical, µW)	5	10	16
	AES-protected ISP		Yes	Yes
	Integrated PLL in CCCs[1]		1	1
Fabric memory	RAM (1,024 bits)		18	36
	4,608-bit blocks		4	8
	FlashROM kbits (1,024 bits)	1	1	1
User I/O	I/O banks	4	4	4
	Maximum user I/Os (packaged device)	120	157	212

Notes: 1. AGLP060 in CS(G)201 does not support the PLL.

Low-Density FPGAs for Replacing CPLDs

The ProASIC3 series of Flash FPGAs offers a breakthrough in power, performance, density and features for today's most demanding high-volume applications. ProASIC3 devices support the Arm Cortex-M1 processor, offering the benefits of programmability and time-to-market at low cost. ProASIC3 devices are based on nonvolatile Flash technology and support 330–35K logic elements and up to 620 high-performance I/Os. For automotive applications, selected ProASIC3 devices are qualified to AEC-Q100 and are available with AEC T1 screening and PPAP documentation.

- 1.5V single voltage operation
- 350 MHz system performance
- Instant-on
- Configuration memory error immune
- Advanced I/O standards
- Secure ISP

ProASIC3/E Devices

ProASIC®3/E Devices	Features	A3P030	A3P060[2]	A3P125[2]	A3P250[2]	A3P400	A3P600	A3P1000[2]	A3PE600	A3PE1500	A3PE3000
Arm® Cortex®-M1 Devices					M1A3P250	M1A3P400	M1A3P600	M1A3P1000		M1A3PE1500	M1A3PE3000
Logic	Logic elements (approximate)	330	700	1,500	3,000	5,000	7,000	11,000	7,000	16,000	35,000
	System gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	1,500,000	3,000,000
	VersaNet globals[3]	6	18	18	18	18	18	18	18	18	18
	AES-protected ISP[1]		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Integrated PLL in CCCs		1	1	1	1	1	1	6	6	6
Fabric Memory	RAM (1,024 bits)		18	36	36	54	108	144	108	270	504
	4,608-bit blocks		4	8	8	12	24	32	24	60	112
	FlashROM kbits (1,024 bits)	1	1	1	1	1	1	1	1	1	1
User I/O	I/O banks	2	2	2	4	4	4	4	8	8	8
	Maximum user I/Os	81	96	133	157	194	235	300	270	444	620

Notes: 1. AES is not available for Arm Cortex-M1 ProASIC3 devices. 2. Available as automotive "T" grade 3. Six chip (main) and three quadrant global networks are available for A3P060 and above.

Low-Density CPLD Replacement with Small Package Footprint

Our innovative ProASIC3 nano devices bring a new level of value and flexibility to high-volume markets. When measured against the typical project metrics of performance, cost, flexibility and time-to-market, ProASIC3 nano devices provide an attractive alternative to ASICs and ASSPs in fast-moving or highly competitive markets. Customer-driven total-system cost reduction was a key design criteria for the ProASIC3 nano program. Single-chip implementation and a broad selection of small footprint packages contribute to lower total system costs.

- 1.5V core for low power
- 350 MHz system performance
- Configuration memory error immune
- Enhanced commercial temperature
- Enhanced I/O features
- ISP and security

ProASIC3 nano Devices

ProASIC®3 nano Devices	Features	A3PN010	A3PN020	A3PN060	A3PN125	A3PN250
Logic	Logic elements (approximate)	100	200	700	1,500	3,000
	System gates	10,000	20,000	60,000	125,000	250,000
	VersaNet globals	4	4	18	18	18
	AES-protected ISP			Yes	Yes	Yes
	Integrated PLL in CCCs			1	1	1
Fabric Memory	RAM (1,024 bits)			18	36	36
	4,608-bit blocks			4	8	8
	FlashROM kbits (1,024 bits)	1	1	1	1	1
User I/O	I/O banks	2	3	2	2	4
	Maximum user I/Os (packaged device)	34	49	71	71	68

Low-Density, Low-Power CPLD Replacement FPGA

ProASIC3L FPGAs feature lower dynamic and static power requirements than the previous generation of ProASIC3 FPGAs and requirements by orders of magnitude than SRAM competitors, combining dramatically reduced power consumption with up to 350 MHz operation. The ProASIC3L family also supports the free implementation of an FPGA-optimized 32-bit Arm Cortex-M1 processor, enabling you to select the Microchip Flash FPGA solution that best meets your speed and power requirements, regardless of application or volume. Optimized software tools using Power-Driven Layout (PDL) provide instant power-reduction capabilities.

- Low-power 1.2V to 1.5V core operation
- 700 Mbps DDR, LVDS capable I/Os
- Up to 350 MHz system performance
- Configuration memory error immune
- ISP and security
- Flash*Freeze technology for low power

ProASIC3L Low-Power Devices

ProASIC®3L Devices	Features	A3P600L	A3P1000L	A3PE3000L
Arm® Cortex®-M1 Devices[1]		M1A3P600L	M1A3P1000L	M1A3PE3000L
Logic	Logic elements (approximate)	7,000	11,000	35,000
	System gates	600,000	1,000,000	3,000,000
	VersaNet globals	18	18	18
	AES-protected ISP[2]	Yes	Yes	Yes
	Integrated PLL in CCCs[3]	1	1	6
Fabric Memory	RAM (1,024 bits)	108	144	504
	4,608-bit blocks	24	32	112
	FlashROM kbits (1,024 bits)	1	1	1
User I/O	I/O banks	4	4	8
	Maximum user I/Os (packaged device)	235	300	620

Notes: 1. Refer to the Cortex-M1 product brief for more information. 2. AES is not available for Cortex-M1 ProASIC3L devices. 3. For the A3PE3000L, the PQ208 package has six CCCs and two PLLs.

Low-Cost FPGA With Integrated Arm Cortex-M3 Processor

SmartFusion SoCs integrate an FPGA fabric, an Arm Cortex-M3 processor, and a programmable Analog Compute Engine (ACE), offering full customization, IP protection and ease-of-use. Based on Microchip's proprietary Flash process, SmartFusion SoCs are ideal for hardware and embedded designers who need a true system-on-chip that gives more flexibility than traditional fixed-function microcontrollers without the excessive cost of soft processor cores on traditional FPGAs.

- Available in commercial, industrial and military grades
- Hard 100 MHz 32-bit Arm Cortex-M3 CPU
- Multi-layer AHB communications matrix with up to 16 Gbps throughput
- 10/100 Ethernet MAC
- Two peripherals of each type: SPI, I²C, UART and 32-bit timers
- Up to 512 KB Flash and 64 KB SRAM
- External Memory Controller (EMC)
- 8-channel DMA controller
- Integrated Analog-to-Digital converters (ADCs) and Digital-to-Analog converters (DACs) with 1 % accuracy
- On-chip voltage, current and temperature monitors
- Up to ten 15 ns high-speed comparators
- Analog Compute Engine (ACE) offloads CPU from analog processing
- Up to 35 analog I/Os and 169 digital GPIOs

SmartFusion Devices

	Features	A2F200	A2F500
Logic	Logic elements (approximate)	2,000	6,000
	System gates	200,000	500,000
	RAM blocks (4,608 bits)	8	24
Microcontroller Subsystem (MSS)	Flash (KB)	256	512
	SRAM (KB)	64	64
	Cortex®-M3 with memory protection unit (MPU)	Yes	Yes
	10/100 Ethernet MAC	Yes	Yes
	External memory controller (EMC)	26-bit address, 16-bit data	26-bit address, 16-bit data[1]
	DMA	8 Ch	8 Ch
	I²C	2	2
	SPI	2	2
	16550 UART	2	2
	32-bit timer	2	2
	PLL	1	2[2]
	32 kHz low power oscillator	1	1
	100 MHz on-chip RC oscillator	1	1
	Main oscillator (32 KHz to 20 MHz)	1	1
Programmable analog	ADCs (8-/10-/12-bit SAR)	2	3[4]
	DACs (12-bit sigma-delta)	2	3[4]
	Signal Conditioning Blocks (SCBs)	4	5[4]
	Comparators[3]	8	10[4]
	Current monitors[3]	4	5[4]
	Temperature monitors[3]	4	5[4]
	Bipolar high voltage monitors[3]	8	10[4]

Notes: 1. Not available on A2F500 for the PQ208 package and A2F060 for the TQ144 package. 2. Two PLLs are available in CS288 and FG484, one PLL in FG256 and PQ208. 3. These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User's Guide for details. 4. Available on FG484 only. PQ208, FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.

FPGAs and SoCs for Military Applications

For more than 25 years, Microchip's FPGAs have lead the industry in high reliability for defense applications. FPGAs are qualified to Mil Std 883 Class B and QML Class Q. Based on Flash architecture, we offer the industry's most reliable and low-power FPGAs and SoC FPGAs. Military-grade FPGAs are available in IGLOO2, ProASICPlus, and ProASIC3/EL device families and SoC FPGAs are available in SmartFusion2, SmartFusion and Fusion device families. In addition to the advantages of the mainstream FPGAs, SoC FPGAs have an embedded Arm Cortex-M3 microcontroller on-chip. SmartFusion and Fusion devices integrate configurable analog peripherals to yield a true system-on-chip solution.

- Tested for high reliability at temperature range of –55ºC to 125ºC
- Product longevity
- ISO-9001 and AS-9100-certified quality management system
- PCI Express Gen1 endpoints
- Instant-on
- Small packages
- Zero FIT FPGA configuration cells
- SECDED memory protection
- Built-in tamper detection and zeroization capability
- NRBG, AES-256, SHA-256 and ECC cryptographic engine
- User Physically Unclonable Function (PUF)
- CRI DPA pass-through license
- Lowest-power operation
- Embedded Arm Cortex-M3 microcontroller subsystem

SoC FPGAs and FPGAs for Automotive

Microchip offers automotive-grade (AEC-Q100) SoC FPGA and FPGAs with industry leading reliability and security features. These devices are power and cost optimized to provide you with the lowest total cost of ownership. Microchip offers dedicated automotive-grade devices with various densities, features, footprints and temperature grades. All devices and packages are AEC-Q100-qualified and tested at extended temperatures. PPAP documentation available on request.

Family	Logic Elements	Temperature Range	Maximum User I/Os	Maximum SERDES
IGLOO®2[1]	6K to 86K	Grade 1 (–40 °C to 135 °C) Grade 2 (–40 °C to 125 °C)	Up to 425	4[1]
SmartFusion®2	6K to 86K	Grade 2 (–40 °C to 125 °C)	Up to 425	4
ProASIC®3	700K to 11K	Grade 1 (–40 °C to 135 °C) Grade 2 (–40 °C to 115 °C)	Up to 300	Not available

Notes: 1. SERDES is only supported in the IGLOO2 devices with Grade 2 temperature range, not on Grade 1 temperature range.

ProASIC3 Package Options

Features	VQG100	FGG144	FGG256	FGG484
Pitch (mm)	0.5	1	1	1
Length × Width (mm)	16 × 16	13 × 13	17 × 17	23 × 23
Device	I/O	I/O	I/O	I/O
A3P060	71	96		
A3P125	71	97		
A3P250	68/13	97/24		
A3P1000		97/25	177/44	300/74

SmartFusion 2 and IGLOO2 Package Options

Type	VFG256[1]		VFG400[1]		TQG144		FGG484[1]		FGG676[1]	
Pitch (mm)	0.8		0.8		0.5 mm		1		1	
Length × Width (mm)	14 × 14		17 × 17		20 × 20		23 × 23		27 × 27	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005S	161		171		84		209			
M2S010TS	138	2	195	4	84		233	4		
M2S025TS	138	2	207	4			267	4		
M2S060TS			207	4			267	4	387	4
M2S090TS							267	4	425	4

Note: 1. All Automotive packages are RoHS compliant and available in lead-free options only. 2. Shadeing indicates that device packages have vertical migration capability.

High-Speed RT FPGAs for Signal Processing Applications

RTG4 FPGAs integrate fourth-generation Flash-based FPGA fabric and high-performance interfaces such as Serialization/Deserialization (SERDES) on a single chip while maintaining the resistance to radiation-induced configuration upsets in the harshest radiation environments, such as space flight (LEO, MEO, GEO, HEO, deep space); high-altitude aviation, medical electronics and nuclear power plant control.

Radiation Tolerance

- Configuration memory upsets immunity to LET > 103 MeV.cm2/mg
- Single-Event Latch-Up (SEL) immunity to LET > 103 MeV.cm2/mg
- SEU-hardened registers eliminate the need for Triple-Module Redundancy (TMR)
- Immune to Single-Event Upsets (SEU) to LET > 37 MeV.cm2/mg
- SEU rate < 10-12 errors/bit-day (GEO Solar Min)
- SRAM has a built-in Error Detection and Correction (EDAC)
- Upset rate < 10-11 errors/bit-day (GEO Solar Min)
- Single Error Correction And Double Error Detection (SECDED)
- Single-Event Transient (SET) upset rate < 10-8 errors/bit-day (GEO Solar Min) with optional SET filter
- Total Ionizing Dose (TID) > 100 Krad

High-Performance FPGA

- Efficient 4-input look-up tables (LUTs) with carry chains for high system performance up to 300 MHz without SET filter
- 209 blocks of dual-port 24.5 kbit SRAM (Large SRAM) with 300 MHz synchronous performance (512 × 36, 1 kbit × 18, 2 kbit × 9 and 2 kbit × 12)
- 462 DSP mathblocks with 18-bit × 18-bit input signed multiplication and 44-bit output accumulator
- High-performance, 300 MHz (without SET filter) across military temperature: –55°C to 125°C
- Up to 16 spacewire clock and data recovery circuitry instances, allowing high-performance spacewire interface up to 400 Mbit/sec

High-Speed Serial Interfaces

Up to 24 Lanes of 3.125 Gbps Serialization/Deserialization (SerDes) Supporting

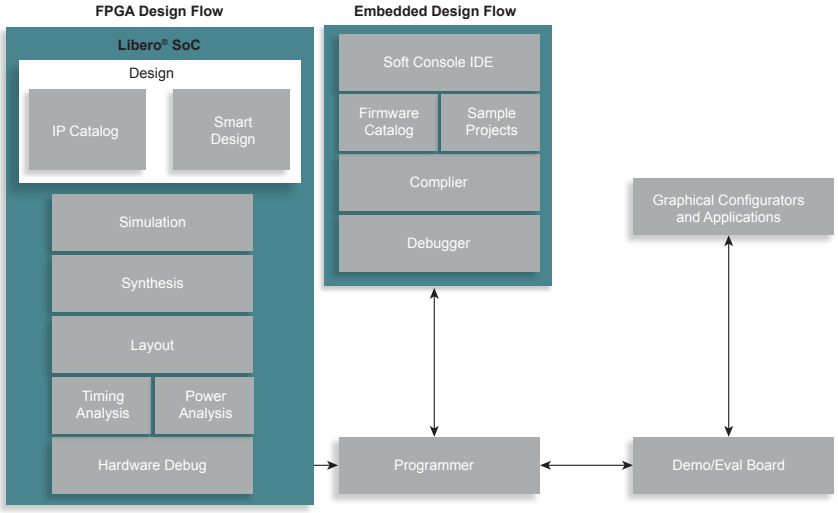
- XGXS/XAUI extension (to implement a 10 Gbps XGMII Ethernet PHY interface)
- Native SerDes interface facilitates implementation of Serial RapidIO (SRIO) in FPGA fabric or an SGMII interface to a soft Ethernet MAC
- PCI express (PCIe) Gen1 hard IP core
- ×1, ×2, and ×4 lane(s) PCI express core
- Up to 2 Kbytes maximum payload size
- 64-/32-bit AXI/AHB master and slave interfaces to the application layer

Libero® SoC Design Suite

Microchip's Libero SoC design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools that are used for designing with power-efficient Flash-based devices.

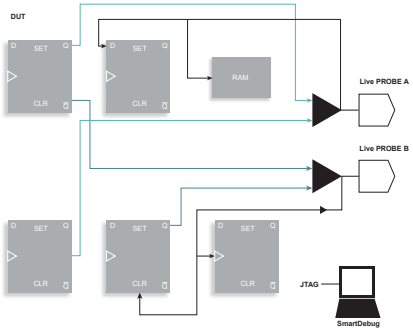
The Libero SoC design suite manages the entire design flow from design entry, synthesis and simulation, through place-and-route, timing and power analysis, with enhanced integration of the embedded design flow. The suite integrates industry-standard Synopsys Synplify Pro synthesis and Mentor Graphics ModelSim simulation with best-in-class constraints management, debug capabilities, timing analysis, power analysis, secure production programming and push button-design flow.

The Libero SoC design suite features an intuitive design flow with GUI wizards to guide the design process. Its easy-to-adopt, single-click synthesis-to-programming flow integrates industry-standard third-party tools and a rich IP library of DirectCores and CompanionCores and it supports complete reference designs and development kits.



SmartDebug

The SmartDebug tool is a new approach to debug the FPGAs and SERDES without using an Integrated Logic Analyzer (ILA). SmartDebug utilizes the dedicated and specialized probe points built into the FPGA fabric, which significantly accelerates and simplifies the debug process. It also provides the ability to select different probe points without additional overhead and saves significant recompile time. SmartDebug supports IGLOO2, SmartFusion2, and RTG4 FPGA families only. The enhanced debug features implemented in these FPGAs give access to any logic element and enable designers to check the state of inputs and outputs in real time, without any need to re-design.



- Uses minimal FPGA resources for debug
- Active probes support static and pseudo static signals
- Live probe supports dynamic signals
- Requires no recompilation or re-programming
- Has observability and controllability features
- Allows on-the-fly changing of probe points

Mi-V RISC-V Ecosystem

The Mi-V Ecosystem of FPGA and embedded systems solutions advances the adoption of the open source RISC-V ISA with design tools, operating systems, design support, boards and CPUs from Microchip and its partners.

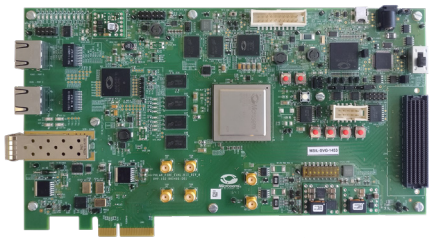
Device Support

Product Family	Device	Software		License Type			
		Libero® IDE	Libero SoC	Eval (Free)	Silver (Free)	Gold	Platinum/ Standalone
RTG4	RT4G150		×	×			×
SmartFusion®2, IGLOO®2	M2S005, M2S010, M2S025 (T devices included) M2GL005, M2GL010, M2GL025 (T devices included)		×	×	×	×	×
	All SmartFusion2 and IGLOO2 devices including S devices		×	×		×	×
SmartFusion, IGLOO, ProASIC®3, Fusion	All Devices		×	×	×	×	×
ProASIC and ProASICPLUS	All Devices	×				×	×
Axcelerator	AX125, AX250, AX500, AX1000	×				×	×
	AX2000	×					×
SX-A, eX, MX	All Devices	×				×	×

License Types

	Evaluation	Silver	Gold	Platinum	Standalone Archive	Standalone (1 yr)
Validity	30 days	1 Yr	1 Yr	1 Yr	Permanent (No Upgrades)	1 Yr
DirectCores	Libero® IP bundle obfuscated and selected RTL IPs	Libero IP bundle obfuscated and selected RTL IPs	Libero IP bundle obfuscated and selected RTL IPs	RTL for Libero IP bundle cores	RTL for Libero IP bundle cores	Libero IP bundle obfuscated and selected RTL IPs
Simulation	ModelSim ME ProMixed language simulation	ModelSim ME Single language simulation	ModelSim ME Pro Mixed language simulation	ModelSim ME Pro Mixed language simulation	Not applicable	Not applicable
Synthesis	Synplify Pro	Synplify Pro	Synplify Pro	Synplify Pro	Not applicable	Not applicable
Programming	Not Supported	Supported	Supported	Supported	Supported	Supported
Identify	Not Supported	Supported	Supported	Supported	Not Supported	Not Supported

PolarFire Evaluation Kit

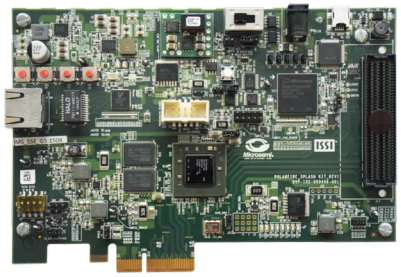


Part No: MPF300TS-1FCG1152EES

This kit is ideal for high-speed transceiver evaluation, 10 Gb Ethernet, IEEE 1588, JESD2048, SyncE, CPRI and more.

- 4 GB 32-bit DDR4, 2GB 16-bit DDR3, and 1Gb SPI Flash Memory
- 2x RJ45 ports with PHY for Ethernet 1588 applications
- Support for SFP+ interface and IOG loopback
- High-speed SerDes interface
- 4x FMC connector (HPC)
- In-silicon temperature monitoring
- On-board 50 MHz system clock

PolarFire Splash Kit

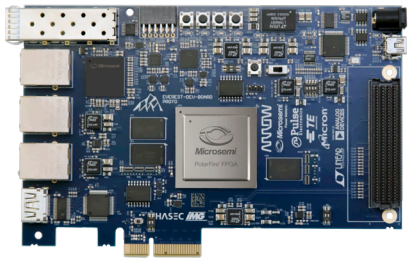


Part No: MPF300TS-1FCG484EES

The PolarFire Splash Kit provides general-purpose interfaces for evaluation and development.

- x32 bit DDR4 and 1 Gb SPI Flash Memory
- RJ45 port with PHY for SGMII applications
- FMC connector (LPC)
- Prototype breadboard area
- PCI express (x4) edge connector
- On-board 50 MHz system clock

Arrow Everest Kit

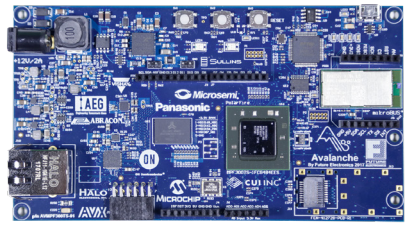


Part No: MPF300TS-1FCG1152EES

This kit is perfect for triple, time-sensitive networking and HDMI applications.

- Triple 1GbE interface
- 1 × 10GbE SFP+ cage
- PCI express (x4) Gen2
- Dual DDR3L (x32 and x16)
- High-speed FMC (HPC) expansion
- HDMI output
- Expansion connectors: PMOD
- Other low-speed interfaces: UART, SPI and I^2C

Future Avalanche Board

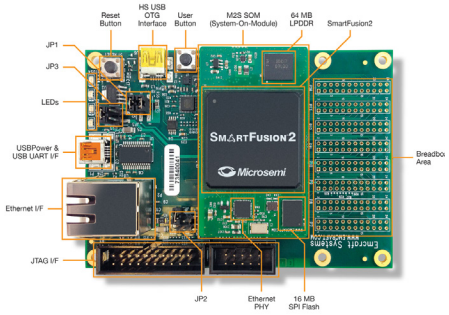


Part No: MPF300TS-FCG484EES

Quickly develop prototypes with this low-cost board.

- 1 GbE interface with PHY (VSC8531)
- Wi-Fi® module
- Expansion connectors: Arduino Shield, MikroBus, PMOD
- DDR3 SDRAM (256Mx16)
- SFP cage
- 64 Mbit SPI Flash
- Other low-speed interfaces: UART and JTAG

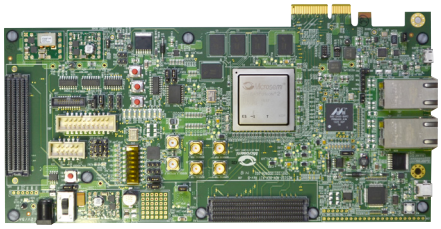
SmartFusion2 Starter Kit



Part No.: SF2-STARTER-KIT, SF2-484-STARTER-KIT, SF2060-STARTER-KIT

- Cost-efficient development environment supporting standard interfaces and Linux-based developments environments
  - 50K LE or 10K LE SmartFusion2 device
  - JTAG interface for programming and debug
  - 10/100 Ethernet
  - USB 2.0 On-The-Go
  - 64 MB LPDDR, 16 MB SPI Flash memory
  - Four LEDs and two push-button switches
  - FlashPro4 programmer
  - USB cables and USB Wi-Fi module

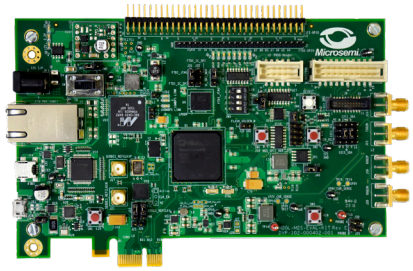
SmartFusion2 Advanced Development Kit



Part No.: M2S150-ADV-DEV-KIT

- Supports numerous standards and interfaces for motor control, industrial automation, high-speed I/O and security applications.
  - 150K LE SmartFusion2 device
  - DDR3 SDRAM, SPI Flash
  - Current measurement test points
  - A pair of SMA connectors, two FMC connectors, PCIe x4 edge connector
  - 2xRJ45 interface for 10/100/1000 Ethernet USB micro-AB connector

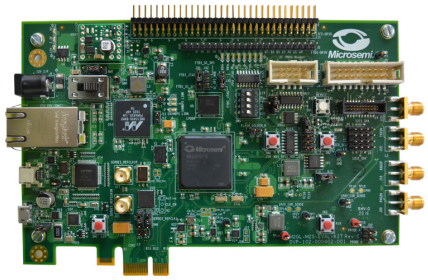
SmartFusion2 Security Evaluation Kit



Part No.: M2S090TS-EVAL-KIT

- Evaluate the data security features of SmartFusion2 SoC
  - 90K LE SmartFusion2 device
  - 64 Mbit SPI Flash memory
  - 512 MB LPDDR
  - PCI Express Gen2 x1 interface
  - Four SMA connector for testing of full-duplex SERDES channel
  - RJ45 interface for 10/100/1000 Ethernet
  - JTAG/SPI programming interface
  - Headers for I^2C, SPI, GPIOs
  - Push-button switches and LEDs for demo purposes
  - Current measurement test points

IGLOO2 Evaluation Kit



Part No.: M2GL-EVAL-KIT

- Comes preloaded with a PCIe control plane demo
  - IGLOO2 FPGA in the FGG484 package (M2GL010T-1FGG484)
  - JTAG/SPI programming interface
  - Gigabit Ethernet PHY and RJ45 connector
  - USB 2.0 OTG interface connector
  - 1 GB LPDDR, 64 MB SPI Flash
  - Headers for I^2C, UART, SPI, GPIOs
  - ×1 Gen2 PCIe edge connector
  - Tx/Rx/Clk SMP pairs

Lowest Power 4K Video and Image Processing

Smart Embedded Vision systems are increasingly being deployed in low-power, small-form factors across a broad spectrum of applications.

Current generation FPGAs must support high-bandwidth video streams, advanced image processing techniques, real-time analysis, including deep learning inference, compression, security, reliability and high-speed interfaces. Microchip's FPGAs enable Smart Embedded Vision by providing:

- Most performance/watts (vs. competing FPGAs)
- In-built security and reliability
- Immunity against Single Event Upsets (SEU)
- Most integrated smart embedded
- Vision platform (video datapath + ISP + deep learning + custom logic)
- Flexible and scalable architecture across PolarFire, SmartFusion2 and IGLOO2 FPGAs

Solution Overview

PolarFire Video and Imaging Kit

- Integrated Sony 8 mp dual cameras
- Supports 4K image processing and rendering
- 12.7G low-power transceiver, 90 mw at 10G
- DDR4@1.6G, CSI-2 Rx@1.0G
- LVDS@1.6G, 1657 GMAC/s Max DSP
- 3x HDMI ports, 2x MIPI CSI-2 Rx/Tx, DSI, HPC FMC

PolarFire Deep Learning Inference

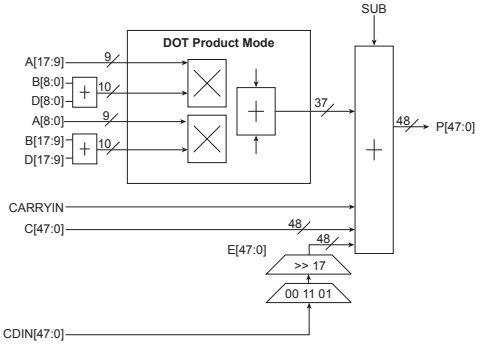
- 35 fps, 3W Tiny Yolov2 demo using PolarFire 300KLE
- Delivering 100 GOPs/W performance
- 25% higher efficiency DSP math blocks vs. competition
- INT8 dot product mode
- 50% lower-power consumption than SRAM FPGA

Smart Embedded Vision Demo

- Dual 1080p60, MIPI CSI2, DDR4 Controller
- RGBBayer, edge detect, down scalar
- Brightness and contrast control
- Display controller to HDMI 1.4

Intuitive Software GUI

- Enables video and audio configurations
- Source selectable picture-in-picture menu
- Alpha blending and overlay
- Image edge detection and enhancements color balance, brightness and contrast



Design Resources

- Complete library of video and imaging IP
- Machine learning inference IP
- MIPI CSI2 camera sensor interface design files
- Parallel camera sensor interface design files

Comprehensive IP Suite

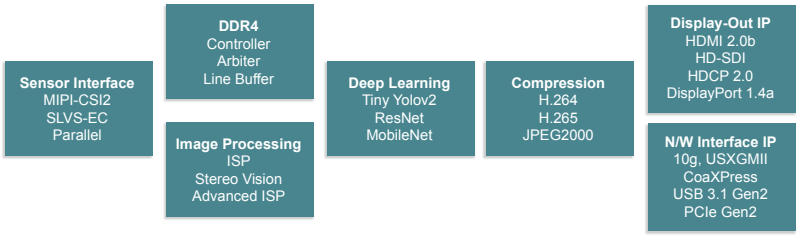
- The IP suite supports PolarFire, SmartFusion2, IGLOO2 and radiationtolerant RTG4 product families.
- Sensor interface—MIPI CSI2, parallel
- Display control (LVDS and parallel RGBHDMI)
- Source code in Verilog and VHDL* (requires licensing fee) Available from our partners: HDMI2.0, HDCP 2.2, Display Port 1.4, SLVS, H.264, JPEG 2000, JPEG and JPEGLS compression and CODEC cores.

*Verilog is only supported on source code for the SmartFusion2/IGLOO2 based solution

Software GUI

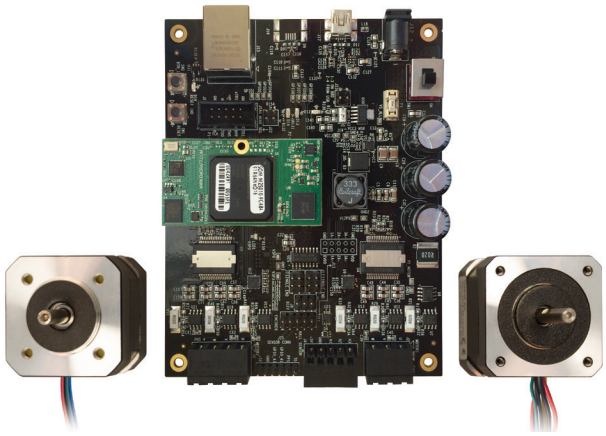
Enables Video and Audio Configurations

- GUI communicates with IP blocks through SmartFusion2 Arm Cortex-M3 processor
- Supports the following demos:
  - Camera sensor to display
  - Image edge detection



Build Safe and Reliable Deterministic Motor Control Applications

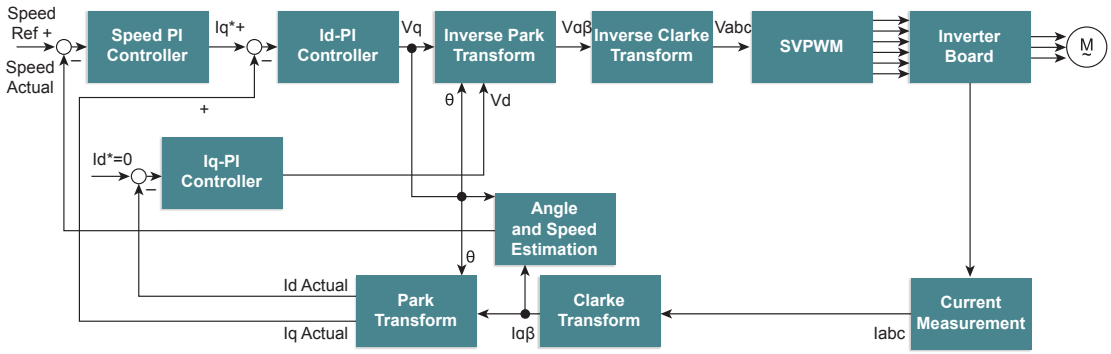
Microchip's Deterministic Motor Control Solution is specially designed to meet the challenging requirements of performance, reliability and safety in an easy-to-use environment. The solution is compliant with industry coding standards for developing safe and reliable software for embedded applications. Microchip offers a modular Intellectual Property (IP) portfolio, tools, reference designs, kits and software to control motors such as Permanent-Magnet Synchronous Motor (PMSM)/brushless DC (BLDC) and stepper motors.



Ordering Code	Supported Device
SF2-MC-STARTER-KIT	M2S010-FG484

Reference Design Features

- Dual-axis deterministic motor control on a single System-on-Chip (SoC) Field Programmable Gate Array (FPGA)
- Efficient, reliable and safe drive/motor control with product longevity
- Compact solution saves board space and reduces product size
- Motor performance is tested for speeds exceeding 100,000 RPM for sensorless Field-Oriented Control (FOC)
- Low latency of 1 µs for FOC loop from ADC measurement to PWM enables switching frequencies up to 500 kHz
- Design flexibility with modular IP suite
- Advanced safety features, such as automatic motor restart and overcurrent protection
- SoC integration of system functions lowers Total Cost Of Ownership (TCO)



Highly Differentiated Features

Secured Production Programming Solution (SPPS) Prevents Overbuilding and Cloning

SPPS enables secured production programing of FPGAs and SoCs by generating and injecting cryptographic keys and configuration bitstreams. This enables prevention of cloning, reverse engineering, malware insertion, leakage of sensitive IP, overbuilding, and other security threats. It is an ideal solution to eliminate the risk of overbuilding customer's systems. It builds upon existing Hardware Security Modules (HSMs), custom firmware and the state-of-the-art security protocols, built into SmartFusion2 SoC FPGA and IGLOO2 FPGA families, to automatically prevent overbuilding.

- Supports multiple programming file formats
- Single- and chain-programming support using SPI and JTAG programming modes
- Auto-update and programming recovery modes
- Interfaces software and hardware security modules
- Allows initial key loading in unstructured environment
- Leverages underlying SmartFusion2 and IGLOO2 security protocols
- Validates devices that can be programmed
- Controls the exact number of devices to be programmed

Microchip enhances your design productivity by providing an extensive suite of proven and optimized IP Cores for use with FPGAs and SoC FPGA that covers key markets and applications. IPs are organized as either Microchip-developed DirectCores™ or third-party-developed CompanionCores™.

DirectCore

Microchip develops and supports DirectCore IP cores for applications with the widest possible interest. Most DirectCores are available for free within our Libero tool suite. Common communications interfaces, peripherals and processing elements are all available as DirectCores.

Functionality	DirectCore Examples
Imaging	MIPI CSI2, ISP, Display Controller
Connectivity	CPRI,16550, 429, PCIF, JESD204B, LiteFast, 1553
DSP	Floating Point, CIC, FFT, FIR, CORDIC, RS
Memory Controller	FIFO, DDR, LPDDR, QDR, SDR, MMC
Processor	Mi-V (RISC V based processor), Arm Cortex-M1, Arm Cortex-M3, 8051, 8051s, ARM7TDMI
Ethernet	10GMAC, TSE, XAUI, QSGMII, RGMII,GMII, SGMII
Security	DES, 3DES, AES, SHA
Error Correction	EDAC, RC

CompanionCore

CompanionCore Partners use their detailed system knowledge of common applications to craft optimized solutions targeted for Microchip SoC FPGAs and FPGAs. CompanionCores are available for purchase from our partners and are easily integrated into your design using our Libero tool suite.

IP Available for Use With Libero

Please contact your local Microchip sales representative for information on price and licensing, as certain Microchip IPs may require a separate license. For more information about DirectCore and CompanionCore, please visit https://www.microsemi.com/product-directory/design-resources/5092-ip-cores.

Support

Microchip is committed to supporting its customers in developing products faster and more efficiently. We maintain a worldwide network of field applications engineers and technical support ready to provide product and system assistance. For more information, please visit www.microsemi.com/FPGA:

- Technical Support: www.microsemi.com/FPGA
- Evaluation samples of any Microchip device: www.microsemi.com/FPGA
- Knowledge base and peer help: www.microchip.com/forums
- Sales and Global Distribution: www.microchip.com/sales

Training

If additional training interests you, Microchip offers several resources including in-depth technical training and reference material, self-paced tutorials and significant online resources.

- Overview of Technical Training Resources: www.microchip.com/training
- MASTERs Conferences: www.microchip.com/masters
- Developer Help Website: www.microchip.com/developerhelp
- Technical Training Centers: www.microchip.com/seminars

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