SHDB62M-DB62M-LL Cable Specifications

2022-06-30

Contents

SHDB62M-DB62M-LL Specifications

These specifications apply to the 1 m and 2 mSHDB62M-DB62M-LL. The SHDB62M-DB62M-LL is a 62 D-sub male to 62 D-sub male low-leakage cable intended for use with PXIe-4162/4163 Source Measure Units.

Caution Do not exceed the operating specifications for the module connected to the SHDB62M-DB62M-LL. Refer to the **Safety, Environmental, and Regulatory Information** for the module for the maximum operating temperature, additional environmental requirements, and safety and EMC guidelines and standards.

Notice Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free from contaminants before returning it to service. Avoid direct handling of connector ends to prevent contaminant buildup on sensitive conductors.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid at an ambient temperature[1] of 23 °C ± 5 °C unless otherwise noted.

Maximum Voltage and Current

Maximum voltage (channel to earth ground)	60 VDC
Maximum current per channel	100 mA

Insulation Resistance[2]

Guarded insulation resistance[3]	3×10^{12} Ω
Non-guarded insulation resistance	1×10^{12} Ω

Physical

Weight	
1 m cable	386 g (13.6 oz)
2 m cable	590 g (20.8 oz)

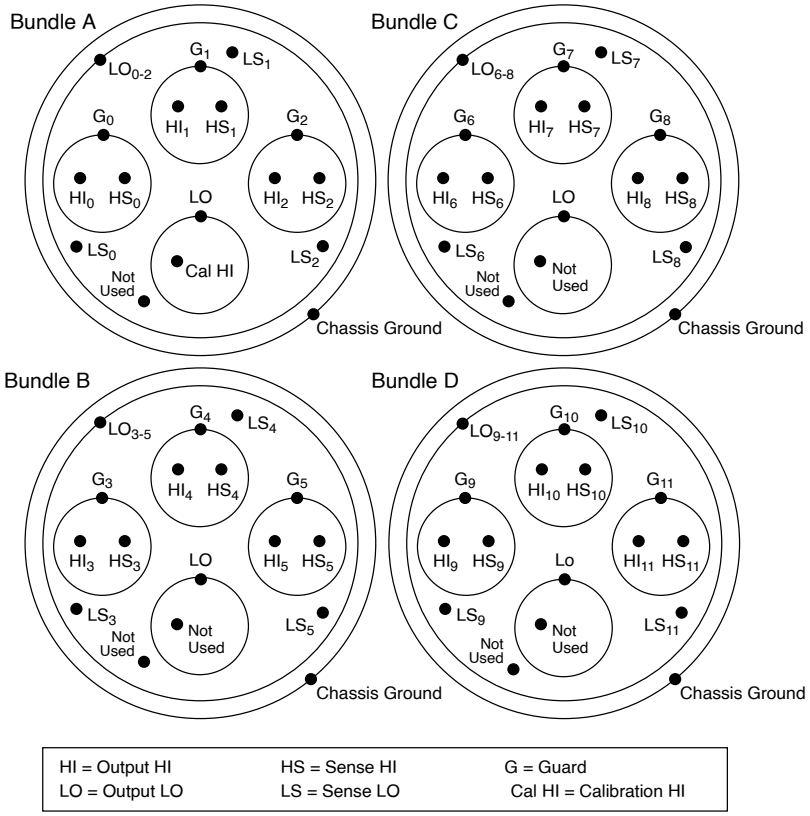
Cable Cross-Section

The outer shield of the SHDB62M-DB62M-LL consists of braided wire that is tied to chassis ground through the shell of the PXIe-4162/4163 front panel connector.

The inner shield, located within the outer shield, provides an additional layer of foil insulation tied to the Output LO pin (pin 10).

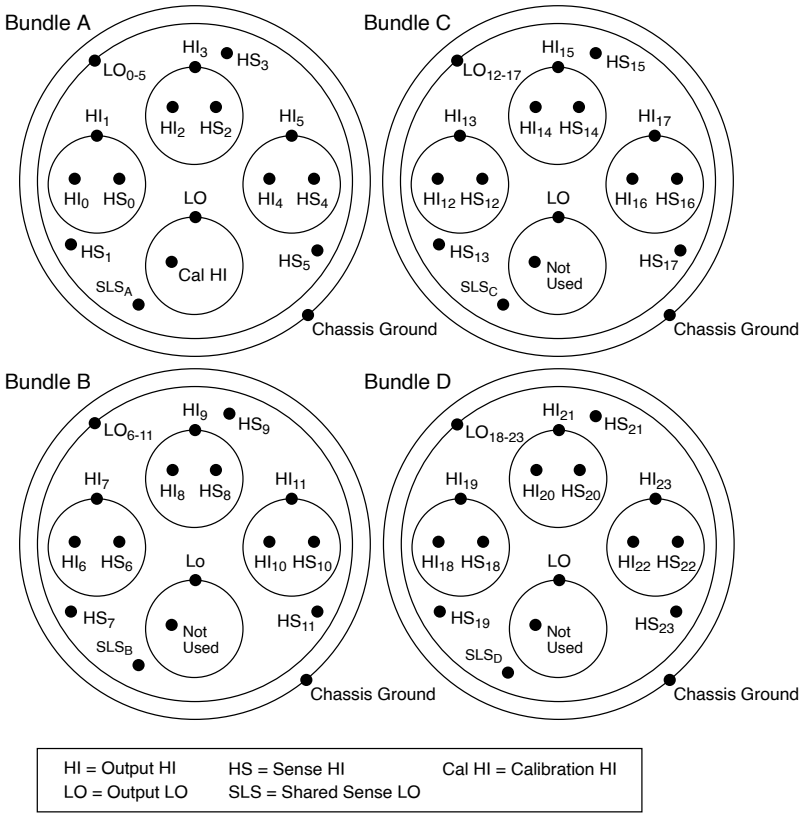
The following diagram shows a cross-section of the SHDB62M-DB62M-LL when used with a PXIe-4162.

Figure 1. Cable Cross-Section with a PXIe-4162



The following diagram shows a cross-section of the SHDB62M-DB62M-LL when used with a PXIe-4163.

Figure 2. Cable Cross-Section with a PXIe-4163



Related reference

- Pinouts for Associated Source Measure Units

Pinouts for Associated Source Measure Units

PXIe-4162/4163 channels are grouped into four separate bundles of cable with an outer shield surrounding each bundle.

PXIe-4162 Pinout

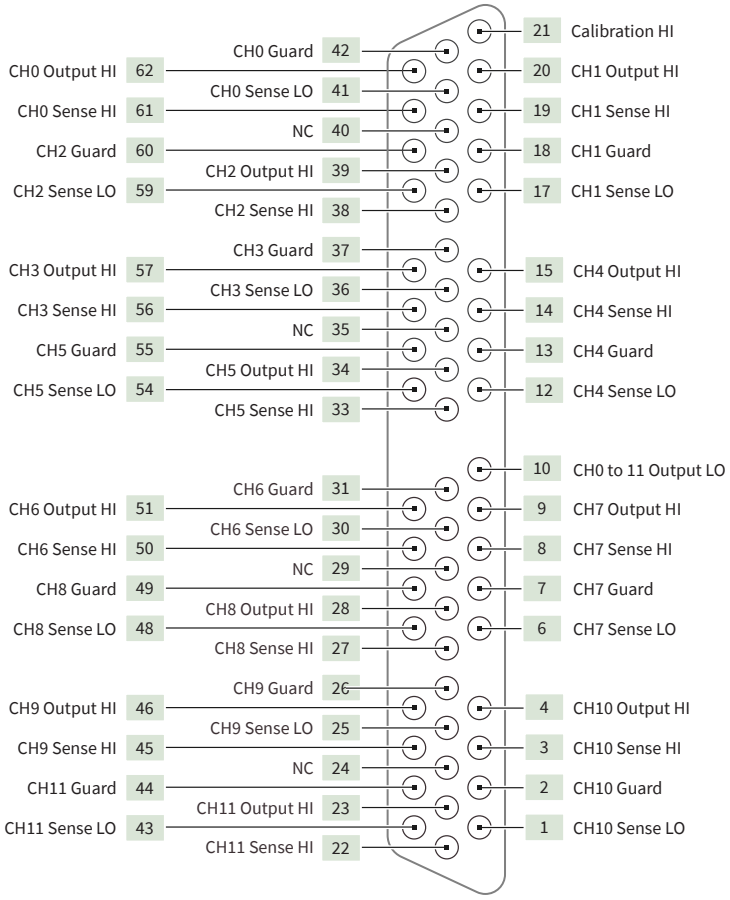


Table 1. PXIe-4162 Signal Descriptions and SHDB62M-DB62M-LL Wires

Bundle	Channel	Pin	Signal Description	Grouping
A	0	41	Sense LO	Unshielded Single Wire 0
		42	Guard[]	Shielded Pair 1
		61	Sense HI	Shielded Pair 0
		62	Output HI	
	1	17	Sense LO	Unshielded Single Wire 1
		18	Guard[]	Shielded Pair 1
		19	Sense HI	
		20	Output HI	
	2	38	Sense HI	Shielded Pair 2
		39	Output HI	
		59	Sense LO	Unshielded Single Wire 2

Bundle	Channel	Pin	Signal Description	Grouping
		60	Guard[]	Shielded Pair 2
	—	21	Calibration HI	Shielded Single Wire 0
		40	Not used	Unshielded Single Wire 3
B	3	36	Sense LO	Unshielded Single Wire 0
		37	Guard[]	Shielded Pair 0
		56	Sense HI	
		57	Output HI	
	4	12	Sense LO	Unshielded Single Wire 0
		13	Guard[]	Shielded Pair 1
		14	Sense HI	
		15	Output HI	
	5	33	Sense HI	Shielded Pair 2
		34	Output HI	
		54	Sense LO	Unshielded Single Wire 2
		55	Guard[]	Shielded Pair 2
	—	35	Not used	Unshielded Single Wire 3
C	6	30	Sense LO	Unshielded Single Wire 0
		31	Guard[]	Shielded Pair 0
		50	Sense HI	
		51	Output HI	
	7	6	Sense LO	Unshielded Single Wire 1
		7	Guard[]	Shielded Pair 1
		8	Sense HI	
		9	Output HI	
	8	27	Sense HI	Shielded Pair 2
		28	Output HI	
		48	Sense LO	Unshielded Single Wire 2
		49	Guard[]	Shielded Pair 2
	—	29	Not used	Unshielded Single Wire 3
D	9	25	Sense LO	Unshielded Single Wire 0

Bundle	Channel	Pin	Signal Description	Grouping
		26	Guard[]	Shielded Pair 0
		45	Sense HI	
		46	Output HI	
	10	1	Sense LO	Unshielded Single Wire 1
		2	Guard[]	Shielded Pair 1
		3	Sense HI	
		4	Output HI	
	11	22	Sense HI	Shielded Pair 2
		23	Output HI	
		43	Sense LO	Unshielded Single Wire 2
		44	Guard[]	Shielded Pair 2
	—	24	Not used	Unshielded Single Wire 3
A, B, C, D	0 to 11	10	Output LO	Shielded Single Wire 0, Inner Shield
—	—	5	Void	—
		11		
		16		
		32		
		47		
		52		
		53		
		58		

PXIe-4163 Pinout

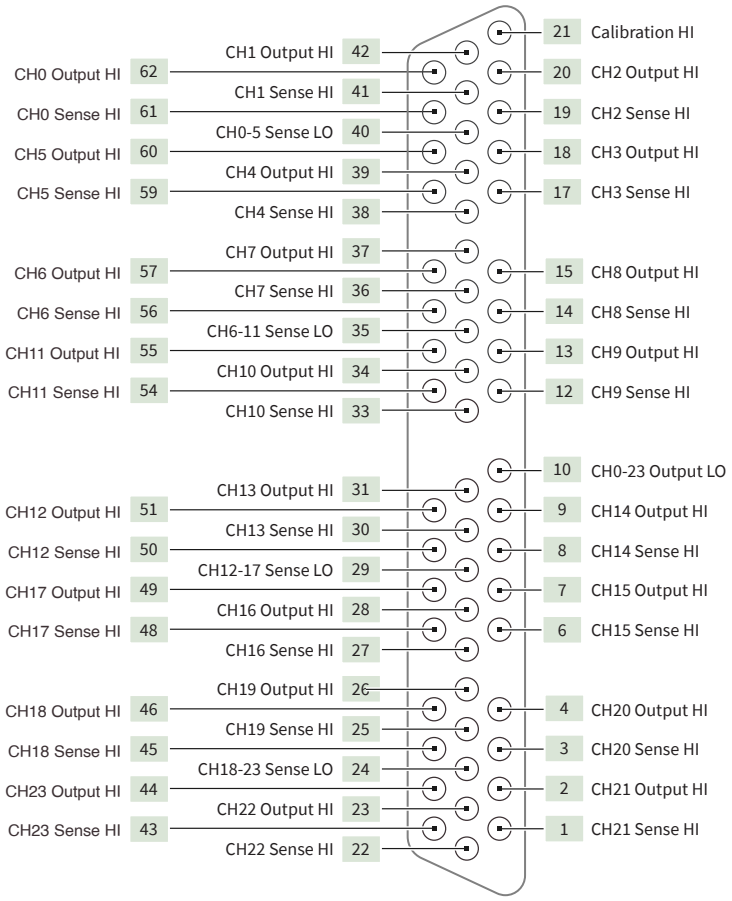


Table 2. PXIe-4163 Signal Descriptions and SHDB62M-DB62M-LL Wires

Bundle	Channel	Pin	Signal Description	Grouping
A	0	61	Sense HI	Shielded Pair 0
		62	Output HI	
	1	41	Sense HI	Unshielded Single Wire 0
		42	Output HI	Shielded Pair 0
	2	19	Sense HI	Shielded Pair 1
		20	Output HI	
	3	17	Sense HI	Unshielded Single Wire 1
		18	Output HI	Shielded Pair 1
	4	38	Sense HI	Shielded Pair 2
		39	Output HI	
	5	59	Sense HI	Unshielded Single Wire 2

Bundle	Channel	Pin	Signal Description	Grouping
		60	Output HI	Shielded Pair 2
	0 to 5	40	Sense LO	Unshielded Single Wire 3
	—	21	Calibration HI	Shielded Single Wire 0
B	6	56	Sense HI	Shielded Pair 0
		57	Output HI	
	7	36	Sense HI	Unshielded Single Wire 0
		37	Output HI	Shielded Pair 0
	8	14	Sense HI	Shielded Pair 1
		15	Output HI	
	9	12	Sense HI	Unshielded Single Wire 1
		13	Output HI	Shielded Pair 1
	10	33	Sense HI	Shielded Pair 2
		34	Output HI	
	11	54	Sense HI	Unshielded Single Wire 2
		55	Output HI	Shielded Pair 2
	6 to 11	35	Sense LO	Unshielded Single Wire 3
C	12	50	Sense HI	Shielded Pair 0
		51	Output HI	
	13	30	Sense HI	Unshielded Single Wire 0
		31	Output HI	Shielded Pair 1
	14	8	Sense HI	
		9	Output HI	
	15	6	Sense HI	Unshielded Single Wire 1
		7	Output HI	Shielded Pair 1
	16	27	Sense HI	Shielded Pair 2
		28	Output HI	
	17	48	Sense HI	Unshielded Single Wire 2
		49	Output HI	Shielded Pair 2
	12 to 17	29	Sense LO	Unshielded Single Wire 3
D	18	45	Sense HI	Shielded Pair 0
		46	Output HI	

Bundle	Channel	Pin	Signal Description	Grouping
	19	25	Sense HI	Unshielded Single Wire 0
		26	Output HI	Shielded Pair 0
	20	3	Sense HI	Shielded Pair 1
		4	Output HI	
	21	1	Sense HI	Unshielded Single Wire 1
		2	Output HI	Shielded Pair 1
	22	22	Sense HI	Shielded Pair 2
		23	Output HI	
	23	43	Sense HI	Unshielded Single Wire 2
		44	Output HI	Shielded Pair 2
	18 to 23	24	Sense LO	Unshielded Single Wire 3
A, B, C, D	0 to 23	10	Output LO	Shielded Single Wire 0, Inner Shield
—	—	5	Void	—
		11		
		16		
		32		
		47		
		52		
		53		
		58		

[1] The ambient temperature of a PXI system is defined as the temperature at the chassis fan inlet (air intake).

[2] Applies up to 30 °C and 60% relative humidity. Guarded and non-guarded insulation resistance decrease to 6×10^{10} Ω at 55 °C and 70% relative humidity.

[3] Guarded insulation resistance only applies with the use of a PXIe-4162, which supports guarding.

[4] Guard terminals are not supported in the highest current ranges: 60 mA or 100 mA.