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# PXle-5170

# Specifications

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2022-07-06



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# PXIe-5170 Specifications

## Definitions

**Warranted** specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. **Warranted** specifications account for measurement uncertainties, temperature drift, and aging. **Warranted** specifications are ensured by design, or verified during production and calibration.

**Characteristics** describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured (meas)** specifications describe the measured performance of a representative model.

Specifications are **Nominal** unless otherwise noted.

## Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges
- Sample rate set to 250 MS/s
- Onboard sample clock locked to onboard reference clock
- PXIe-5170 module warmed up for 15 minutes at ambient temperature.<sup>[1]</sup>
- PXI Express chassis fan speed set to HIGH, foam fan filters removed if present, and empty slots contain PXI chassis slot blockers and filler panels. For more information about cooling, refer to the **Maintain Forced-Air Cooling Note to Users** available at [ni.com/manuals](http://ni.com/manuals).

- Calibration IP used properly when using LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes (instrument design libraries) to create FPGA bitfiles. Refer to the **NI Reconfigurable Oscilloscopes Help** for more information about the calibration API.

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 45 °C
- External calibration cycle maintained
- External calibration performed at 23 °C ± 3 °C

Typical specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature ranges of 0 °C to 45 °C

Nominal and Measured specifications are valid under the following conditions unless otherwise noted.

- Room temperature, approximately 23 °C

## Vertical

### Analog Input

<b>Number of channels</b>	
PXIe-5170 (4 CH)	Four (simultaneously sampled)
PXIe-5170 (8 CH)	Eight (simultaneously sampled)
Input type	Referenced single-ended
Connectors	SMA

## Impedance and Coupling

Input impedance	50 $\Omega$ $\pm$ 1.5%, typical
Input coupling	AC, DC

Figure 1. Voltage Standing Wave Ratio (VSWR)

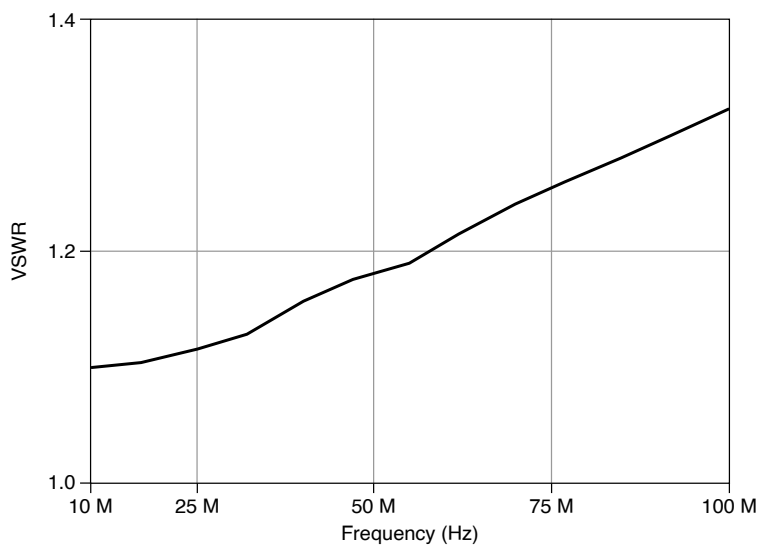
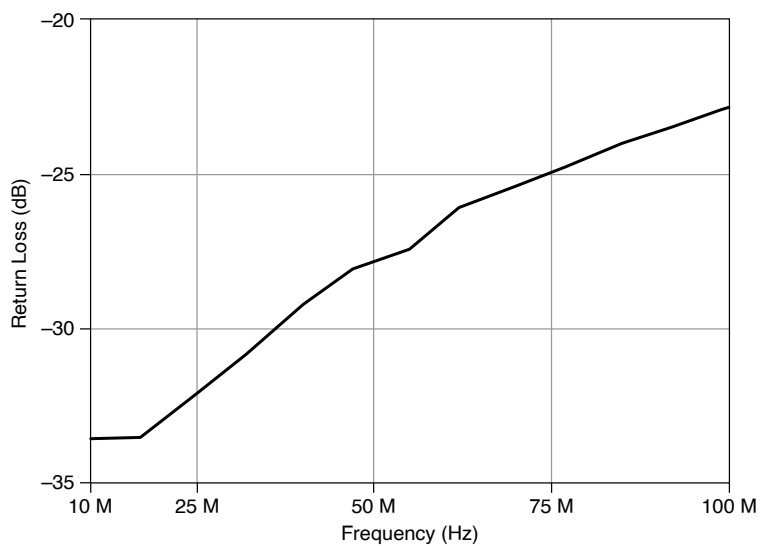


Figure 2. Input Return Loss



## Voltage Levels

Full-scale (FS) input range ( $V_{pk-pk}$ )	0.2 V
	0.4 V
	1 V
	2 V
	5 V
Maximum input overload <sup>[2]</sup>	Peaks  ≤ 5 V

## Accuracy



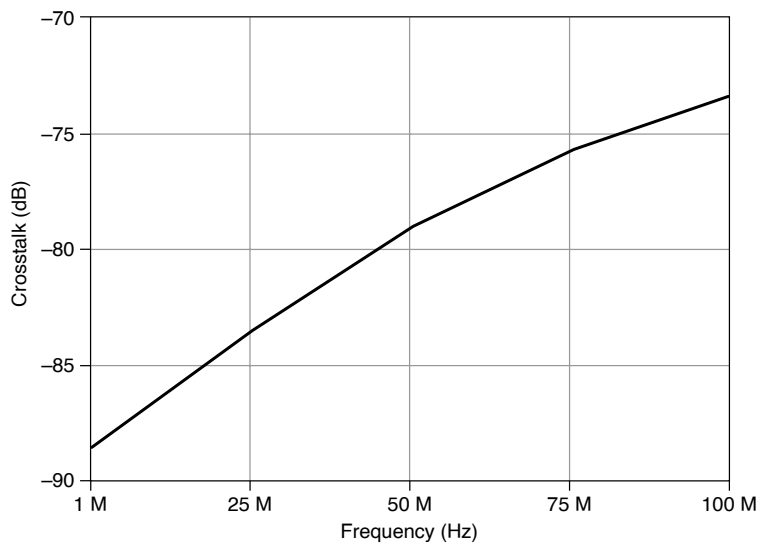
**Notice** Electromagnetic interference can adversely affect the measurement accuracy of this product. The coaxial channel inputs of this device (CH 0 to CH 7) are not protected for electromagnetic interference. As a result, this device may experience reduced measurement accuracy or other temporary performance degradation when connected cables are routed in an environment with radiated or conducted radio frequency electromagnetic interference. To limit radiated emissions and to ensure that this device functions within specifications in its operational electromagnetic environment, take precautions when designing, selecting, and installing measurement probes and cables.

Resolution	14 bits
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Input Range	Accuracy		Drift
	Typical <sup>[4]</sup>	Warranted <sup>[5]</sup>	Nominal <sup>[6]</sup>
$V_{pk-pk}$	$\pm(\% \text{ of }  \text{Reading}  + \% \text{ of FS} + \text{mV})$	$\pm(\% \text{ of }  \text{Reading}  + \% \text{ of FS} + \text{mV})$	$\pm(\% \text{ of }  \text{Reading}  + \% \text{ of FS} + \text{mV}) \text{ per } ^\circ\text{C}$
0.2 V	$\pm(0.45 + 0.6 + 0.2)$	$\pm(0.90 + 0.65 + 0.7)$	$\pm(0.015 + 0.002 + 0.004)$
0.4 V	$\pm(0.45 + 0.24 + 0.2)$	$\pm(0.80 + 0.25 + 0.7)$	$\pm(0.012 + 0.002 + 0.004)$
1 V	$\pm(0.45 + 0.2 + 0.2)$	$\pm(0.80 + 0.25 + 0.7)$	$\pm(0.010 + 0.002 + 0.004)$
2 V	$\pm(0.40 + 0.2 + 0.2)$	$\pm(0.60 + 0.25 + 0.7)$	$\pm(0.005 + 0.002 + 0.004)$
5 V	$\pm(0.40 + 0.2 + 0.2)$	$\pm(0.55 + 0.25 + 0.7)$	$\pm(0.005 + 0.002 + 0.004)$

Table 1. DC Accuracy<sup>[3]</sup>

DC accuracy sampling drift, full bandwidth ( $\pm\%$ of  Reading  per MHz from 250 MHz) <sup>[7]</sup>	$\pm 0.03$ , nominal
<b>AC amplitude accuracy<sup>[3]</sup></b>	
Accuracy	$\pm 0.095$ dB at 50 kHz, typical <sup>[4]</sup>
	$\pm 0.15$ dB at 50 kHz, warranted <sup>[5]</sup>
Drift <sup>[6]</sup>	$\pm 0.0013$ dB per $^\circ\text{C}$
<b>Conversion error rate<sup>[8]</sup></b>	
250 MS/sec	$< 1 \times 10^{-10}$
200 MS/sec	$< 1 \times 10^{-15}$
150 MS/sec	$< 1 \times 10^{-20}$

Figure 3. Channel-to-Channel Crosstalk<sup>[9]</sup>

## Bandwidth and Transient Response

Bandwidth (-3 dB) <sup>[10]</sup>	100 MHz, warranted
<b>Input Frequency</b>	<b>Full Bandwidth</b>
<50 MHz	-0.5 dB to 0.5 dB
50 MHz to 90 MHz	-1.0 dB to 0.5 dB

Table 2. Passband Amplitude Flatness, Warranted<sup>[10]</sup>

AC-coupling cutoff (-3 dB) <sup>[11]</sup>	120 kHz
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Figure 5. Frequency Response, Full Bandwidth, Measured

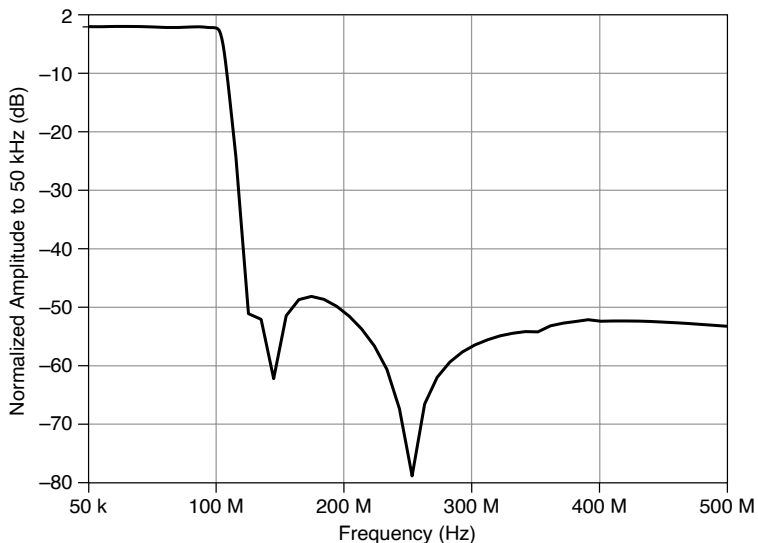
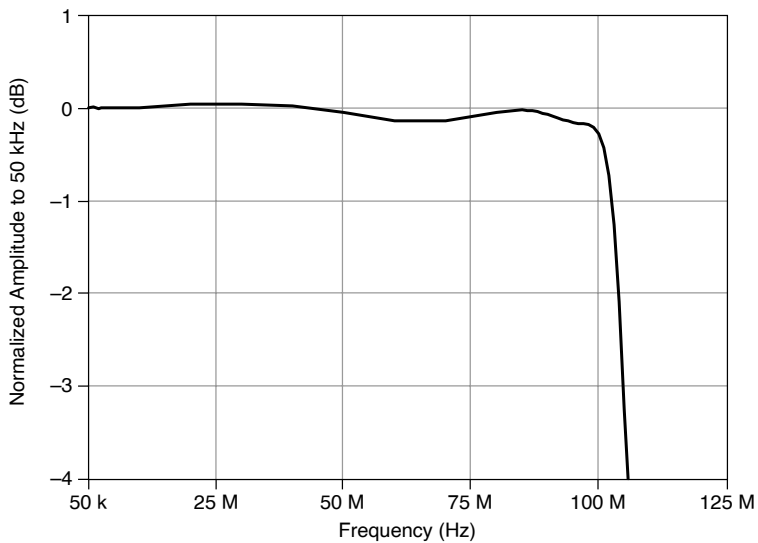


Figure 5. Frequency Response (Zoomed), Full Bandwidth, Measured



## Spectral Characteristics

Input Range ( $V_{pk-pk}$ )	Input Frequency	Full Bandwidth
0.2 V to 2 V	<10 MHz	-80.0 dBc
	$\geq 10$ MHz to <30 MHz	-76.0 dBc
5 V	<10 MHz	-77.0 dBc

Input Range ( $V_{pk-pk}$ )	Input Frequency	Full Bandwidth
	$\geq 10$ MHz to $< 30$ MHz	-73.0 dBc

Table 3. Spurious-Free Dynamic Range (SFDR)<sup>[12]</sup>

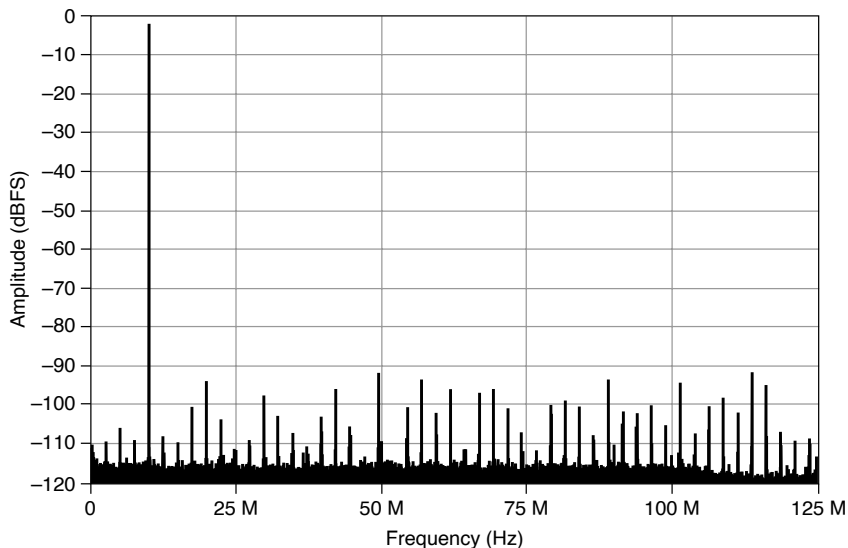
Input Frequency	Full Bandwidth
$< 10$ MHz	-77.0
$\geq 10$ MHz to $< 30$ MHz	-73.0

Table 4. Total Harmonic Distortion (THD)<sup>[13]</sup>

Input Range ( $V_{pk-pk}$ )	Input Frequency	Full Bandwidth
0.2 V	$< 30$ MHz	10.8
All other input ranges	$< 30$ MHz	11.0

Table 5. Effective Number of Bits (ENOB)<sup>[12]</sup>

Figure 6. Single-Tone Spectrum, 2.98 dBm Input Signal at Connector, 1  $V_{pk-pk}$  Input Range, 9.9 MHz Input Tone, Full Bandwidth, Measured



## Noise

RMS noise <sup>[14]</sup>	0.017% of FS, typical
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Input Range ( $V_{pk-pk}$ )	Full Bandwidth (dBm/Hz)
0.2 V	-159.2 dBm/Hz
0.4 V	-153.7 dBm/Hz
1 V	-145.7 dBm/Hz
2 V	-139.7 dBm/Hz
5 V	-131.7 dBm/Hz

Table 6. Average Noise Density (dBm/Hz), Typical<sup>[14]</sup>

Input Range ( $V_{pk-pk}$ )	Full Bandwidth
0.2 V	149.2 dBFS/Hz
All other input ranges	149.7 dBFS/Hz

Table 7. Average Noise Density (dBFS/Hz), Typical<sup>[14]</sup>

Input Range ( $V_{pk-pk}$ )	Full Bandwidth (nV/ $\sqrt{\text{Hz}}$ )
0.2 V	3.5 nV/ $\sqrt{\text{Hz}}$
0.4 V	6.5 nV/ $\sqrt{\text{Hz}}$
1 V	16.4 nV/ $\sqrt{\text{Hz}}$
2 V	32.7 nV/ $\sqrt{\text{Hz}}$
5 V	81.8 nV/ $\sqrt{\text{Hz}}$

Table 8. Average Noise Density (nV/ $\sqrt{\text{Hz}}$ ), Typical<sup>[14]</sup>

## Horizontal

## Sample Clock

### Sources

Internal	Onboard clock (internal VCXO)
External	AUX I/O CLK IN (front panel MHDMMR connector)
	PXIe_DStarA (backplane connector)

Sample rate range, real-time <sup>[15]</sup>	3.815 kS/s to 250 MS/s
<b>Timebase frequency</b>	
Internal	250 MHz
External	150 MHz – 250 MHz <sup>[16]</sup>
<b>Timebase accuracy</b>	
Phase-locked to onboard clock	±25.0 ppm, warranted
Phase-locked to external clock	Equal to the external clock accuracy
Duty cycle tolerance	45% to 55%

## Phase-Locked Loop (PLL) Reference Clock

<b>Sources</b>	
Internal	Onboard clock (internal VCXO) PXI_Clk10 (backplane connector)
External (10 MHz)	AUX I/O CLK IN (front panel MHDMM connector)
Duty cycle tolerance	45% to 55%

## External Sample Clock

Source	AUX I/O CLK IN (front panel MHDMM connector)
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Impedance	50 $\Omega$	
Coupling	AC	
<b>Input voltage range</b>		
As a 250 MHz sine wave	1 dBm through 18 dBm	
As a fast slew rate input (square wave, $V_{pk-pk}$ )	0.4 V to 5 V	
<b>Maximum input overload</b>		
As a 250 MHz sine wave	20 dBm	
As a fast slew rate input (square wave, $V_{pk-pk}$ )	6 V	

## External Reference Clock In

Source	AUX I/O CLK IN (front panel MHDMM connector)	
Impedance	50 $\Omega$	
Coupling	AC	
Frequency <sup>[17]</sup>	10 MHz	
<b>Input voltage range</b>		
As a 250 MHz sine wave	1 dBm through 18 dBm	
As a fast slew rate input (square wave, $V_{pk-pk}$ )	6 V	

Duty cycle tolerance	45% to 55%
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## Reference Clock Out

Source	PXI_Clk10 (backplane connector)
Destination	AUX I/O CLK OUT (front panel MHDMM connector)
Output impedance	50 $\Omega$
Logic type	3.3 V LVCMOS
Maximum current drive	$\pm 8$ mA

## PXIe\_DStarA

Source	System timing slot
Destinations	Onboard clock (internal VCXO) FPGA

## PXI\_Clk100

Source	PXI backplane
Destination	FPGA

## Trigger



**Note** The following characteristic behaviors are valid when using the device with the NI-SCOPE API. When using instrument design libraries, these characteristics may not be valid.

Supported trigger	Reference (Stop) Trigger
Trigger types	Edge Window Hysteresis Digital Immediate Software
Trigger sources	PXIe-5170 (8CH): CH 0 to CH 7 PXIe-5170 (4CH): CH 0 to CH 3 PFI <0..7> PXI_Trig <0..6> Software

### Time resolution

#### Analog triggers<sup>[18]</sup>

With interpolation

Sample Clock period / 1024

Without interpolation	Sample Clock period
Digital triggers	2x Sample Clock period
<b>Minimum dead time<sup>[18]</sup></b>	
With interpolation	240 x Sample Clock period
Without interpolation	130 x Sample Clock period
Holdoff	From dead time to $[(2^{64} - 1) \times \text{Sample Clock timebase period}]$
Trigger delay	From 0 to $[(2^{51} - 1) \times \text{Sample Clock timebase period}]$
Trigger accuracy <sup>[19]</sup>	0.5% of full scale
Trigger jitter <sup>[19]</sup>	15 pS <sub>rms</sub>
Minimum threshold duration <sup>[20]</sup>	Sample Clock period

## Programmable Function Interface (PFI 0..7, AUX I/O Front Panel Connector)

Connector	AUX I/O
Direction	Bidirectional per channel
Direction control latency	25 ns
<b>As an Input (Trigger)</b>	



Destination	FPGA diagram
	Start Trigger (Acquisition Arm)
	Reference (Stop) Trigger
	Arm Reference Trigger
	Advance Trigger
Input impedance	10 k $\Omega$
$V_{IH}$	2 V
$V_{IL}$	0.8 V
Maximum input overload	0 V to 3.3 V, 5 V tolerant
Minimum pulse width	10 ns

### As an Output (Event)

Sources	FPGA diagram
	Ready for Start
	Start Trigger (Acquisition Arm)
	Ready for Reference
	Reference (Stop) Trigger
	End of Record
	Ready for Advance

	Advance Trigger
	Done (End of Acquisition)
Output impedance	50 $\Omega$
Logic type	3.3 V CMOS
Maximum current drive	12 mA
Minimum pulse width	10 ns

### Power Output (+3.3 V)

Connector	AUX I/O/+3.3 V front panel connector
Voltage output	3.3 V $\pm$ 10%
Maximum current drive	200 mA
Output impedance	<1 $\Omega$

### Waveform Specifications

<b>Onboard memory size<sup>[21]</sup></b>	
PXIe-5170 (4 CH)	0.75 GB
PXIe-5170 (8 CH)	1.5 GB
Minimum record length	1 sample

Number of pretrigger samples	Zero up to (record length - 1)
Number of posttrigger samples	Zero up to record length

Channels	Max Records per Channel	Record Length
1	1	805306192
1	10	80530432
1	1000	805120
1	100,000	7840
1	1M	592
2	1	402653096
2	10	40265216
2	1000	402560
2	100,000	3920
2	1M	296
4	1	201326548
4	10	20132608
4	1000	201280
4	100,000	1960
4	1M	148
8	1	100663274
8	10	10066304
8	1000	100640
8	100,000	980
8	1M	74

## Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at [ni.com/manuals](http://ni.com/manuals).

## FPGA

FPGA support	Xilinx Kintex-7 XC7K325T FPGA
<b>Xilinx Kintex-7 XC7K325T FPGA Resources</b>	
Slice registers	407,600
Slice look-up tables (LUT)	203,800
DSPs	840
18 Kb block RAMs	890



**Note** Note that some of these resources are consumed by the logic necessary to operate the device and integrate with software, and are thus out of the control of users.

## Calibration

### External Calibration

External calibration corrects for gain, offset, and timing errors at all input ranges.

All calibration constants are stored in nonvolatile memory.

### Self-Calibration

Self-calibration is done on software command. The calibration corrects for intermodule synchronization errors.

## Calibration Specifications

Interval for external calibration	2 years
Warm-up time <sup>[22]</sup>	15 minutes

## Software

### Driver Software

This device was first supported in LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes 14.0 and NI-SCOPE 15.1. NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the device. NI-SCOPE provides application programming interfaces for many development environments.

### Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

### Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PXIe-5170 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.



**Note** InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE-specific soft front panel instead of InstrumentStudio.

Interactive control of the PXIe-5170 was first available via InstrumentStudio in NI-SCOPE 18.1 and via the NI-SCOPE SFP in NI-SCOPE 15.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5170. MAX is included on the driver media.

## Synchronization

Channel-to-channel skew, between the channels of a PXIe-5170	<120 ps <sup>[23]</sup>
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## Synchronization with the NI-TClk API<sup>[24]</sup>

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5170 and NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

### Module-to-module skew, between PXIe-5170 modules using NI-TClk<sup>[25]</sup>

#### NI-TClk synchronization without manual adjustment<sup>[26]</sup>

Skew, Peak-to-Peak<sup>[27]</sup> 300 ps

#### NI-TClk synchronization with manual adjustment<sup>[26]</sup>

Skew after manual adjustment	≤10 ps
Sample Clock delay/adjustment resolution	3.5 ps

## Power

	Instrument Design Libraries <sup>[28]</sup>	NI-SCOPE <sup>[28]</sup>
+3.3 VDC	6.0 W	5.9 W
+12 VDC	14.5 W	13.4 W
Total power	20.5 W	19.3 W

Table 9. PXIe-5170 (4CH) Power Consumption

	Instrument Design Libraries <sup>[28]</sup>	NI-SCOPE <sup>[28]</sup>
+3.3 VDC	6.4 W	6.3 W
+12 VDC	17.0W	17.2W
Total power	23.4 W	23.5 W

Table 10. PXIe-5170 (8CH) Power Consumption, Typical

Total maximum power allowed	38.25 W <sup>[29]</sup>
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## Dimensions and Weight

Dimensions	18.5 cm × 2.0 cm × 13.0 cm (7.3 in. × 0.8 in. × 5.1 in.)  3U, 1 slot, PXI Express Gen 2 x8 Module
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## Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
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Pollution Degree	2
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Indoor use only.

## Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 4 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

## Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

## Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
<p><b>Random vibration</b></p> <p>Operating 5 Hz to 500 Hz, 0.3 g<sub>rms</sub> (Tested in accordance with IEC 60068-2-64.)</p> <p>Nonoperating 5 Hz to 500 Hz, 2.4 g<sub>rms</sub> (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)</p>	



## Compliance and Certifications

### Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1



**Note** For UL and other safety certifications, refer to the product label or the [Product Certifications and Declarations](#) section.

### Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-2-1 (IEC 61326-2-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



**Note** In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.



**Note** Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



**Note** For EMC declarations, certifications, and additional information, refer to the [Product Certifications and Declarations](#) section.

## CE Compliance

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

## Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit [ni.com/product-certifications](http://ni.com/product-certifications), search by model number, and click the appropriate link.

## Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Commitment to the Environment** web page at [ni.com/environment](http://ni.com/environment). This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

## Waste Electrical and Electronic Equipment (WEEE)

**EU Customers** At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit [ni.com/environment/weee](http://ni.com/environment/weee).

## 电子信息产品污染控制管理办法 ( 中国 RoHS )

**中国客户** National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 [ni.com/environment/rohs\\_china](http://ni.com/environment/rohs_china)。(For information about China RoHS compliance, go to [ni.com/environment/rohs\\_china](http://ni.com/environment/rohs_china).)

<sup>1</sup> Warm-up begins after the chassis is powered, the device is recognized by the host, and the ADC clock is configured using either instrument design libraries or the NI-SCOPE device driver.

<sup>2</sup> Signals exceeding the maximum input overload may cause damage to the device.

<sup>3</sup> Verification of these specifications requires the **DC Adjustment Device Temperature (°C)** value. If you are using version 14.0 of the software, visit [ni.com/info](http://ni.com/info) and enter the Info Code exxpmp for information on how to read this value. Otherwise, use NI-SCOPE to read the value.

<sup>4</sup> When the reading from the **Device Temperature** sensor is within  $\pm 10$  °C of the **DC Adjustment Device Temperature (°C)** value.

<sup>5</sup> When the reading from the **Device Temperature** sensor is within  $\pm 38$  °C of the **DC Adjustment Device Temperature (°C)** value. This increased temperature span encompasses the majority of temperature differences between the last external calibration environment and the operating environment.

<sup>6</sup> Used to calculate additional temperature error when the difference between the **Device Temperature** sensor and the **DC Adjustment Device Temperature (°C)**

value is greater than  $\pm 10$  °C (for typical specifications) or  $\pm 38$  °C (for warranted specifications).

<sup>7</sup> Used to calculate additional DC accuracy error when using an external sample clock of frequency <250 MHz. To calculate the additional error, solve the following for the analog path of interest:  $\frac{250\text{MHz} - \text{frequency}}{1,000,000} \times \text{DC accuracy sampling drift}$

<sup>8</sup> A **conversion error** is defined as deviation greater than 0.6% of full scale.

<sup>9</sup> Measured on one channel with test signal applied to another channel, with the same range setting on both channels.

<sup>10</sup> Normalized to 50 kHz.

<sup>11</sup> With AC coupling enabled, the input impedance is 260 k $\Omega$  to ground. Verified using a 50  $\Omega$  source.

<sup>12</sup> -1 dBFS input signal corrected to FS. 358 Hz resolution bandwidth (RBW).

<sup>13</sup> Includes the second through the fifth harmonics. -1 dBFS input signal.

<sup>14</sup> Verified using a 50  $\Omega$  terminator connected to input.

<sup>15</sup> Divide by **n** decimation from 250 MS/s. For more information about the sample clock and decimation, refer to the **NI Reconfigurable Oscilloscopes Help** at [ni.com/manuals](http://ni.com/manuals).

<sup>16</sup> Variable external sample clock support was added in NI-SCOPE 18.7.

<sup>17</sup> The PLL reference clock frequency must be accurate to  $\pm 25$  ppm.

<sup>18</sup> Trigger interpolation is used when the Enable TDC NI-SCOPE attribute is set to TRUE. Otherwise, trigger interpolation is not used.

<sup>19</sup> Analog triggers. For input frequencies less than 90 MHz.

<sup>20</sup> Data must exceed each corresponding trigger threshold for at least the minimum duration to ensure analog triggering.

21 Onboard memory is shared among all enabled channels.

22 Warm-up begins after the chassis is powered, the device is recognized by the host, and the device is configured using the instrument design libraries or NI-SCOPE. Running an included sample project or running self-calibration using NI-MAX will configure the device and start warm-up.

23 For input frequencies less than 75 MHz.

24 NI-TClk installs with NI-SCOPE.

25 Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules. Specifications are valid under the following conditions:

- All modules installed in the same PXI Express chassis.
- NI-TClk used to align the sample clocks of each module.
- All parameters set to identical values for each module.
- Self-calibration completed.
- Ambient temperature within  $\pm 1$  °C of self-calibration.

For other configurations, including multi-chassis systems, contact NI Technical Support at [ni.com/support](https://ni.com/support).

26 Manual adjustment is the process of minimizing synchronization jitter and skew by adjusting Trigger Clock (TClk) signals using the instrument driver.

27 Caused by clock and analog delay differences. Tested with a PXIe-1082 chassis with maximum slot to slot skew of 100 ps. Valid within  $\pm 1$  °C of self-calibration.

28 Power consumed depends on the FPGA image and driver software used. This specifications represents the maximum power for the NI-SCOPE use case or the typical value when using the Instrument Design Libraries (IDL).

29 Maximum allowable power when using a custom LabVIEW FPGA image.