PXIe-5641 Specifications

2022-07-01

Contents

NI 5641R Specifications

This document lists the specifications for the NI PXIe-5641R reconfigurable IF transceiver. Specifications are warranted by design and under the following conditions unless otherwise noted:

- 10 minutes warm-up time
- Calibration adjustment cycle maintained
- Chassis fan speed set to High

Specifications indicated as maximum or minimum values describe the warranted traceable product performance over ambient temperature ranges of 0 °C to 55 °C, unless otherwise noted.

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 25 ± 10 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under **Specifications** or **Typical** values. **Nominal** values are not covered by warranty.

Specifications are subject to change without notice. Visit ni.com/manuals for the most current specifications and product documentation.

To access NI 5641R documentation, navigate to Start≫All Programs≫National Instruments≫NI-5640R≫Documentation .

Caution Do not operate the NI PXIe-5641R in a manner not specified in this document. Product misuse can result in a hazard. You can

compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to NI for repair.

IF Input

Number of channels	2
ADC resolution	14 bits
Sample rate	30 MS/s to 100 MS/s
Full-scale input range	+8.5 dBm peak at 10 MHz ± 1 dB typical (1.7 $V_{peak-peak}$ sine, 0.60 V_{RMS})
Maximum input level without damage	+24 dBm peak (10$V_{peak-peak}$ sine, 3.5 V_{RMS})
Input coupling	AC
Input impedance	50 Ω nominal
Input return loss	<-15 dB typical, 250 kHz to 80 MHz
Maximum DC input voltage without damage	10 V
Average noise density	-143 dBm/Hz typical
Signal-to-noise ratio	>76 dB typical (-1 dBfs at 68 MHz tone, bandwidth = 10 MHz)
Maximum instantaneous bandwidth	20 MHz (limited by digital downconverter)
Passband flatness (referenced to 10 MHz) 250 kHz to 80 MHz	<+0.33 dB, -0.55 dB typical

AC coupling cutoff frequency (-3 dB)	50 kHz typical
Input group delay variation	10 ns peak-to-peak typical, 250 kHz to 80 MHz
Stopband rejection	>50 dB typical at 120 MHz, referenced to 10 MHz
Channel-to-channel crosstalk	
<40 MHz	<-70 dB typical
40 MHz to 80 MHz	<-60 dB typical

IF Input Performance

Figure 1. Measured Input Frequency Response (Passband)

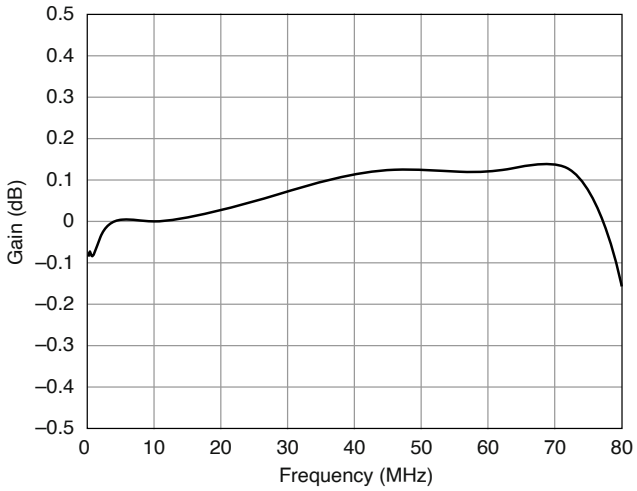


Figure 2. Measured Input Frequency Response (Broadband)

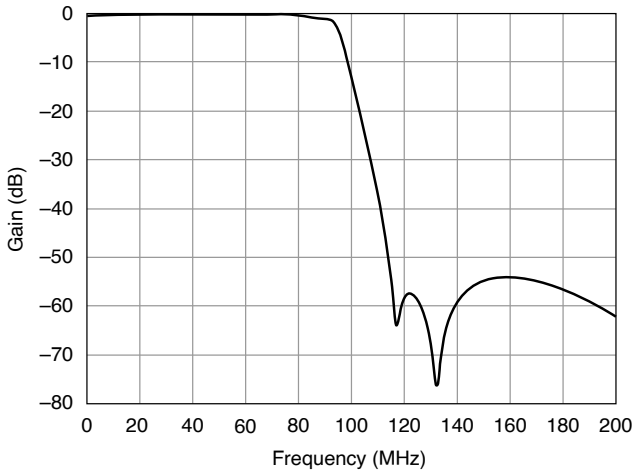


Figure 3. Measured Input Frequency Response (Low Frequency)

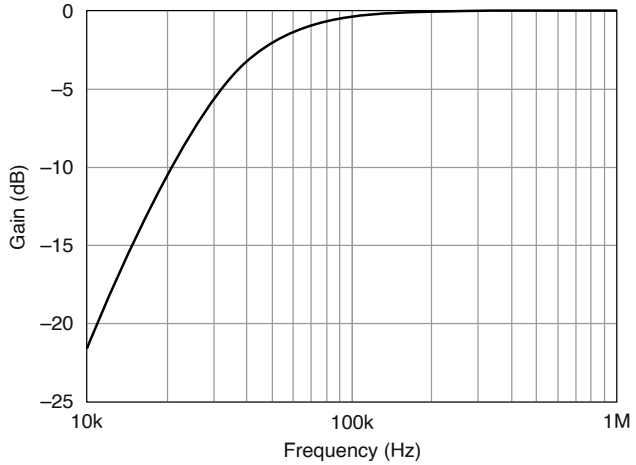
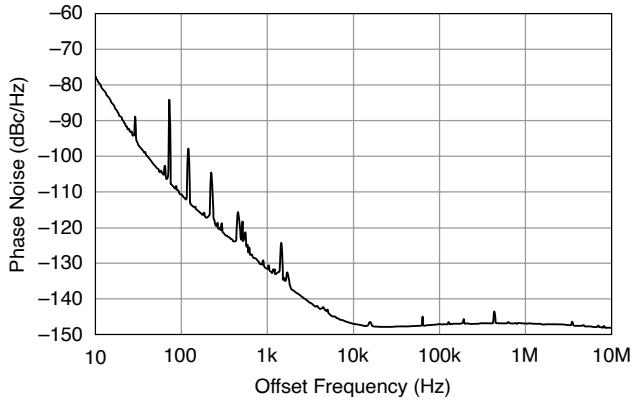


Figure 4. Measured Phase Noise (Carrier Frequency = 62.922 MHz)

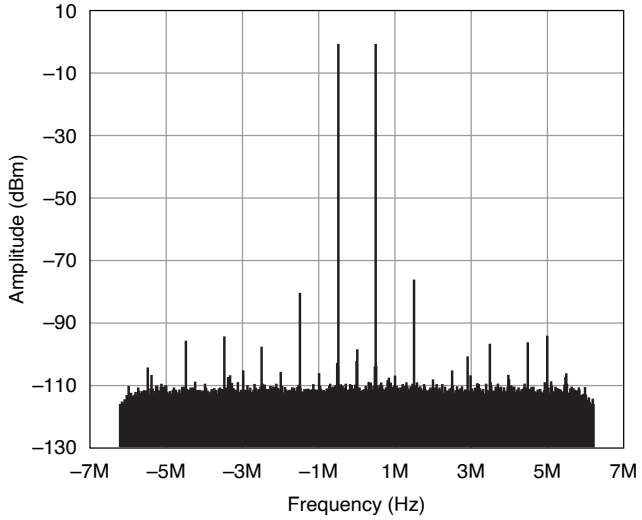


IF Input Spectral Characteristics

Third-order intercept (TOI)	+38 dBm typical

IF Input Spectral Characteristics Performance

Figure 5. Measured Analog Input Two-Tone Intermodulation Distortion (IMD) (Center frequency at 70 MHz, Two Carriers at 70 MHz ± 0.5 MHz, 0 dBm each)



Digital Downconverter Characteristics

Number of channels	Up to 6 per ADC channel
DDC resolution	16 bits for both I and Q data
Decimation[1]	÷4 to ÷4,096
Tuning resolution	ADC clock/2^{32}

Related reference

- Internal Timebase

Digital Downconverter (DDC) Performance

Figure 6. DDC Filter Performance, 20 MHz Span (Solid) and Aliasing After Decimation (Dashed)

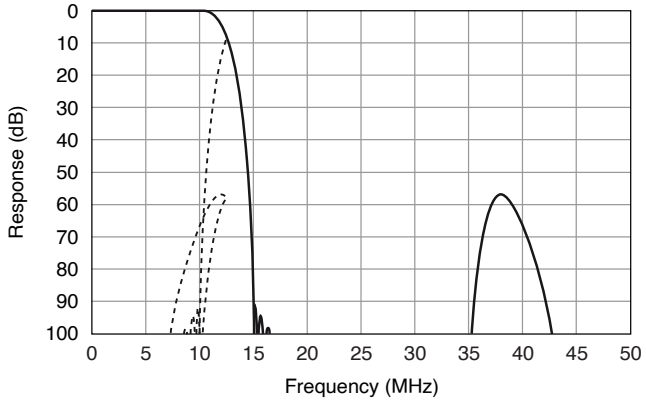
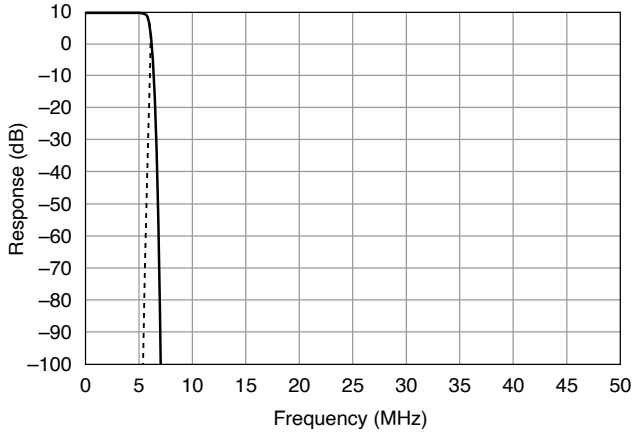


Figure 7. DDC Filter Performance, 10 MHz Span



Sample DDC filter performance plots use NI-5640R 1.3 instrument driver library example filter designs. The dark lines in the above figures show the true response of the digital filter in the DDC. The dashed lines show the effect of aliasing after decimation. Notice that for a 10 MHz span, the DDC filter aliasing artifacts have virtually no impact; whereas for a full 20 MHz span, signals at frequency offsets near ±40 MHz can alias back up to -66 dBc within the ±10 MHz passband near the band edges.

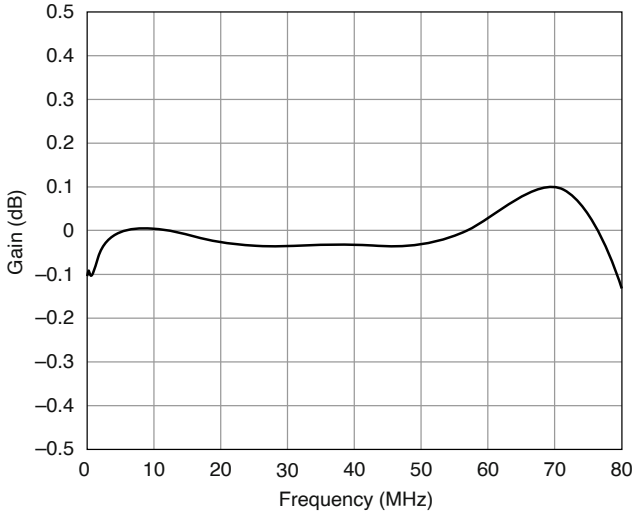
IF Output

Number of channels	2
DAC resolution	14 bits
Sample rate	30 MS/s to 200 MS/s
Output coupling	AC-coupled
Output impedance	50 Ω nominal
Output return loss	<-15 dB typical, 250 kHz to 80 MHz
Maximum DC bias voltage without damage	10 V
Average noise density	-153 dBm/Hz typical
Signal-to-noise ratio +2 dBm output level -4 dBm output level	 >69 dB typical >64 dB typical
Full-scale output range[2] CIC and inverse sync ON Filters off, uncompensated	 -4 dBm peak at 10 MHz ± 1 dB typical (0.4 $V_{peak-peak}$ sine, 0.14 V_{RMS}) +2 dBm peak at 10 MHz ± 1 dB typical (0.8 $V_{peak-peak}$ sine, 0.28 V_{RMS})
Output protection	Indefinite duration short to ground

Maximum reverse power without damage	+24 dBm peak (10 $V_{peak-peak}$, 3.5 V_{RMS})
Passband flatness (referenced at 10 MHz)	<±1 dB typical, 250 kHz to 80 MHz (with CIC and sync compensation filter engaged)
AC coupling cutoff frequency (-3 dB)	50 kHz typical
Channel-to-channel crosstalk	
<40 MHz	<-70 dB typical
≥40 MHz to 80 MHz	<-60 dB typical

IF Output Performance

Figure 8. Measured Analog Output Passband Flatness (Referenced to 10 MHz)



IF Output Spectral Characteristics Performance

Figure 9. Measured Analog Output Single-Tone Distortion
(Carrier Frequency = 7.36 MHz, Inverse Sync Filter OFF, Output Amplitude = -3 dBFS)

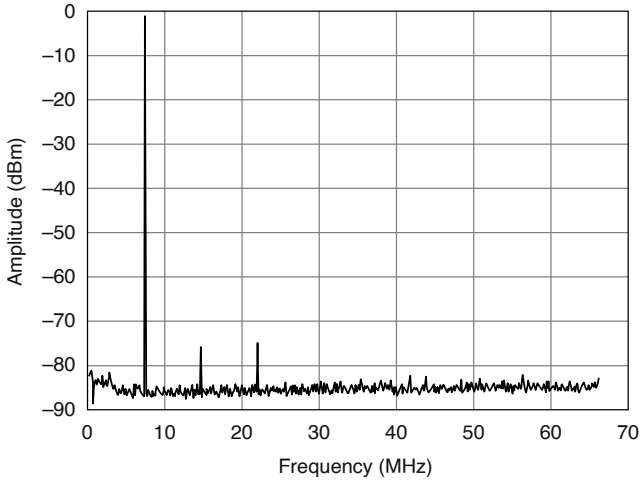
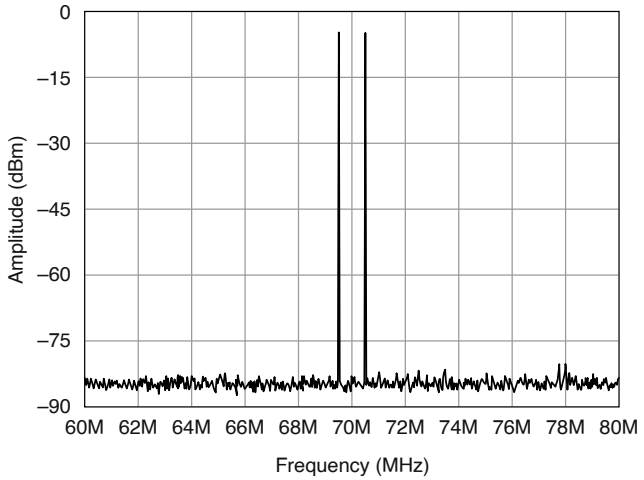


Figure 10. Measured Analog Output Two-Tone IMD
(Center Frequency at 70 MHz, Carriers at 70 MHz ± 0.5 MHz, -5 dBm Each, Inverse Sync Filter ON)



Digital Upconverter Characteristics

Number of channels	1 per DAC channel
DUC resolution	14 bits for both I and Q data

Interpolation	4x to 252x
Modulation bandwidth	Up to 40 MHz
Tuning resolution	DAC clock/2^{32}. (For example, a 200 MHz clock results in a 46.6 mHz tuning resolution.)

System Level Performance

System Level Modulation Quality

Conditions	8-QAM, symbol rate: 3.125 MHz, PRN 9 sequence, power: -5 dBm, filter alpha 0.22, filter length 128, root-raised cosine

Modulation error ratio (MER)[3]

10 MHz carrier	>57 dB typical
40 MHz carrier	>54 dB typical
70 MHz carrier	>46 dB typical

Data Transfer Rate

(Using NI PXIe-1062Q chassis, NI PXIe-8130 controller, single-threaded, half-duplex transfer; transfer rate is dependent upon controller and chassis hardware, software, and backplane usage.)

NI PXIe-5641R to host	120 MB/s typical
Host to NI PXIe-5641R	52 MB/s typical

Timebase System

Internal Timebase

Timebase frequency[4]	200 MHz ± 35 ppm, maximum
Minimum Sample Clock divisor	2 for ADC, 1 for DAC
Supported divisors	1, 2, 4, 8, and 16

External Clock/External Frequency Reference

Impedance	50 Ω nominal, AC-coupled
Input amplitude range Sine wave 0.63 $V_{peak-peak}$ to 2.8 $V_{peak-peak}$ (0 dBm to 13 dBm) Square wave 0.25 $V_{peak-peak}$ to 2.8 $V_{peak-peak}$	
Maximum input level without damage	+24 dBm (10 $V_{peak-peak}$, 3.5 V_{RMS})
Maximum PLL lock time	250 ms
External Reference Clock range[5]	1 MHz to 100 MHz in 1 MHz increments, ±100 ppm
External Sample Clock range[6]	30 MHz to 200 MHz

Trigger System

Modes	Digital input, software

Sources	
Using instrument driver	TRIG or software
Using LabVIEW FPGA	TRIG, RTSI <0..7> (mapped to PXIe_TRIG<0..7>), or software
Slope	
Using instrument driver	Rising
Using LabVIEW FPGA	Rising or falling

External Trigger Channel (TRIG)

Impedance	10 kΩ nominal, DC-coupled
Range	0 V to 3.3 V typical, 5 V tolerant
V_{IH}	2.2 V typical
V_{IL}	0.95 V typical
Overvoltage protection	-3.5 V to +8 V continuous
Maximum trigger frequency	<10 MHz typical, system dependent
Input rise/fall time	<10 ns/V typical

AUX I/O Connector

Number of digital lines	7

I/O direction	Pin-configurable
Input voltage range	0 V to 3.3 V typical, 5 V tolerant
V_{IH}	2.5 V typical
V_{IL}	1 V typical
V_{OH}	3.5 V typical, no load
V_{OL}	0.1 V typical, no load
Overvoltage protection	-0.5 to +5.5 V
Output type	3.3 V CMOS
Output current	±24 mA
Output impedance	56 Ω
+5 V power output voltage	5 V ± 10%
+5 V power output current	500 mA, ±150 mA typical, electronically fused

FPGA

Model	Xilinx Virtex 5 SX95T
Logic cells	94,208
Multipliers/DSP blocks (18 * 18)	640

Block RAM	8,784 (kbits max)

Onboard DRAM

Memory size	128 MB
Theoretical maximum data rate	1,600 MB/s

Maximum Power Requirements

+3.3 VDC	3 A
+12 VDC	3 A
Total power	38.25 W

Physical Characteristics

Dimensions	3U, one slot, PXI Express module 21.6 cm * 2.0 cm * 13.0 cm (8.5 in * 0.8 in * 5.1 in)
Weight	397 g (13.4 oz)

Table 1. I/O Connectors

Connector Name	Type	Function
AI CH <0..1>	SMA	Analog input terminals for the NI PXIe-5641R
AO CH <0..1>	SMA	Analog output terminals for the NI PXIe-5641R
CLK IN	SMB	Input terminal for an external Reference Clock or Sample Clock
TRIG	SMB	Input or output terminal for device trigger signals
DIO (AUX I/O)	9-pin DIN mini-circular	Input or output terminal for device digital I/O (DIO) channels

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 40 °C
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- Waste Electrical and Electronic Equipment (WEEE)—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- 中国 RoHS— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

[1] Higher decimation is possible using LabVIEW FPGA, depending on performance requirements.

[2] Instrument driver enables CIC and inverse sync compensation by default, and the compensation cannot be bypassed.

[3] MER performance estimated using short (7.62 cm, or 3 in.) loopback cables from output to input.

[4] Adjusted during calibration

[5] The CLK IN connector on the NI PXIe-5641R can function as either a Reference Clock input or a Sample Clock input.

[6] The CLK IN connector on the NI PXIe-5641R can function as either a Reference Clock input or a Sample Clock input.