TEA2093TS

GreenChip synchronous rectifier controller

Rev. 1 — 7 June 2022 Product data sheet

1 General description

The TEA2093TS is a member of a new generation of synchronous rectifier (SR) controller ICs for switched mode power supplies. It includes an adaptive gate drive for maximum efficiency at any load.

The TEA2093TS is a dedicated controller IC for synchronous rectification on the secondary side of asymmetrical half-bridge flyback and standard flyback converters. It incorporates the sensing stage and driver stage for driving the SR MOSFET, which is rectifying the output of the secondary transformer winding.

The TEA2093TS can generate its own supply voltage for battery-charging applications with low output voltage or for applications with high-side rectification.

The TEA2093TS is fabricated in a silicon-on-insulator (SOI) process.

2 Features and benefits

2.1 Efficiency features

- Adaptive gate drive for maximum efficiency at any load
- Typical supply current in no-load operation below 200 µA

2.2 Application features

- Operates in a wide output voltage range down to 0 V
- Drain sense pin capable of handling input voltages up to 120 V
- Self-supplying for operation with low output voltage
- Self-supplying for high-side rectification without the use of an auxiliary winding
- Operates with standard and logic level SR MOSFETs
- Supports USB BC, USB PD, and quick charge applications
- TSOP6 package

2.3 Control features

- Adaptive gate drive for fast turn-off at the end of conduction
- Undervoltage lockout (UVLO) with active gate pull-down

3 Applications

The TEA2093TS is intended for flyback power supplies. In such applications, it can drive the external synchronous rectifier MOSFET, which replaces the diode for the rectification of the voltage on the secondary winding of the transformer.

It can be used in all power supplies needing high efficiency, like:

- Chargers
- Adapters
- Asymmetrical half-bridge flyback power supplies
- Flyback power supplies with very low and/or variable output voltage

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA2093TS/1	TSOP6	plastic surface-mounted package; 6 leads	SOT457

5 Marking

Table 2. Marking codes

Type number	Marking code
TEA2093TS/1	TEA2093

6 Block diagram

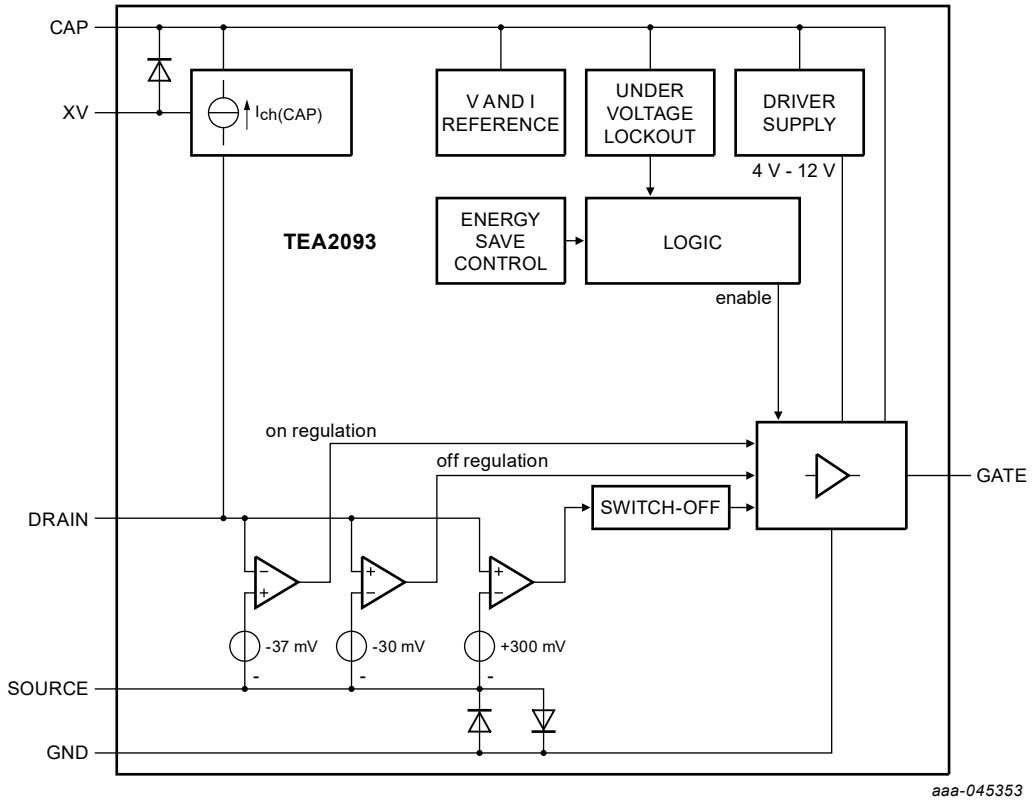


Figure 1. TEA2093TS block diagram

7 Pinning information

7.1 Pinning

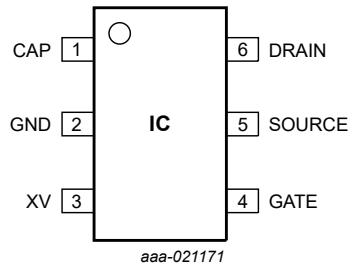


Figure 2. TEA2093TS pin configuration (SOT457)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CAP	1	capacitor input for internal supply voltage
GND	2	ground
XV	3	external supply input
GATE	4	gate driver output for SR MOSFET
SOURCE	5	source sense input of SR MOSFET
DRAIN	6	drain sense input of SR MOSFET

8 Functional description

8.1 Introduction

The TEA2093TS is a controller IC for synchronous rectification (SR) in asymmetrical half-bridge flyback and standard flyback applications. It can drive the external synchronous rectifier MOSFET for the rectification of the voltage on the secondary winding of the transformer. Figure 3 shows a typical configuration.

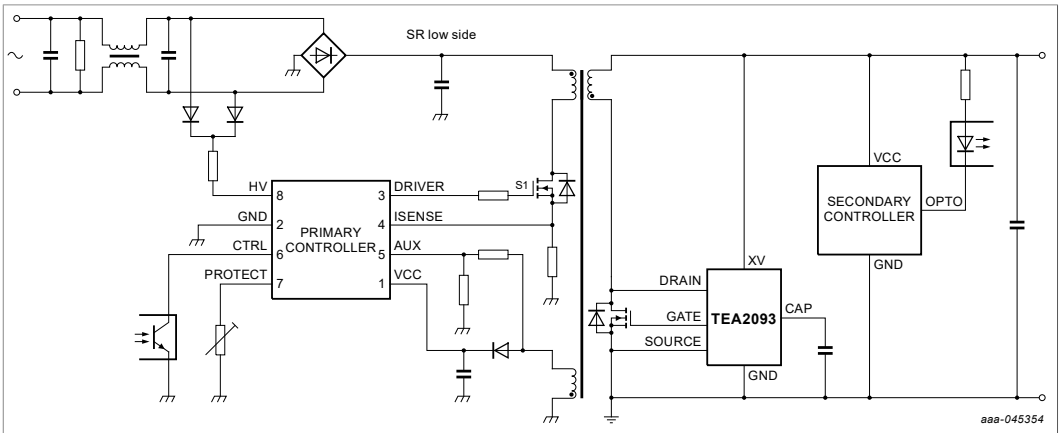


Figure 3. TEA2093TS configuration with low-side rectification

8.2 Start-up and undervoltage lockout (UVLO; CAP and XV pins)

The capacitor on the CAP pin supplies the TEA2093TS. It is charged via the DRAIN pin when the XV voltage is < 4.7 V. The charge current ($I_{ch(CAP)}$) charges the capacitor to 4 V. When this voltage is reached, it stops charging. If the external voltage exceeds 4.7 V, the XV pin increases the capacitor voltage via an integrated diode. The increase of the capacitor voltage gives a higher gate driver voltage ($V_{G(max)}$).

When the voltage on the CAP pin exceeds $V_{start(CAP)}$ (3.7 V typical), the IC leaves the UVLO state and activates the synchronous rectifier circuitry. When the voltage drops to below 3.6 V (typical), the UVLO state is reentered and the SR MOSFET gate driver output is actively kept low.

8.3 Drain sense (DRAIN pin)

The drain sense pin is an input pin capable of handling input voltages up to 120 V. At a positive drain sense voltage, the gate driver is in off-mode with the gate driver pulled down (pin GATE). At a negative drain sense voltage, the IC enables the synchronous rectification (SR) by sensing the drain source differential voltage.

8.4 Synchronous rectification (DRAIN and SOURCE pins)

The IC senses the voltage difference between the drain sense (DRAIN pin) and the source sense (SOURCE pin) connections. This drain source differential voltage of the SR MOSFET is used to drive the gate of the SR MOSFET.

In the regulation phase, the IC regulates the difference between the drain and the source sense inputs to an absolute level of 37 mV. When the absolute difference exceeds 37 mV ($V_{reg(drv)}$), the gate driver output increases the gate voltage of the external SR MOSFET until the 37 mV level is reached. The SR MOSFET does not switch off at low current.

When the absolute difference is < 30 mV, the gate driver output decreases the gate voltage of the external SR MOSFET. The voltage waveform on the SR MOSFET gate follows the waveform of the current through the SR MOSFET. When the current through the SR MOSFET reaches zero, the SR MOSFET is quickly switched off.

After SR MOSFET switch-off, the drain voltage increases. When the drain voltage exceeds 300 mV, a low ohmic gate pull-down of 7 Ω keeps the gate of the SR MOSFET switched off.

8.5 Gate driver (GATE pin)

The gate driver circuit charges the gate of the external SR MOSFET during the rising part of the current. The driver circuit discharges the gate during the falling part of the current. The gate driver has a source capability of typically 0.50 A and a sink capability of typically 0.65 A, allowing fast turn-on and fast turn-off of the external SR MOSFET.

The maximum output voltage of the driver is limited to 12 V. This high output voltage drives all MOSFET brands to the minimum on-state resistance. In applications where the IC is supplied with 5 V, the maximum output voltage of the driver is 4.2 V and logic level SR MOSFETs can be used (see Figure 3).

The IC is self-supplying in applications with high-side rectification or in battery-charging applications with an output voltage below 4.7 V. When the XV pin is connected to ground for driving standard SR MOSFETs, the driver is regulated to 9 V. When the XV pin is connected to the converter output for driving logic-level SR MOSFETs, the driver is regulated to 4 V if the output voltage is below 4.7 V.

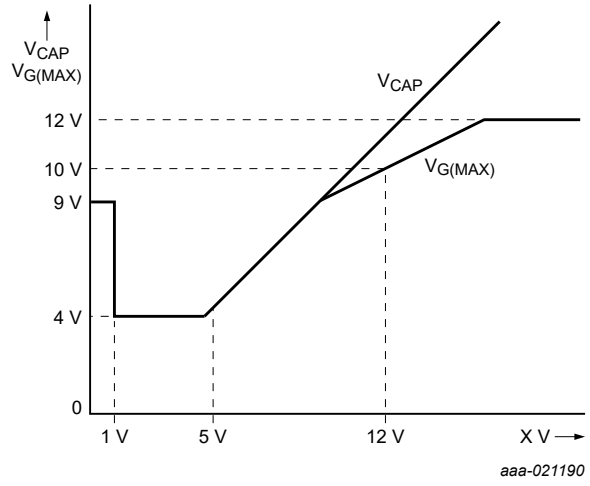


Figure 4. Maximum gate voltage $V_{g(max)}$

During start-up conditions ($V_{CAP} < V_{start(CAP)}$) and UVLO, the driver output voltage is actively pulled low.

8.6 Source sense (SOURCE pin)

The IC is equipped with an additional source sense pin (SOURCE). This pin is used for measuring the drain-to-source voltage of the external SR MOSFET. The source sense input must be connected as close as possible to the SOURCE pin of the external SR MOSFET. It minimizes errors, caused by voltage differences on PCB tracks due to parasitic inductance in combination with large dI/dt values.

9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{XV}	voltage on pin XV		−0.4	+38	V
$V_{sense(DRAIN)}$	sense voltage on pin DRAIN		−0.8	+120	V
$V_{sense(SOURCE)}$	sense voltage on pin SOURCE		−0.4	+0.4	V
Currents					
I_{XV}	current on pin XV	peak current	-	0.5	A
General					
P_{tot}	total power dissipation	T_{amb} = 90 °C	-	300	mW
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C
Electrostatic discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	class 2			
		human body model [1]	-	2000	V
		charged device model	-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	200	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	JEDEC test board	115	K/W

11 Characteristics

Table 6. Characteristics

−25 °C < T_j < +125 °C; V_{xv} = 12 V; C_{CAP} = 1 µF; C_{GATE} = 10 nF (capacitor between the GATE and the GND pins); all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified. Limits are production tested at 25 °C. Statistical characterization in the temperature operating range ensure these limits.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (XV and CAP pins)						
$V_{start(CAP)}$	start voltage on pin CAP	V_{XV} = 0 V	3.55	3.70	3.90	V
$V_{stop(CAP)}$	stop voltage on pin CAP	V_{XV} = 0 V	3.45	3.60	3.80	V
$I_{ch(CAP)}$	charge current on pin CAP	V_{XV} = 0 V; V_{CAP} = 7 V; V_{DRAIN} = 12 V; T_j = 25 °C	−95	−70	−50	mA
		V_{XV} = 2 V; V_{CAP} = 3.65 V; V_{DRAIN} = 12 V; T_j = 25 °C	−95	−70	−50	mA
$V_{I(CAP)}$	input voltage on pin CAP	V_{XV} = 0 V; V_{DRAIN} = 12 V	8.70	9.20	9.60	V
		V_{XV} = 2 V; V_{DRAIN} = 12 V	3.80	4.00	4.15	V
		V_{XV} = 5 V	4.15	4.30	4.75	V
		V_{XV} = 12 V	11.0	11.3	11.7	V
$I_{I(XV)}$	input current on pin XV	power save operation; V_{XV} = 5 V	90	160	300	µA
		normal operation; without gate charge; V_{XV} = 5 V; T_j = 25 °C	1.35	1.60	1.85	mA
Synchronous rectification sense input (DRAIN and SOURCE pins)						
$V_{reg(drv)}$	driver regulation voltage	V_{SOURCE} = 0 V; T_j = 25 °C	−40	−37	−35	mV
V_{swoff}	switch-off voltage	V_{SOURCE} = 0 V; T_j = 25 °C	200	300	400	mV
$t_{d(act)(drv)}$	driver activation delay time	V_{SOURCE} = 0 V; normal operation; time for step on V_{DRAIN} (2 V to −0.5 V) to rising of V_{GATE} at 10 % of end value	-	65	-	ns
$t_{d(deact)(drv)}$	driver deactivation delay time	V_{SOURCE} = 0 V; normal operation; time for step on V_{DRAIN} (−0.5 V to 2 V) to falling of V_{GATE} at 10 % begin value	-	40	-	ns

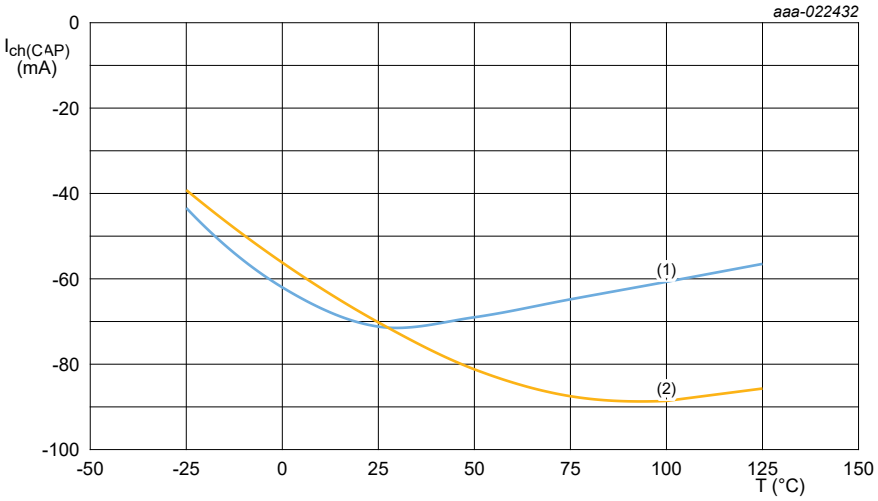
Table 6. Characteristics...*continued*

−25 °C < T_j < +125 °C; V_{xv} = 12 V; C_{CAP} = 1 µF; C_{GATE} = 10 nF (capacitor between the GATE and the GND pins); all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified. Limits are production tested at 25 °C. Statistical characterization in the temperature operating range ensure these limits.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gate driver (GATE pin)						
I_{source}	source current	peak current				
		V_{XV} = 5 V; V_{ds} = −0.5 V; V_g = 0 V	-	−0.13	-	A
		V_{XV} = 12 V; V_{ds} = −0.5 V; V_g = 0 V	-	−0.50	-	A
I_{sink}	sink current	regulation current				
		V_{XV} = 5 V; V_{ds} = 0 V; V_g = 4 V	-	150	-	mA
		V_{XV} = 12 V; V_{ds} = 0 V; V_g = 10 V	-	210	-	mA
		peak current				
		V_{XV} = 5 V; V_{ds} = 4 V; V_g = 4 V	-	0.35	-	A
		V_{XV} = 12 V; V_{ds} = 4 V; V_g = 4 V	-	0.65	-	A
$R_{pd(G)}$	gate pull-down resistance	V_{DRAIN} = 4 V; I_{GATE} = 30 mA; V_{XV} = 12 V; T_j = 25 °C	6.00	6.80	7.60	Ω
$V_{G(max)}$	maximum gate voltage	V_{XV} = 0 V	7.80	8.90	9.60	V
		V_{XV} = 2 V	3.75	3.95	4.15	V
		V_{XV} = 5 V	4.00	4.20	4.40	V
		V_{XV} = V_{CAP} = 5 V	4.90	4.95	5.00	V
		V_{XV} = 12 V	9.40	9.80	10.70	V
		V_{XV} = 18 V to 38 V	11.80	12.30	12.70	V

11.1 Temperature curves

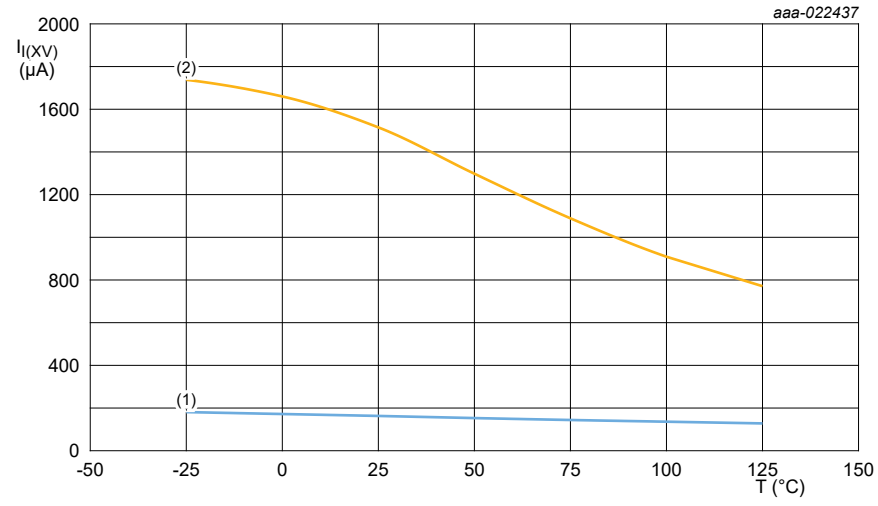
11.1.1 Charge current (CAP pin)



(1) $I_{ch(CAP)}$ at V_{CAP} = 7 V; V_{XV} = 0 V
(2) $I_{ch(CAP)}$ at V_{CAP} = 3.65 V; V_{XV} = 2 V

Figure 5. $I_{ch(CAP)}$ as a function of temperature

11.1.2 Operating current (XV pin)



(1) $I_{I(XV)}$) - power save operation
(2) $I_{I(XV)}$ - normal operation

Figure 6. $I_{I(XV)}$ as a function of temperature

11.1.3 Driver regulation voltage

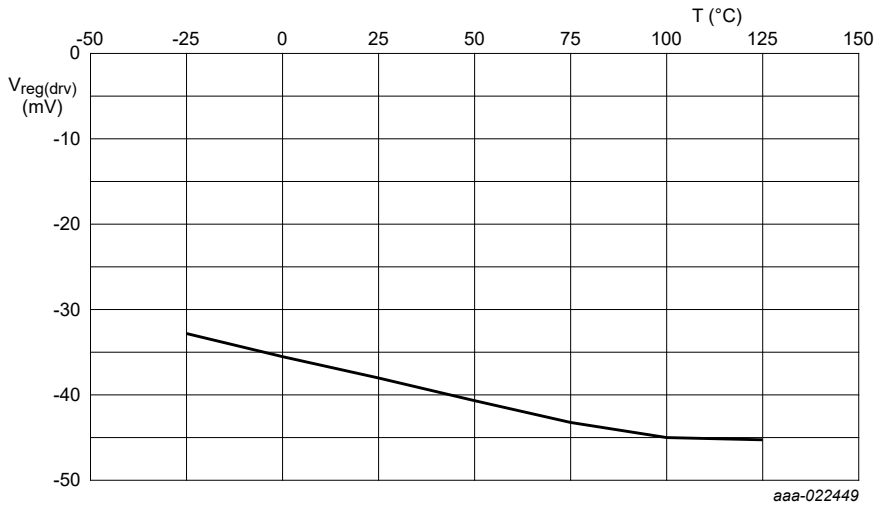


Figure 7. $V_{reg(drv)}$ as a function of temperature

11.1.4 Gate pull-down resistance

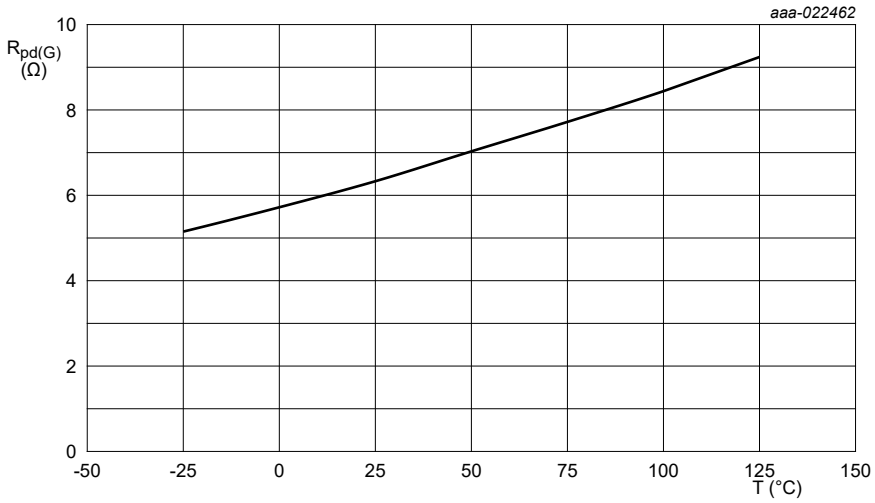


Figure 8. $R_{pd(G)}$ as a function of temperature

11.1.5 Switch-off voltage

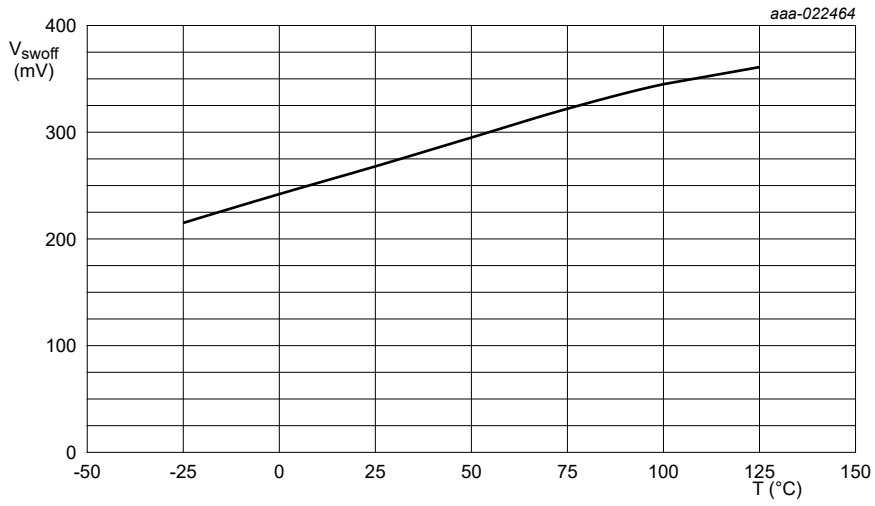


Figure 9. V_{swoff} as a function of temperature

12 Application information

A flyback switched mode power supply with the TEA2093TS consists of a primary side controller with a primary switch, a transformer, and an output stage. To obtain low conduction loss rectification, an SR MOSFET is used in the output stage. The SR MOSFET can be placed low-side (see Figure 3) or can be placed high-side (see Figure 10). In the high-side application, the TEA2093TS is self-supplying. The capacitor on the CAP pin supplies the TEA2093TS. When the drain voltage is positive, it is charged via the DRAIN pin.

The gate drive voltage for the synchronous rectifier switch is derived from the voltage difference between the corresponding drain sense and source sense pins.

Special attention must be paid to the connection of the drain sense and source sense pins. The voltages measured on these pins are used for the gate drive voltage. Wrong measurement results in a less efficient gate drive because a gate voltage that is either too low or too high. The connections to these pins must not interfere with the power wiring.

The power wiring conducts currents with high dI/dt values. It can easily cause measurement errors resulting from induced voltages due to parasitic inductances. The separate source sense pins make it possible to sense the source voltage of the external MOSFETs directly. So, the current carrying power ground tracks are not required.

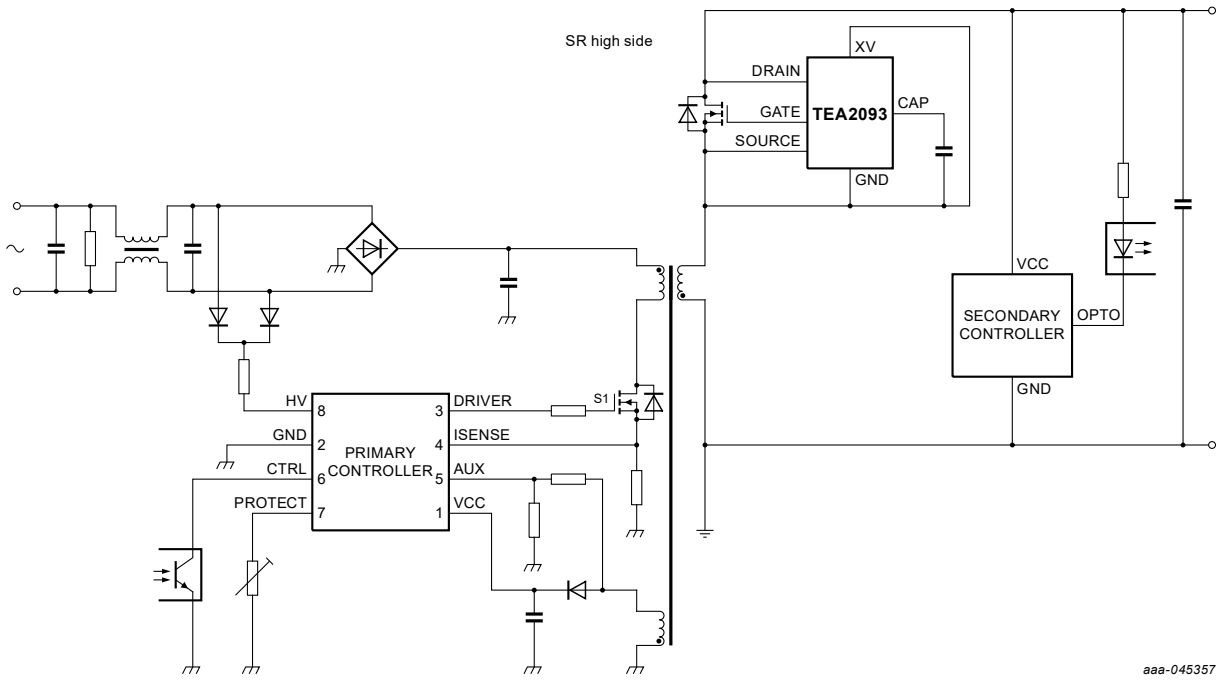
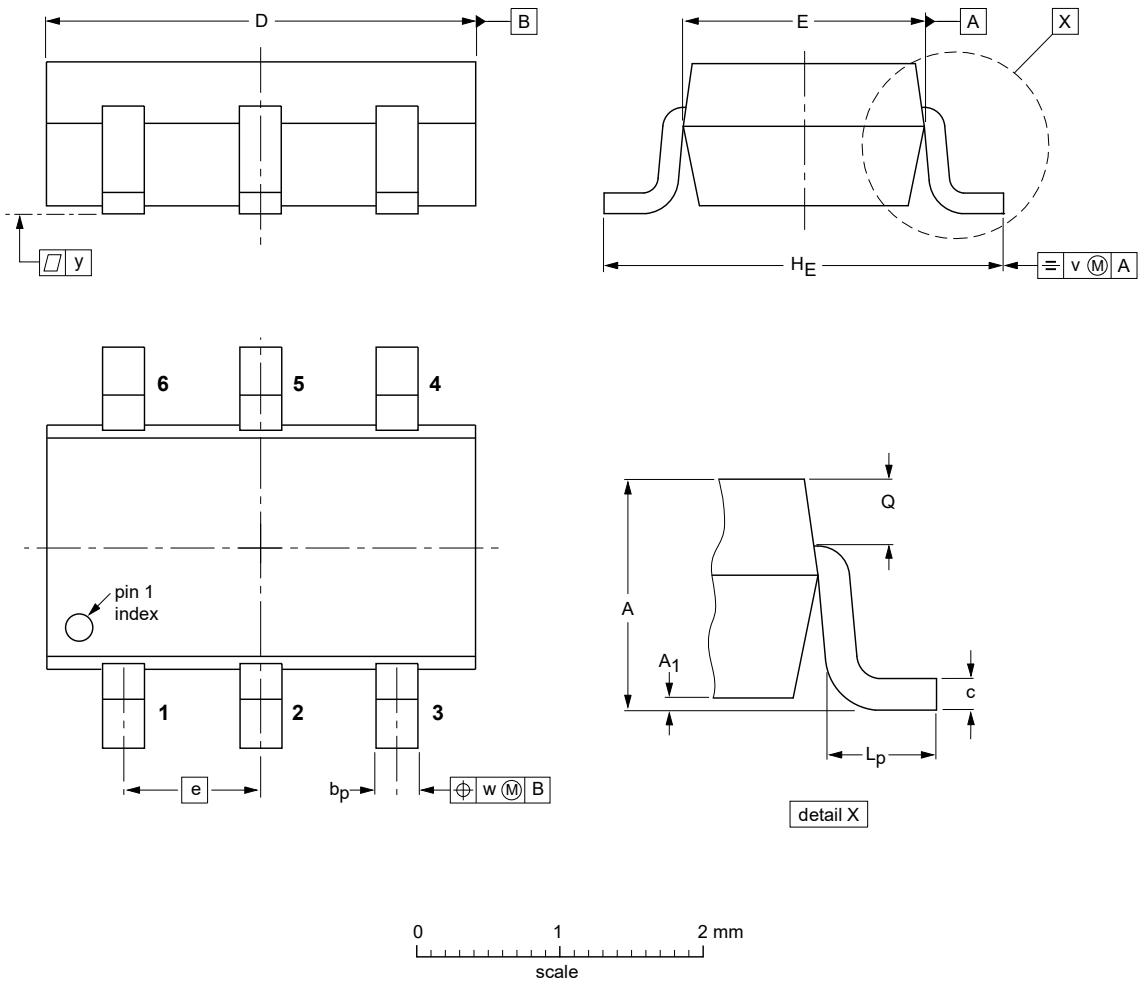


Figure 10. TEA2093TS configuration with high-side rectification

13 Package outline

Table 7.

Plastic surface-mounted package (TSOP6); 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~05-11-07~~ 06-03-16

Figure 11. Package outline SOT457 (TSOP6)

14 Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA2093TS v.1	20220607	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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