TSV771, TSV772

Datasheet

High bandwidth (20 MHz) low offset (200 µV) rail-to-rail 5 V Op Amp

TSV771
SOT23-5

TSV772
DFN8 2x2 mm

TSV772
MiniSO8

TSV772
SO8

Maturity status link	Channel	Automotive	Package
TSV771	1		SOT23-5
	1	•	SOT23-5
TSV772	2		DFN8
	2		MiniSO8
	2		SO8
	2	•	MiniSO8
	2	•	SO8

Related products	
TSV7721, TSV7722	Low rail 22 MHz amplifier
TSV791, TSV792	Rail-to-rail amplifier with higher GBW 50 MHz

Features

- Gain bandwidth product 20 MHz, unity gain stable
- Low input offset voltage: 50 µV typ., 200 µV max.
- Low input bias current: 2 pA typ.
- Low noise: 7 nV/√Hz
- Slew rate: 13 V/µs
- Wide supply voltage range: 2.0 V to 5.5 V
- Rail-to-rail input and output
- 4 kV HBM ESD tolerance
- Input common-mode range includes low rail
- Extended temperature range: -40 °C to +125 °C
- Automotive grade versions available
- Benefits:
  - Accuracy of measurement virtually unaffected by noise or input bias current
  - Signal conditioning for high frequencies

Applications

- High bandwidth low-side and high-side current sensing
- Photodiode amplifiers
- A/D converters input buffers
- Power management in solar powered systems
- Automotive high bandwidth signal conditioning
- Active filters

Description

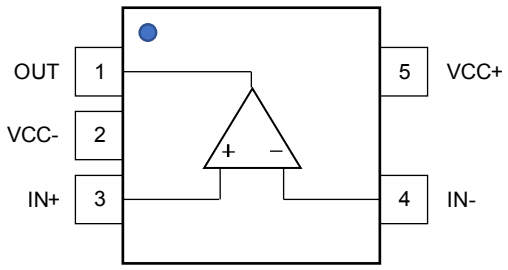
The TSV771 and TSV772 are a single and dual 20 MHz-bandwidth unity-gain-stable amplifier. The rail-to-rail input stage and the slew rate of 10.5 V/µs make the TSV771 and TSV772 ideal for low-side current measurement. The excellent accuracy provided by maximum input voltage of 200 µV allows amplifying accurately small-amplitude input signal.

The TSV771 and TSV772 can operate from a 2.0 V to 5.5 V single supply and is fully characterized for an output capacitor of 47 pF, therefore allowing easy usage as A/D converters input buffer.

1 Pin description

1.1 TSV771 single operational amplifier

Figure 1. Pin connections (top view)



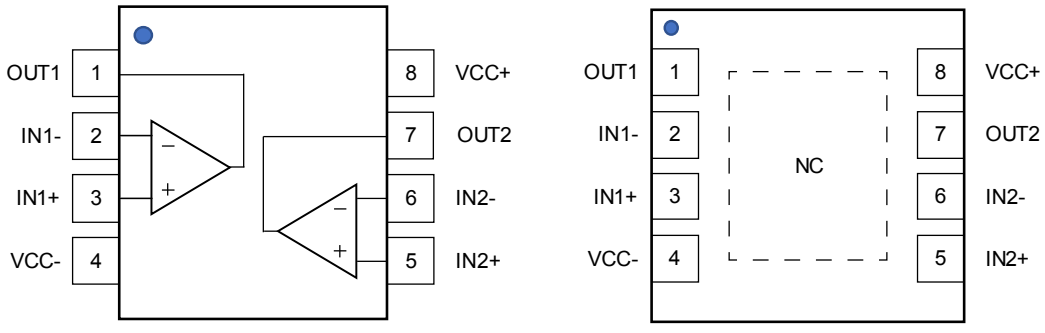
SOT23-5

Table 1. Pin description

Pin n°	Pin name	Description
1	OUT	Output channel
2	VCC-	Negative supply voltage
3	IN+	Non-inverting input channel
4	IN-	Inverting input channel
5	VCC+	Positive supply voltage

1.2 TSV772 dual operational amplifier

Figure 2. Pin connections (top view)



MiniSO8 and SO8 DFN8 2 x 2 mm(1)

1. The exposed pad of the DFN8 2x2 can be connected to VCC- or left floating.

Table 2. Pin description

Pin n°	Pin name	Description
1	OUT1	Output channel 1
2	IN1-	Inverting input channel 1
3	IN1+	Non-inverting input channel 1
4	VCC-	Negative supply voltage
5	IN2+	Non-inverting input channel 2
6	IN2-	Inverting input channel 2
7	OUT2	Output channel 2
8	VCC+	Positive supply voltage

2 Absolute maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter[1]	Value	Unit
V_{CC}	Supply voltage	-0.3 to 6.0	V
V_{id}	Input voltage differential (V_{IN+} - V_{IN-})	± V_{CC}	V
V_{IN}[2]	Input pins voltage	(V_{CC-}) - 0.3 V to V_{CC+} + 0.3	V
I_{IN}	Input current	± 10	mA
T_{stg}	Storage temperature	150	°C
$R_{th\text{-}ja}$[3]	Thermal resistance junction-to-ambient	-	°C / W
	DFN8 (2 mm x 2 mm)	76	
	SOT23-5	250	
	MiniSO8	127	
	SO8	113	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model [4]	4	kV
	CDM: charged device model [5]	1.5	kV

1. *All voltage values are with respect to VCC- pin, unless otherwise specified.*
2. *The maximum input voltage value may be extended to the condition that the input current is limited to ±10 mA.*
3. *$R_{th\ j\text{-}a}$ are typical values obtained with a PCB according to JEDEC 2s2p without vias.*
4. *Human Body Model: the test HBM is done in accordance with the standards ESDA-JS-001-2017 and Q100-002.*
5. *Charged device model: the test CDM is done in accordance with the standards ESDA-JS-002-2018 and Q100-011.*

Table 4. Operating conditions

Symbol	Parameter	Value
V_{CC}	Supply voltage	2.0 to 5.5 V
V_{icm}	Common-mode input voltage range	V_{CC-} – 0.2 V to V_{CC+} + 0.1 V
T_{oper}	Operating free air temperature range	-40 °C to +125 °C

3 Electrical characteristics

Table 5. Electrical characteristics at V_{CC} = 5.0 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			±200	µV
		-40 °C ≤ T ≤ 125 °C			±700	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C ≤ T ≤ 125 °C			±5	µV/°C
I_{ib}	Input bias current	T = 25 °C		2		pA
		-40 °C ≤ T ≤ 125 °C		75		
I_{io}	Input offset current	T = 25 °C		1		pA
		-40 °C ≤ T ≤ 125 °C		20		
A_{VD}	Open loop gain	V_{CC-}+100 mV ≤ V_{OUT} ≤ V_{CC+} -100 mV, T = 25 °C	110			dB
		V_{CC-}+100 mV ≤ V_{OUT} ≤ V_{CC+} -100 mV, -40 °C ≤ T ≤ 125 °C	95			
		R_L = 2 kΩ, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} -200 mV, T = 25 °C	105			
		R_L = 2 kΩ, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} -200 mV, 40 °C ≤ T ≤ 125 °C	90			
CMR1	Common-mode rejection ratio 20.log($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+} -1.8 V, T = 25 °C	98	120		dB
		V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+} -1.8 V, -40 °C ≤ T ≤ 125 °C	90	110		
CMR2		V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	81	100		
		V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	76	92		
SVR	Supply voltage rejection ratio 20.log($\Delta V_{io}/\Delta V_{CC}$)	2.0 V ≤ V_{CC} ≤ 5.5 V, T = 25 °C, V_{icm} = 0 V	90	110		dB
		2.0 V ≤ V_{CC} ≤ 5.5 V, -40 °C ≤ T ≤ 125 °C, V_{icm} = 0 V	90	110		
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{sink} (R_L connected to V_{CC+})	T = 25 °C	45	65		mA
		-40 °C ≤ T ≤ 125 °C	30			
	I_{source} (R_L connected to V_{CC-})	T = 25 °C	45	65		
		-40 °C ≤ T ≤ 125 °C	30			

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (per channel, R_L > 1 MΩ)	T = 25 °C		1.9	2.1	mA
		-40 °C ≤ T ≤ 125 °C			2.1	
AC performance						
GBP	Gain bandwidth product		17	20		MHz
SR	Slew rate	A_V = 1 V/V, 10% to 90%(1)	11	13		V/µs
t_s	Settling time	R_L = 4.7 kΩ, AV = -1 V/V, to 0.1%, V_{in} = 1 Vp-p		300		ns
		R_L = 4.7 kΩ, AV = -1 V/V, to 0.01%, V_{in} = 1 Vp-p(2)		470		
t_{rec}	Overload recovery time	V_{OUT} 100 mV from rail, A_V = +1		235		ns
CR	Cross talk	V_{OUT} = 4 Vpp, A_V = +101, f = 1 kHz		120		dB
Φ_m	Phase margin			50		degrees
GM	Gain margin			9		dB
C_{in}	Differential input capacitance			6.5		pF
	Common-mode input capacitance			2.5		
en	Input voltage noise density	f = 1 kHz		13		nV/√Hz
		f = 10 kHz		7		
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		7		µVpp

1. *Slew rate value is the average of rising and falling values.*
2. *Settling time at 0.01% is guaranteed by design.*

Table 6. Electrical characteristics at V_{CC+} = 3.3 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			±200	µV
		-40 °C ≤ T ≤ 125 °C			±700	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C ≤ T ≤ 125 °C			±5	µV/°C
I_{ib}	Input bias current	T = 25 °C		1.8		pA
		-40 °C ≤ T ≤ 125 °C		60		
I_{io}	Input offset current	T = 25 °C		1		pA
		-40 °C ≤ T ≤ 125 °C		20		
A_{VD}	Open loop gain	V_{CC-}+100 mV ≤ V_{OUT} ≤ V_{CC+} -100 mV, T = 25 °C	105			dB
		V_{CC-}+100 mV ≤ V_{OUT} ≤ V_{CC+} -100 mV, -40 °C ≤ T ≤ 125 °C	90			
		R_L = 2 kΩ, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} -200 mV, T = 25 °C	100			
		R_L = 2 kΩ, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} -200 mV, -40 °C ≤ T ≤ 125 °C	85			
CMR1	Common-mode rejection ratio 20.log($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+} -1.8 V, T = 25 °C	93	115		dB
		V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+} -1.8 V, -40 °C ≤ T ≤ 125 °C	85	108		
CMR2		V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	77	98		
		V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	70	90		
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{sink} (R_L connected to V_{CC+})	T = 25 °C	45	60		mA
		-40 °C ≤ T ≤ 125 °C	30			
	I_{source} (R_L connected to V_{CC-})	T = 25 °C	45	65		
		-40 °C ≤ T ≤ 125 °C	30			
I_{CC}	Supply current (per channel, R_L > 1 MΩ)	T = 25 °C		1.8	2.0	mA
		-40 °C ≤ T ≤ 125 °C			2.0	
AC performance						
GBP	Gain bandwidth product		17	20		MHz
SR	Slew rate	A_V = 1 V/V, 10% to 90%[1]	11	13		V/µs
t_s	Settling time	R_L = 4.7 kΩ, AV = -1 V/V, to 0.1%, V_{in} = 1 Vp-p		310		ns
		R_L = 4.7 kΩ, A_V = -1 V/V, to 0.01%, V_{in} = 1 Vp-p[2]		480		
t_{rec}	Overload recovery time	V_{OUT} 100 mV from rail, A_V = +1		260		ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Φ_m	Phase margin			48		degrees
GM	Gain margin			9		dB
C_{in}	Differential input capacitance			6.5		pF
	Common-mode input capacitance			2.5		
en	Input voltage noise density	f = 1 kHz		13		nV/√Hz
		f = 10 kHz		7		
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		7		µVpp

1. *Slew rate value is the average of rising and falling values.*
2. *Settling time at 0.01% is guaranteed by design.*

Table 7. Electrical characteristics at V_{CC+} = 2.0 V, V_{icm} = V_{OUT} = V_{CC}/2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC Performance						
V_{io}	Input offset voltage (V_{icm} = 0 V)	T = 25 °C			±200	µV
		-40 °C ≤ T ≤ 125 °C			±700	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C ≤ T ≤ 125 °C			±5	µV/°C
I_{ib}	Input bias current	T = 25 °C		1		pA
		-40 °C ≤ T ≤ 125 °C		40		
I_{io}	Input offset current	T = 25 °C		1		pA
		-40 °C ≤ T ≤ 125 °C		15		
A_{VD}	Open loop gain	V_{CC-}+100 mV ≤ V_{OUT} ≤ V_{CC+} -100 mV, T = 25 °C	95			dB
		V_{CC-}+100 mV ≤ V_{OUT} ≤ V_{CC+} -100 mV, -40 °C ≤ T ≤ 125 °C	80			
		R_L = 2 kΩ, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} -200 mV, T = 25 °C	90			
		R_L = 2 kΩ, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} -200 mV, 40 °C ≤ T ≤125 °C	80			
CMR	Common-mode rejection ratio 20.log($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	73	94		dB
		V_{CC-} -0.1 V ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	67	86		
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{sink} (R_L connected to V_{CC+})	T = 25 °C	45	60		mA
		-40 °C ≤ T ≤ 125 °C	30			
	I_{source} (R_L connected to V_{CC-})	T = 25 °C	45	65		
		-40 °C ≤ T ≤ 125 °C	30			
I_{CC}	Supply current (per channel, R_L > 1 MΩ, V_{icm} = 0 V)	T = 25 °C		1.7	1.9	mA
		-40 °C ≤ T ≤ 125 °C			1.9	
AC performance						
GBP	Gain bandwidth product		17	20		MHz
SR	Slew rate	AV = 1 V/V, 10% to 90%(1)	9	11		V/µs
t_s	Settling time	R_L = 4.7 kΩ, AV = -1 V/V, to 0.1%, V_{in} = 1 Vp-p		450		ns
		R_L = 4.7 kΩ, A_V = -1 V/V, to 0.01%, V_{in} = 1 Vp-p(2)		570		
t_{rec}	Overload recovery time	V_{OUT} 50 mV from initial value, A_V = +1		300		ns
Φ_m	Phase margin			47		degrees
GM	Gain margin			8		dB
C_{in}	Differential input capacitance			6.5		pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{in}	Common-mode input capacitance			2.5		pF
en	Input voltage noise density	f = 1 kHz		30		nV/√Hz
		f = 10 kHz		14		
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		10		µVpp

1. *Slew rate value is the average of rising and falling values.*
2. *Settling time at 0.01% is guaranteed by design.*

4 Typical performance characteristics

R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF, unless otherwise specified.

Figure 3. Supply current vs. supply voltage

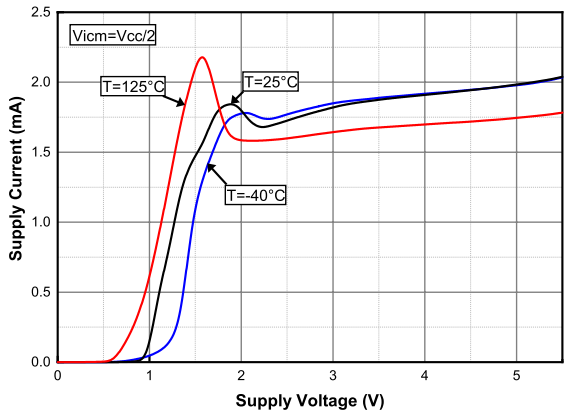


Figure 4. Input offset voltage distribution at V_{CC} = 5 V

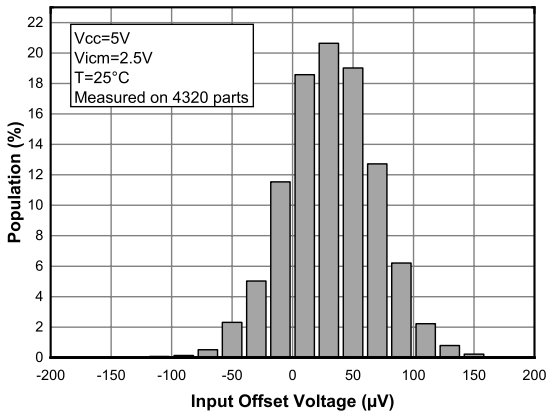


Figure 5. Input offset voltage distribution at V_{CC} = 2 V

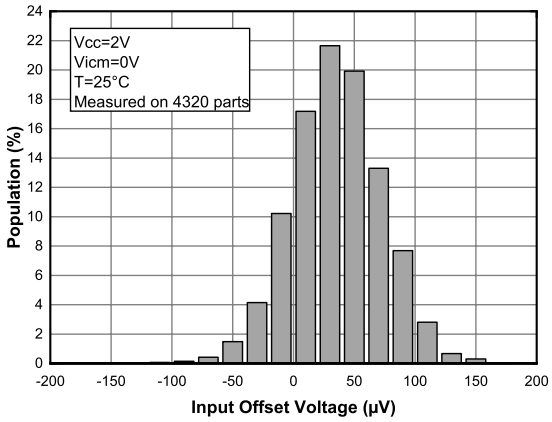


Figure 6. Input offset voltage vs. temperature at V_{CC} = 5 V

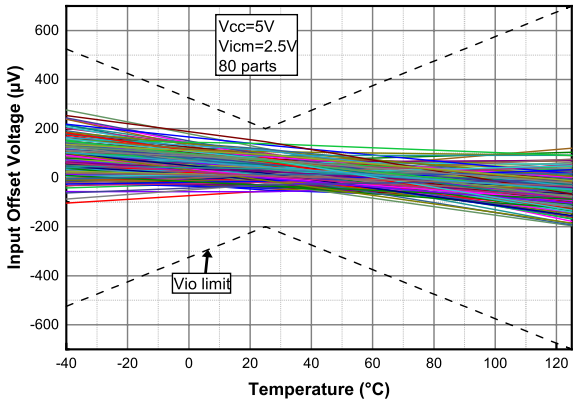


Figure 7. Input offset voltage vs. temperature at V_{CC} = 2 V

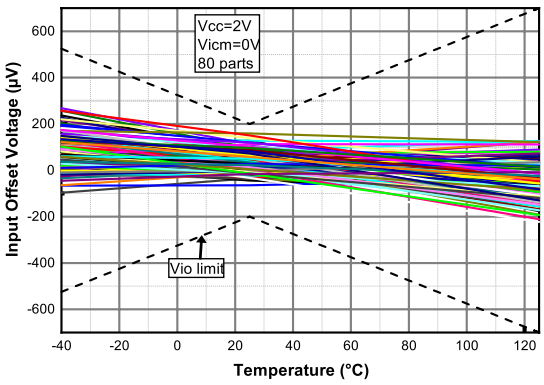


Figure 8. Input offset voltage thermal drift distribution at V_{CC} = 5 V

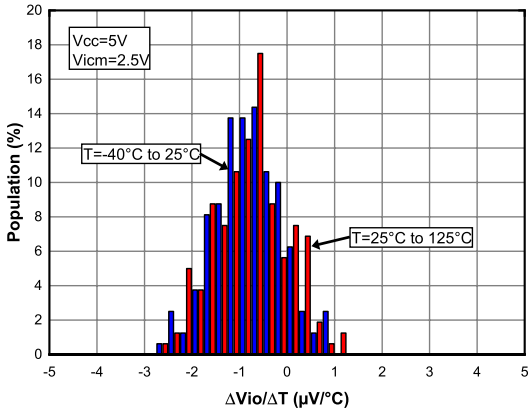


Figure 9. Input offset voltage thermal drift distribution at V_{CC} = 2 V

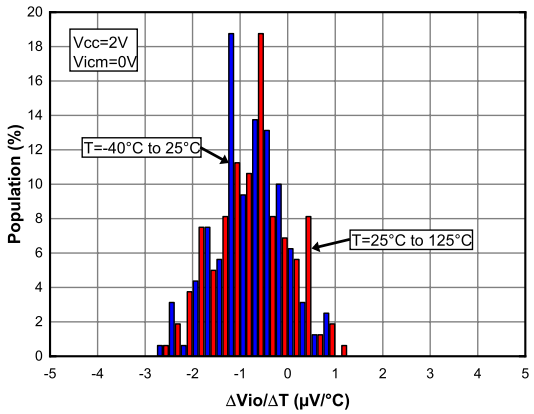


Figure 10. Input offset voltage vs. supply voltage

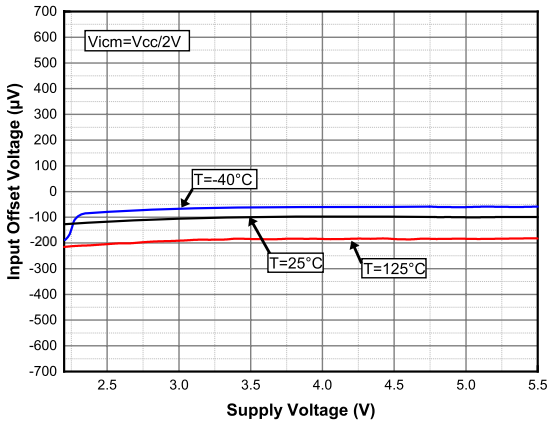


Figure 11. Input offset voltage vs. common-mode voltage at V_{CC} = 5 V

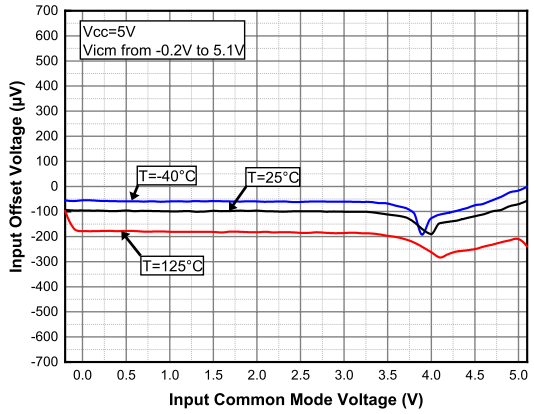


Figure 12. Input offset voltage vs. common-mode voltage at V_{CC} = 2 V

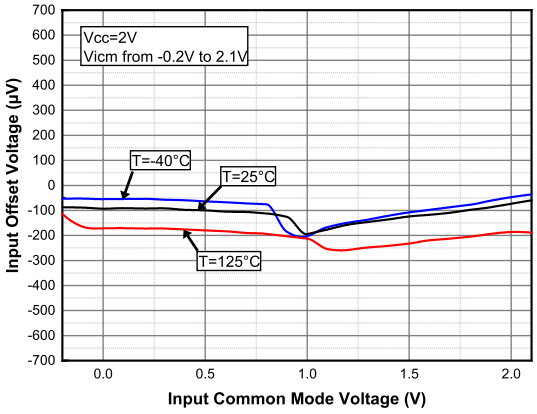


Figure 13. Input bias current vs. temperature

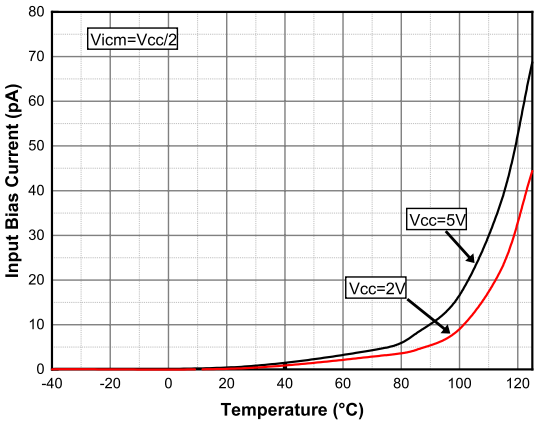


Figure 14. Input bias current vs. common-mode voltage at V_{CC} = 5 V

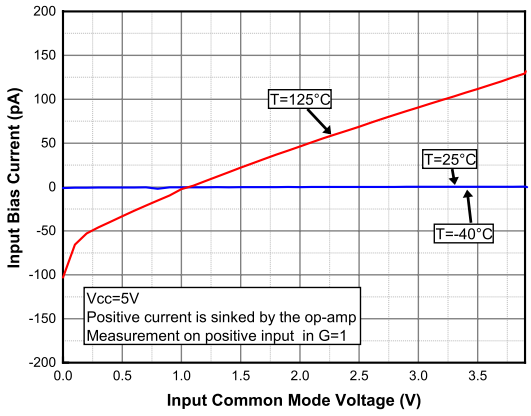


Figure 15. Output current vs. output voltage at V_{CC} = 5 V

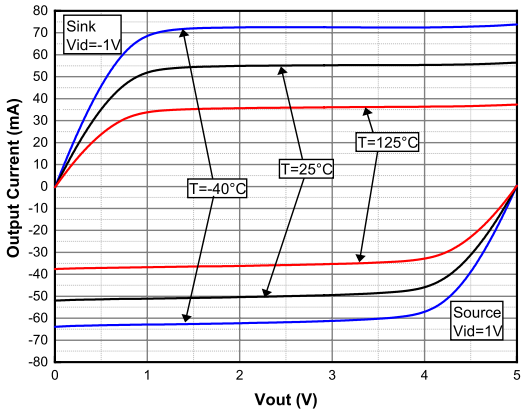


Figure 16. Output current versus output voltage at V_{CC} = 2 V

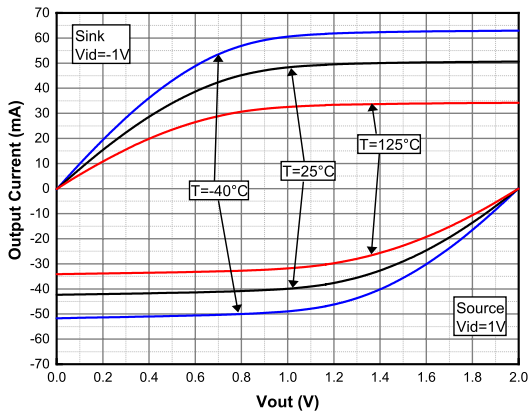


Figure 17. Output saturation voltage (V_{OL}) vs. supply voltage

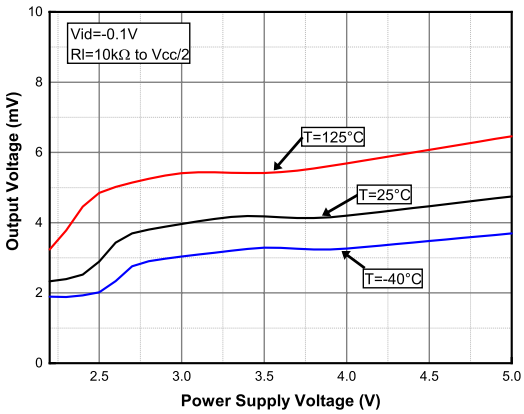


Figure 18. Output saturation voltage (V_{OH}) vs. supply voltage

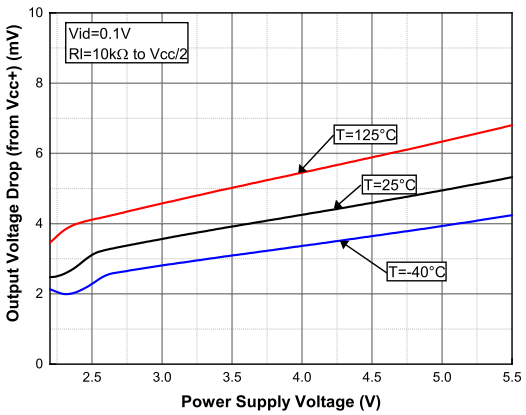


Figure 19. Positive slew rate at V_{CC} = 5 V

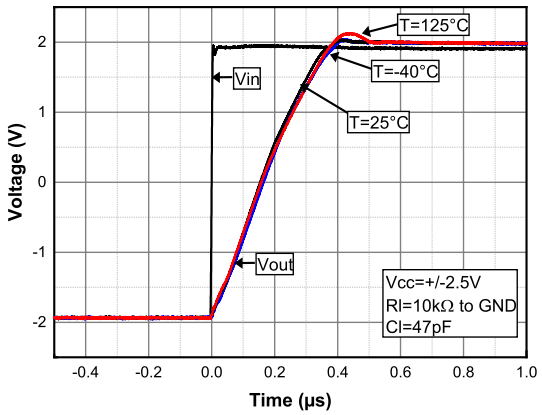


Figure 20. Negative slew rate at V_{CC} = 5 V

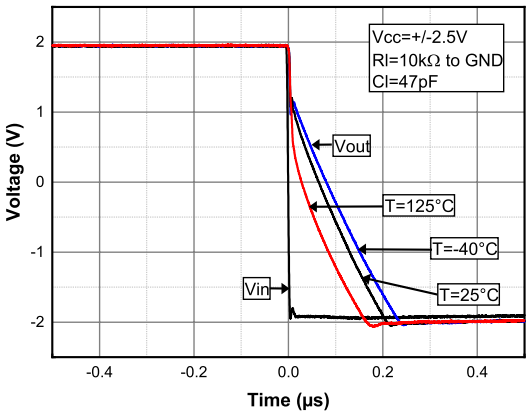


Figure 21. Slew rate vs. V_{CC}

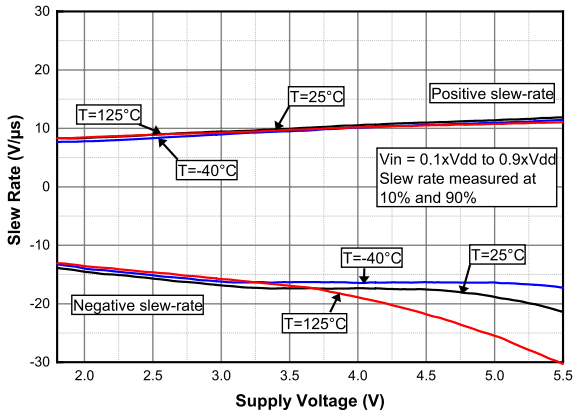


Figure 22. Open loop bode diagram at V_{CC} = 5 V

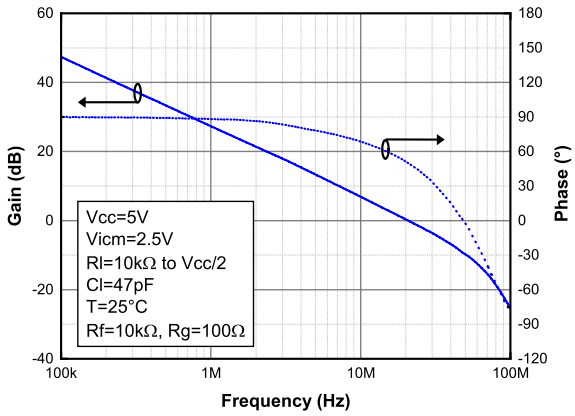


Figure 23. Open loop bode diagram at V_{CC} = 2 V

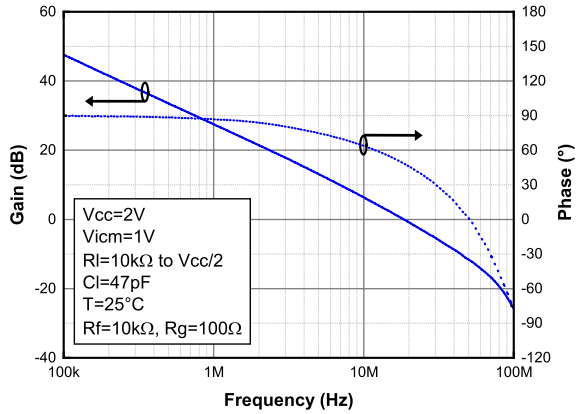


Figure 24. Closed loop bode diagram at V_{CC} = 5 V

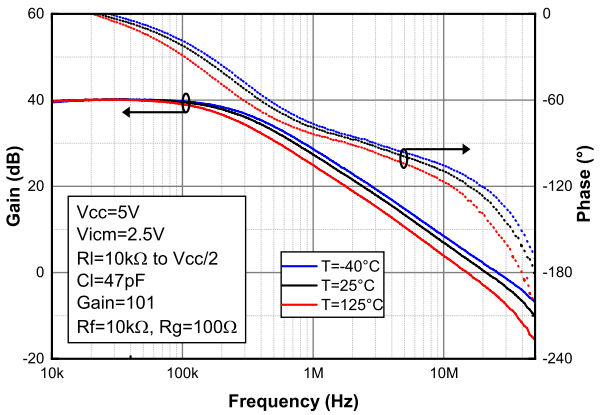


Figure 25. Closed loop bode diagram at V_{CC} = 2 V

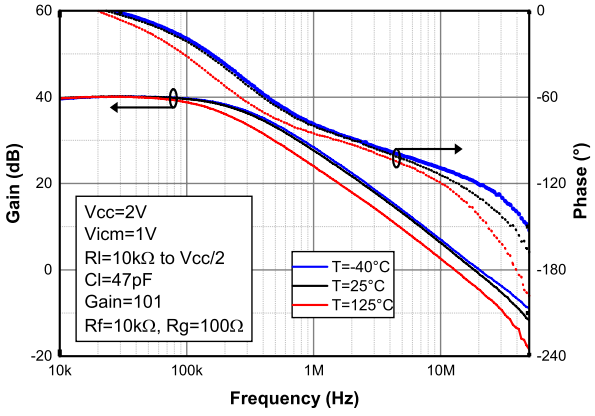


Figure 26. Phase margin vs. common-mode voltage and load current at V_{CC} = 5 V

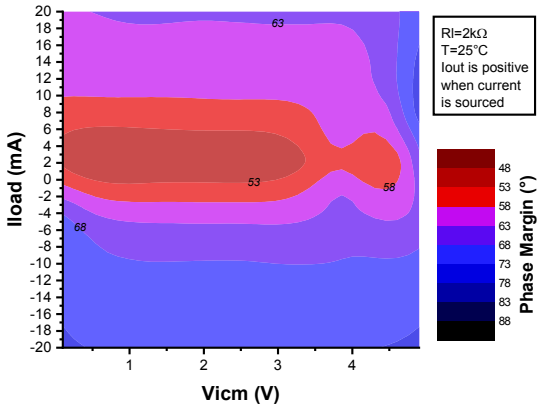


Figure 27. Phase margin vs. capacitive load

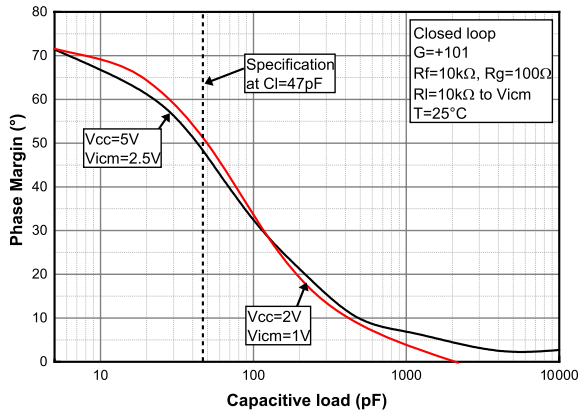


Figure 28. Small step response at V_{CC} = 5 V

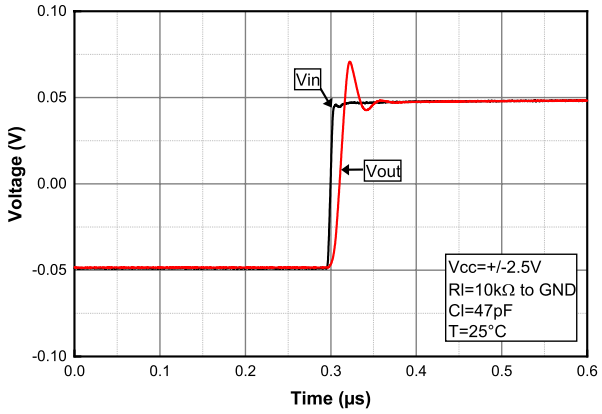


Figure 29. Small step response at V_{CC} = 2 V

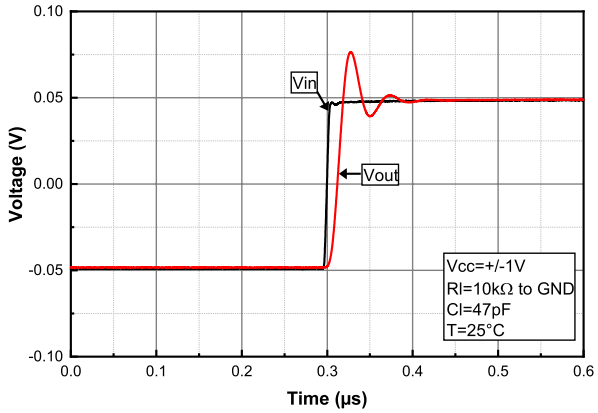


Figure 30. Desaturation from low rail at V_{CC} = 5 V

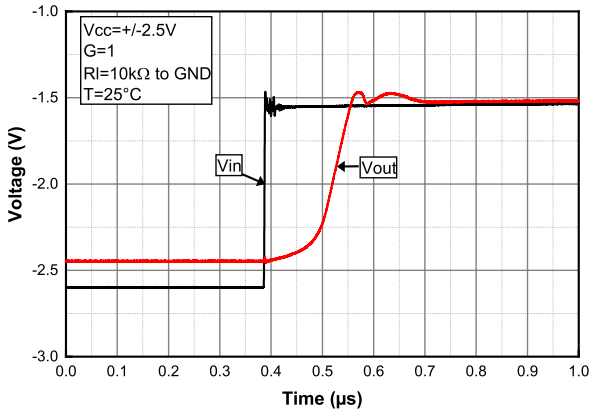


Figure 31. Desaturation from high rail at V_{CC} = 5 V

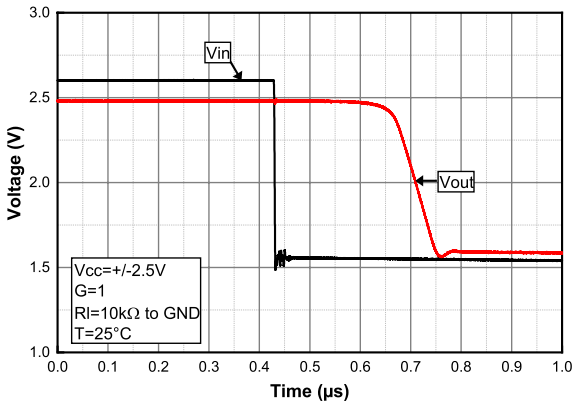


Figure 32. Settling time output high to low at V_{CC} = 5 V

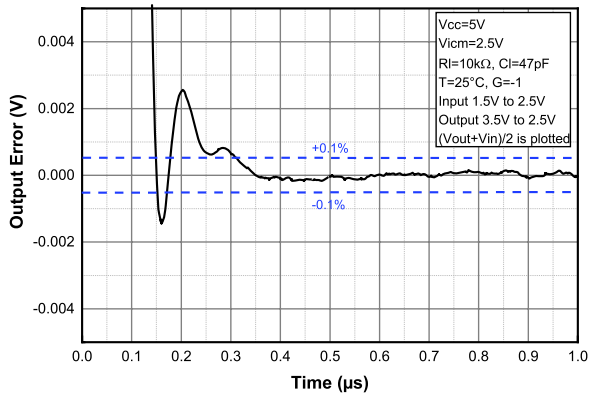


Figure 33. Settling time output low to high at V_{CC} = 5 V

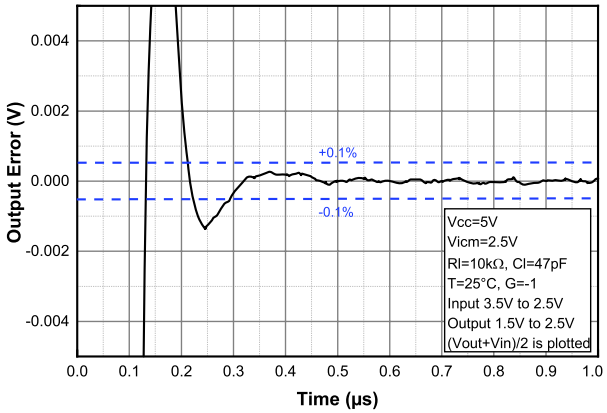


Figure 34. Small step overshoot vs. load capacitance

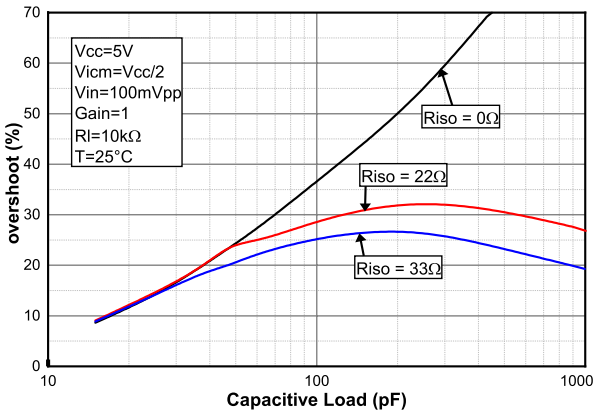


Figure 35. Linearity vs. load resistance at V_{CC} = 5 V

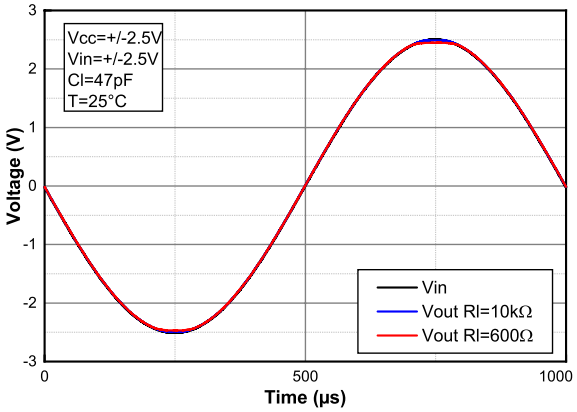


Figure 36. Noise vs. frequency

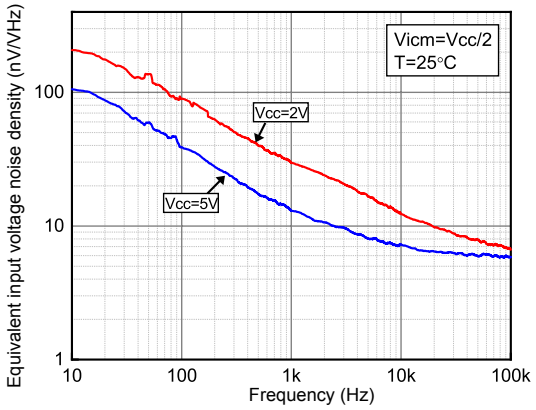


Figure 37. Noise vs. time at V_{CC} = 5 V

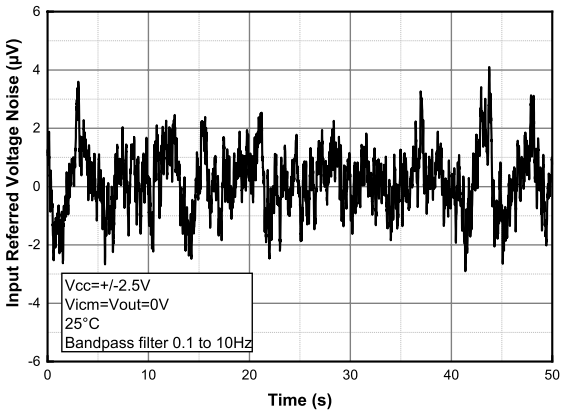


Figure 38. THD+N vs. frequency

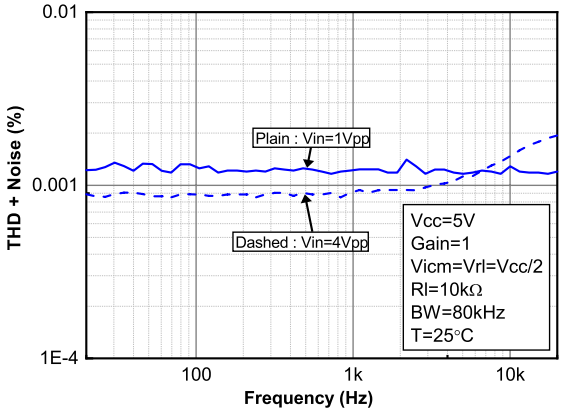


Figure 39. THD+N vs. output voltage

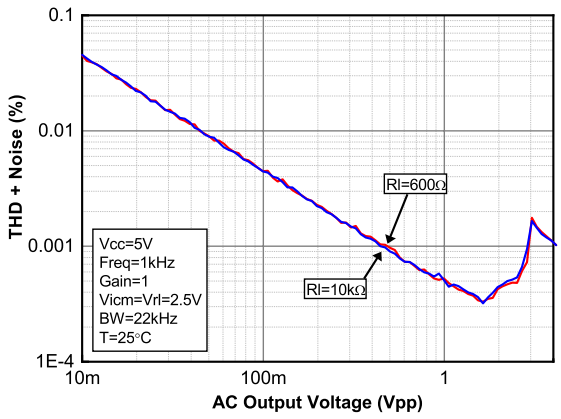


Figure 40. CMRR vs. frequency at V_{CC} = 5 V

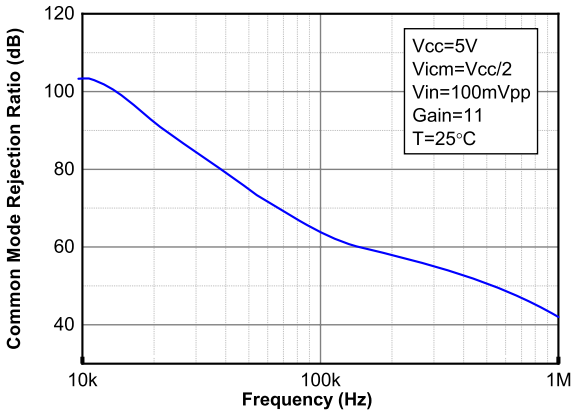


Figure 41. PSRR vs. frequency at V_{CC} = 5 V

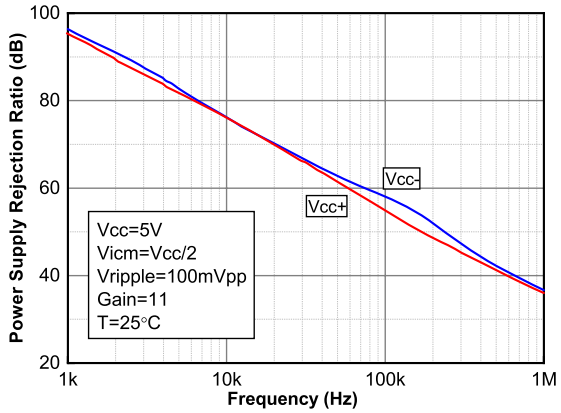


Figure 42. Turn-on time at V_{cc} = 5 V

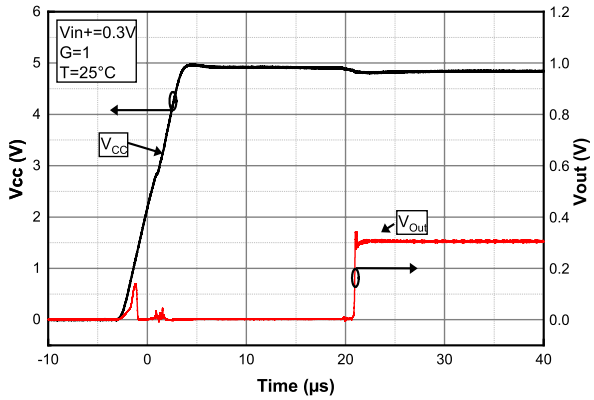
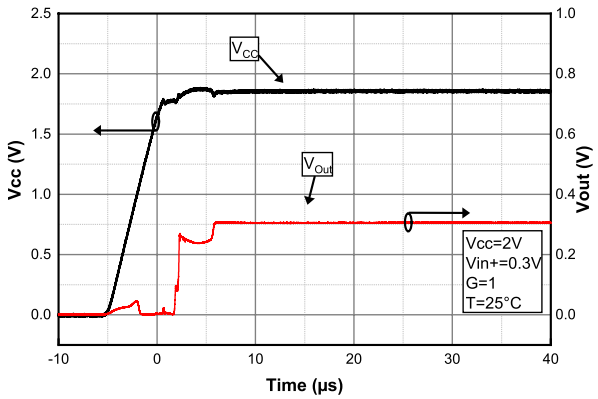


Figure 43. Turn-on time at V_{CC} = 2 V



5 Application information

5.1 Operating voltages

The TSV771 and TSV772 devices can operate from 2.0 to 5.5 V. The parameters are fully specified at 2.0 V, 3.3 V and 5 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSV771 and TSV772 devices characteristics over the full operating range. Additionally, the main specifications are guaranteed in extended temperature range from -40 to 125 °C.

The TSV772 device is rail-to-rail input and output and features two input transistor pairs, allowing the op amp to operate over all the common mode range, from V_{cc-} - 0.2 V, to V_{cc+} + 0.1 V. The input pair transition typically occurs at V_{cc+} - 1 V, as seen in Figure 11 and Figure 12. The precision and dynamic performances are particularly optimized on the low pair, from V_{cc-} - 0.1 V to V_{cc+} - 1.8 V, and operating in this V_{icm} range is advised for the best performance whenever possible. Besides, operating near the pair transition should be avoided when precision is a concern, as CMRR can be lower in these conditions.

5.2 Input offset voltage drift over the temperature

The input voltage drift variation over the temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset (V_{io}) is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during the production at the application level. The maximum input voltage drift over the temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift overtemperature is computed using the following equation:

$$\frac{\Delta V_{io}}{\Delta T} = max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right| \quad (1)$$

Where T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3. The absolute worst case value between -40 °C and 125 °C is reported in the datasheet.

5.3 Unused channel

When one of the two channels of TSV771 and TSV772 are not used, it must be properly connected in order to avoid internal oscillations that can negatively impact the signal integrity on the other channel, as well as the current consumption. Two different configurations can be used:

Gain or buffer configuration: the channel can be set in gain, the input can be set to any voltage within the V_{icm} operating range.

Comparator configuration: the channel can be set to a comparator configuration (without negative feedback). In this case, positive and negative inputs can be set to any value provided these values are significantly different (100 mV or more, to avoid oscillation between positive and negative state and within operating range) and the differential input is lower than the maximum specified in the operating range.

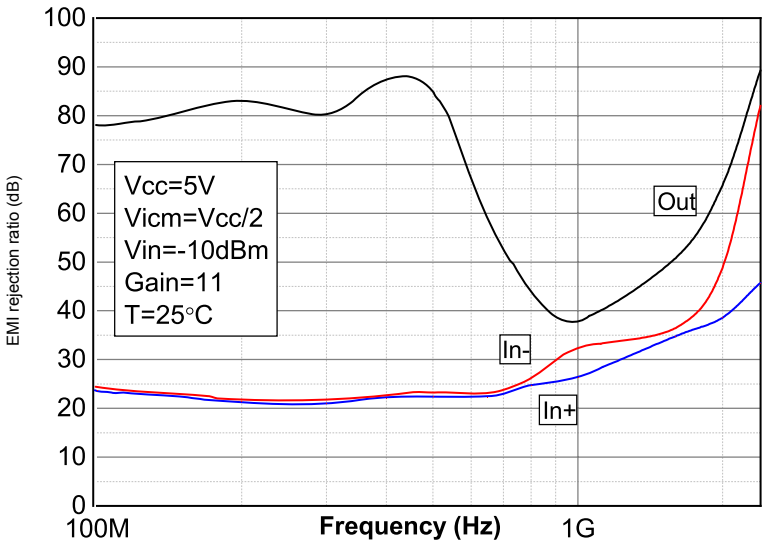
5.4 EMI rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined in Eq. (2):

$$EMIRR = 20 . log\left(\frac{V_{in\,pp}}{\Delta V_{io}}\right) \quad (2)$$

The TSV771 and TSV772 have been specially designed to minimize susceptibility to EMIRR and shows a low sensitivity. As can be seen in Figure 44. EMIRR on In+, In- and Out pins, EMI rejection ratio has been measured on both inputs and output, from 400 MHz to 2.4 GHz.

Figure 44. EMIRR on In+, In- and Out pins



EMIRR performances might be improved by adding small capacitances (in the pF range) on the inputs, power supply and output pins.

These capacitances help to minimize the impedance of these nodes at high frequencies.

5.5 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSV772 is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A \quad (3)$$

T_J is the die junction temperature

P_D is the power dissipated in the package

θ_{JA} is the junction-to-ambient thermal resistance of the package

T_A is the ambient temperature

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$P_D = (V_{CC} \times I_{CC}) + (V_{CC+} - V_{OUT}) \times ILoad$ when the op amp is sourcing the current.

$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times ILoad$ when the op amp is sinking the current.

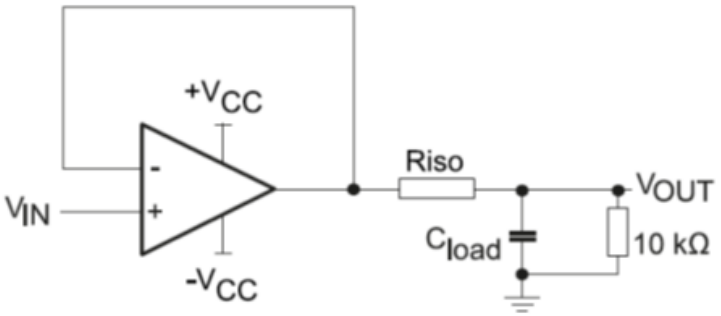
Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

5.6 Capacitive load and stability

Stability analysis must be performed for large capacitive loads over 47 pF; increasing the load capacitance to high values produces gain peaking in the frequency response, with overshoot and ringing in the step response.

Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads. For additional capacitive load drive capability in unity-gain configuration, stability can be improved by inserting a small resistor R_{ISO} (10 Ω to 33 Ω) in series with the output (see Figure 34. Small step overshoot vs. load capacitance). This resistor significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L. R_{ISO} modifies the maximum capacitive load acceptable from a stability point of view, as described in Figure 45. Test configuration for R_{ISO}:

Figure 45. Test configuration for R_{ISO}

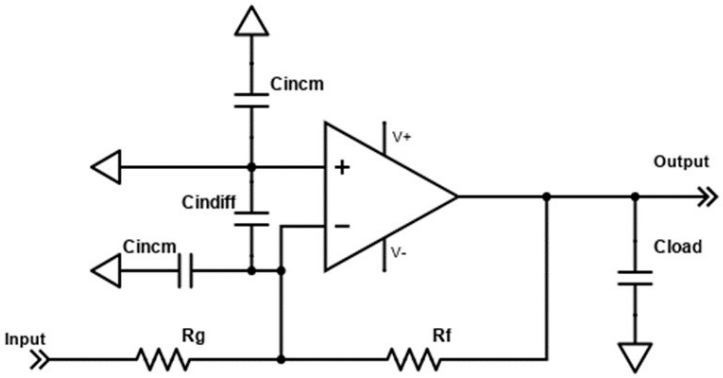


Please note that R_{ISO} = 33 Ω is sufficient to make the TSV771 and TSV772 stable whatever the capacitive load.

5.7 Resistor values for high speed op amp design

Due to its high gain bandwidth product (GBP), this op amp is particularly sensitive to parasitic impedances. Board parasitics should be taken into account in any sensitive design. Indeed, excessive parasitic (both capacitive and inductive) in the op amp frequency range can alter performances and stability. These issues can often be mitigated by lowering the resistive impedances. More specifically, the RC network created by the schematic resistors (Rf and Rg) and the parasitic capacitances of both the op amp (as documented in Table 1 to Table 5 and illustrated in Figure 46) and the PCB can generate a pole below or in the same order of magnitude than the closed-loop bandwidth of the circuit. In this case, the feedback circuit is not able to fully play its role at high frequency, and the application can be unstable. This issue can happen when the schematic gain is low (typically < 5), or the device is used in follower mode with a resistor in the feedback. In these cases, it is advised to use a low value feedback resistor (Rf), typically 1 kΩ.

Figure 46. Inverting amplifier configuration with parasitic input capacitances

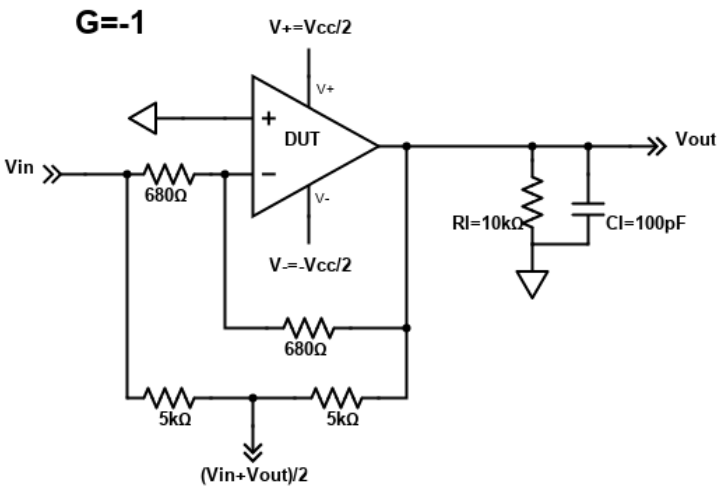


Also, some designs use an input resistor on the positive input, generally of the same value than the input resistance on the negative input. This resistor can be useful to balance the input currents on the positive and negative inputs, and reduce the impact of those input currents on precision. However, this is not useful on the TSV772 as the input currents are very low. Furthermore, this resistor can also interact with the input capacitances to generate a pole. The frequency of this pole should be kept higher than the closed-loop bandwidth frequency. The macromodel provided takes into account the circuit parasitic capacitors. Thus, a transient SPICE simulation (100 mV step) is an easy way to evaluate the stability of the application. However, this cannot replace a hardware evaluation of the application circuit.

5.8 Settling time

Settling time in an application can be defined as the amount of time between the input changes, and the output reaching its final value. It is usually defined with a given tolerance, so the output stability is reached when the output stays within the given range around the final value. In Figure 30 and Figure 31, the settling time is measured in an inverting configuration, using the so-called “false summing node” circuit.

Figure 47. Settling time measurement configuration



This circuit is used with a step input voltage from a positive or negative value, to 0 V. The measurement point being (V_{in} + V_{out}) / 2, and V_{out} being in an ideal circuit equal to V_{in}; the measurement point gives half of the error on V_{out}, comparatively to V_{in}. This error is compared to the tolerance, 0.1% for this circuit, to deduce the settling time. This characteristic is particularly useful when driving an ADC. It is related to the slew rate, GBP and stability of the circuit. It also varies with the circuit gain, the circuit load, and the input voltage step value. However, computing the value of the settling time in a given configuration is not straightforward. The macromodel can give a good estimation, but prototyping can be needed for fine circuit optimization.

5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimizing parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.10 Decoupling capacitor

In order to ensure op amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op amp supply pins. A good decoupling helps to reduce electromagnetic interference impact.

5.11 Macro model

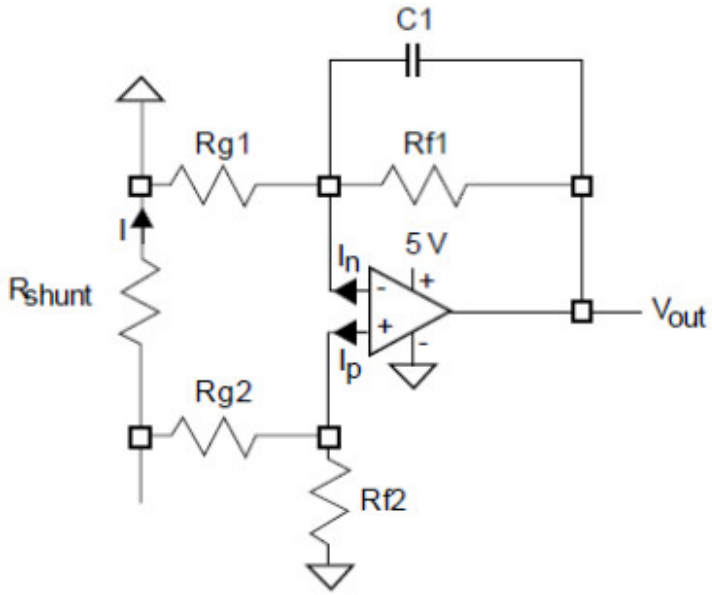
Accurate macromodels of the TSV771 and TSV772 devices are available on the STMicroelectronics' website at: www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSV771 and TSV772 operational amplifiers. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace on-board measurements.

6 Typical applications

6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSV771 and TSV772 (see Figure 48. Low-side current sensing schematic).

Figure 48. Low-side current sensing schematic



V_{out} can be expressed as follows:

$$V_{Out} = R_{shunt} \cdot I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right) \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p \cdot \frac{R_{g2} \cdot R_{f2}}{R_{g2} + R_{f2}} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \cdot R_{f1} - V_{io} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) \quad (4)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, this equation can be simplified as follows:

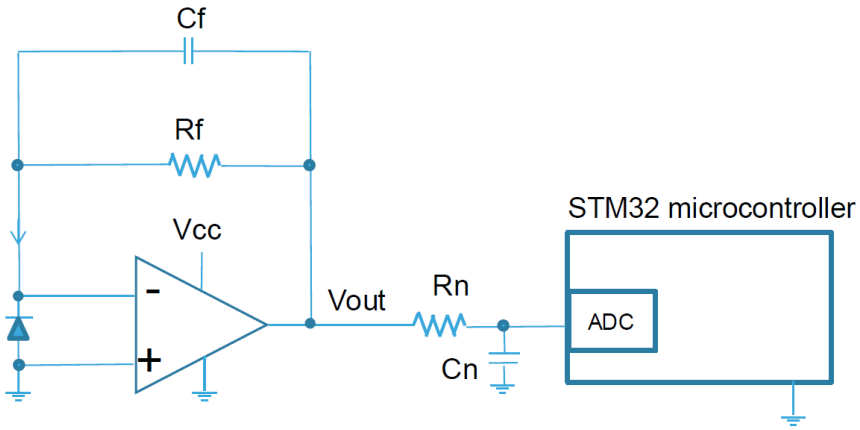
$$V_{Out} = R_{shunt} \cdot I \cdot \frac{R_f}{R_g} - V_{io} \cdot \left(1 + \frac{R_f}{R_g}\right) + R_f \cdot I_{io} \quad (5)$$

The main advantage of using the TSV771 and TSV772 for a low-side current sensing relies on its low V_{io}, compared to general purpose operational amplifiers. For the same current and targeted accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost. Particular attention must be paid to the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

6.2 Photodiode transimpedance amplification

The TSV7722, with high bandwidth and slew rate, is well suited for photodiode signal conditioning in a transimpedance amplifier circuit. This application is useful in high performance UV sensors, smoke detectors or particle sensors.

Figure 49. Photodiode transimpedance amplifier circuit



The transimpedance amplifier circuit converts the small photodiode output current in the nA range, into a voltage signal readable by an ADC following Eq. (6):

$$V_{out} = R_f \cdot I_{photodiode} \quad (6)$$

The feedback resistance is usually in the MΩ range, in order to get a large enough voltage output range. However, together with the diode parasitic capacitance, the op amp input capacitances and the PCB stray capacitance, this feedback network creates a pole that makes the circuit oscillate. Using a small (few pF) capacitor in parallel with the feedback resistor is mandatory to stabilize the circuit. The value of this capacitor can be tuned to optimize the application settling time with a SPICE simulation using the op amp macromodel, or by prototyping.

For more details on tuning this circuit, please read the application note AN4451.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SOT23-5 package information

Figure 50. SOT23-5 package outline

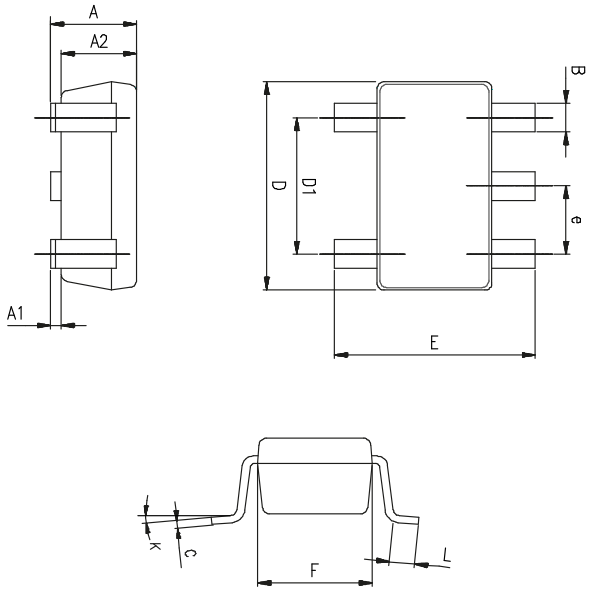


Table 8. SOT23-5 mechanical data

Dimensions						
Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0°		10°	0°		10°

7.2 DFN8 2x2 package information

Figure 51. **DFN8 2x2 package outline**

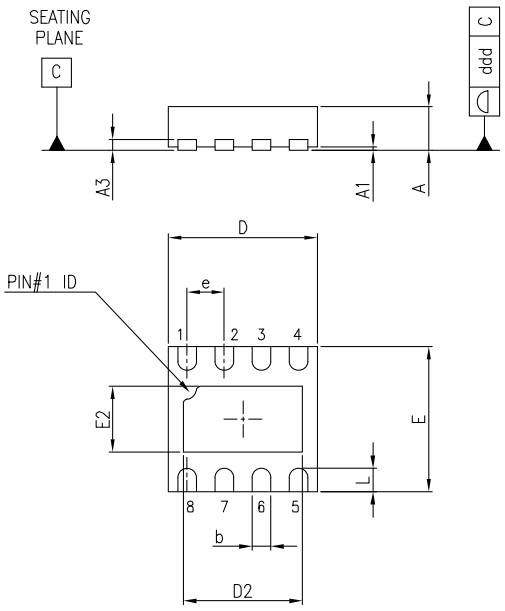
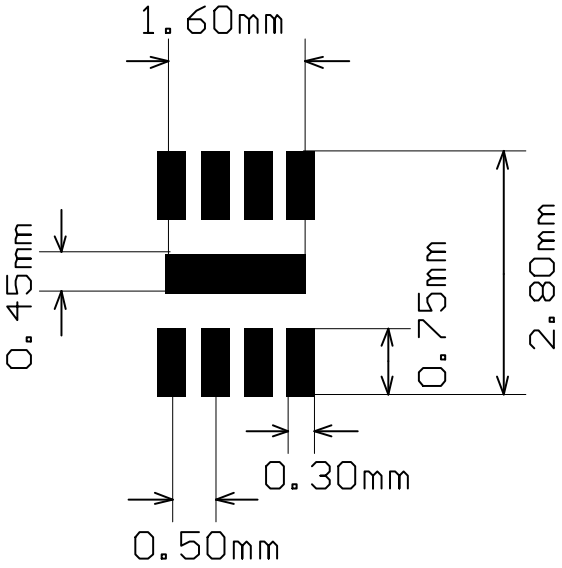


Table 9. **DFN8 2x2 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

Figure 52. **DFN8 2x2 recommended footprint**



7.3 SO8 package information

Figure 53. **SO8 package outline**

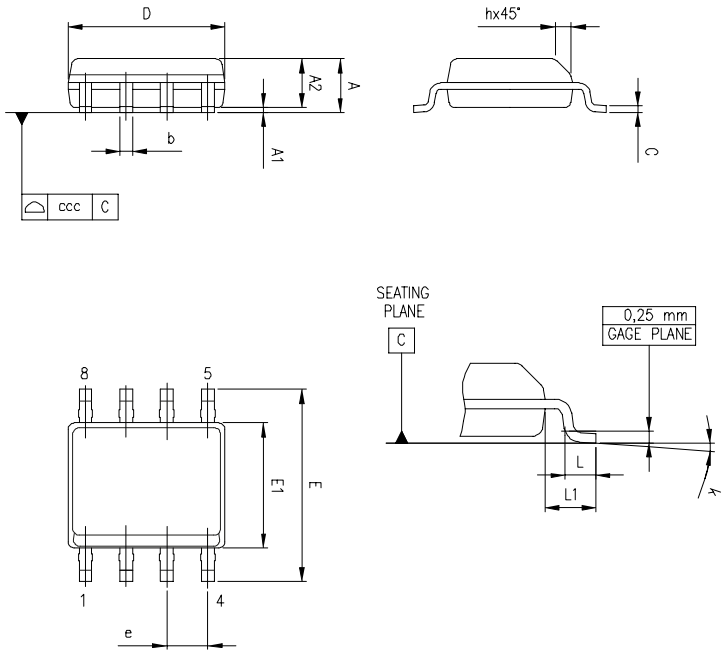


Table 10. **SO-8 mechanical data**

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

8 Ordering information

Table 11. Order code

Order code	Temperature range	Package	Marking
TSV771ILT	-40 to +125 °C	SOT23-5	K236
TSV772IQ2T		DFN8 2x2	K5R
TSV772IST		MiniSO8	K5R
TSV772IDT		SO8	TSV772I
TSV771IYLT	-40 to +125 °C Automotive grade(1)	SOT23-5	K237
TSV772IYST		MiniSO8	K231
TSV772IYDT		SO8	TSV772Y

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.*

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
12-Oct-2021	1	Initial release.
25-Nov-2021	2	Updated CDM value in Table 2 and Table 9. Order code.
15-Jun-2022	3	Added new part number TSV771, new SOT23-5 package, new Section 1.1 and new Section 7.1 . Updated Section 8 . Minor text changes.

Contents