CUI INC
a bel group

SERIES: VQA3S-S | DESCRIPTION: IGBT DRIVER DC-DC

FEATURES

- designed for SiC driver applications
- reinforced insulation
- CMTI > 200 kV/μs
- ultra-low isolation capacitance 3.5pF (typ.)
- -40 ~ 105°C temperature range
- continuous short circuit protection
- 5 kVac isolation test voltage
- UL/cUL 62368 certified

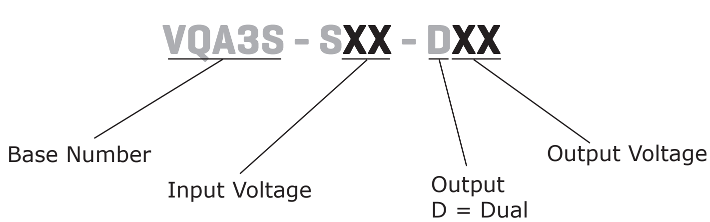
RoHS c UL US

MODEL

model	input voltage typ (Vdc)	input voltage range (Vdc)	output voltage (Vdc)	output current max (mA)	ripple and noise[1] max (mVp-p)	efficiency typ (%)
VQA3S-S5-D15-S	5	4.5~5.5	15 -5	80 -40	150	82
VQA3S-S5-D18-S	5	4.5~5.5	18 -3.5	80 -80	150	82
VQA3S-S5-D20-S	5	4.5~5.5	20 -4	80 -40	150	82
VQA3S-S12-D15-S	12	10.8~13.2	15 -2.5	100 -100	100	87
VQA3S-S12-DX15-S	12	10.8~13.2	15 -4	120 -120	100	87
VQA3S-S12-D18-S	12	10.8~13.2	18 -3	100 -100	100	87
VQA3S-S12-D20-S	12	10.8~13.2	20 -5	90 -90	100	87
VQA3S-S15-D15-S	15	13.5~16.5	15 -4	120 -120	100	87
VQA3S-S15-D20-S	15	13.5~16.5	20 -5	90 -90	100	87
VQA3S-S24-D15-S	24	21.6~26.4	15 -4	120 -120	100	82
VQA3S-S24-D20-S	24	21.6~26.4	20 -5	90 -90	100	81

Notes: 1. Ripple and noise are measured at 20 MHz BW by "parallel cable" method. See application notes.

PART NUMBER KEY



INPUT

parameter	conditions/description	min	typ	max	units
surge voltage[2]	5 Vdc input model 12 Vdc input model 15 Vdc input model 24 Vdc input model	-0.7 -0.7 -0.7 -0.7		9 18 21 30	Vdc Vdc Vdc Vdc
input filter	capacitance filter				

Note: 2. For 1 second maximum.

OUTPUT

parameter	conditions/description			min	typ	max	units
output voltage	VQA3S-S5-D15-S	+Vo -Vo	Pin6 & Pin7 +Io=80mA Pin5 & Pin6 -Io=-40mA	14.55 -4.45	15.3 -4.7	16.05 -4.95	Vdc Vdc
	VQA3S-S5-D18-S	+Vo -Vo	Pin6 & Pin7 +Io=80mA Pin5 & Pin6 +Io=-80mA	16.74 -3.13	17.64 -3.3	18.54 -3.67	Vdc Vdc
	VQA3S-S5-D20-S	+Vo -Vo	Pin6 & Pin7 +Io=80mA Pin5 & Pin6 -Io=-40mA	18.8 -3.8	19.8 -4	20.8 -4.2	Vdc Vdc
	VQA3S-S12-D15-S	+Vo -Vo	Pin6 & Pin7 +Io=100mA Pin5 & Pin6 -Io=-100mA	13.86 -2.28	14.61 -2.40	15.36 -2.53	Vdc Vdc
	VQA3S-S12-DX15-S	+Vo -Vo	Pin6 & Pin7 +Io=120mA Pin5 & Pin6 -Io=-120mA	14.25 -3.60	15.00 -3.80	15.75 -4.00	Vdc Vdc
	VQA3S-S12-D18-S	+Vo -Vo	Pin6 & Pin7 +Io=100mA Pin5 & Pin6 -Io=-100mA	17.10 -3.00	18.00 -3.15	18.90 -3.30	Vdc Vdc
	VQA3S-S12-D20-S	+Vo -Vo	Pin6 & Pin7 +Io=90mA Pin5 & Pin6 -Io=-90mA	18.50 -4.95	19.50 -5.20	20.50 -5.45	Vdc Vdc
	VQA3S-S15-D15-S	+Vo -Vo	Pin6 & Pin7 +Io=120mA Pin5 & Pin6 -Io=-120mA	13.76 -3.80	14.51 -4.00	15.26 -4.20	Vdc Vdc
	VQA3S-S15-D20-S	+Vo -Vo	Pin6 & Pin7 +Io=90mA Pin5 & Pin6 -Io=-90mA	18.50 -4.95	19.50 -5.20	20.50 -5.45	Vdc Vdc
	VQA3S-S24-D15-S	+Vo -Vo	Pin6 & Pin7 +Io=120mA Pin5 & Pin6 -Io=-120mA	14.55 -3.96	15.30 -4.16	16.05 -4.36	Vdc Vdc
	VQA3S-S24-D24-S	+Vo -Vo	Pin6 & Pin7 +Io=90mA Pin5 & Pin6 -Io=-90mA	19.00 -4.75	20.00 -5.00	21.00 -5.25	Vdc Vdc
capacitive load	5 Vdc input models	15 Vdc output 18 Vdc output 20 Vdc output				1,000 680 470	µF µF µF
	12 Vdc input models	15 Vdc output 18 Vdc output 20 Vdc output				2,200 1,000 470	µF µF µF
	15 Vdc input model	15 Vdc output 20 Vdc output				2,200 2,200	µF µF
	24 Vdc input models	15 Vdc output 20 Vdc output				2,200 2,200	µF µF
line regulation	5 Vdc input models all other inputs				1.1 1.1	1.4 1.5	% %
load regulation[3]	5 Vdc input models	+Vo output -Vo output			8 10	15 15	% %
	VQA3S-S12-D15-S	+Vo output -Vo output			8 13	17 17	% %
	all other inputs	+Vo output -Vo output			6 8	15 15	% %
temperature coefficient	at full load				±0.04	±0.1	%/°C
switching frequency	at full load, nominal input				200		kHz
CMTI	input to output			±200			kV/µs

Note: 3. At 10 ~ 100% load

PROTECTIONS

parameter	conditions/description	min	typ	max	units
short circuit protection	continuous, auto-recovery				

SAFETY AND COMPLIANCE

parameter	conditions/description	min	typ	max	units
isolation voltage	input to output for 1 minute, 1 mA max	5,600			Vdc
partial discharge	input to output according to IEC 61800-5-1	1,700			V
isolation resistance	input to output at 500 Vdc	1,000			MΩ
isolation capacitance	input to output, 100 kHz/0.1 V		3.5	5	pF
safety approvals	certified to 62368: UL/cUL designed to meet 62368: EN/IEC				
conducted emissions	5 Vdc input model: CISPR32/EN55032 CLASS B (see recommended circuit) other models: CISPR32/EN55032 CLASS A (see recommended circuit)				
radiated emissions	5 Vdc input model: CISPR32/EN55032 CLASS B (see recommended circuit) other models: CISPR32/EN55032 CLASS A (see recommended circuit)				
ESD	5 Vdc input models: IEC/EN 61000-4-2 Contact ±6kV, perf. Criteria B other models: IEC/EN 61000-4-2 Contact ±8kV, perf. Criteria B				
MTBF	as per MIL-HDBK-217F at 25°C	3,500,000			hours
RoHS	yes				

ENVIRONMENTAL

parameter	conditions/description	min	typ	max	units
operating temperature	see derating curve	-40		105	°C
storage temperature		-55		125	°C
storage humidity	non-condensing	5		95	%

SOLDERABILITY

parameter	conditions/description	min	typ	max	units
pin soldering temperature	1.5mm from case for 10 seconds			300	°C

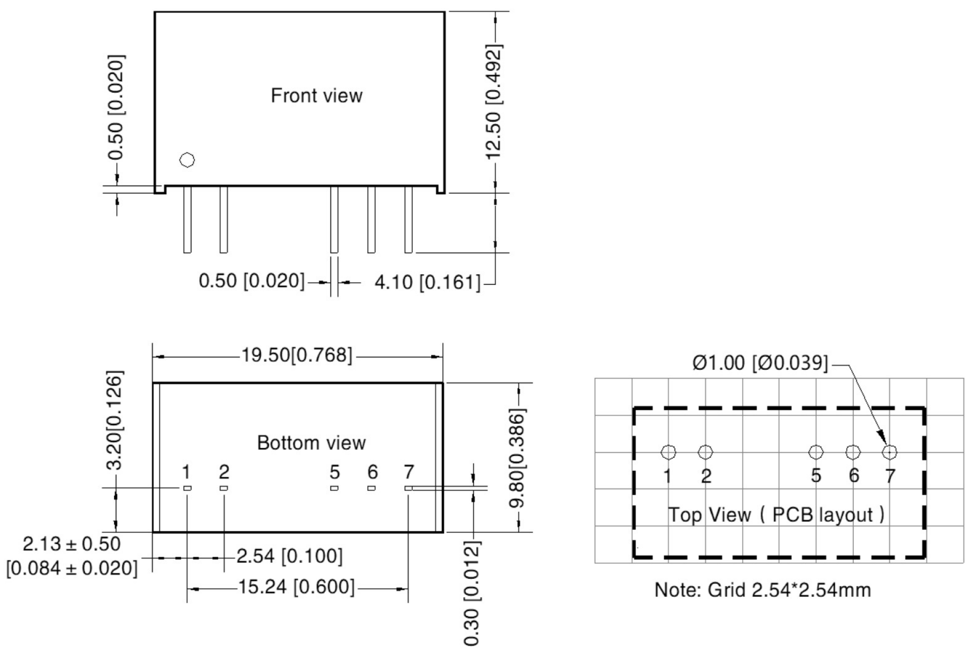
MECHANICAL

parameter	conditions/description	min	typ	max	units
dimensions	19.50 x 9.80 x 12.5 (0.768 x 0.386 x 0.492 inch)				mm
material	plastic, flame retardant and heat resistant				
weight			4.3		g
cooling method	natural convection				

MECHANICAL DRAWING

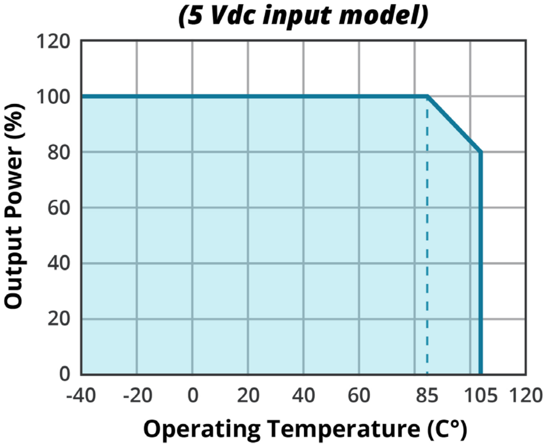
units: mm [inches]
tolerance: ±0.50 [±0.020]
pin section tolerance: ±0.10 [±0.004]

PIN CONNECTIONS	
PIN	FUNCTION
1	Vin
2	GND
5	-Vo
6	0V
7	+Vo

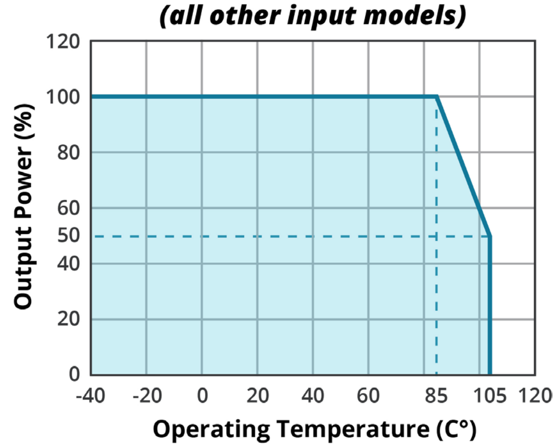


DERATING CURVES

TEMPERATURE DERATING CURVE (5 Vdc input model)

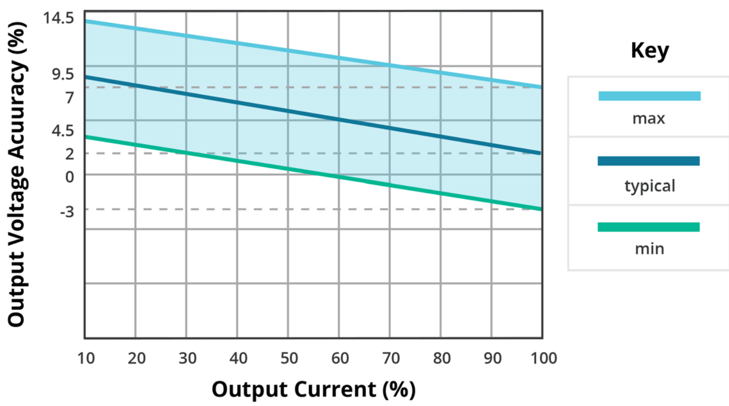


TEMPERATURE DERATING CURVE (all other input models)

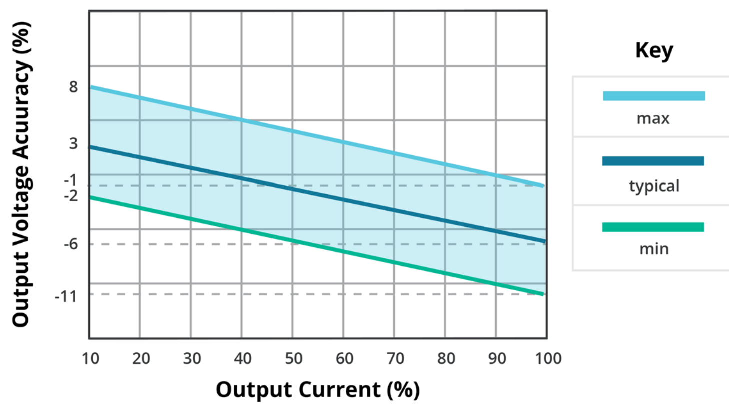


REGULATION CURVES

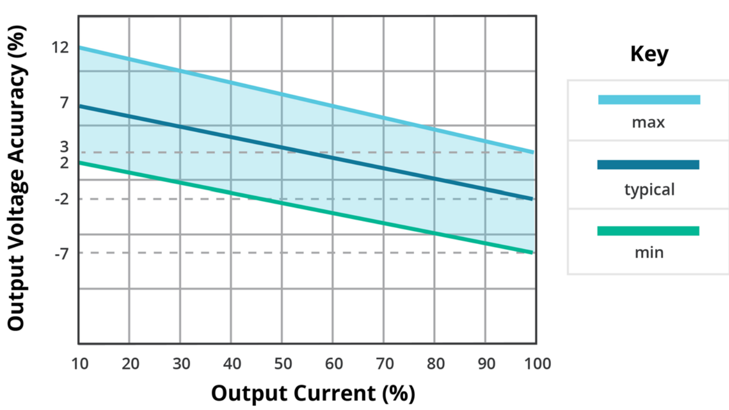
OUTPUT REGULATION CURVE
VQA3S-S5-D15-S
(+Vo)



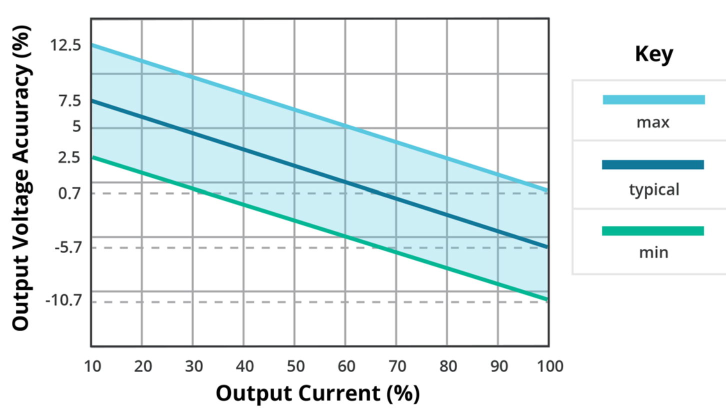
OUTPUT REGULATION CURVE
VQA3S-S5-D15-S
(-Vo)



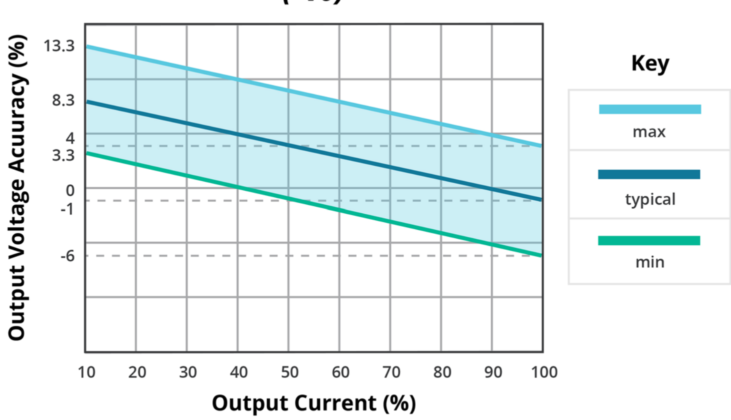
OUTPUT REGULATION CURVE
VQA3S-S5-D18-S
(+Vo)



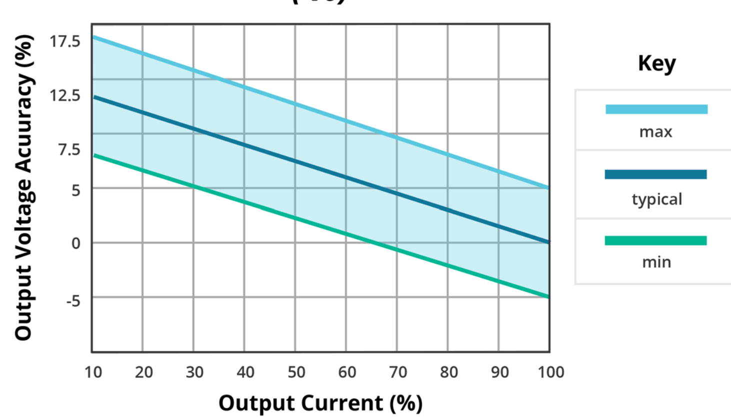
OUTPUT REGULATION CURVE
VQA3S-S5-D18-S
(-Vo)



OUTPUT REGULATION CURVE
VQA3S-S5-D20-S
(+Vo)

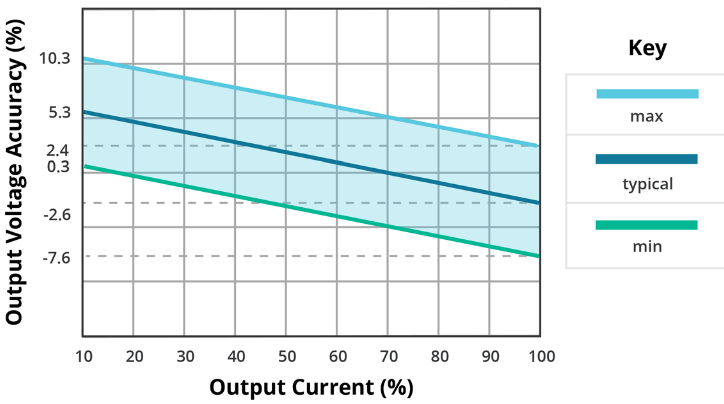


OUTPUT REGULATION CURVE
VQA3S-S5-D20-S
(-Vo)

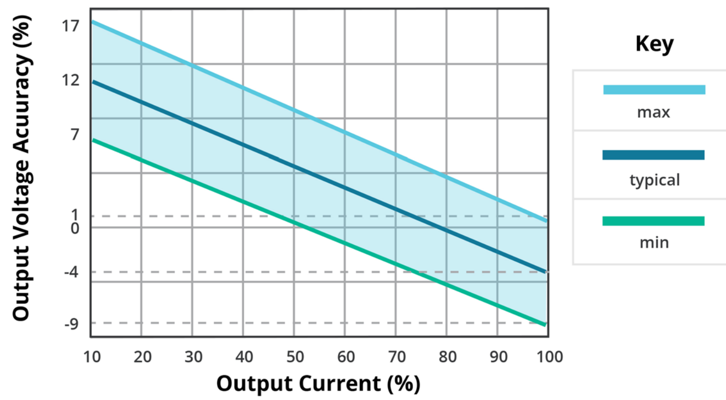


REGULATION CURVES (CONTINUED)

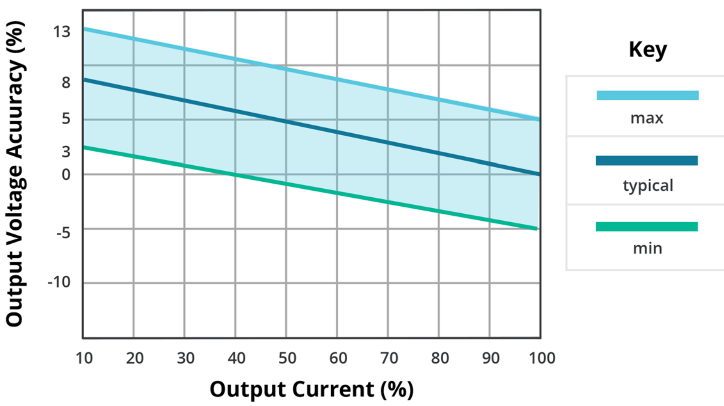
OUTPUT REGULATION CURVE
VQA3S-S12-D15-S
(+Vo)



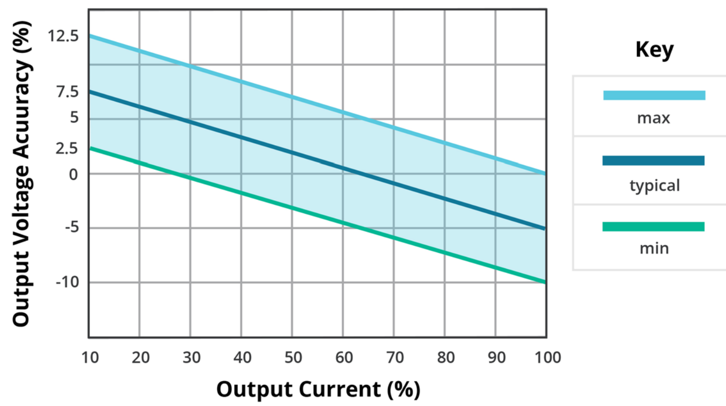
OUTPUT REGULATION CURVE
VQA3S-S12-D15-S
(-Vo)



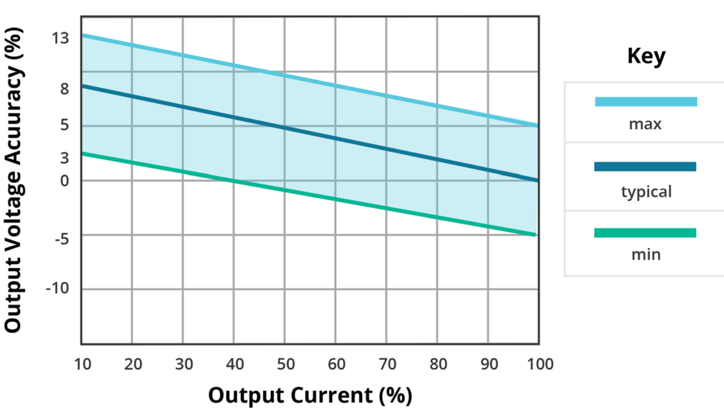
OUTPUT REGULATION CURVE
VQA3S-S12-DX15-S
(+Vo)



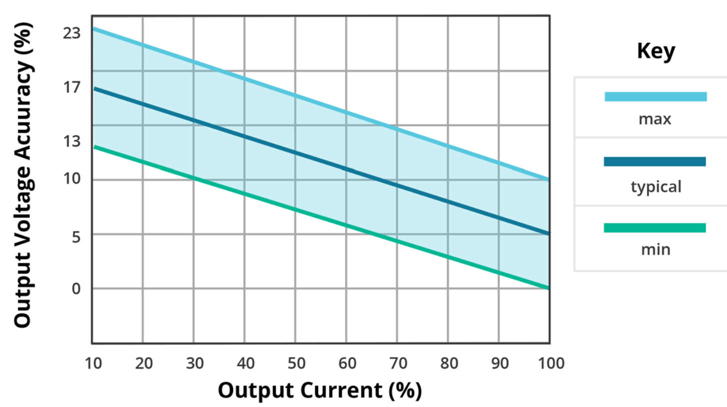
OUTPUT REGULATION CURVE
VQA3S-S12-DX15-S
(-Vo)



OUTPUT REGULATION CURVE
VQA3S-S12-D18-S
(+Vo)

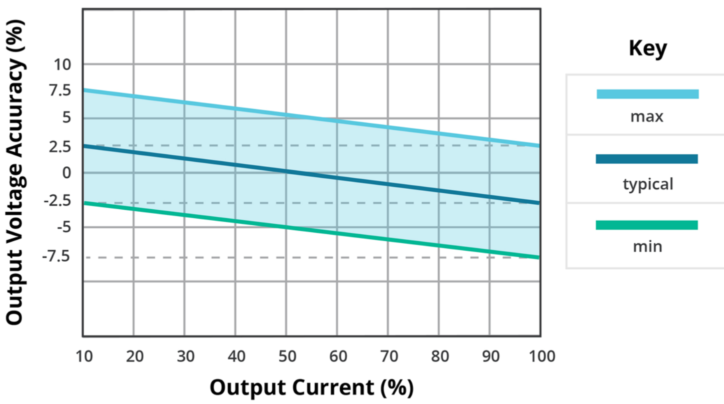


OUTPUT REGULATION CURVE
VQA3S-S12-D18-S
(-Vo)

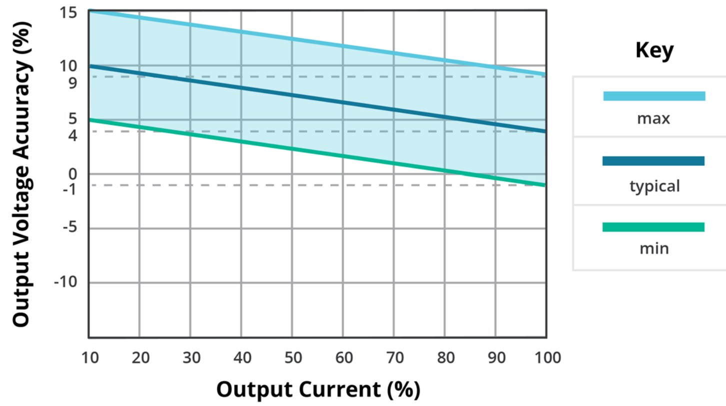


REGULATION CURVES (CONTINUED)

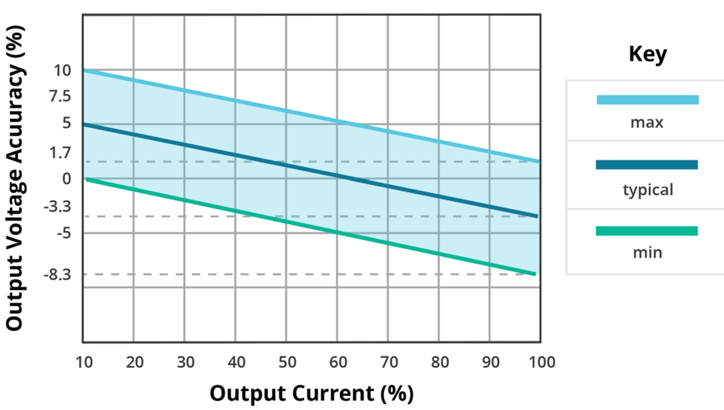
OUTPUT REGULATION CURVE
VQA3S-S12-D20-S
(+Vo)



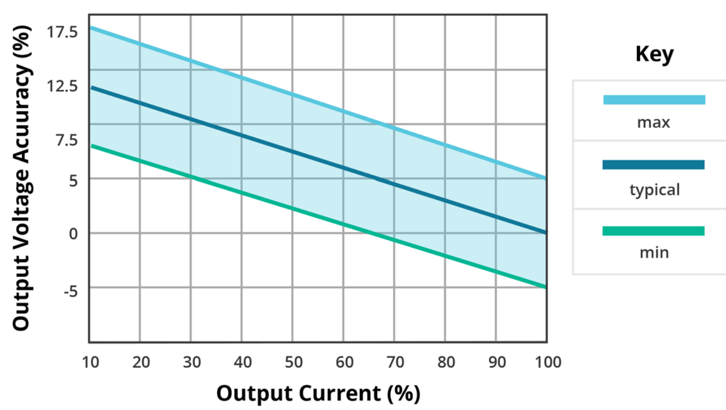
OUTPUT REGULATION CURVE
VQA3S-S12-D20-S
(-Vo)



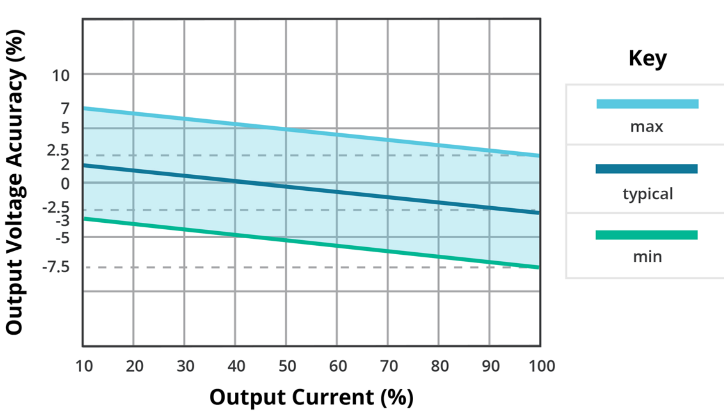
OUTPUT REGULATION CURVE
VQA3S-S15-D15-S
(+Vo)



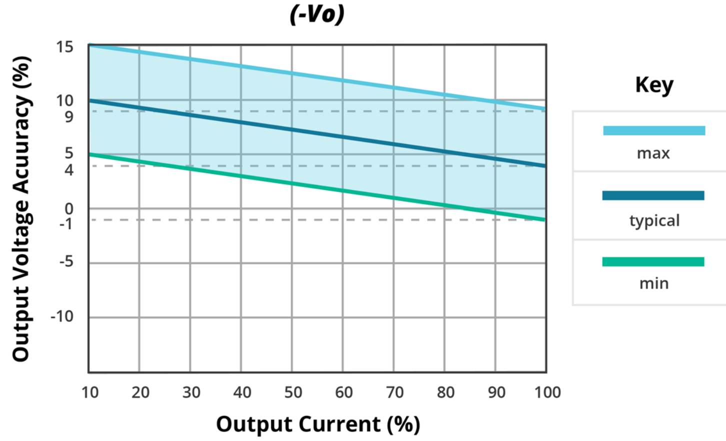
OUTPUT REGULATION CURVE
VQA3S-S15-D15-S
(-Vo)



OUTPUT REGULATION CURVE
VQA3S-S15-D20-S
(+Vo)

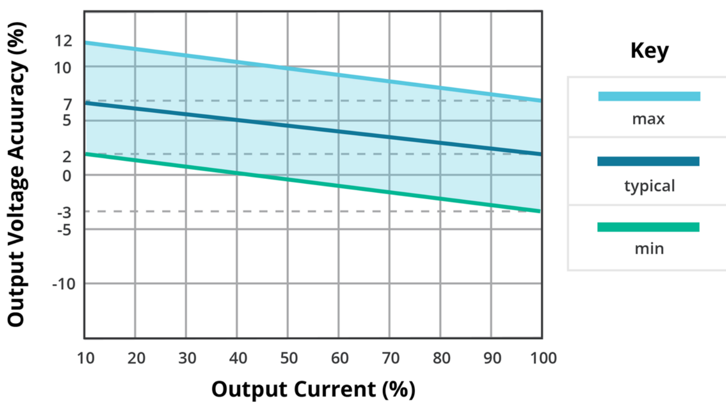


OUTPUT REGULATION CURVE
VQA3S-S15-D20-S
(-Vo)

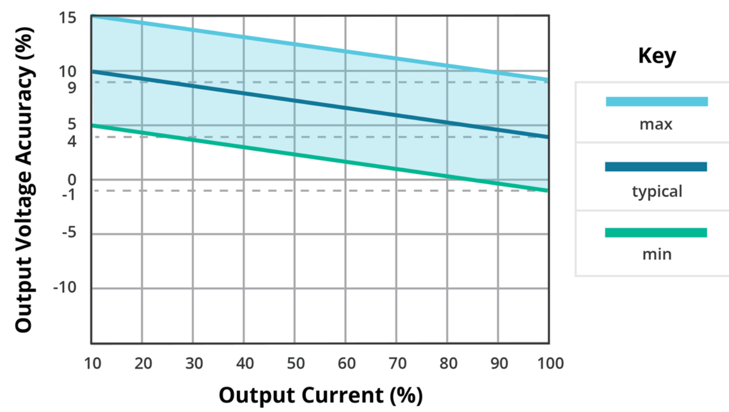


REGULATION CURVES (CONTINUED)

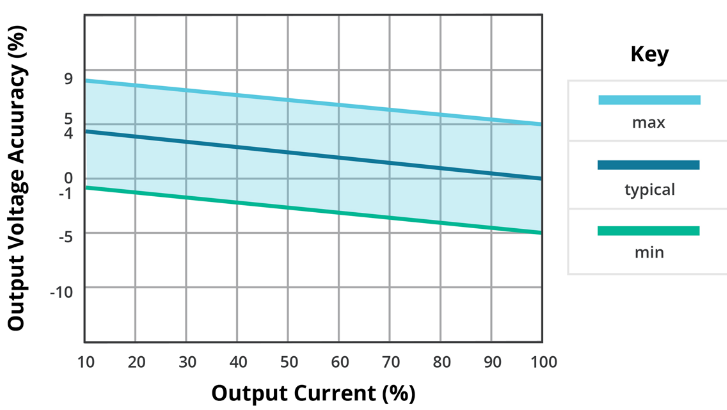
OUTPUT REGULATION CURVE
VQA3S-S24-D15-S
(+Vo)



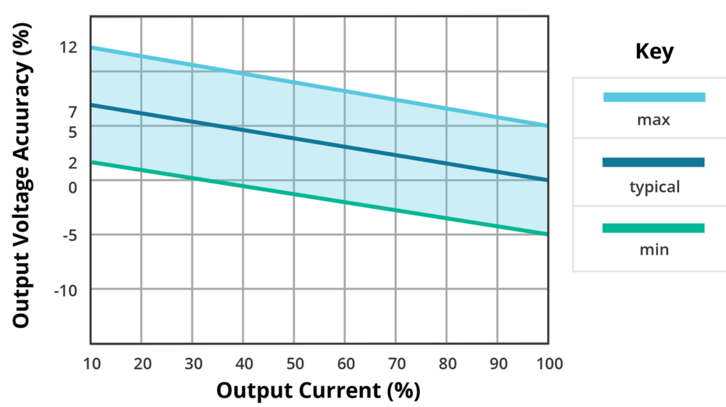
OUTPUT REGULATION CURVE
VQA3S-S24-D15-S
(-Vo)



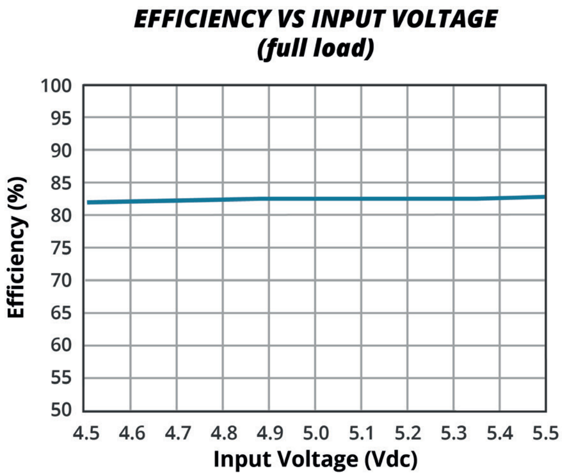
OUTPUT REGULATION CURVE
VQA3S-S24-D20-S
(+Vo)

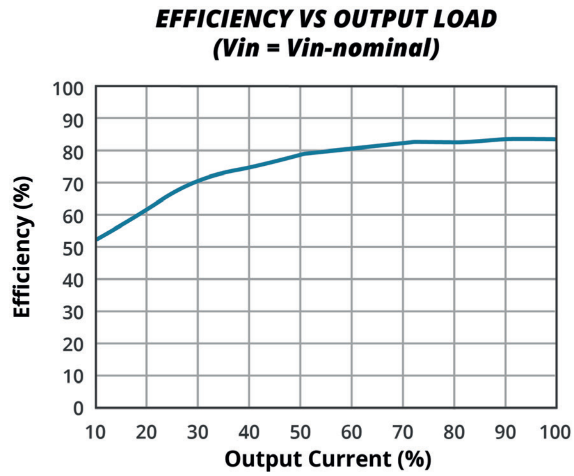


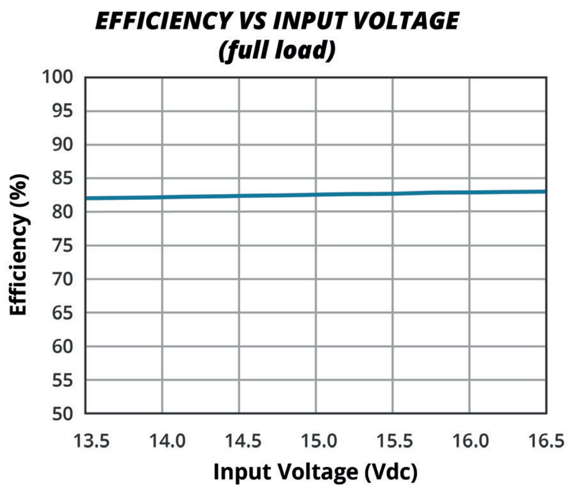
OUTPUT REGULATION CURVE
VQA3S-S24-D20-S
(-Vo)

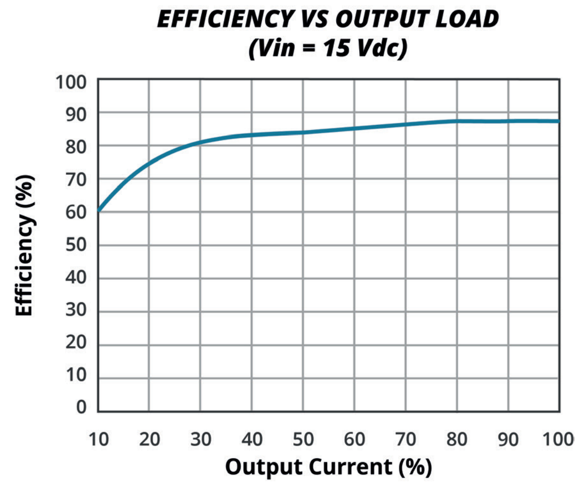


EFFICIENCY CURVES









EMC RECOMMENDED CIRCUIT

Figure 1

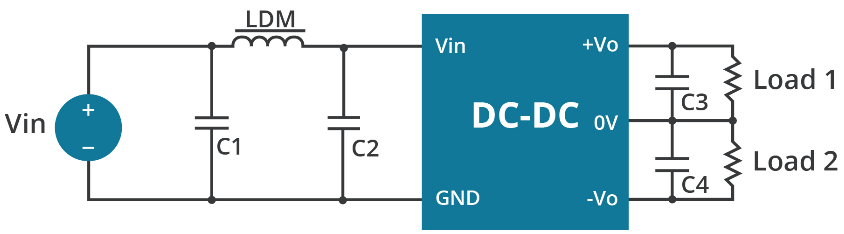


Table 1

Project		5V	12V, 15V, 24V
EMI	C1/C2	4.7µF/16V	1µF/50V
	C3/C4	10µF/50V (low resistance)	100µF/30V (low resistance)
	LDM	6.8µH	33µH

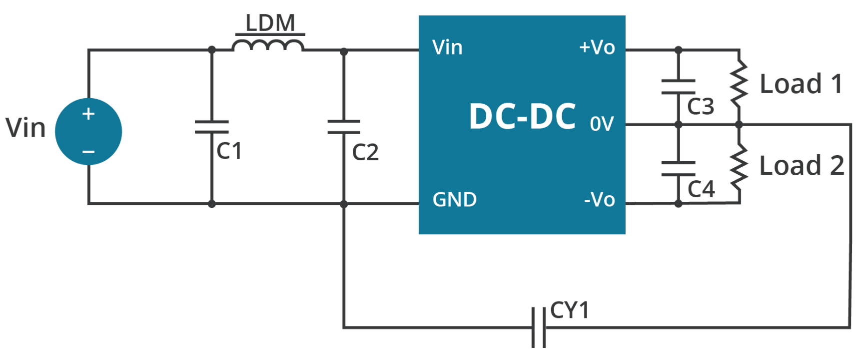
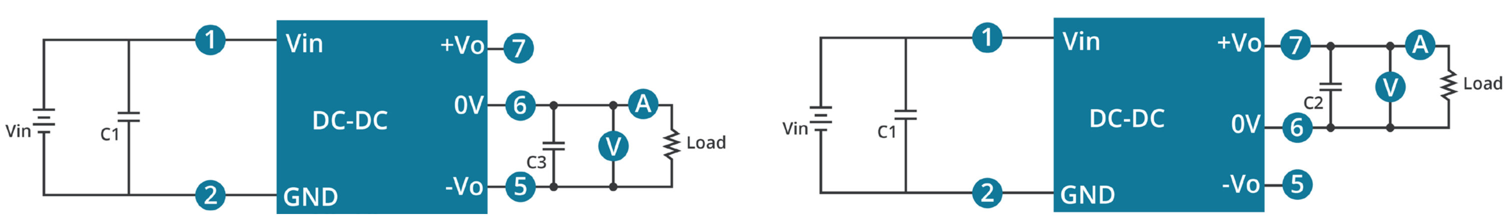


Table 2

Project		5V
EMI	C1/C2	4.7µF/16V
	C3/C4	10µF/50V (low resistance)
	LDM	6.8µH
	CY1	330pF

TEST CONFIGURATION

Figure 2



C1, C2, C3: 100 µF/35V (low internal resistance)

APPLICATION CIRCUIT

Figure 3

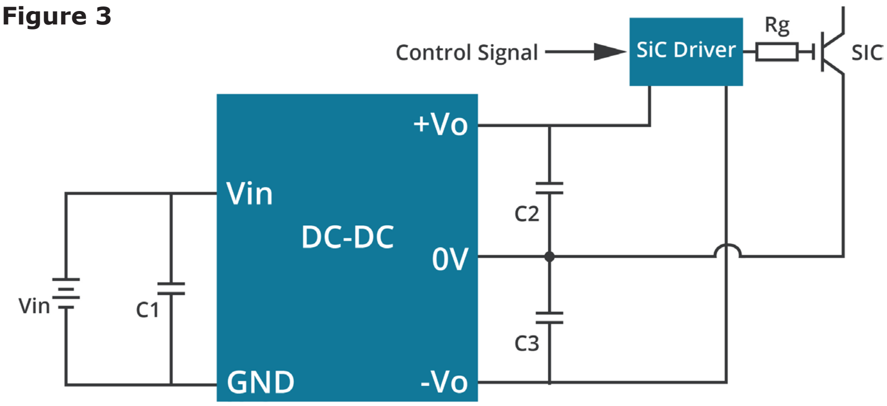


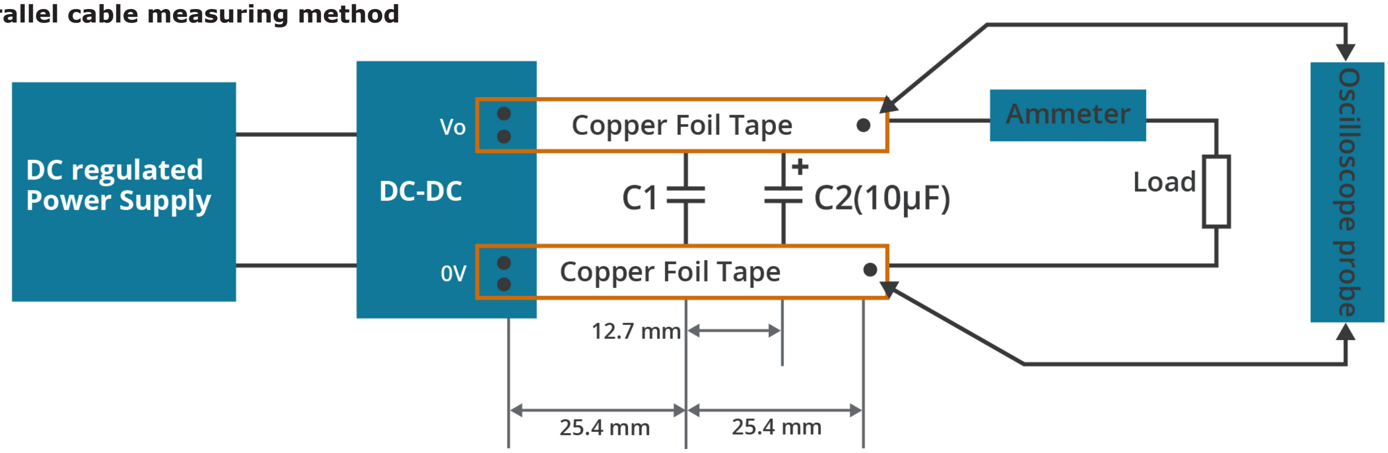
Table 3

C1/C2/C3
100µF/35V (low resistance)

MEASURING RIPPLE AND NOISE

Figure 4

Parallel cable measuring method



Notes:
a. C1: Ceramic capacitor with 1µF capacitance.
b. C2: Capacitor suitable for fixed input products. Please refer to datasheet. Normally 10µF is recommended.
c. Distance between two paralleled copper foils is 2.5mm of which the sum of voltage drops should be less than 2% of nominal voltage.

Notes:
1. The lead connecting the power supply module and SiC driver must as short as possible.
2. The output filtering capacitor should be connected as close as possible to the converter and the SiC driver.
3. The peak of the SiC driver gate drive current is high, so low internal resistance electrolytic capacitor is recommended to be used for the power supply module output filter capacitor.
4. The average output power of the driver must be lower than that of the power supply module.
5. The maximum capacitive load is tested at nominal input voltage and full load.
6. Consider fixing with glue near the module if being used in vibration occasion.
7. All specifications are measured at Ta=25°C, humidity <75%, nominal input voltage and rated output load unless otherwise specified.

REVISION HISTORY

rev.	description	date
1.0	initial release	10/11/2022

The revision history provided is for informational purposes only and is believed to be accurate.

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