

## MOSFET

### 950V CoolMOS™ PFD7 SJ Power Device

The latest 950V CoolMOS™ PFD7 series sets a new benchmark in the super junction (SJ) technologies. This technology is designed to address Lighting and Industrial SMPS applications by combining best-in-class performance with state-of-the-art ease of use. Compared to the CoolMOS™ P7 families, the PFD7 offers an integrated ultra-fast body diode enabling usage in resonant topologies with markets lowest reverse recovery charge (Q<sub>rr</sub>).

#### Features

- Integrated ultra-fast body diode
- Best-in-class reverse recovery charge Q<sub>rr</sub>
- Best-in-class FOM R<sub>DS(on)</sub> \* E<sub>oss</sub>, reduced Q<sub>g</sub>, C<sub>iss</sub>, and C<sub>oss</sub>
- Best-in-class V<sub>(GS)th</sub> of 3V and smallest V<sub>(GS)th</sub> variation of ±0.5V
- Integrated fast body diode
- Best-in-class CoolMOS™ quality and reliability
- Fully optimized portfolio
- Best-in-class R<sub>DS(on)</sub> in THD and SMD packages
- ESD protection min. Class 2 (HBM)

#### Benefits

- Excellent hard commutation robustness enabling usage in resonant topologies
- Extra safety margin for designs with increased bus voltage
- Enabling increased power density solutions
- Improved full load efficiency in industrial SMPS applications
- Price competitiveness over previous CoolMOS™ families
- Improved production yield by reducing ESD related failures

#### Potential applications

- Suitable for hard & soft switching topologies
- Optimized for usage in LLC and ZVS topologies
- PFC & LLC applications in Lighting and Industrial SMPS

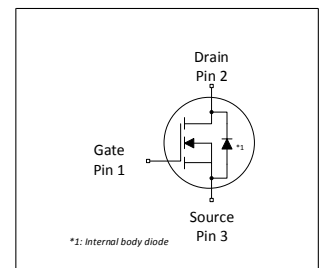
#### Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
V <sub>DS</sub> @ T <sub>j</sub> = 25 °C	950	V
R <sub>DS(on),max</sub>	310	mΩ
Q <sub>g,typ</sub>	61	nC
I <sub>D</sub>	8.7	A
E <sub>oss</sub> @ 500V	4.2	μJ
Body diode di <sub>F</sub> /dt	1300	A/μs
Q <sub>oss</sub> @ 500V	0.14	μC

Type / Ordering Code	Package	Marking	Related Links
IPA95R310PFD7	PG-TO220 FullPAK	95R310D7	see Appendix A



RoHS

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	8.7 5.6	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	62	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	42	mJ	$I_D=2.1\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.32	mJ	$I_D=2.1\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	2.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	31	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	$I_S$	-	-	6	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	62	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 6\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>F</sub> /dt	-	-	1300	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 6\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.50$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	4.00	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	950	-	-	V	$V_{GS}=0\text{V}$ , $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	2.5	3	3.5	V	$V_{DS}=V_{GS}$ , $I_D=0.52\text{mA}$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=950\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=25^\circ\text{C}$ $V_{DS}=950\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20\text{V}$ , $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.24	0.31	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=10.4\text{A}$ , $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$ , $I_D=10.4\text{A}$ , $T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	1	-	$\Omega$	$f=250\text{kHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1765	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Output capacitance	$C_{oss}$	-	23	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	39	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	391	-	pF	$I_D=\text{constant}$ , $V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=10.4\text{A}$ , $R_G=5.3\Omega$ ; see table 9
Rise time	$t_r$	-	10	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=10.4\text{A}$ , $R_G=5.3\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	61	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=10.4\text{A}$ , $R_G=5.3\Omega$ ; see table 9
Fall time	$t_f$	-	4	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=10.4\text{A}$ , $R_G=5.3\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	8	-	nC	$V_{DD}=760\text{V}$ , $I_D=10.4\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate to drain charge	$Q_{gd}$	-	19	-	nC	$V_{DD}=760\text{V}$ , $I_D=10.4\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate charge total	$Q_g$	-	61	-	nC	$V_{DD}=760\text{V}$ , $I_D=10.4\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=760\text{V}$ , $I_D=10.4\text{A}$ , $V_{GS}=0$ to $10\text{V}$

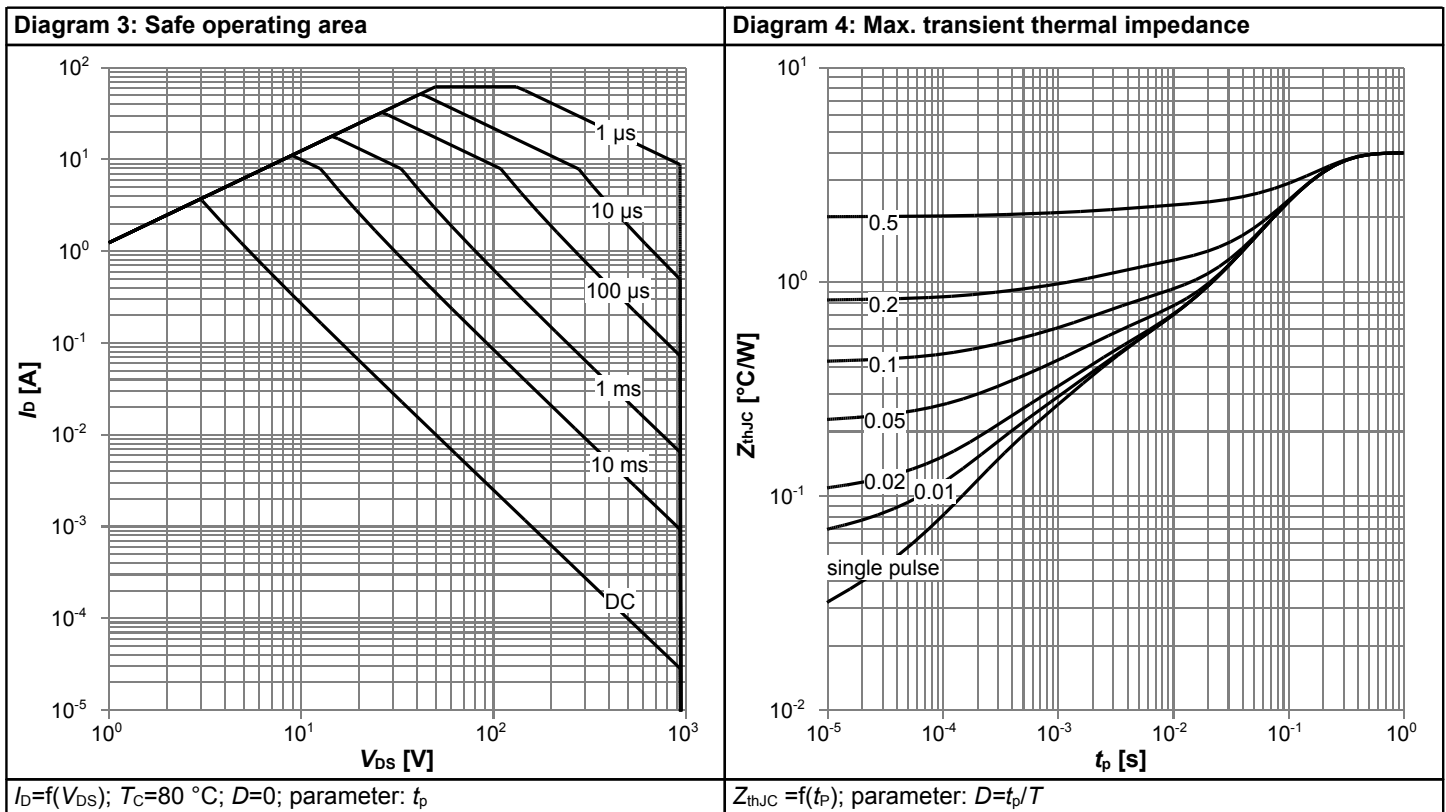
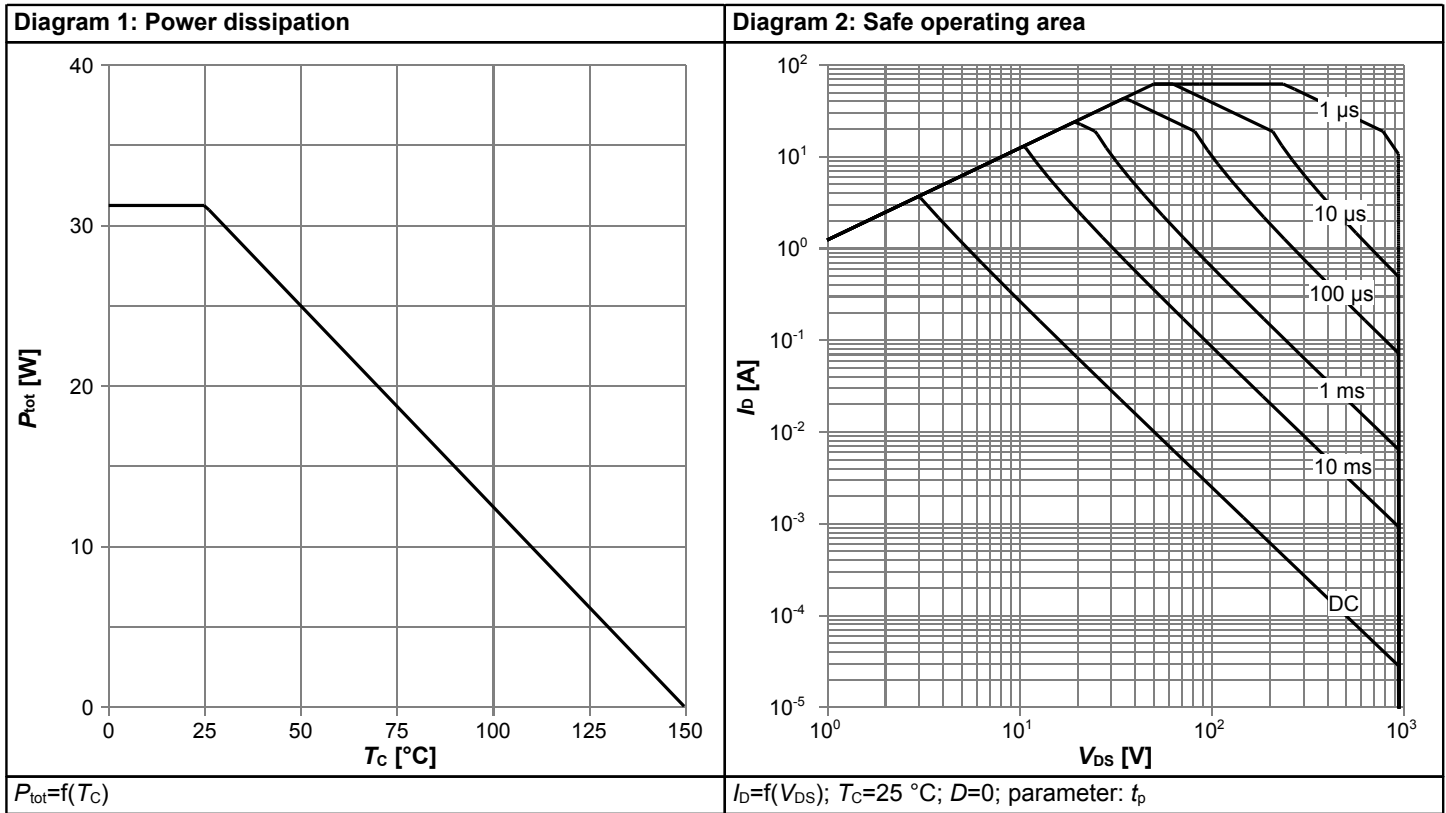
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

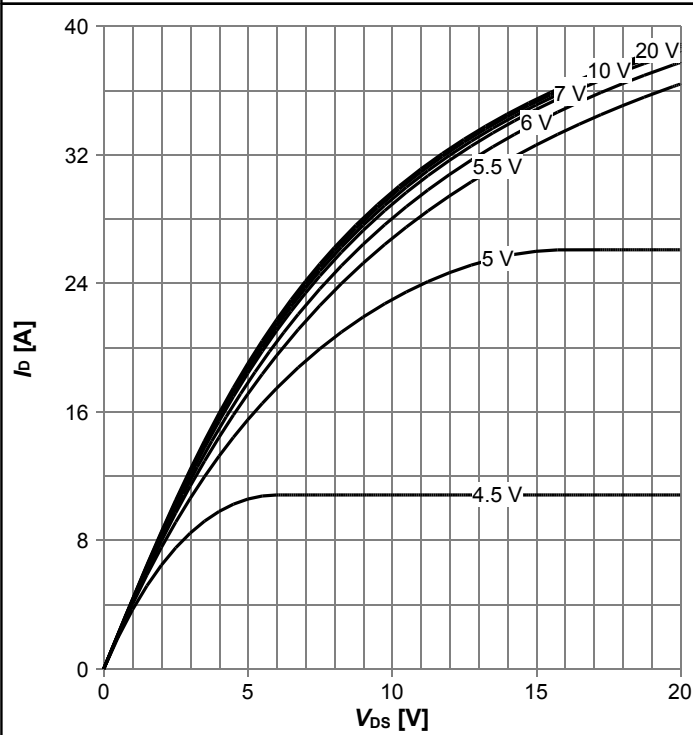
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1.1	-	V	$V_{GS}=0V, I_F=10.4A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	146	-	ns	$V_R=400V, I_F=10.4A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	0.78	-	$\mu C$	$V_R=400V, I_F=10.4A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	10.4	-	A	$V_R=400V, I_F=10.4A, di_F/dt=100A/\mu s$ ; see table 8

### 4 Electrical characteristics diagrams

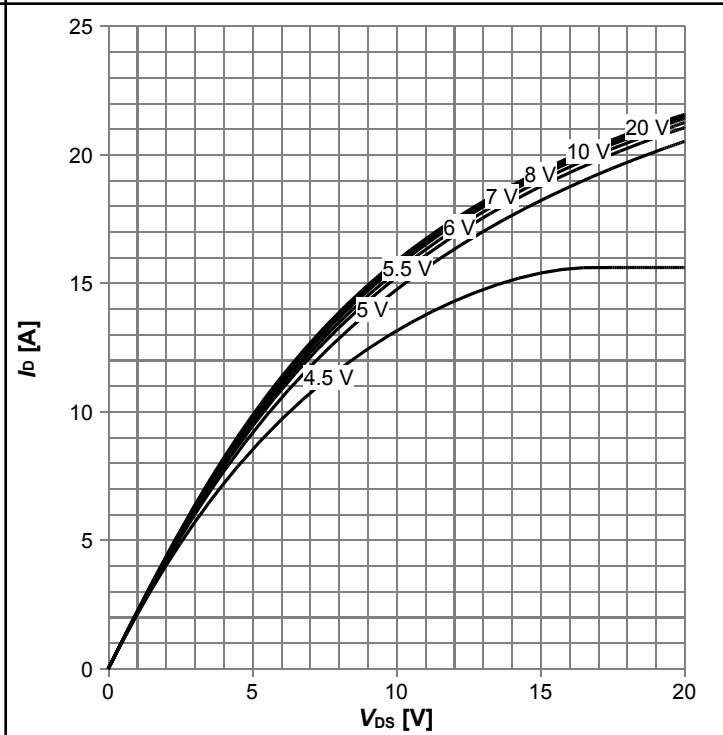


**Diagram 5: Typ. output characteristics**



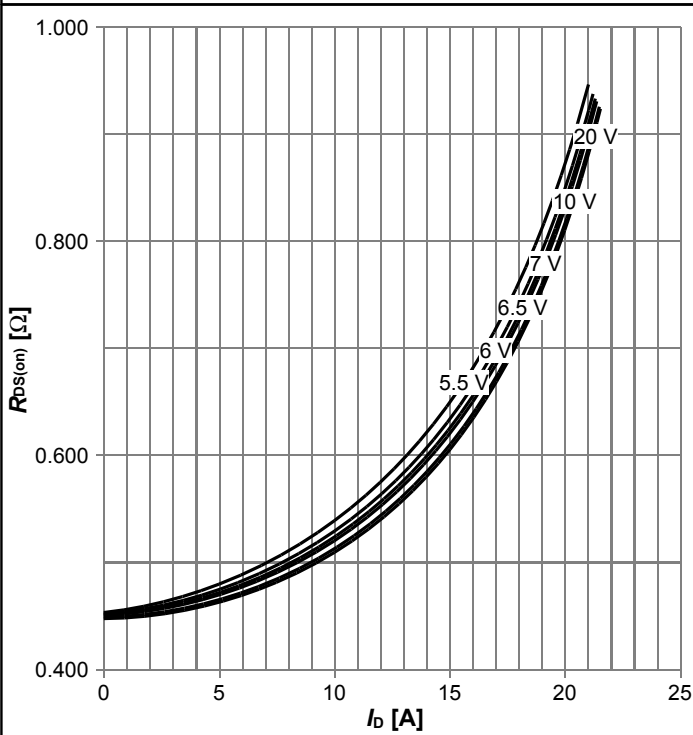
$I_D=f(V_{DS}); T_j=25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. output characteristics**



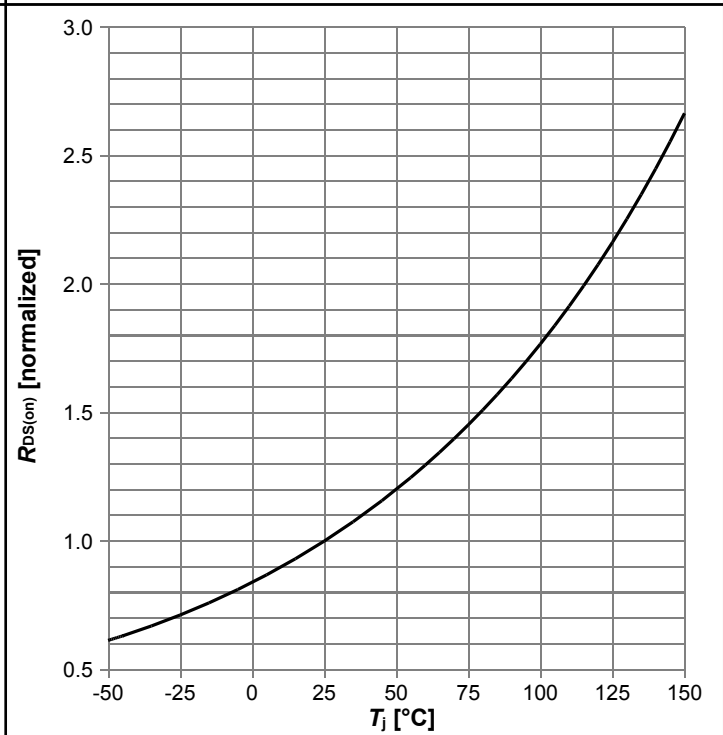
$I_D=f(V_{DS}); T_j=125\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**



$R_{DS(on)}=f(I_D); T_j=125\text{ °C};$  parameter:  $V_{GS}$

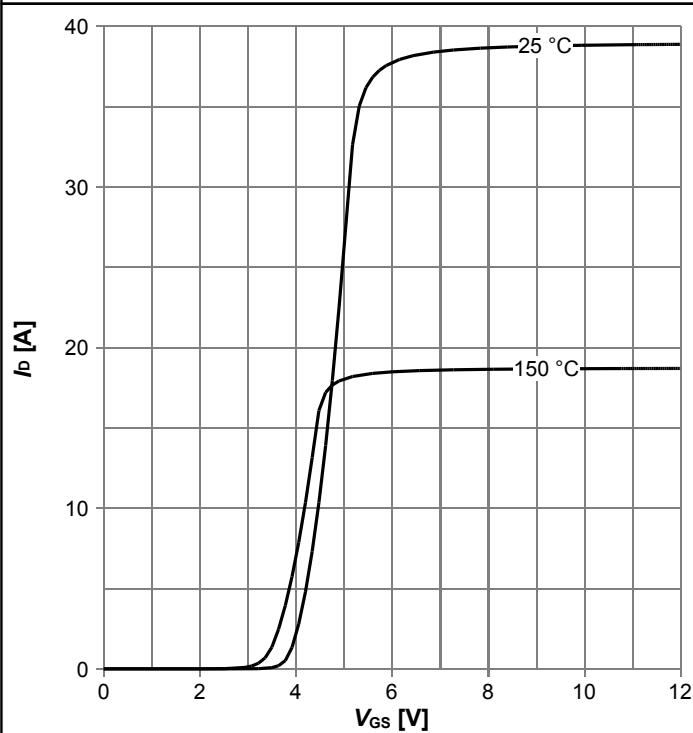
**Diagram 8: Drain-source on-state resistance**



$R_{DS(on)}=f(T_j); I_D=10.4\text{ A}; V_{GS}=10\text{ V}$

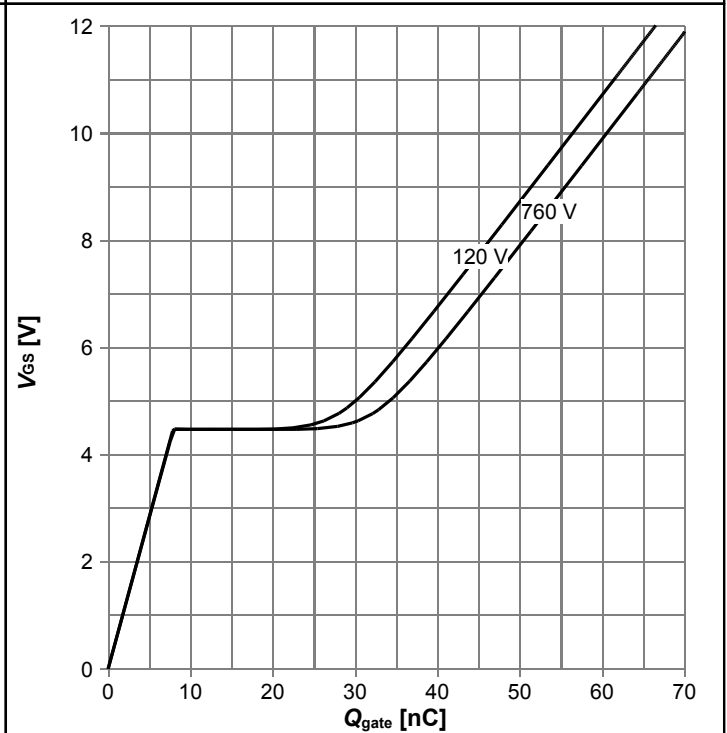


Diagram 9: Typ. transfer characteristics



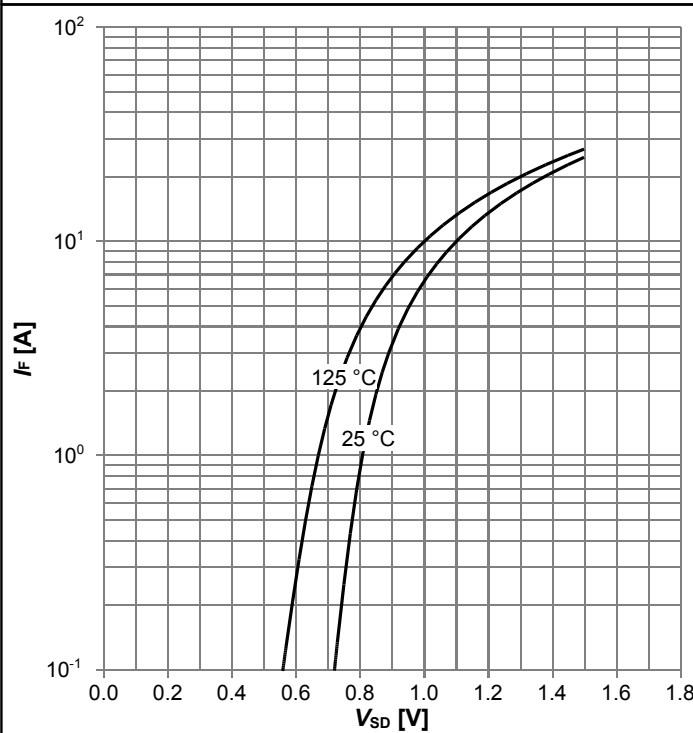
$I_D = f(V_{GS})$ ;  $V_{DS} = 20V$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



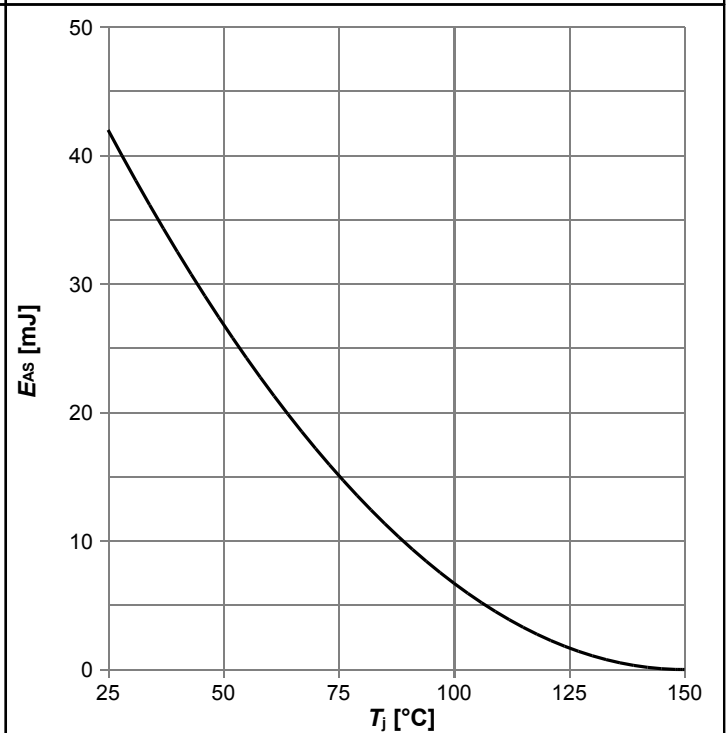
$V_{GS} = f(Q_{gate})$ ;  $I_D = 10.4$  A pulsed; parameter:  $V_{DD}$

Diagram 11: Forward characteristics of reverse diode



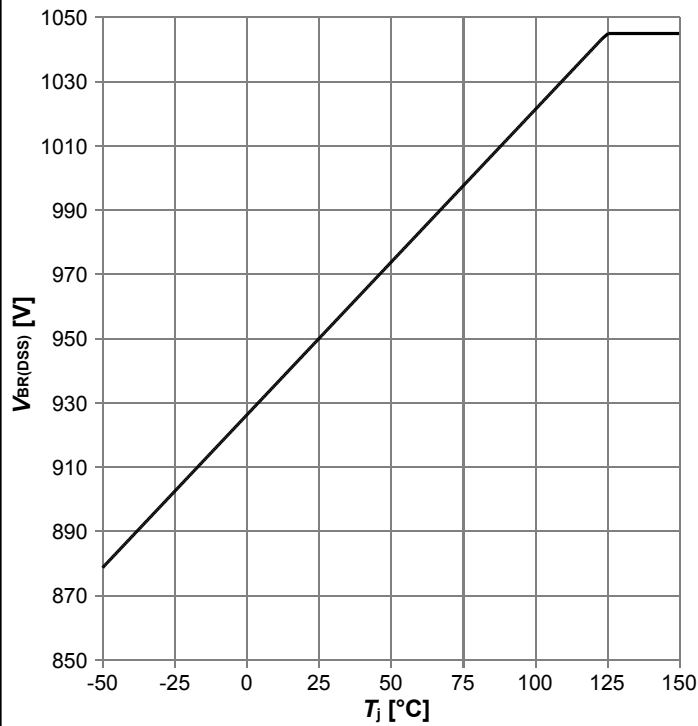
$I_F = f(V_{SD})$ ; parameter:  $T_j$

Diagram 12: Avalanche energy



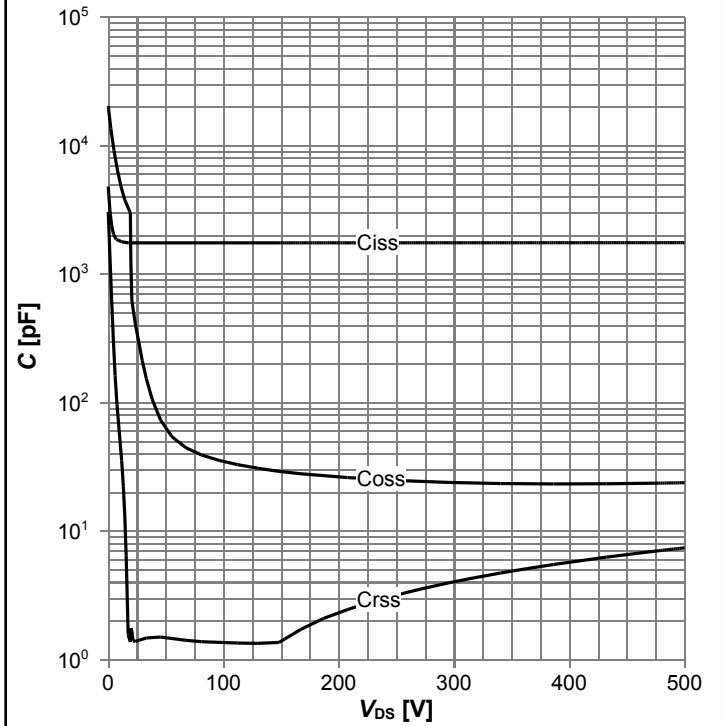
$E_{AS} = f(T_j)$ ;  $I_D = 2.1$  A;  $V_{DD} = 50$  V

**Diagram 13: Drain-source breakdown voltage**



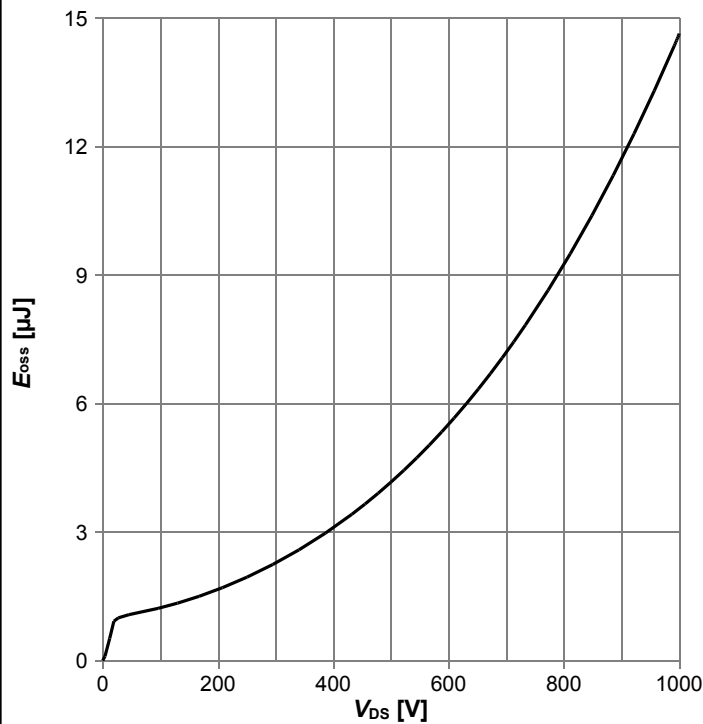
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

**Diagram 15: Typ. Coss stored energy**



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

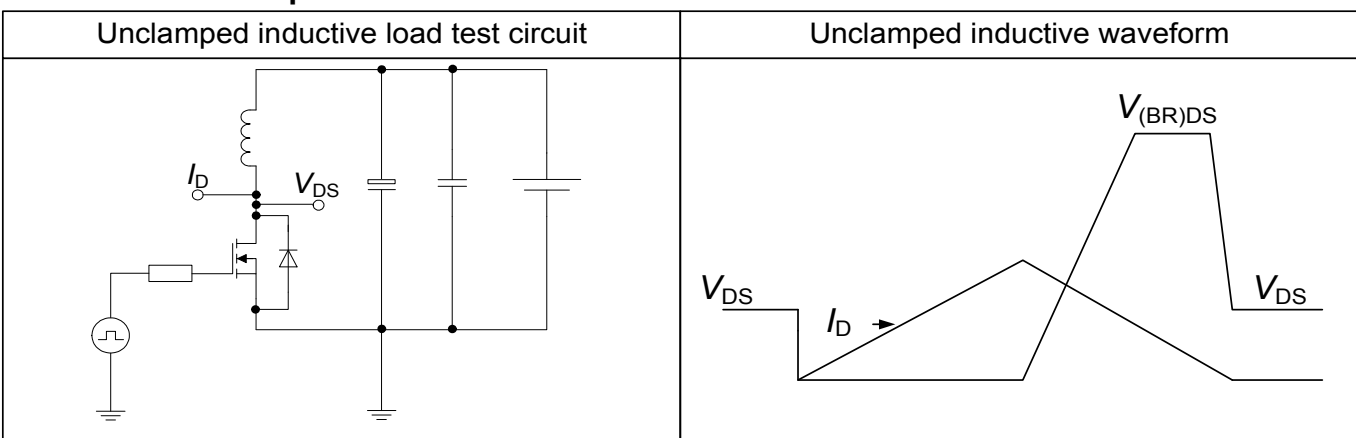
**Table 8 Diode characteristics**



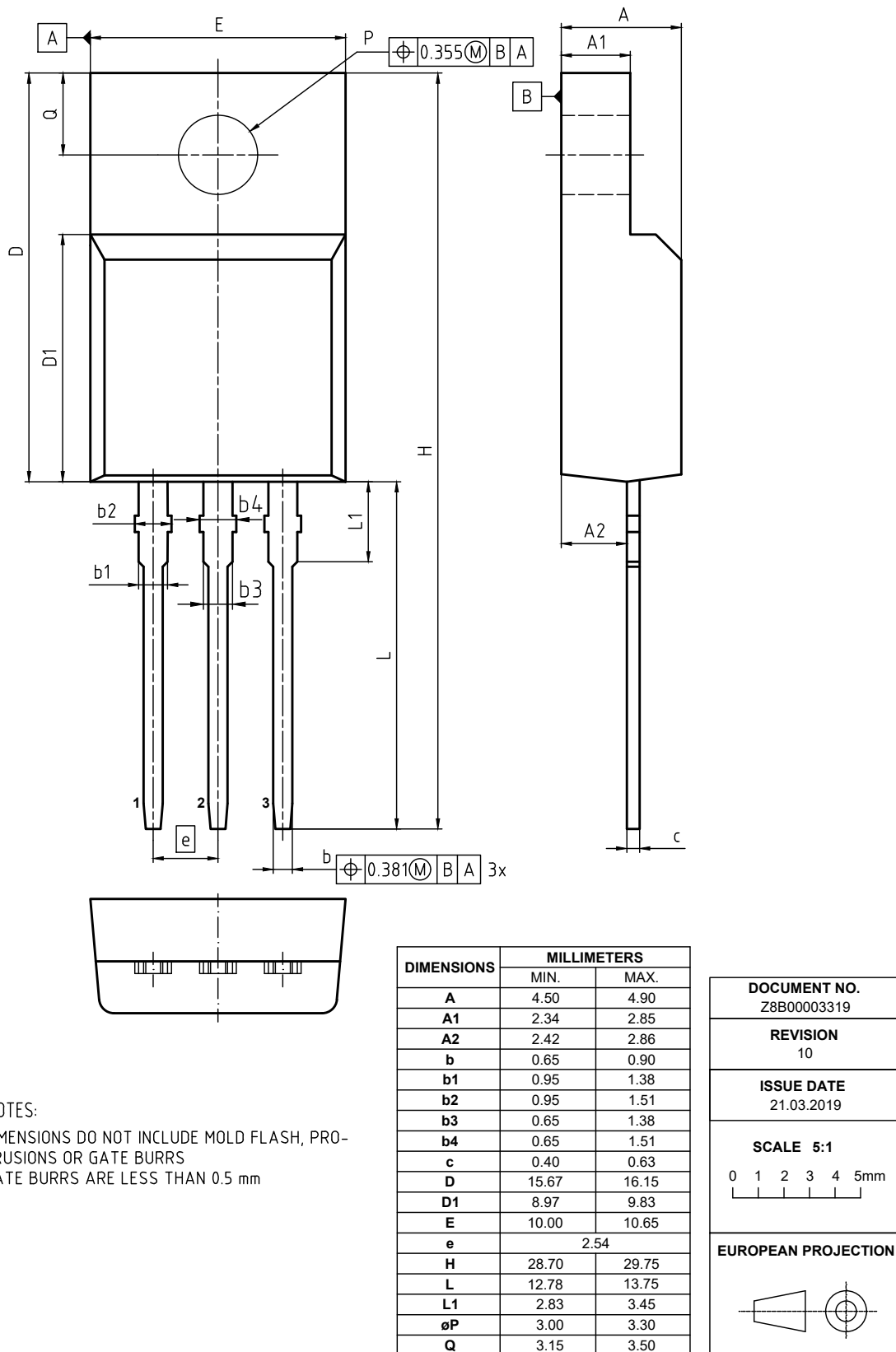
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



NOTES:  
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS  
GATE BURRS ARE LESS THAN 0.5 mm

Figure 1 Outline PG-TO220 FullPAK, dimensions in mm

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS PFD7 950V Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS PFD7 950V application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS PFD7 950V simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPA95R310PFD7

**Revision: 2022-04-22, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-03-18	Release of final version
2.1	2022-04-22	Modified features

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