

**Power Management IC Series for Mobile Phones**

# High-efficiency Power Management IC

## BH6053GU, BH6951GU, BH6952GU

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**●Description**

The High-Efficiency Power Management IC is considered to be the best power supply for CPU application. It integrates a step-down DC/DC converter and a multi channel LDO for portable devices. Each LDO can be controlled externally.

**●Features**

- 1) Fixed operation frequency (f=1.1MHz)
- 2) Low-current consumption at low load by using a LDO configured with a DC/DC converter
- 3) Includes soft start
- 4) Compact package
- 5) Includes over current limiter
- 6) Includes TSD (Thermal Shut Down)
- 7) Includes UVLO (Under Voltage Look Out)

**●Applications**

The device is suitable for use with all portable equipment, such as cellular phones, digital cameras, portable music players, portable video games and PDAs.

**● Product Lineup**

Parameter	BH6053GU	BH6951GU	BH6952GU
LDO ch number	5ch	-	2ch
DC/DC converter ch number	1ch	1ch	1ch
Package	VCSP85H3 (32pin) 3.54mm×3.54mm	VCSP85H2 (16pin) 2.60mm×2.60mm	VCSP85H3 (24pin) 3.06 mm×3.06mm

●Absolute maximum ratings

Parameter	Symbol	Limits	Unit
Maximum applied voltage	Vmax	7	V
Power dissipation	BH6053GU	1350 <sup>*1</sup>	mW
	BH6951GU	870 <sup>*2</sup>	
	BH6952GU	1210 <sup>*3</sup>	
Operating temperature range	Topr	-30 to 75	°C
Storage temperature range	Tstr	-55 to 125	°C

\*1 50mm×58mm×1.75mm At glass epoxy board mounting. Reduced by 13.5mW/°C when more than Ta=25°C.  
 \*2 50mm×58mm×1.75mm At glass epoxy board mounting. Reduced by 8.7mW/°C when more than Ta=25°C.  
 \*3 50mm×58mm×1.75mm At glass epoxy board mounting. Reduced by 12.1mW/°C when more than Ta=25°C.

●Recommended operating range

Parameter	Symbol	Limits	Unit	Condition
Power supply voltage	BH6053GU	3.0 ~ 4.5	V	REG1~5I, B ATP voltage
	BH6951GU			B ATP voltage
	BH6952GU			REG1~2I, B ATP voltage

●Electrical characteristics

[BH6053GU circuit current]

Unless otherwise specified Ta=25 °C, VCC=VBAT= REG1I= REG23I= REG4I = B ATP= REG5I=3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[Circuit current (No load)]						
Circuit current 1	ICC1	-	9.1	14.0	μA	CNT1,2,3,4,5 SWEN=0V (Operated only reference voltage source)
Circuit current 2	ICC2	-	4.2	5.7	mA	CNT1,2,3,4,5 =0V SWEN,MODE=2.8V
Circuit current 3	ICC3	-	25	42.4	μA	CNT1,2,3,4,5=0V SWEN =2.8V, MODE=0V
Circuit current 4	ICC4	-	82	145	μA	CNT1,2,5=2.8V, CNT3,4 =0V SWEN =2.8V, MODE=0V
Circuit current 5	ICC5	-	65	116	μA	CNT1,2,5=2.8V, CNT3,4=0V SWEN=0V, MODE=0V
Circuit current 6	ICC6	-	116	189	μA	CNT1,2,3,4,5=2.8V, SWEN=0V, MODE=0V

[BH6951GU circuit current]

Unless otherwise specified Ta=25 °C, VCC=VBAT= B ATP=3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[Circuit current (No load)]						
Circuit current 1	ICC1	-	8.1	12.8	μA	SWEN=0V (Operated only reference voltage source)
Circuit current 2	ICC2	-	4.2	5.8	mA	SWEN, MODE=2.8V
Circuit current 3	ICC3	-	24	42.5	μA	SWEN =2.8V, MODE=0V

[BH6952GU circuit current]

Unless otherwise specified Ta=25 °C, VCC=VBAT= REG1I= REG2I= B ATP=3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[Circuit current (No load)]						
Circuit current 1	ICC1	-	8.1	13.0	μA	CNT1, 2, SWEN=0V (Operated only reference voltage source)
Circuit current 2	ICC2	-	4.2	5.7	mA	CNT1, 2=0V SWEN, MODE=2.8V
Circuit current 3	ICC3	-	24	41.4	μA	CNT1, 2=0V SWEN =2.8V, MODE=0V
Circuit current 4	ICC4	-	54	91.8	μA	CNT1, 2=2.8V SWEN =2.8V, MODE=0V
Circuit current 5	ICC5	-	37	62.9	μA	CNT1, 2=2.8V SWEN=0V, MODE=0V

[DC/DC converter]

Unless otherwise specified Ta=25 °C, VCC=VBAT=3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
[DC/DC converter]							
1.5V Output voltage	DC/DC mode	Vosw1	1.450	1.500	1.550	V	Io=400mA, MODE=3.6V SWVSEL=0V
	REG_L mode	Voldo1	1.450	1.500	1.550	V	Io=50mA, MODE=0V SWVSEL=0V
1.2V Output voltage	DC/DC mode	Vosw2	1.150	1.200	1.250	V	Io=400mA, MODE=3.6V SWVSEL=3.6V
	REG_L mode	Voldo2	1.150	1.200	1.250	V	Io=50mA, MODE=0V SWVSEL=3.6V
Output current	DC/DC mode	Iosw	-	-	400	mA	
	REG_L mode	Ioldo	-	-	100	mA	
Efficiency	Eff	-	85	-	%	Io=100mA, Vo=1.5V	
		-	85	-	%	Io=200mA, Vo=1.5V	
Switching frequency	Fosc	0.78	1.05	1.35	MHz	DC/DC mode	

Inductor: D312C (TOKO, INC)

[REG1]

Unless otherwise specified Ta=25 °C, VCC=VBAT =3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[REG1]						
Circuit current	Iq	-	15	28	μA	Io=0mA
2.6V Output voltage	Vo1	2.544	2.600	2.656	V	Io=150mA, REG1VSEL=0V
2.85V Output voltage	Vo2	2.794	2.850	2.906	V	Io=150mA, REG1VSEL=3.6V
Output current	Io	200	-	-	mA	
I/O voltage difference	Vsat1	-	0.2	0.3	V	VBAT=2.6V, Io=150mA
I/O voltage difference	Vsat2	-	0.2	0.3	V	VBAT=2.85V, Io=150mA
Load stability	dVo1	-	24	70	mV	Io=1 ~ 150mA
Input stability	dVo2	-	3	30	mV	VBAT=3.1 ~ 4.5V, Io=150mA
Output voltage temperature coefficient	dVo3	-	±100	-	ppm/°C	Ta=-30 ~ 75 °C, Io=150mA
2.6V Ripple rejection ratio	RR260	50	60	-	dB	Io=150mA, VBAT=3.6V, *1
2.85V Ripple rejection ratio	RR280	50	60	-	dB	Io=150mA, VBAT=3.7V, *1
Current overload limiter	Iolim	-	150	-	mA	Fold back, Vo=0V
Output noise voltage	VNO	-	129	180	μVrms	BW=20 ~ 80kHz, Io=150mA

\*1 Input signal level : -14dBV, Input frequency : 1KHz, Measurement frequency band width : 20Hz to 80kHz

[REG2]

Unless otherwise specified Ta=25 °C, VCC= VBAT =3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[REG2]						
Circuit current	Iq	-	15	28	μA	Io=0mA
Output voltage	Vo	1.755	1.800	1.845	V	Io=120mA
Output current	Io	150	-	-	mA	
Load stability	dVo1	-	13	60	mV	Io=1 ~ 120mA
Input stability	dVo2	-	6	30	mV	VBAT=3.0 ~ 4.5V, Io=120mA
Output voltage temperature coefficient	dVo3	-	±100	-	ppm/°C	Ta=-30 ~ 75 °C, Io=120mA
Ripple rejection ratio	RR52	50	60	-	dB	Io=120mA, *1
Current overload limiter	Iolim	-	160	-	mA	Fold back, Vo=0V
Output noise voltage	VNO	-	119	160	μVrms	BW=20~80kHz, Io=120mA

\*1 Input signal level : -14dBV, Input frequency : 1KHz, Measurement frequency band width : 20Hz to 80kHz

[REG3]

Unless otherwise specified Ta=25 °C, VCC=VBAT =3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[REG3]						
Output voltage	Vo	3.240	3.300	3.360	V	Io=150mA
Output current	Io	150	-	-	mA	
I/O voltage difference	Vsat	-	0.2	0.3	V	VBAT=3.3V, Io=150mA
Load stability	dVo1	-	13	60	mV	Io=1~150mA
Input stability	dVo2	-	6	30	mV	VBAT=3.5~4.5V, Io=150mA
Output voltage temperature coefficient	dVo3	-	±100	-	ppm/°C	Ta=-30~75 °C, Io=150mA
Ripple rejection ratio	RR62	50	60	-	dB	Io=150mA, VBAT=4.2V, *1
Current overload limiter	Iolim	-	150	-	mA	Fold back, Vo=0V
Output noise voltage	VNO	-	123	160	μVrms	BW=20~80kHz, Io=150mA

\*1 Input signal level : -14dBV, Input frequency : 1KHz, Measurement frequency band width : 20Hz to 80kHz

[REG4]

Unless otherwise specified, Ta=25 °C, VCC=VBAT =3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[REG4]						
Circuit current	Iq	-	35	54	μA	Io=0mA
Output voltage	Vo	1.755	1.800	1.845	V	Io=50mA
Output current	Io	50	-	-	mA	
Load stability	dVo1	-	8	60	mV	Io=1~50mA
Input stability	dVo2	-	1	30	mV	VBAT=3.0~4.5V, Io=50mA
Output voltage temperature coefficient	dVo3	-	±100	-	ppm/°C	Ta=-30~75 °C, Io=50mA
Ripple rejection ratio	RR52	50	60	-	dB	Io=50mA, *1
Current overload limiter	Iolim	-	90	-	mA	Fold back, Vo=0V
Output noise voltage	VNO	-	110	190	μVrms	BW=20~80kHz, Io=50mA

\*1 Input signal level : -14dBV, Input frequency : 1KHz, Measurement frequency band width : 20Hz to 80kHz

[REG5]

Unless otherwise specified, Ta=25 °C, VCC=VBAT =3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[REG5]						
Circuit current	Iq	-	20	38	μA	Io=0mA
1.5V output voltage	Vo1	1.460	1.500	1.540	V	Io=30mA, SWVSEL=0V
1.2V output voltage	Vo2	1.160	1.200	1.240	V	Io=30mA, SWVSEL=3.6V
Output current	Io	50	-	-	mA	
Load stability	dVo1	-	8	60	mV	Io=1~30mA
Input stability	dVo2	-	1	30	mV	VBAT=3.0~4.5V, Io=30mA
Output voltage temperature coefficient	dVo3	-	±100	-	ppm/°C	Ta=-30~75 °C, Io=30mA
Ripple rejection ratio	RR62	50	60	-	dB	Io=30mA
Current overload limiter	Iolim	-	90	-	mA	Fold back, Vo=0V
Output noise voltage	VNO	-	110	160	μVrms	BW=20~80kHz, Io=30mA

\*1 Input signal level : -14dBV, Input frequency : 1KHz, Measurement frequency band width : 20Hz to 80kHz

[Interface, UVLO]

Unless otherwise specified, Ta=25 °C, VCC=VBAT= 3.6V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
[CPU Interface 1 (CNT1,2,3,4,5,SWEN,MODE)]						
H Level Input current	IiH1	-10	1.95	10	μA	VIH=3.6V
L Level Input current	IiL1	-10	0	10	μA	VIL=0V
[CPU Interface 2 (SWVSEL,REG1VSEL)]						
H Level Input current	IiH2	-10	0	10	μA	VIH=3.6V
L Level Input current	IiL2	-10	0	10	μA	VIL=0V
[CPU Interface 3 (CNT1,2,3,4,5,SWEN,MODE)]						
H Level Input voltage	VIH	1.4	-	-	V	
L Level Input voltage	VIL	-	0	0.25	V	
[CPU Interface 4 (SWVSEL,REG1VSEL)]						
H Level Input voltage	VIH	VCC×0.8	-	VCC	V	
L Level Input voltage	VIL	-	-	VCC×0.2	V	
[UVLO (Under Voltage Lock Out)]						
Detecting voltage 1	VDETHL	2.4	2.5	2.6	V	VBAT=3.6→0V SWEEP
Detection release hysteresis	VHYS	25	50	100	mV	

●Reference data

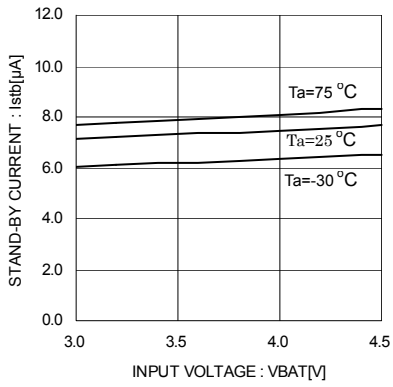


Fig.1 Circuit current  
(At BH6053GU stand by)

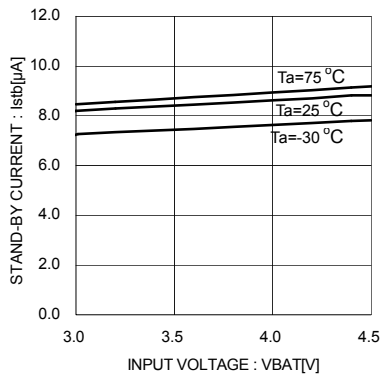


Fig.2 Circuit current  
(At BH6951GU stand by)

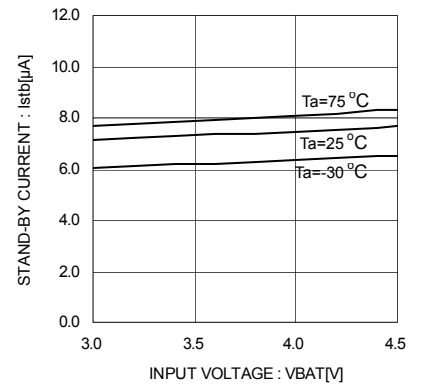


Fig.3 Circuit current  
(At BH6952GU stand-by)

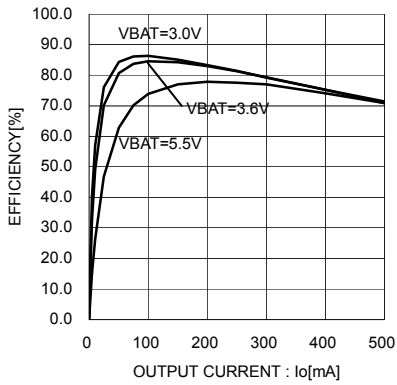


Fig.4 Efficiency  
(DC/DC converter 1.5V)

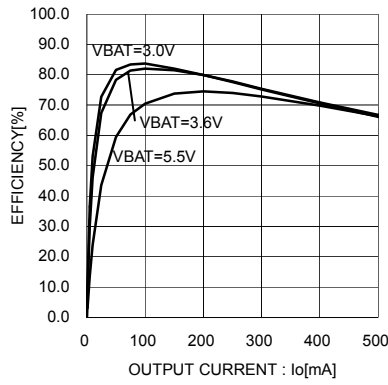


Fig.5 Efficiency  
(DC/DC converter 1.2V)

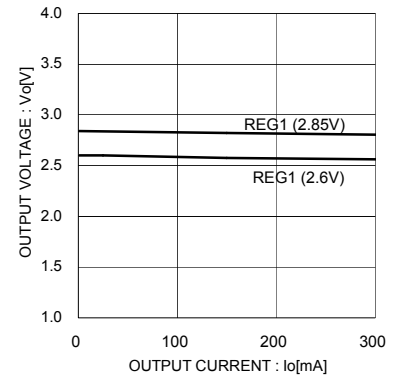


Fig.6 Load stability  
(REG1)

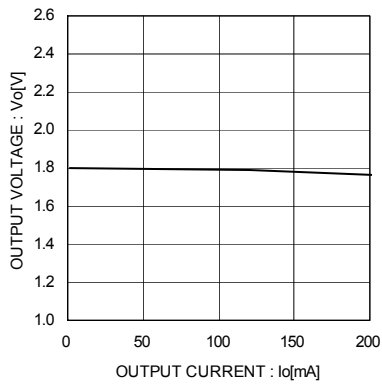


Fig.7 Load stability  
(REG2)

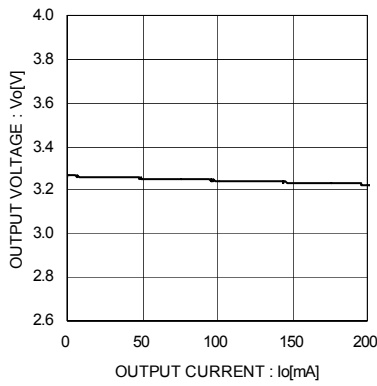


Fig.8 Load stability  
(REG3)

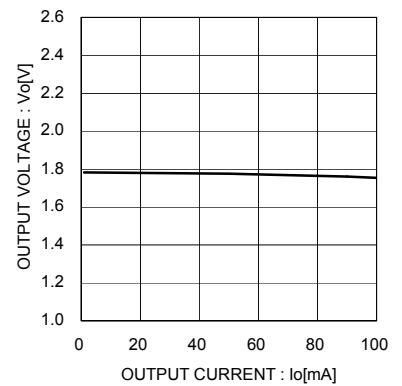


Fig.9 Load stability  
(REG4)

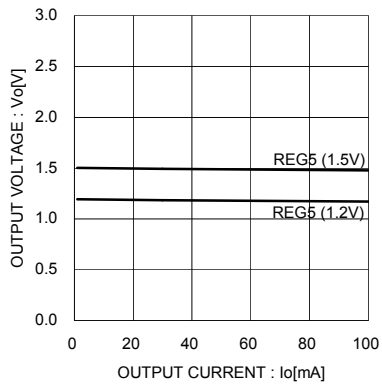


Fig.10 Load stability  
(REG5)

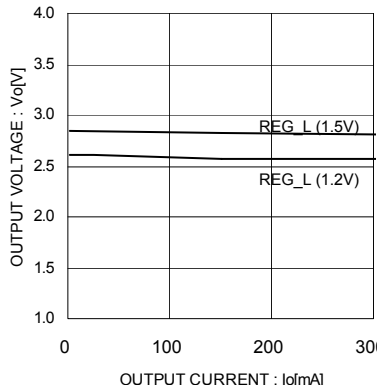


Fig.11 Load stability  
(REG\_L)

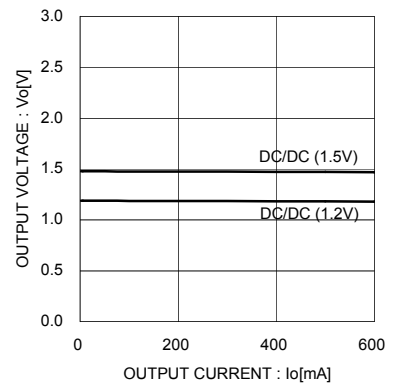


Fig.12 Load stability  
(DC/DC converter)

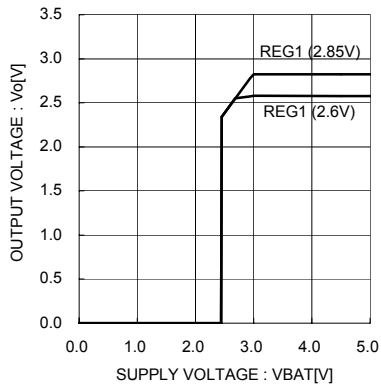


Fig.13 Input stability (REG1)

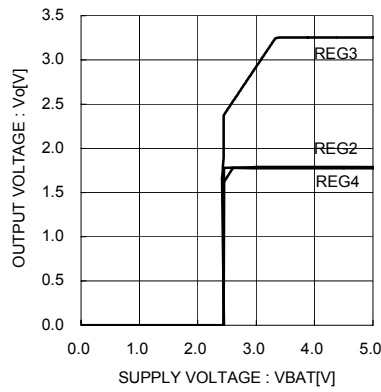


Fig.14 Input stability (REG2, REG3, REG4)

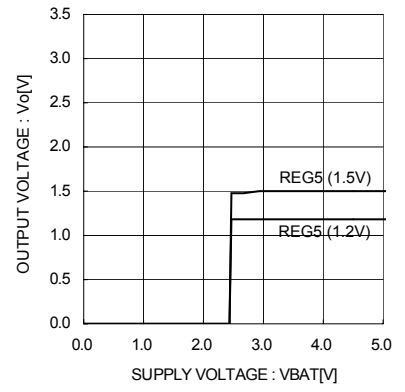


Fig.15 Input stability (REG5)

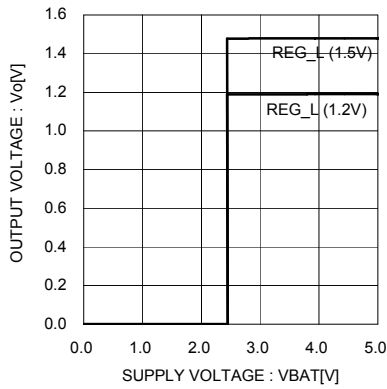


Fig.16 Input stability (REG\_L)

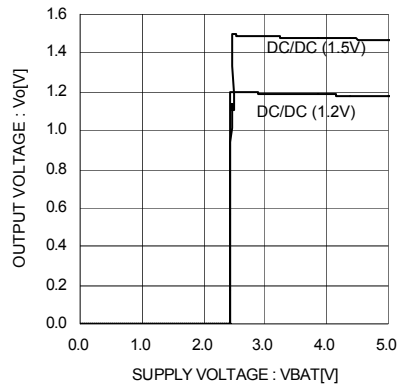


Fig.17 Input stability (DC/DC converter)

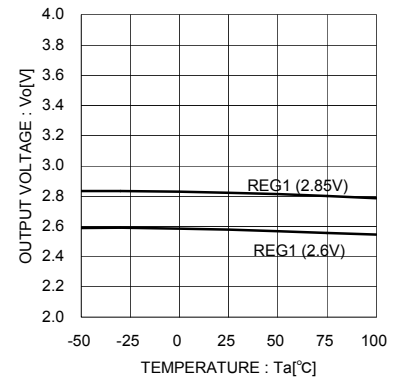


Fig.18 Output temperature fluctuation rate (REG1)

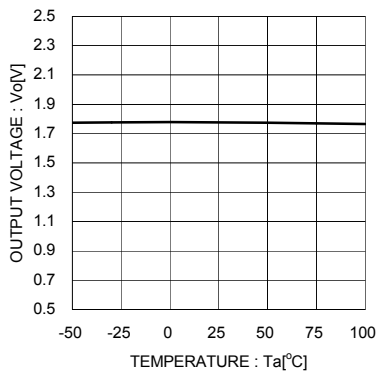


Fig.19. Output temperature fluctuation rate (REG2)

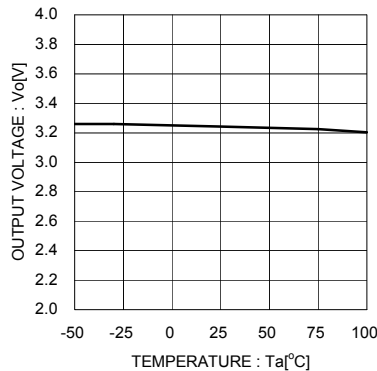


Fig.20 Output temperature fluctuation rate (REG3)

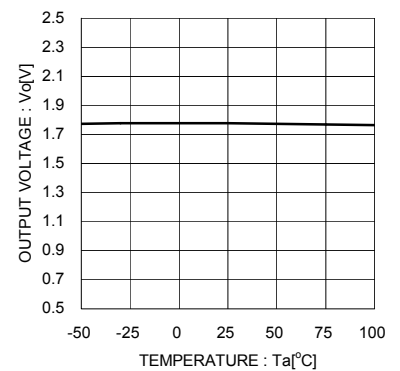


Fig.21 Output temperature fluctuation rate (REG4)

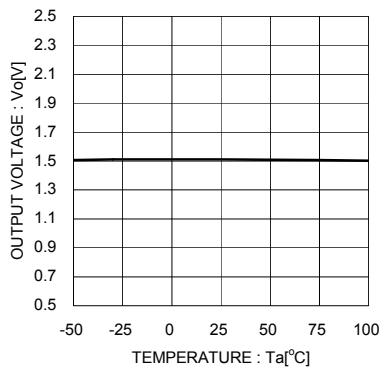


Fig.22 Output temperature fluctuation rate (REG5)

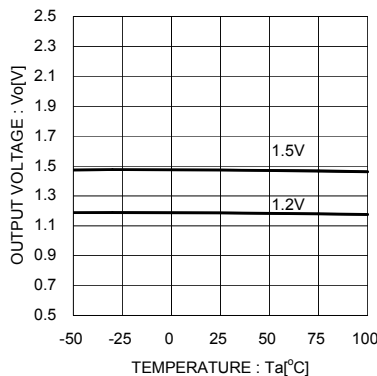


Fig.23 Output temperature fluctuation rate (DC/DC converter, REG\_L)

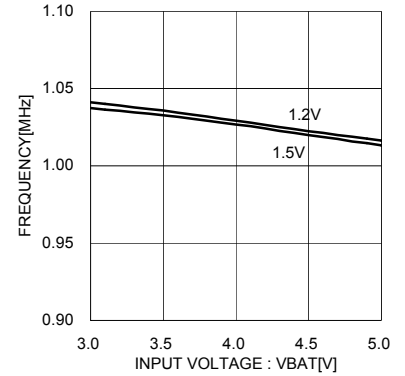


Fig.24 Switching frequency

●Block diagram, recommended circuit example, pin location diagram

F1	T4	F2	CNT4	F3	CNT2	F4	VREF24	F5	VREF12	F6	T3
E1	REG4V	E2	REG4I	E3	CNT3	E4	CNT1	E5	REG1VSEL	E6	CNT5
D1	GND2	D2	SWVSEL					D5	GND1	D6	REG5V
C1	LDOOUT	C2	BATP	INDEX post				C5	REG5I	C6	REG3V
B1	SWOUT	B2	GNDP	B3	SOFT	B4	SWEN	B5	REG1I	B6	REG23I
A1	T1	A2	FBIN	A3	MODE	A4	REG1V	A5	REG2V	A6	T2

Fig.25 Pin location diagram (BH6053GU Bottom View)

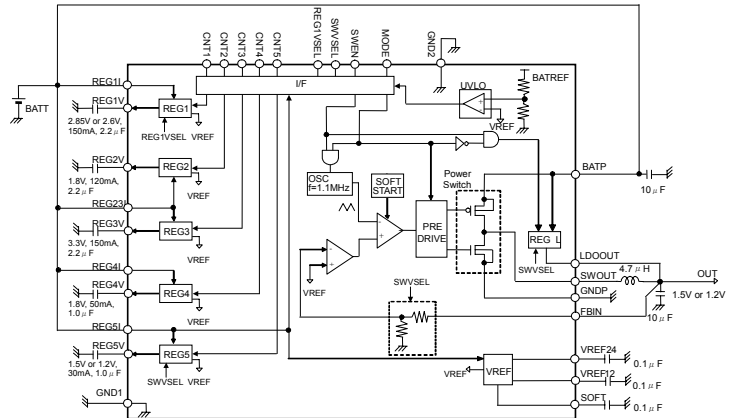


Fig.26 Block diagram and recommended circuit diagram (BH6053GU)

D1	T4	D2	SWVSEL	D3	GND1	D4	T3
C1	LDOOUT	C2	BATP	C3	VREF24	C4	VREF12
B1	SWOUT	B2	GNDP	B3	SOFT	B4	SWEN
A1	T1	A2	FBIN	A3	MODE	A4	T2

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Fig.27 Pin location diagram (BH6951GU Bottom View)

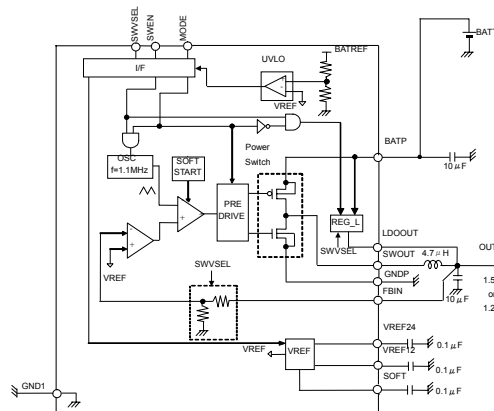


Fig.28 Block diagram and recommended circuit diagram (BH6951GU)

E1	T4	E2	VREF24	E3	VREF12	E4	REG1VSEL	E5	T3		
D1	GND2	D2	SWVSEL	D3	GND1	D4	REG2I	D5	REG2V		
C1	LDOOUT	C2	BATP					C4	CNT1	C5	CNT2
B1	SWOUT	B2	GNDP	B3	SOFT	B4	SWEN	B5	REG1I		
A1	T1	A2	FBIN	A3	MODE	A4	REG1V	A5	T2		

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Fig.29 Pin location diagram (BH6952GU Bottom View)

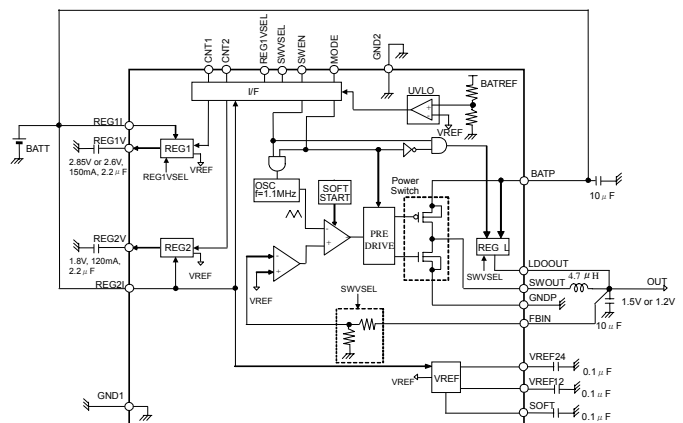


Fig.30 Block diagram and recommended circuit diagram (BH6952GU)



[Pin assignment table ]

Pin name	Pin No			Equivalent Pin circuit
	BH6053	BH6951	BH6952	
REG1I	B5	-	B5	F
REG1V	A4	-	A4	I
REG2I	-	-	D5	L
REG2V	A5	-	D4	I
REG23I	B6	-	-	F
REG3V	C6	-	-	I
REG4I	E2	-	-	F
REG4V	E1	-	-	D
REG5I	C5	-	-	L
REG5V	D6	-	-	I
VREF24	F4	C3	E2	K
VREF12	F5	C4	E3	D
GND1	D5	D3	D3	J
GND2	D1	-	D1	J
GNDP	B2	B2	B2	J
SWOUT	B1	B1	B1	C
BATP	C2	C2	C2	L

Pin name	Pin No			Equivalent Pin circuit
	BH6053	BH6952	BH6951	
LDOOUT	C1	C1	C1	I
FBIN	A2	A2	A2	G
SOFT	B3	B3	B3	B
MODE	A3	A3	A3	H
SWEN	B4	B4	B4	H
CNT1	E4	-	C4	H
CNT2	F3	-	C5	H
CNT3	E3	-	-	H
CNT4	F2	-	-	H
CNT5	E6	-	-	H
REG1VSEL	E5	-	E4	A
SWVSEL	D2	D2	D2	A
T1	A1	A1	A1	L
T2	A6	A4	A5	L
T3	F6	D4	E5	L
T4	F1	D1	E1	L

[Control table]

Output voltage Control of each model is shown as follows.

Pin name	Input level	
	L	H
SWEN	DC/DC converter circuit OFF	DC/DC converter circuit ON
MODE	REG_L mode	DC/DC mode
SWVSEL	REG_L, DC/DC, REG5=1.5V output	REG_L, DC/DC, REG5=1.2V output
CNT1	REG1 OFF	REG1 ON
REG1VSEL	REG1=2.6V output	REG1=2.85V output
CNT2	REG2 OFF	REG2 ON
CNT3	REG3 OFF	REG3 ON
CNT4	REG4 OFF	REG4 ON
CNT5	REG5 OFF	REG5 ON

●I/O Equivalent circuit diagram

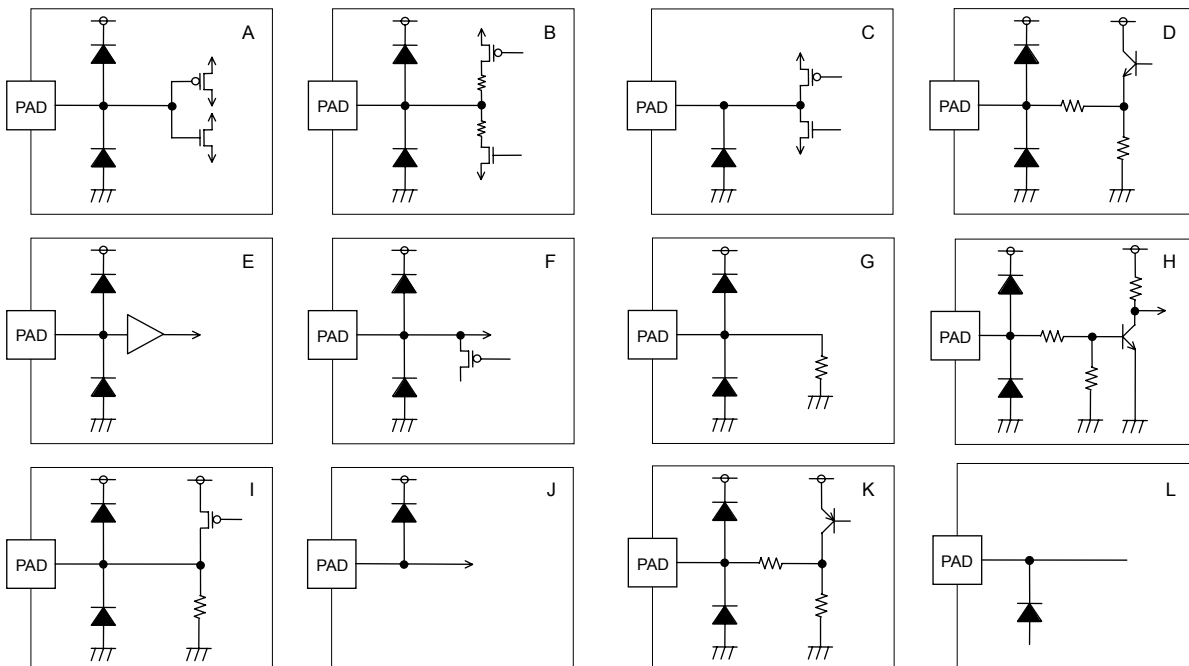


Fig.31

●Operation dissipation of each block

1) About LDO

Each LDO can be controlled by input H or L level in the control Pin assignment.

The DC/DC converter can be controlled by input H or L level in SWEN and MODE.

It has 2 modes to obtain a high efficiency at a low load.

This purpose is to use as follows.

	Application	SWEN	MODE
DC/DC mode	At high-output current.	H	H
LDO mode	Stand by, At low-output current	H	L
DC/DC OFF mode	DC/DC converter OFF	L	L

2) Under Voltage Lock Out (UVLO)

When the power supply voltage is decreased, all LDOs, including the DC/DC converter, are shut down.

UVLO operates when the power supply voltage is decreased till reaches the detection voltage. When the power supply voltage is recovered to the detection voltage, UVLO is automatically released.

3) Current overload limiter

The current overload limiter function of the LDO shows the following characteristics:

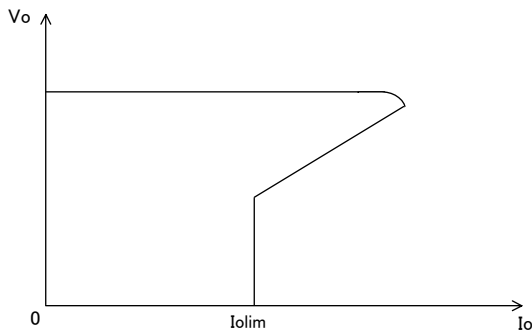


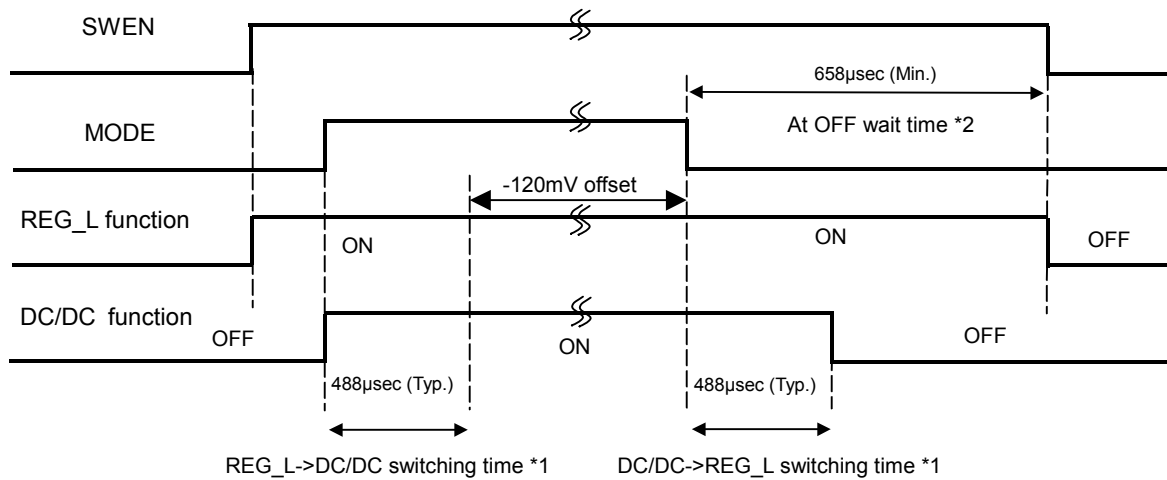
Fig.32

4) Soft start of the DC/DC converter

Soft start operates when the DC/DC converter is turned on. The function of soft start is to raise output voltage gradually, and to prevent an excess output voltage.

● **Timing chart**

The DC/DC converter is operated by the control of SWEN, MODE Pins.



Time is calculated by the standard operation frequency.

\*1 REG\_L→DC/DC mode switching time and DC/DC→REG\_L mode switching time are defined by 512 counts of the switching frequency. The resulting time is 488µsec when switching frequency is 1.05MHz.

\*2. When the DC/DC converter is turned off (SWEN=MODE=H→SWEN=L),

1. switch MODE to LOW to change REGL,
2. switch SWEN to L after 658µsec.

Note: BH6952GU can turn off the DC/DC converter directly from DC/DC MODE without changing to REG\_L.

● **Selection of application parts**

Decoupling capacitor

LDO block

	Output terminal	Recommended value	Type
BH6053GU	REG1 ~ 3V	2.2µF	Ceramic capacitor
	REG4V, 5V	1.0µF	Ceramic capacitor
BH6952GU	REG1V, 2V	2.2µF	Ceramic capacitor

Put these elements near each output part for stable operation.

Reference voltage block

To stabilize the reference voltage, mount the ceramic capacitor of 0.1µF between VREF12, VREF24, and GND pin.

Put 0.1µF at the SOFT pin.

The SOFT Pin is a time setup pin of the Soft start, of the DC/DC converter.

Input voltage block

Connect a capacitor to the power supply pin for stable input voltage supply.

Connect a capacitor near each input pin for a stable operation.

[External component of DC/DC converter]

	Output terminal	Inductor	Capacitor	
		Recommended value	Recommended value	Type
BH6053GU	SWOUT	4.7µH	10µF	ceramic capacitor
BH6951GU				
BH6952GU				

Put these elements near each output part for stable operation.

### ●Attention point of board layout

In designing the board pattern, the power supply line should be at a low impedance. Connect the bypass capacitor, if necessary. The wiring impedance must be particularly lower around the DC/DC converter.

### ●Heat loss

In heat design, operate the DC/DC converter accordingly:

1. Power temperature  $T_a$  must be less than 75 temperature.
2. The power loss of IC must be less than specified dissipation  $P_d$ .

Note: The temperature is a guarantee temperature. Take into consideration temperature operation margins.

### ●Operation Notes

- 1) Absolute maximum ratings  
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
- 2) Operating conditions  
Characteristics are guaranteed under the conditions of each specified parameter.
- 3) Reverse polarity connection of the power supply  
Connecting the of power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.
- 4) Power supply line  
Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks.  
Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.
- 5) GND voltage  
Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals (except SWOUT) should be lower than the GND potential voltage including an electric transients.
- 6) Short circuit between terminals and GND or other devices  
Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.
- 7) Operation in a strong electromagnetic field  
Using the ICs in a strong electromagnetic field can cause operation malfunction.
- 8) Inspection with set PCB  
During testing, turn on or off the power before mounting or dismounting the board from the test Jig.  
Do not power up the board without waiting for the output capacitors to discharge. The capacitors in the low output impedance terminal can stress the device. Pay attention to the electro static voltages during IC handling, transportation, and storage.
- 9) Input terminals  
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and breakdown of the input terminal. Therefore, pay thorough attention not to apply a voltage lower than the GND to the input terminals. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply a voltage lower than the power supply voltage to the input terminals, or a voltage within the guaranteed value of electrical characteristics.

- 10) Inspection with set PCB  
During testing, turn on or off the power before mounting or dismantling the board from the test Jig.  
Do not power up the board without waiting for the output capacitors to discharge. The capacitors in the low output impedance terminal can stress the device. Pay attention to the electro static voltages during IC handling, transportation, and storage.
- 11) Input terminals  
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and breakdown of the input terminal. Therefore, pay thorough attention not to apply a voltage lower than the GND to the input terminals. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply a voltage lower than the power supply voltage to the input terminals, or a voltage within the guaranteed value of electrical characteristics.
- 12) Ground wiring pattern  
The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.
- 13) External capacitor  
When using external ceramic capacitors, consider degradation in the nominal capacitance value due to DC bias and changes in the capacitance with temperature.
- 14) Not connecting input terminals  
Unused input terminals should be connected to the power supply or GND line. Open terminals of high impedance CMOS gate can cause unstable states in the logic gate, consequently causing an increase in the power supply current.
- 15) Thermal shutdown circuit (TSD)  
When junction temperatures become 150°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.
- 16) Thermal design  
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
- 17) LDO  
Use each output of the LDO separately. Do not use in connection with each output.
- 18) DC/DC converter  
Select the low DCR inductors to decrease power loss for the DC/DC converter.

●Power dissipation characteristics

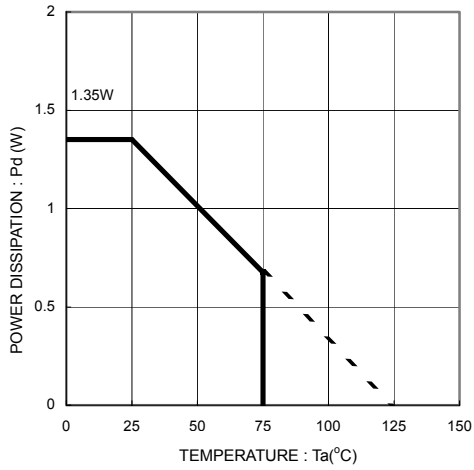


Fig.33 BH6053GU

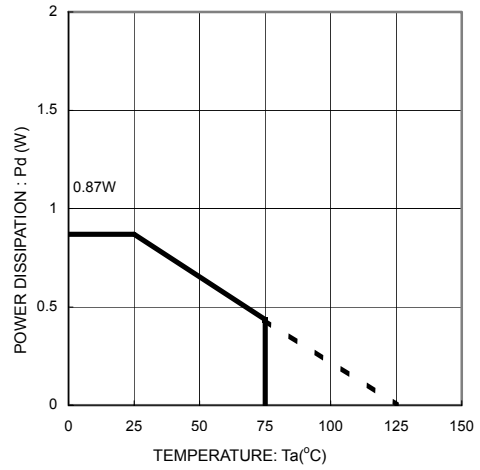


Fig.34 BH6951GU

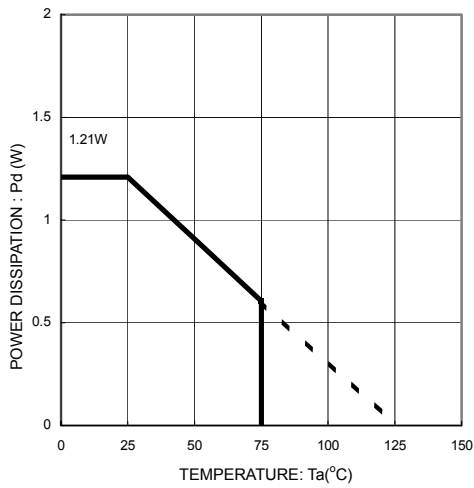
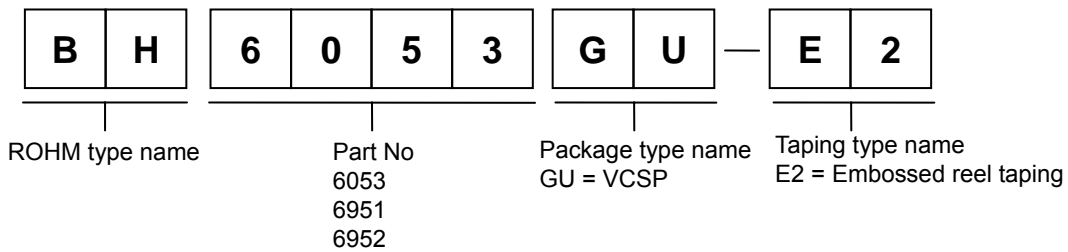


Fig.35 BH6952GU

Mounting board specification  
 Material Glass epoxy  
 Size 50mm×58mm×1.75mm (8 layer)

●Order type name selection





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