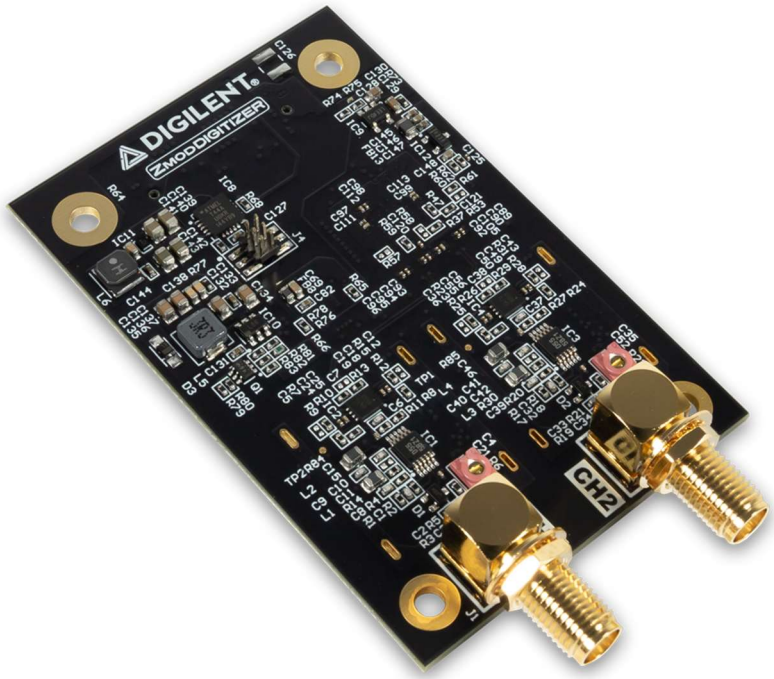

Zmod Digitizer 1430-125: 2-channel 14-bit Digitizer Module

Description:

The Digilent Zmod Digitizer is a SYZYGY™ compatible module containing a dual-channel ADC and the associated front end. The Zmod Digitizer is intended to be used with any SYZYGY™ compatible carrier board having the required capabilities.

When coupled to a base board using the SYZYGY™ expansion, like the Eclypse Z7 or Genesys ZU, the combination will serve as a powerful prototyping platform for instrumentation, high-speed control, and SDR. By utilizing these expansion capabilities, users can spend more time on the analytical and system-level aspects of the solution rather than having to focus on the component-level interactions of the devices.

The Zmod Digitizer module is a variant of the similar Zmod Scope module but optimized for RF signal acquisition and frequency-domain analysis. The simpler DC-coupled input and 60 MHz anti-aliasing input filter improves immunity to stray RF radiation and the versatile and very low-jitter on-board clock generator enables acquisition at key rates, including 122.8 MHz often used in SDR applications.

Features:

- Channels: 2
- Channel type: Single-ended
- Resolution: 14-bit
- Input range: ±1 V
- Absolute Resolution: 0.13 mV
- Sample rate (real time): 125 MS/s, max
- Input impedance: 1 MΩ || 5 pF
- Analog bandwidth:
    - 60+ MHz @ -3 dB
    - 20 MHz @ -0.5 dB
    - 8 MHz @ -0.1 dB
- Input protected to: ±50 V
- Product Compliance:
    - HTC: 8473301180
    - ECCN: EAR99

Included:

- Zmod Digitizer 1430-125
- Digilent custom packaging with protective foam

Software:

It is supported by the Zmod Digitizer Controller IP core, which is intended for use in Vivado, and provides access to the vast majority of the Zmod's features to user FPGA designs. This IP handles the "hard part" of creating a project for the Zmod: configuring the ADC and transferring data from the SYZYGY™ port into an AXI-stream interface that plays nicely with Xilinx's IP ecosystem. The IP core and IP user guide are linked from the Zmod Digitizer resource center. The IP core is provided through the vivado-library IP repository on Github.