Datasheet
March 22, 2004
MU4001, Rev 1.1

TD242LP

USB On-The-Go Low Power, Two Port, Single Chip Host/Peripheral Controller

Description

TransDimension's TD242LP is a **Low Power**, single chip USB Host and Peripheral controller that is the second controller in the family of integrated low-cost, high-performance, On-the-Go (OTG) controllers optimized and specifically designed for embedded systems, peripherals, mobile communication, and consumer products. The TD243 was the first controller in the USB OTG family delivered to the market by TransDimension. The TD242LP is a combination of a standard USB Host controller and an OTG Dual-Role Device controller. The TD242LP enables any embedded system to operate as a USB Host and Peripheral, thereby dramatically expanding the degree of interconnectivity and extending the applicability of USB into many new areas, especially low power, mobile markets. Software support for the TD242LP is available from SoftConnex Technologies, Inc., a wholly owned subsidiary of TransDimension Inc., and includes USBLink OTG Stack, ported to a wide variety of RTOSs, interface code to the TD242LP and USB device drivers. Peer-to-Peer connectivity is made simple with the TD242LP since USB connectivity is achieved without PC intervention. Applications include mobile and post-PC products such as cellular phone, palmtop PC, PDA, MP3 players, projectors, and Internet appliances, to name a few. The TD242LP can operate in the following modes:

- USB On-the-Go Dual-Role Device: One OTG port plus a standard USB host with one downstream port
- Simultaneous standard USB host with one downstream port and one USB peripheral upstream port
- Standard USB host with two downstream ports

The host controller in the TD242LP is the only true transfer level embedded USB host and On-the-Go controller that can be interfaced directly to most popular microprocessors and is easily programmable. The active endpoint and transfer descriptors are located in the on-chip memory, thus significantly reducing processor overhead relative to any comparable product on the market.

The full speed peripheral controller is very flexible and software configurable, in terms of the active bi-directional endpoint number (12), type, size, and buffering mechanism of each endpoint.

Features

- Concurrent operation of On-The-Go, Host and Peripheral ports
- Fully compliant with USB On-the-Go specification and USB Specification Rev. 2.0 for full-speed (12Mb/s) and low-speed (1.5Mb/s) USB devices
- High-performance USB host: Full USB bandwidth utilization with low load on system microprocessor without bus mastering
- Transaction scheduling and transfer level protocol implemented in hardware including bandwidth management, data toggle and retry
- Isochronous transfer with loose timing requirements on the microprocessor
- Fast microprocessor access cycle (~25MB/s for 16-bit data bus)
- Double/multi buffering support for all four types of USB transfers
- Separate transfer descriptor and data memory space
- Capable of supporting up to 500mA to peripherals when using external 5V power supply from an external charge pump
- No built-in charge pump leads to smaller die size and more cost savings
- Integrated on-chip pull-up and pull-down resistors
- Power saving mode for whole chip and host controller, and suspend mode for peripheral controller
- Integrated PLL supports external crystal or crystal oscillators of 6MHz, 12MHz, 24MHz, and 48MHz
- Single 3.3V power supply, 2.5V to 3.3 V I/O (LVCMOS/TTL), 5 V tolerant
- Software and hardware Host Negotiation Protocol
- Session Request Protocol
- Direct interface to microprocessors, RISC, CISC, and DSPs including but not limited to x86, Intel XScale & StrongARM, Hitachi SH3, Fujitsu SPARCLite, NEC and Toshiba MIPS, ARM7,

ARM9, Motorola PowerPC, ColdFire and Dragonball among others

- Embedded RTOS software available for WinCE, Linux, VxWorks, Nucleus, LynxOS, QNX, pSOS, PowerTV, SMX, AMX, ThreadX, VRTX, ITRON, Symbian OS and MS-DOS operating systems among others

- USB device driver software available including printer, speaker, mass storage, hub, modem, Ethernet, mouse, keyboard, digital camera, video camera, cell phone, STB, PDA, etc.
- Programmable IRQ polarities
- 64 ball TF-BGA & 64 pin LQFP packages available

Architecture

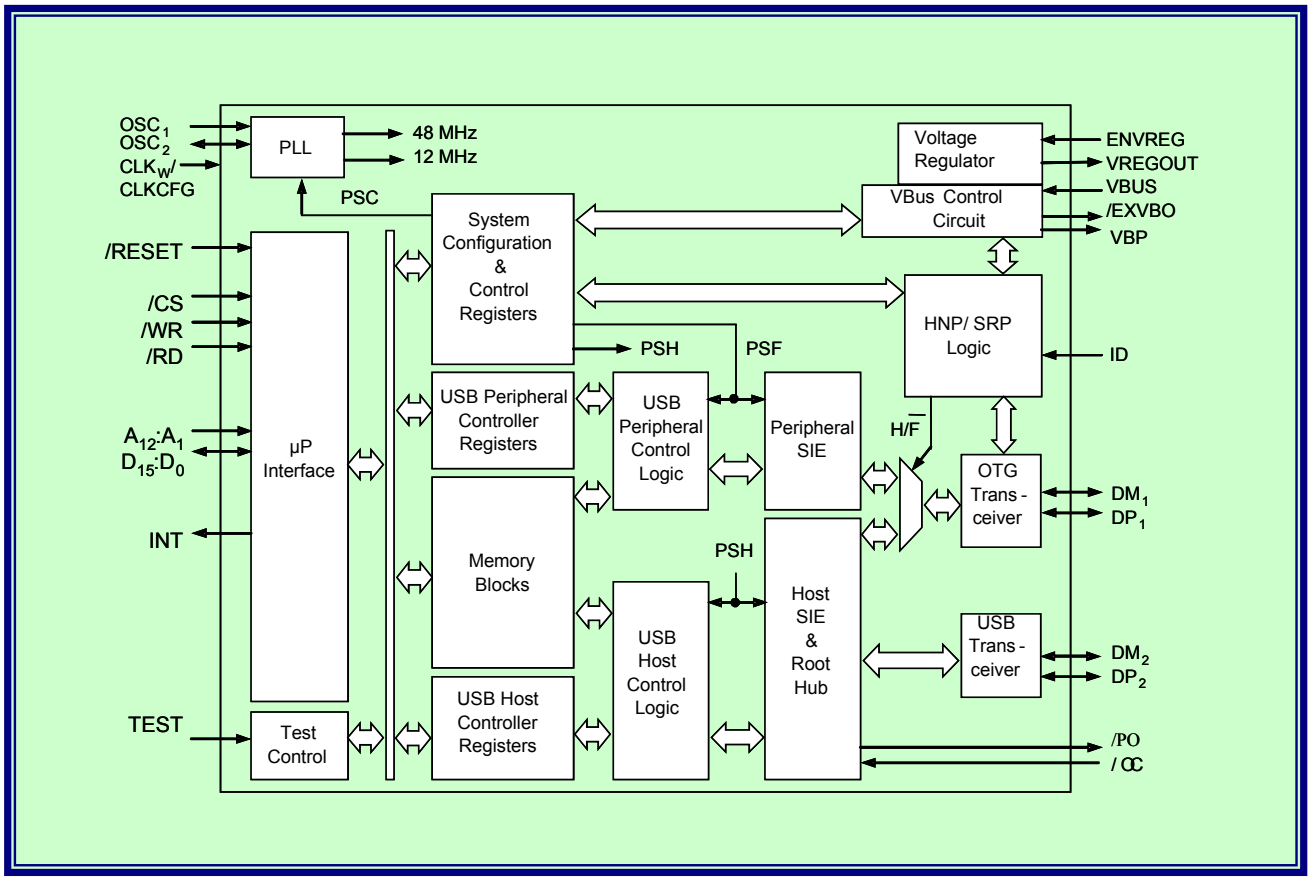


Figure 1 – TD242LP Architectural Block Diagram

USB/OTG Host logic blocks: The USB Host Controller Logic, the host Serial Interface Engine (SIE) and the root hub are responsible for the fully complaint (not reduced) USB host of the TD242LP - supporting transfer level user interface, scheduling/processing transactions, and monitoring/handling port events.

USB/OTG Peripheral logic blocks: The USB Peripheral Controller Logic, together with the peripheral SIE, manages all low-level USB peripheral protocols upon which a fully compliant full speed USB peripheral is operated.

Interrupt Handling: Interrupts from the TD242LP to a microprocessor are minimum, as an interrupt is generated only at the end of a USB transfer (for both host and peripheral), which can have a size of up to 4 Mbytes*. Moreover, an interrupt event may be delayed inside the TD242LP, and be bundled with others to further reduce the number of interrupt occurrences.

- Even though invisible to the high level software, low level interrupts are necessary to handle 4KByte internal data RAM.

Memory blocks: The Host Controller Logic, the Peripheral Controller logic, and the microprocessor are all entitled to have access to the memory blocks for data and control. A RAM Arbiter sequences all RAM access.

Register banks: There are 3 register banks used for System Configuration, Host Control, and Peripheral Control.

Host Negotiation Protocol (HNP): The user may select one of two HNP types supported in the TD242LP. The user simply selects software or hardware HNP, depending on their application, with each type of HNP having its own merits. Hardware HNP is a built-in state machine, which reduces microprocessor interrupts, whereas, software HNP is maintained and manipulated in the software space and provides an extra option to the user.

Both types of HNP, when enabled, will support negotiation with an attached OTG device, in order to determine in which role (A-device or B-device) the TD242LP will operate as, in a session. The TD242LP contains the required analog components (comparators, etc.) and digital logic to support the operation. The microprocessor interfaced to the TD242LP can also disable this negotiation process, and configure the Dual-Role Device port of the TD242LP to operate as a host or peripheral. HNP may only be implemented in conjunction with a Mini-AB receptacle.

Session Request Protocol (SRP): The USB OTG specification is positioned to service mobile products that are battery powered. The SRP protocol allows the A-device to conserve power by turning the USB VBus signal off depending on whether there is USB traffic. The B-device will have the capability to initiate bus activity via SRP and hence the A-device will be capable of responding to this via SRP. The TD242LP On-The-Go port fully complies to the SRP protocol as described and defined in the USB On-The-Go specification.

Operational Modes: The TD242LP can be operated in different modes via software configuration:

	Port 1	Port 2	Application
On-The-Go	OTG	Host	OTG application and one host port (concurrent OTG/Host operation supported. The OTG port may behave in either host or peripheral modes and dynamically switch between roles through the HNP, or when directed by a user by changinig of USB cable connection)
Host Only	Host	Host	Host only controller with two ports
Peripheral and Host	Peripheral	Host	Peripheral and Host ports

Microprocessor interface: The TD242LP is a memory mapped device that can easily interface, gluelessly, to the system bus of most popular microprocessors, CISC, RISC and DSPs including but not limited to x86, Intel XScale & StrongARM, Hitachi SH3, Fujitsu SPARCLite, NEC and Toshiba MIPS, ARM7, ARM9, Motorola PowerPC, ColdFire and Dragonball, among others. Reference designs and evaluation boards for some of these processors are available with new designs being added and tailored to fit particular customer needs.

Software support: TransDimension is a leader in the USB embedded market, bringing both software and silicon to its customers. TransDimension provides development and support packages and a wide spectrum of USB host and On-The-Go software support in C source code to reduce development cost and time to market for its customers. Software for a variety of operating systems is fully tested and supported to easily interoperate with the above listed microprocessors. TransDimension is a Microsoft Windows embedded partner.

TransDimension is a Microsoft Windows Embedded Partner (WEP) and supplies Host Controller Driver (HCD) Interface code to the TD242LP for Linux and WinCE operating systems, as well as applicable USB class and device drivers for use in a wide variety of mobile and post-PC products.

For many other Real Time Operating Systems (RTOS) as listed previously, TransDimension and SoftConnex supply the USBLink On-The-Go software solution, which utilizes proven software technologies from SoftConnex's USBLink Host and USBLink Peripheral software products, thereby providing a complete, integrated solution for USB On-The-Go applications.

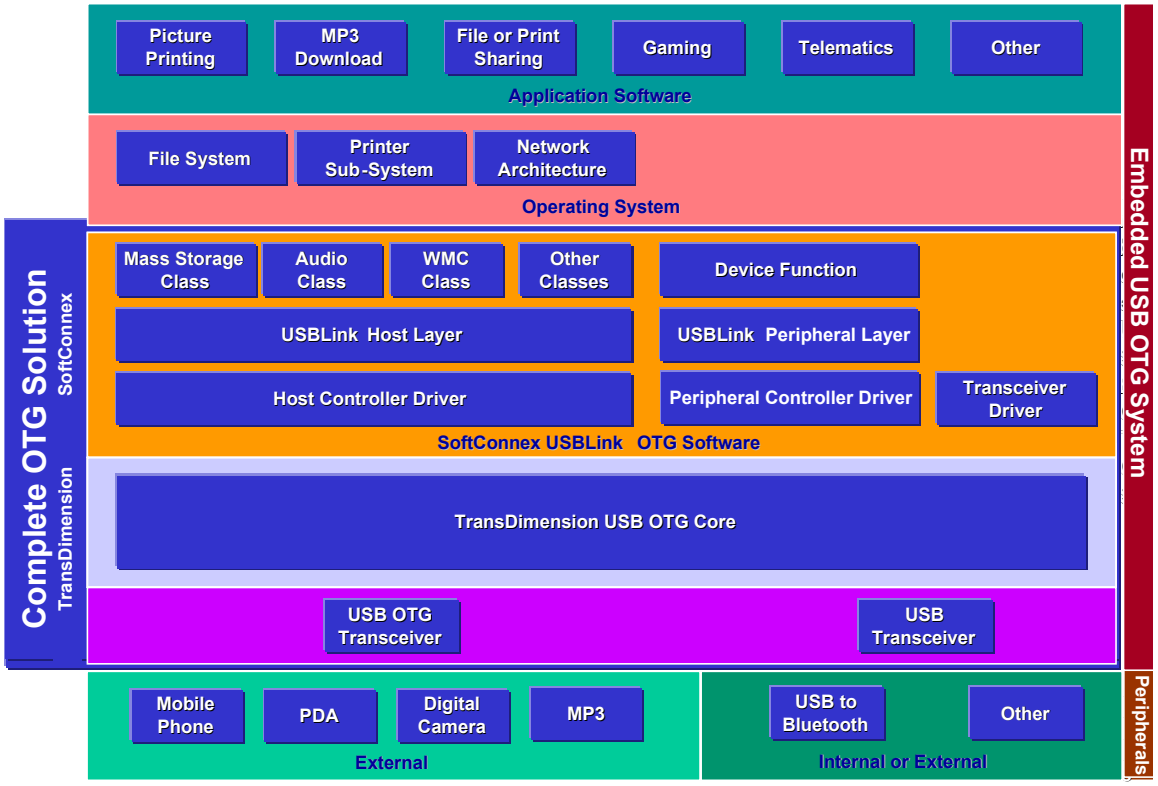


Figure 2 – Software Stack and TransDimension's Complete USB OTG solution

TD242LP Reference Designs, Evaluation/Demo Boards and Developer Kits

Reference Designs

The reference designs listed below will include schematics, application notes and instructions on how to interface to the associated microprocessor of interest. In addition, software will be available for specific operating systems including: WinCE, Linux, uCLinux, VxWorks, Nucleus, Lynx, QNX, Symbian OS, OS20, OS40, pSOS, PowerTV, SMX, ThreadX, VRTX, ITRON, MS-DOS operating systems. Contact your local TransDimension representative for ordering information of additional new reference designs for other microprocessors, CISC, RISC, and DSPs including Fujitsu SPARCLite, NEC and Toshiba MIPS, Motorola PowerPC, among others.

- TD242LP / Intel StrongARM (SA1110) USB On-The-Go Reference Design
- TD242LP / Intel XScale (PXA250) USB On-The-Go Reference Design
- TD242LP / Hitachi SH-3 / SH-4 USB On-The-Go Reference Design
- TD242LP / Motorola ColdFire 5272 USB On-The-Go Reference Design
- TD242LP / ARM7 USB On-The-Go Reference Design

Evaluation / Demo Kits

BGA242S: Evaluation Board with TD242LP silicon in TF-BGA package
The BGA242S will be a small board (3.0”x 4.8”) that brings out all of the pins necessary to interface with microprocessors available on the market, today. The BGA242S board will have 2 USB receptacles (one USB OTG mini-AB and one standard USB host receptacle) ready to connect to any USB peripheral, hub or USB host. The main components on the BGA242S board will consist of the TD242LP silicon in TF-BGA package, a PC104 interface connector and Vbus distribution/manipulation electronic circuitry. Please see your local TransDimension sales representative for ordering information and specifications when this product is available.

PCE242: PCI card with TD242LP silicon in TF-BGA package
The PCE242 card and associated documentation will contain everything you need to perform an evaluation of the functionality and development on the TD242LP chip, in a PCI bus environment. The PCE242 card is a standard PCI card that may be inserted into any PCI slot, inside a personal computer or laptop docking station.

The PCE242 card may be used in any 33 MHz PCI system and it will automatically adjust to a 3.3V or 5V PCI environment. The PCE242 PCI card quickly allows customers to start developing software around the TD242LP controller. TransDimension will supply the drivers necessary to evaluate the PCI104 PCI card and associated daughter card in both OTG and Host mode simultaneously, under the Microsoft MS-DOS based operating systems and/or Linux operating systems. Please see your local TransDimension sales representative for ordering information, specifications and availability.

Pin Descriptions and Packaging

The following notations are used to indicate the type of a signal/pin:

I	INPUT	O	OUTPUT	PL	ACTIVE LEVEL PROGRAMMABLE
IO	BI-DIRECTIONAL	WO	WIRED OR	NA	NOT APPLICABLE
PW	POWER/GROUND	PS	PASSIVE	NC	NO CONNECT
H	ACTIVE HIGH	L	ACTIVE LOW		

Pin/Signal Name	Signal Type	Active Level	Pin/Signal Description
OSC_1	I		A 6 MHz passive crystal should be connected across the two pins. Optionally, a 6 MHz oscillator can be sourced through OSC1 or a 12, 24, or 48 MHz oscillator can be sourced through OSC2 (12/24 MHz option available for the BGA package only).
OSC_2	IO		
/RESET	I	L	Hardware reset.
/CS	I	L	Chip select.
/WR	I	L	Write strobe.
/RD	I	L	Read strobe.
A_{12}:A_1	I		Address bus for an addressing space of 8K bytes (4K bytes Data memory + 512 bytes each of Registers, ETD Memory and EP Memory).
D_{15}:D_0	IO		16-bit data bus.
TEST	I	H	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation.
/EXVBO	O	L	Turn on/off the external V_{BUS} (5V) for OTG operation (1: V_{BUS} off; 0: V_{BUS} on).
/PO	O	L	Turn on/off the gang power for all Host ports.
/OC	I	L	Over current condition indicator for gang powered Host ports.
INT[1]	O/WO	PL	Interrupt to the MCU. This pin can be software configured as a regular output or WO. (WO is the default).
ID	I		Connected to the ID pin of the mini-AB connector (Port 1) for OTG applications. With the help of an internal pull-up resistor, it determines the chip's responsibility in an OTG application, (0: A-DEVICE, 1: B-DEVICE).

[1] The active level for INT is programmable by software but defaults to active low after power on or hardware reset. This feature allows glue-less interfacing with most microprocessors. Caution must be taken in user software to make sure relevant operations (interrupt) are disabled before alterations to default active levels are made.

<table>
<tr><td>DM_1, DP_1</td><td>IO</td><td></td><td>Data lines for Port 1, which may serve as a USB Host, Peripheral or OTG port. If not used, these two pins should be left floating.</td></tr>
<tr><td>DM_2, DP_2</td><td>IO</td><td></td><td>Data lines for Port 2, a dedicated USB Host port. If not used, these two pins should be left floating.</td></tr>
<tr><td>VBUS</td><td>I</td><td></td><td>V_{BUS} input sampled during HNP/SRP operations by the OTG port. This pin should be left floating when Port 1 is not used for OTG applications.</td></tr>
<tr><td>VBP</td><td>IO</td><td>H</td><td>V_{BUS} pulsing control. This pin is used only when Port 1 is an OTG port for a B-DEVICE.

This pin is sensed at power on or hardware reset (/RESET) to determine the frequency of the crystal or the crystal oscillator as outlined in the following table:

<table>
<tr><th>VBP</th><th>Frequency(QFP)</th></tr>
<tr><td>0</td><td>6 MHz Crystal
6 MHz 2.5V Oscillator input on OSC1
6 MHz 3.3V Oscillator input on CLKw</td></tr>
<tr><td>1</td><td>48 MHz 2.5V Oscillator input on OSC2
48 MHz 3.3V Oscillator input on CLKw</td></tr>
</table>
</td></tr>
<tr><td>CLK_W</td><td>I</td><td></td><td>This pin is available only in the QFP package

If 3.3V I/O is used along with an oscillator source (instead of a crystal), then the 3.3V input clock should go to this pin instead of the OSC1/OSC2.

If not used, this pin should be grounded.</td></tr>
<tr><td>CLKCFG</td><td>I</td><td></td><td>This pin is available only in the BGA package

The state of this pin is used along with the VBP during power on or hardware reset to provide additional configurations of 12/24 MHz for the BGA package as show below:

<table>
<tr><th>VBP</th><th>CLKCFG</th><th>Frequency(BGA)</th></tr>
<tr><td>0</td><td>0</td><td>6 MHz Crystal
6 MHz 2.5V Oscillator input on OSC1</td></tr>
<tr><td>0</td><td>1</td><td>12 MHz 2.5V Oscillator input on OSC2</td></tr>
<tr><td>1</td><td>0</td><td>48 MHz 2.5V Oscillator input on OSC2</td></tr>
<tr><td>1</td><td>1</td><td>24 MHz 2.5V Oscillator input on OSC2</td></tr>
</table>
</td></tr>
<tr><td>ENVREG</td><td>I</td><td></td><td>Enables the internal Voltage Regulator if asserted. If not used, this pin should be tied to V_{SS}.</td></tr>
<tr><td>VREGOUT</td><td>PW</td><td></td><td>Internal Voltage Regulator output of 2.5V

If enabled, this output should be connected to the $V_{DD2.5}$, $V_{DD2.5A}$ (and V_{DDW} if Wide-range IO is at 2.5V) supplies of the chip.

If the Regulator is disabled, then this pin should be treated as another $V_{DD2.5}$ supply input to the chip.</td></tr>
<tr><td>$V_{DD3.3A}$</td><td>PW</td><td></td><td>Analog +3.3V.</td></tr>
<tr><td>$V_{DD2.5A}$</td><td>PW</td><td></td><td>Analog +2.5V.</td></tr>
</table>

V_{SSA}	PW		Analog ground.
$V_{DD2.5}$	PW		Digital +2.5V.
V_{DDW}	PW		Wide-range IO +3.3V or +2.5V.
V_{SS}	PW		Digital/Wide-range IO ground.
NC	PS		No connection. These pins should be left floating.

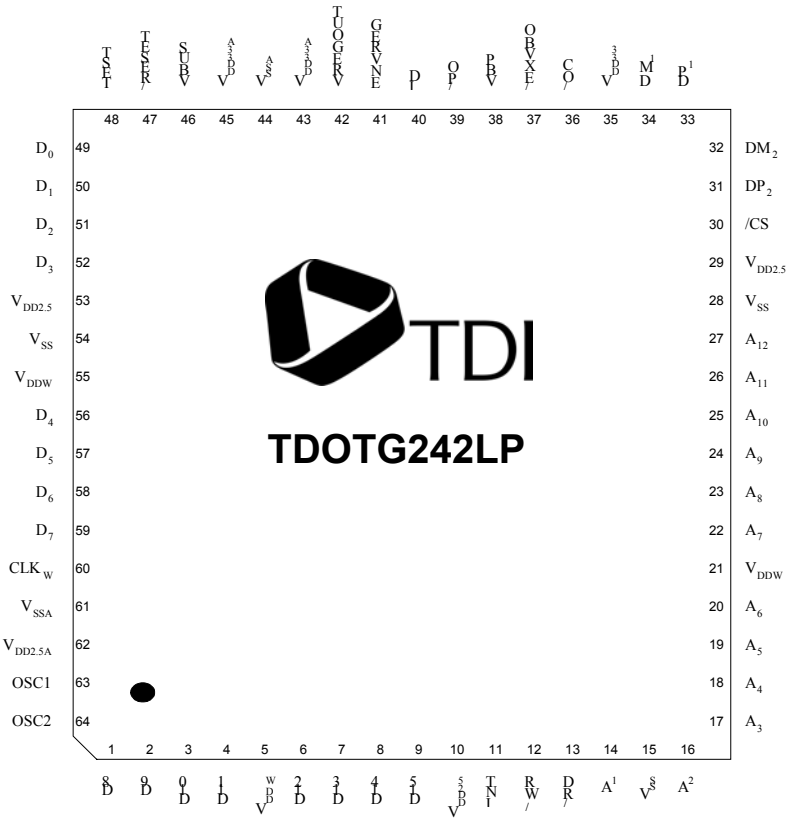
Figure 3 – Detailed Pin Descriptions

Note:

1. Software attention may be required if some pins are not used, whether they are pulled-up, pulled-down or left floating. This is especially true for OTG related pins.

1	D_8	17	A_3	33	DP_1	49	D_0
2	D_9	18	A_4	34	DM_1	50	D_1
3	D_{10}	19	A_5	35	$V_{DD3.3}$	51	D_2
4	D_{11}	20	A_6	36	/OC	52	D_3
5	V_{DDW}	21	V_{DDW}	37	/EXVBO	53	$V_{DD2.5}$
6	D_{12}	22	A_7	38	VBP	54	V_{SS}
7	D_{13}	23	A_8	39	/PO	55	V_{DDW}
8	D_{14}	24	A_9	40	ID	56	D_4
9	D_{15}	25	A_{10}	41	ENVREG	57	D_5
10	$V_{DD2.5}$	26	A_{11}	42	VREGOUT	58	D_6
11	INT	27	A_{12}	43	$V_{DD3.3A}$	59	D_7
12	/WR	28	Vss	44	V_{SSA}	60	CLK_W
13	/RD	29	$V_{DD2.5}$	45	$V_{DD3.3A}$	61	V_{SSA}
14	A_1	30	/CS	46	VBUS	62	$V_{DD2.5A}$
15	V_{SS}	31	DP_2	47	/RESET	63	OSC_1
16	A_2	32	DM_2	48	TEST	64	OSC_2

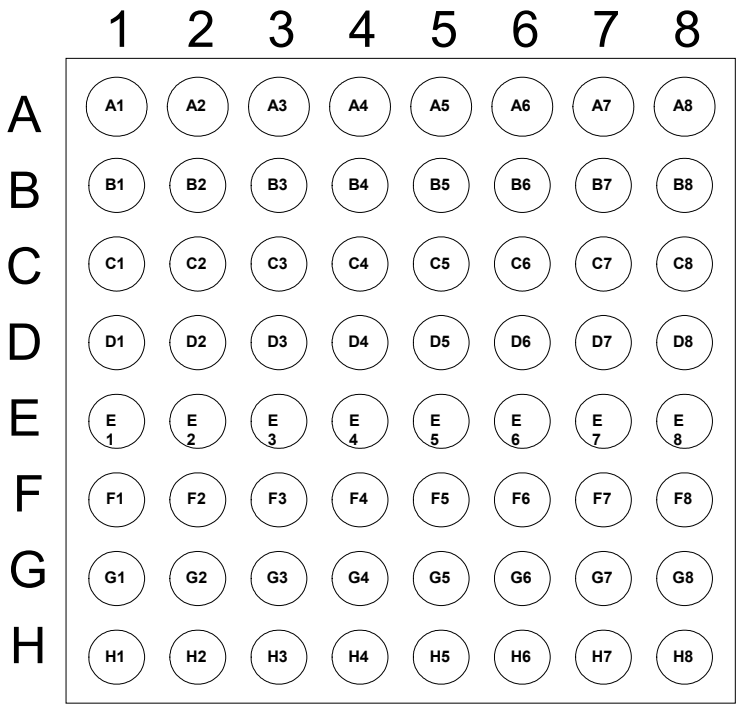
TD242LP pin assignment for the 64-pin LQFP



TD242LP LQFP 64-pin package (top view)

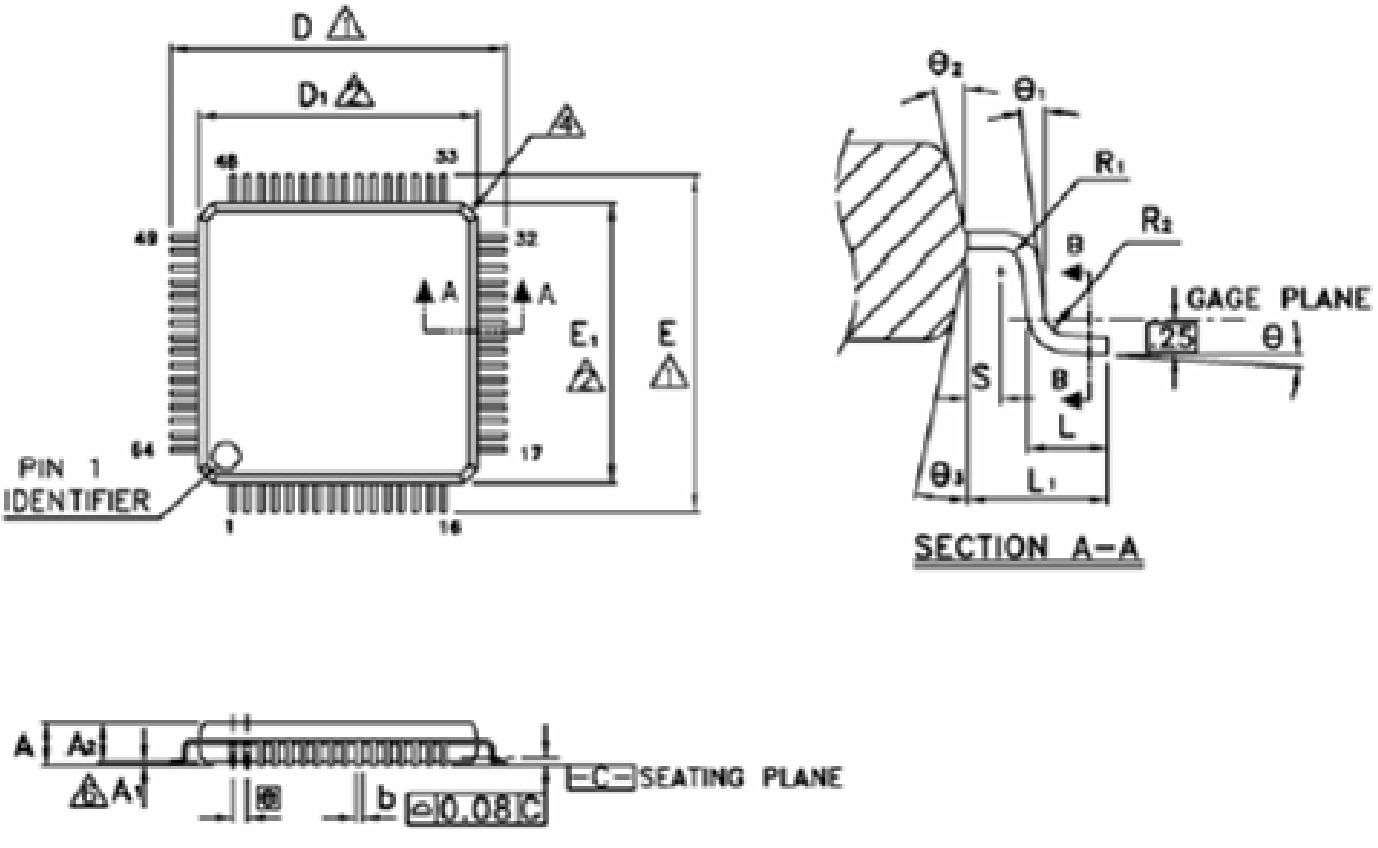
A1	OSC_2	C1	D_{10}	E1	D_{15}	G1	A_1
A2	OSC_1	C2	D_{11}	E2	$V_{DD2.5}$	G2	A_3
A3	V_{SSA}	C3	D_9	E3	/RD	G3	A_6
A4	D_6	C4	D_7	E4	V_{SS}	G4	A_8
A5	V_{DDW}	C5	CLKCFG	E5	V_{SS}	G5	A_{11}
A6	$V_{DD2.5}$	C6	D_2	E6	VBP	G6	/CS
A7	D_1	C7	VBUS	E7	/PO	G7	DP_1
A8	TEST	C8	V_{SSA}	E8	ID	G8	DM_1
B1	D_8	D1	D_{12}	F1	INT	H1	A_2
B2	$V_{DD2.5}$	D2	D_{13}	F2	/WR	H2	A_4
B3	$V_{DD2.5A}$	D3	D_{14}	F3	A_5	H3	V_{DDW}
B4	D_5	D4	V_{SS}	F4	A_7	H4	A_9
B5	D_4	D5	V_{SS}	F5	A_{10}	H5	A_{12}
B6	D_3	D6	ENVREG	F6	$V_{DD3.3}$	H6	$V_{DD2.5}$
B7	D_0	D7	$V_{DD3.3A}$	F7	/OC	H7	DP_2
B8	/RESET	D8	VREGOUT	F8	/EXVBO	H8	DM_2

TD242LP pin assignment for the 64-pin BGA



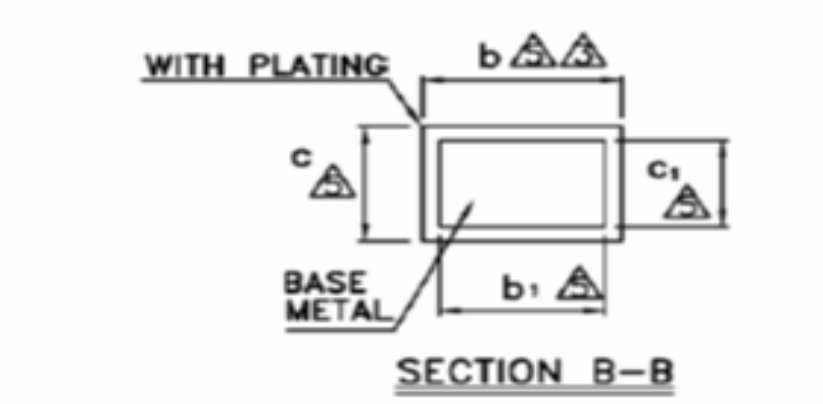
TD242LP BGA 64 – pin package (top view)

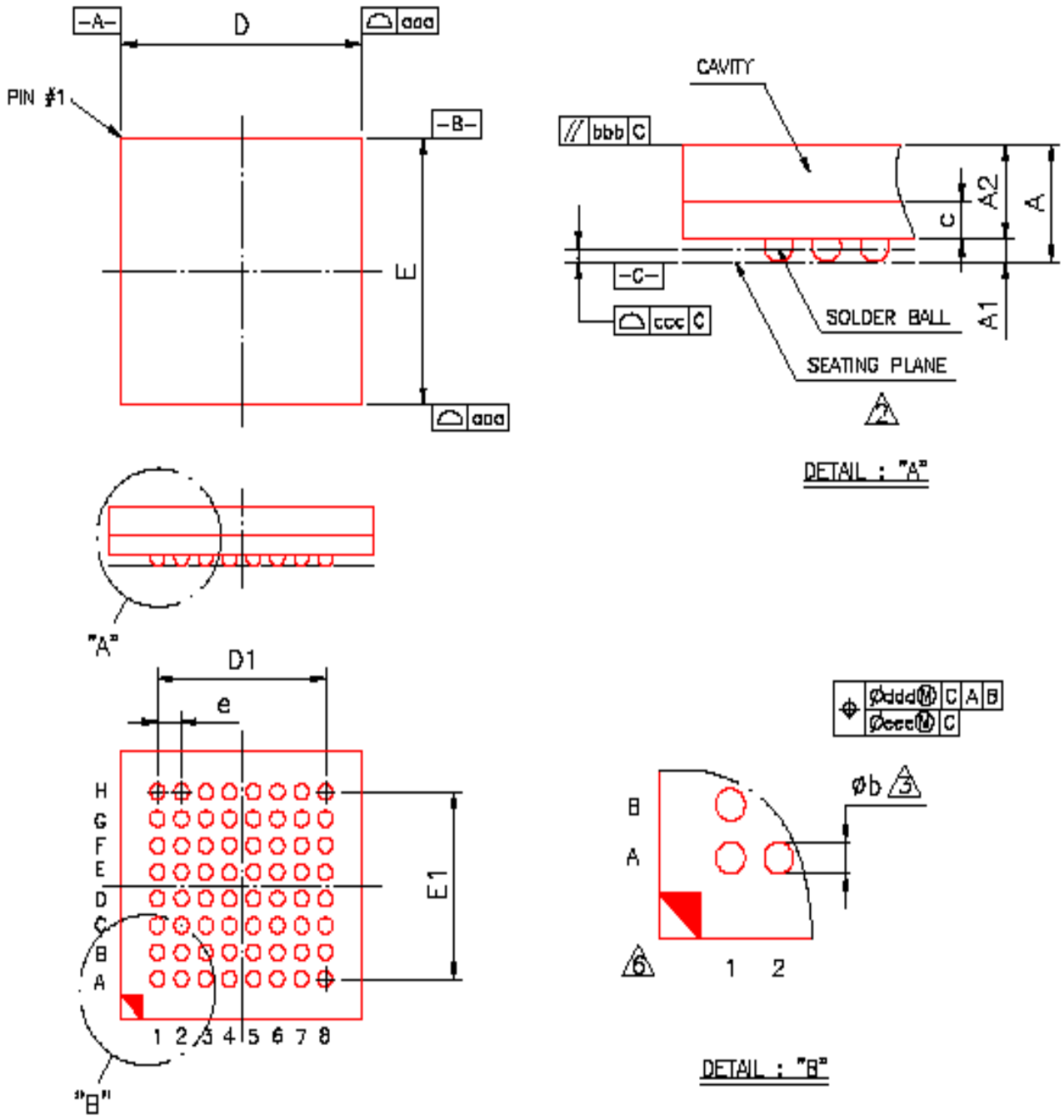
64 pin LQFP Mechanical Drawings:



Note: 0.5mm equals 0.019685 inches. Please use these numbers for the pin pitch.

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.012	0.015	0.018
b_1	0.17	0.20	0.23	0.012	0.014	0.016
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D_1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E_1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		




-A-
D
aaa
PIN #1
-B-
E
aaa
CAVITY
bbb C
c
A2
A
-C-
ccc C
SOLDER BALL
A1
SEATING PLANE
2
DETAIL : "A"
"A"
D1
e
H
G
F
E
D
C
B
A
E1
1 2 3 4 5 6 7 8
"B"
Øddd M C A B
Øeee M C
Øb 3
B
A
6
1 2
DETAIL : "B"

Note: 0.5mm equals 0.019685 inches. Please use these numbers for the pin pitch.

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	——	1.20	---	---	0.047
A1	0.18	0.21	0.26	0.008	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.38	0.40	0.013	0.014	0.016
D	4.90	5.00	5.10	0.193	0.197	0.201
E	4.90	5.00	5.10	0.193	0.197	0.201
D1	——	3.50	---	---	0.138	---
E1	——	3.50	---	---	0.138	---
e	——	0.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.12			0.005		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	8/8			8/8		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-205.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

OTG242LP USB On-The-Go Application Scenarios

Connect a Cellular phone to:
a cellular phone to transfer directories, songs, files
a PDA to exchange files, surf the web
a digital camera to upload pictures to the web
an MP3 player to exchange songs
a scanner to scan business cards
a portable hard disk to upload/download/broadcast music

Connect a Digital Camera to:
a digital camera to exchange pictures
a cellular phone to upload pictures to web
a printer to print pictures
a STB to view photos on a Television set

Connect an MP3 player to:
an MP3 player to exchange songs
a CD player to upload songs
a USB speaker to play songs
a portable hard disk to upload/download songs

Connect a Personal Computer to:
a cellular phone to synchronize/broadcast data, MP3 files
a PDA to synchronize data, transfer files
a digital camera to upload pictures and email out
a portable hard disk to store data
an MP3 player to upload/download songs

Connect a Digital Video Recorder to:
a cellular phone to transfer directories, songs, files
a PDA to exchange files, surf the web
a digital camera to upload pictures to the web

Connect a logic analyzer to:
a cellular phone to broadcast data
a PDA to transfer data
a digital camera to download waveforms
a printer to print waveforms
a projector to project onto a screen for anlysis

Connect a PDA to:
a keyboard for user interface
a PDA to exchange files
a digital camera to upload/download pictures
a portable disk drive to upload/download/store files
a printer to print files
a cellular phone to upload/download files
an MP3 player upload/download files

Connect a Portable Hard Disk to:
a digital video recorder to store video clips
an MP3 player to store songs
a digital camera to store pictures

Connect a CarKit (AutoPC) to: **(next revision of silicon will support Carkit Spec.)**
an MP3 player to play songs over a stereo connection
a cellular phone to enable handsfree telephone operation,
download latest phone list to your car

Applicable Documents and Specifications

- On-The-Go supplement to the USB 2.0 specification, Revision 1.0, Dec 18, 2001.
  URL Link: http://www.usb.org/developers/data/otg1_0.pdf
- USB 2.0 specification, URL Link: http://www.usb.org/developers/data/usb_20.zip
- USB On-The-Go Marketing Overview, Feb 26, 2002. URL Link: http://www.usb.org/data/developers/otg/presentations/london/OTG_marketing.pdf

Ordering information

Silicon/Boards	Pin/Ball Number	Package Type	TransDimension Order Number
TD242LP Silicon	64	TF-BGA	TDOTG242-00BC
	64	LQFP	TDOTG242-000C
TD242LP Silicon Lead (Pb)-Free	64	TF-BGA	TDOTG242-0FBC
	64	LQFP	TDOTG242-0F0C
BGA242S Board			TDOTG242-1010
PCE242 Board			TDOTG242-2000

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March 22, 2004
MU4001, Rev. 1.1