RAA210130

15V, 30A Single Channel Digital PMBus Step-Down Power Module

The RAA210130 is a fully PMBus enabled DC/DC step-down power supply capable of delivering up to 30A of current from a compact 10mmx13mmx7.8mm thermally enhanced BGA package.

Operating across an input voltage range of 4.75V to 15V, the RAA210130 offers adjustable output voltages down to 0.45V and achieves up to 96% efficiency. The RAA210130 implements the proprietary Renesas digital synthetic current modulation scheme to achieve an industry-leading combination of transient response, ease of tuning, and efficiency across the full load range. With minimal external components, simple configuration, robust fault management, and highly accurate regulation capability, implementing a high-performance regulator has never been easier.

A standard PMBus interface with PMBus V1.3 compatibility facilitates device configuration, addresses sequencing and fault management, provides real-time full telemetry and point-of-load monitoring, and detailed fault reporting. All of these features are conveniently accessible through the PowerNavigator™ software tool.

A fully customizable cycle-by-cycle current (peak overcurrent and peak undercurrent limit), voltage, and temperature protection scheme is capable of latching off or restarting the output in response to system faults.

Applications

- Server, telecommunications, storage, and data communications
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory

Features

- Complete digital power supply
- 30A single channel output current
  - 4.75V to 15V single rail input voltage
  - Up to 96% efficiency
- Programmable output voltage
  - 0.45V to 3.3V output voltage settings
  - ±0.7% accuracy over line, load, and temperature
- Advanced linear digital modulation scheme
  - Up to 1.25MHz fixed switching frequency operations
  - Dual edge modulation with optional diode braking for faster transient response
  - Excellent V_{OUT} transition performance.
- PMBus V1.3 compatible
  - Fully programmable through PMBus
  - Up to 16 user configurations stored in device Non-Volatile Memory (NVM)
  - Real-time telemetry for V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, and f_{SW}.
- Advanced soft-start/stop, sequencing, and margining
- Complete customizable over/under voltage, current, and temperature protections
- Black Box status recording with first fault indicator
- 10mmx13mmx7.8mm BGA package

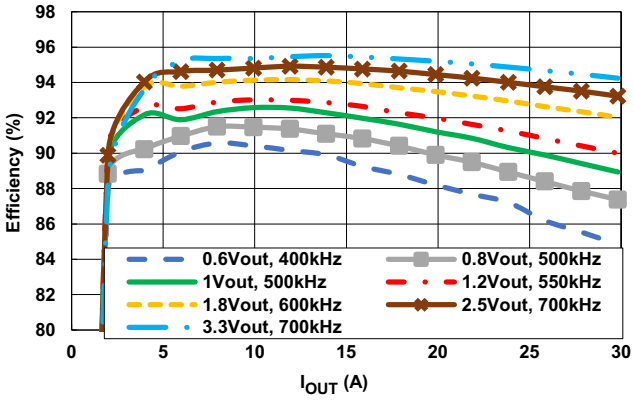


Figure 1. Efficiency vs Load Current at V_{IN} = 12V, with External 5V and 3.3V Supply

Contents

1. Overview

1.1 Block Diagram

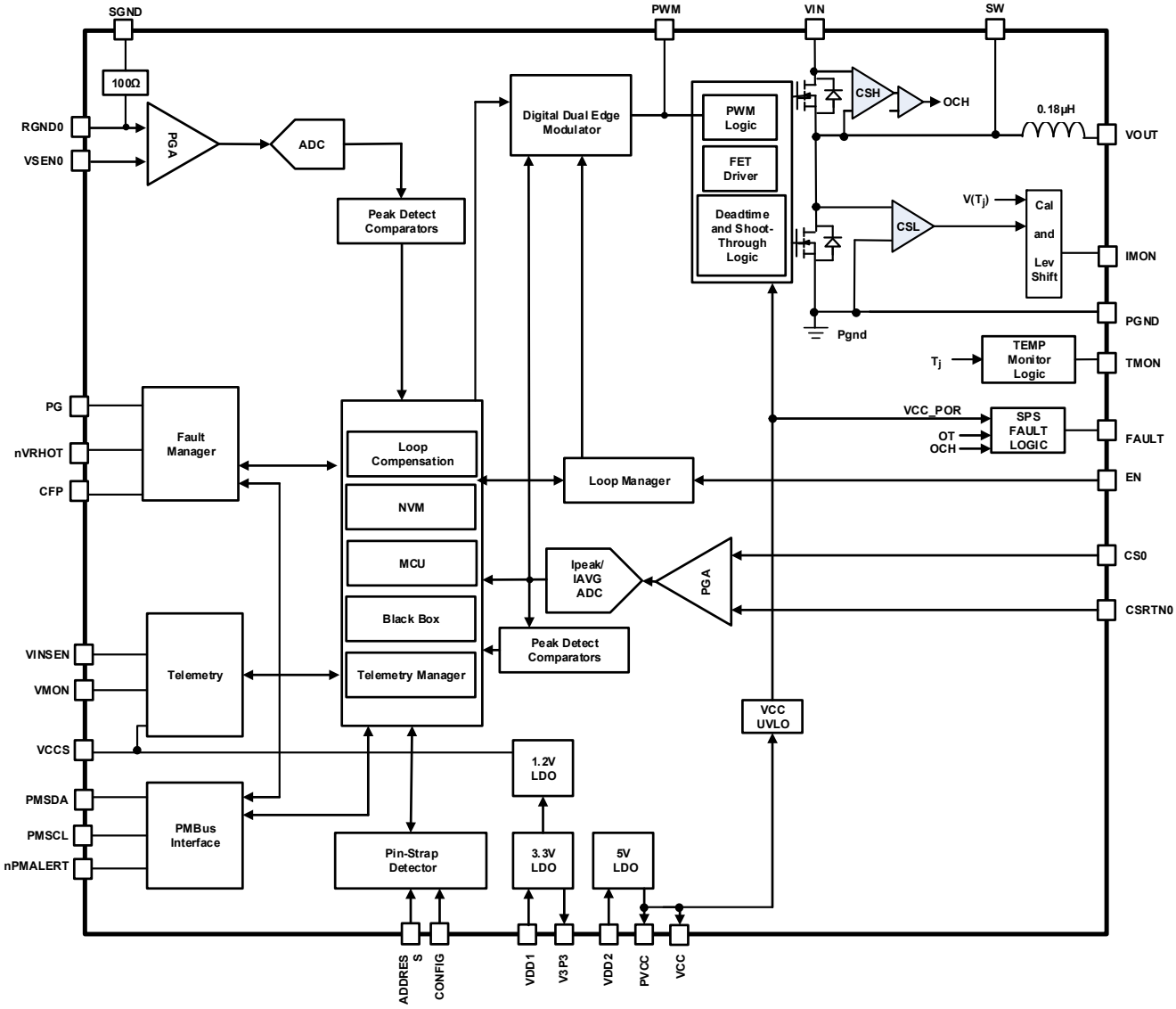


Figure 2. Block Diagram

1.2 Typical Applications

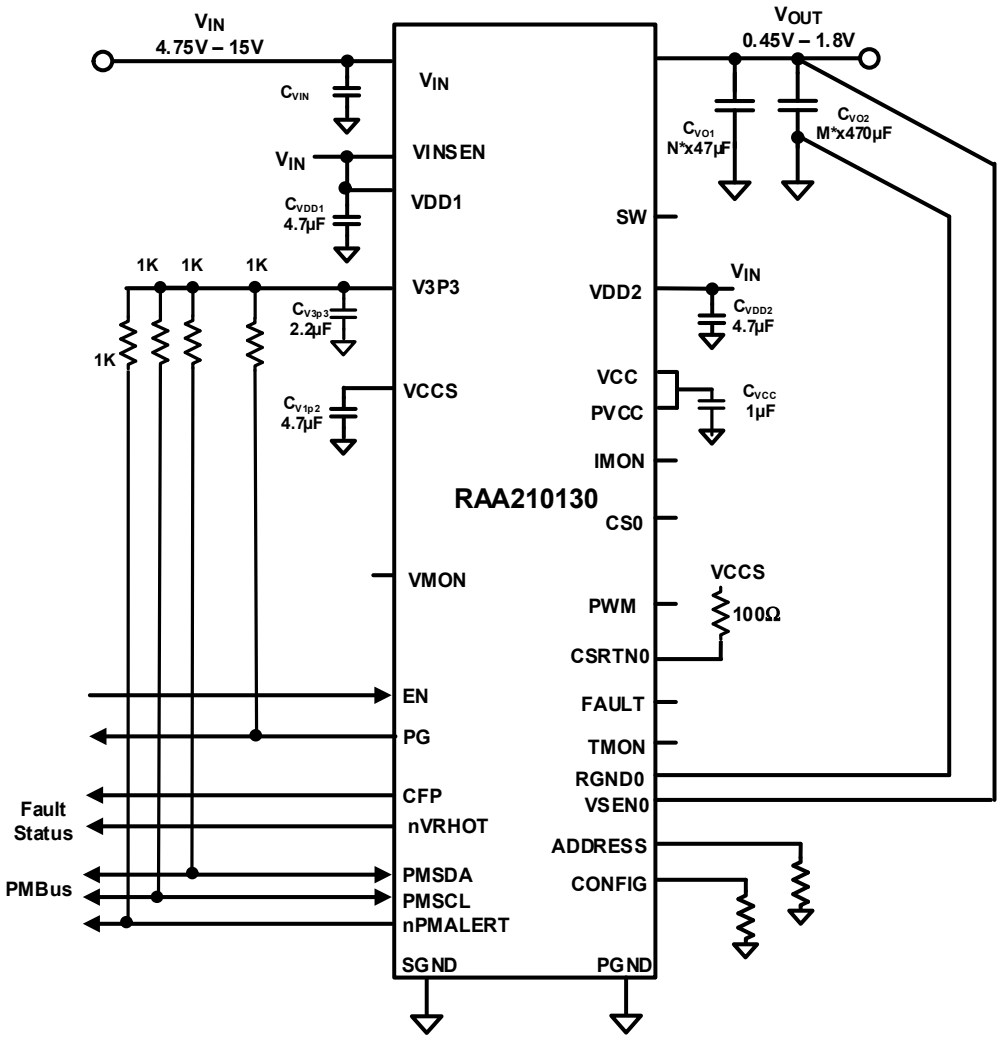


Figure 3. Typical Application Circuit for V_{IN} = 4.75V-15V and V_{OUT} = 0.45V-1.8V, 30A Load

*See the number of capacitors used in Table 1 for each output voltage.

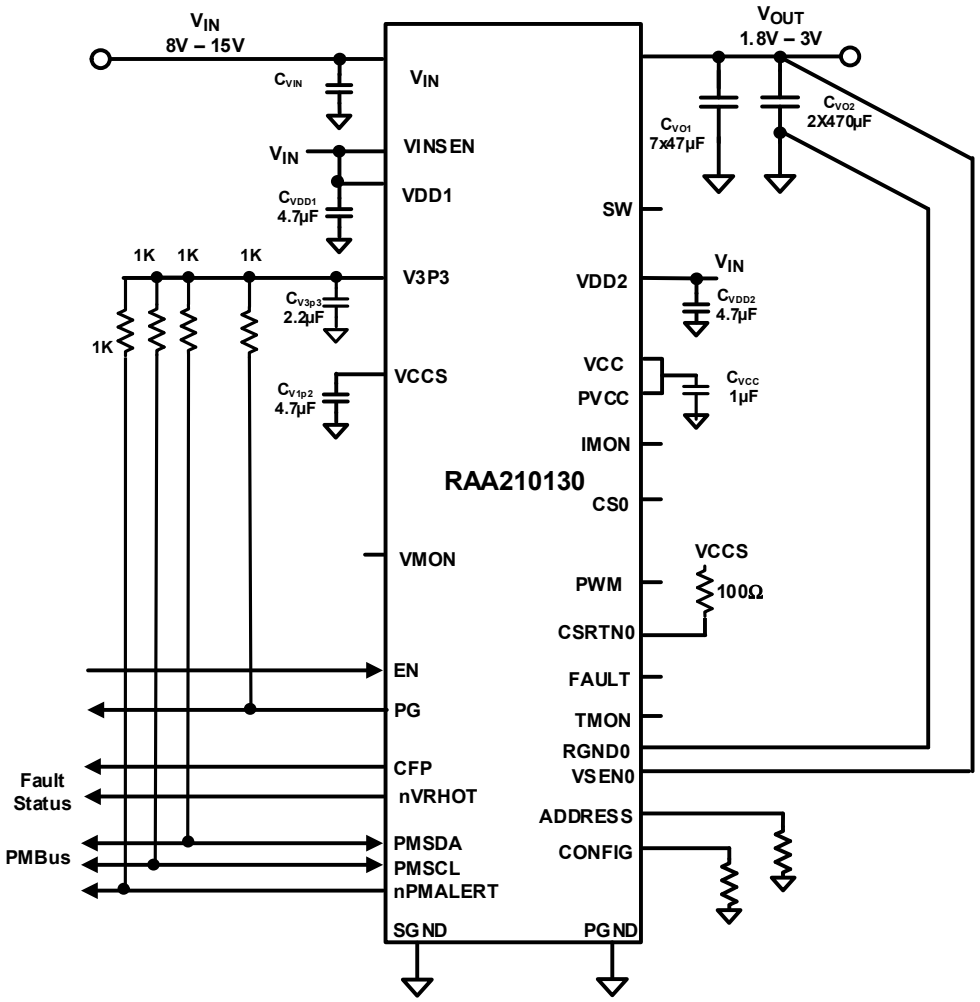


Figure 4. Typical Application Circuit for V_{IN} = 8V-15V, V_{OUT} = 1.8V-3V, 30A Load

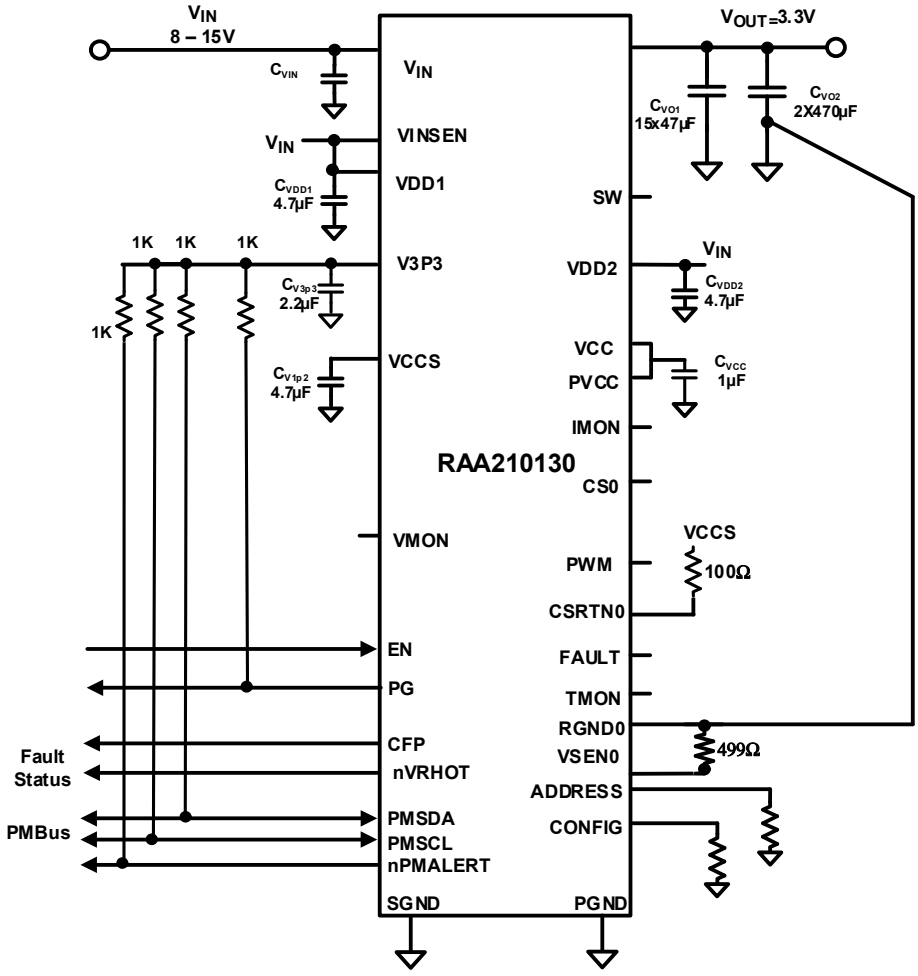


Figure 5. Typical Application Circuit for 3.3V Output, 30A Load

See the RAA210130 Design Matrix in Table 1 for recommended minimum V_{IN}, switching frequency, output capacitors combination, and other parameters for the various V_{OUT}.

Table 1. RAA210130 Design Matrix

V_{IN} Minimum (V)	V_{OUT} (V)	F (kHz)	C_{OUT}[1]
4.75	0.45	400	15x47µF + 3x470µF
4.75	0.6	400	10x47µF + 2x470µF or 15x47µF + 3x470µF
4.75	0.8	500	10x47µF + 2x470µF
4.75	0.9	500	10x47µF + 2x470µF
4.75	1	500	10x47µF + 2x470µF
4.75	1.05	500	10x47µF + 2x470µF
4.75	1.2	550	7x47µF + 2x470µF
4.75	1.35	600	7x47µF + 2x470µF
4.75	1.5	600	7x47µF + 2x470µF
4.75	1.8	600	7x47µF + 2x470µF
8	2.5	700	7x47µF + 2x470µF

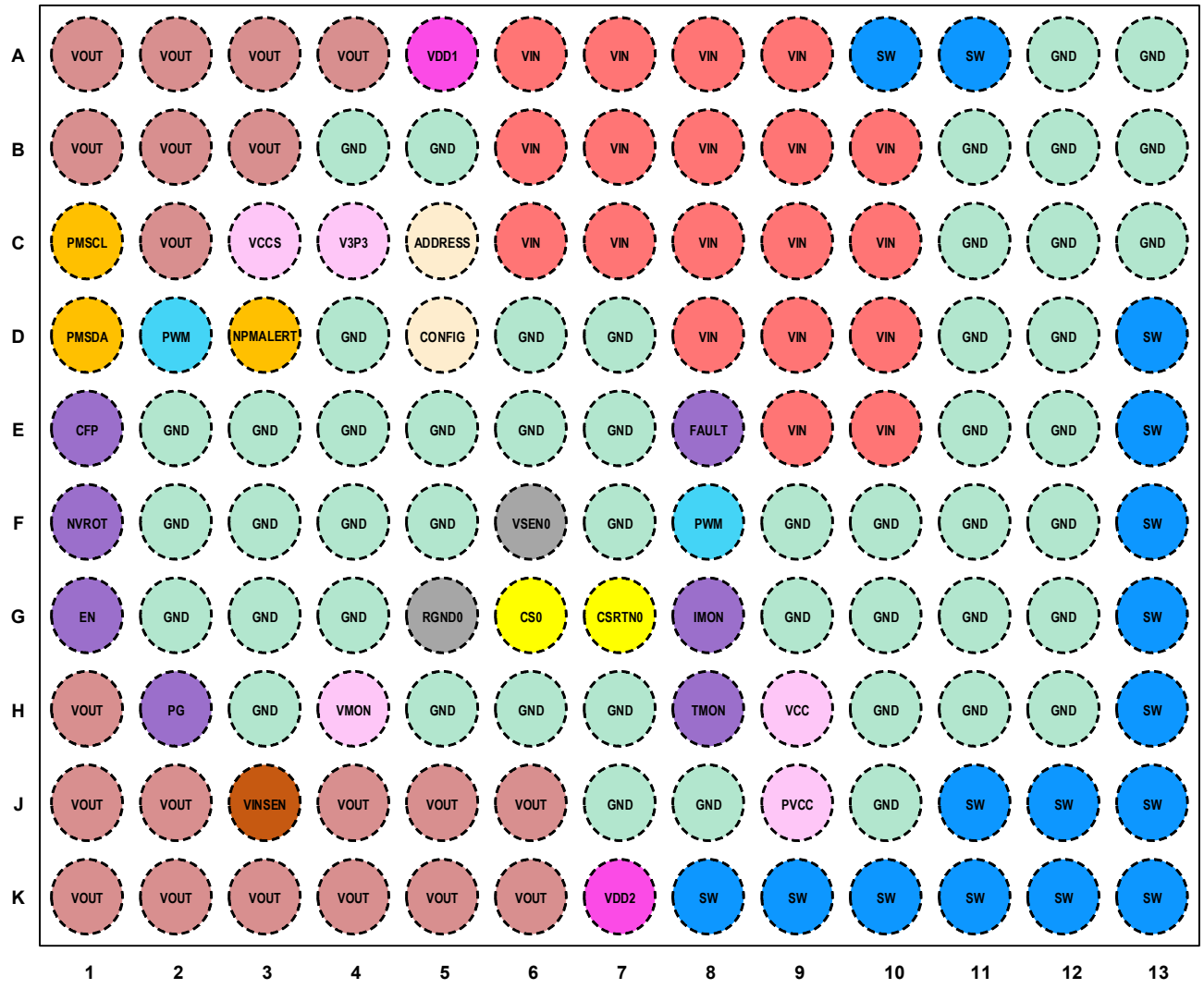
Table 1. RAA210130 Design Matrix (Cont.)

V_{IN} Minimum (V)	V_{OUT} (V)	F (kHz)	C_{OUT}[1]
8	3	700	7x47µF + 2x470µF
8	3.3	700	15x47µF + 2x470µF

1. For the output capacitors listed, use the capacitor part numbers listed below or ones that are similar.
   - 47µF: GRT21BC80G476ME13L
   - 470µF: T55D477M004C0008

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

See Table 4 for design layout considerations.

Pin Number	Pin Name	Description
A1, A2, A3, A4, B1, B2, B3, C2 H1, J1, J2, K1 K2, K3, K4, K5 K6, J4, J5, J6	VOUT	Regulated power module output. Apply the output between VOUT and PGND.
A5	VDD1	Input of 3.3V LDO, place a 2.2µF capacitor from this pin to GND.
A6, A7, A8, A9, B6, B7, B8, B9, B10, C6, C7 C8, C9, C10 D8, D9, D10 E9, E10	VIN	Power input. Connect the pads directly to an input rail in the range of 4.75V to 15V. Connect the input ceramic capacitors between VIN and PGND as close as possible to the module.
A10, A11, D13 E13, F13, G13 H13, J11, J12, J13, K8, K9 K10, K11, K12 K13	SW	Switch node connection. The pads are connected to the junction of the high-side MOSFET source, output filter inductor, drain of the low-side MOSFET, and return path for the UGATE high-side MOSFET drive.
A12, A13, B11, B12, B13, C11, C12, C13, D11, D12, E11, E12, F9, F10, F11 F12, G9, G10 G11, G12, H10, H11, H12, J10	PGND	Power ground. The pads are the sources of the lower MOSFET inside the module and should be connected to the negative terminals of the external input capacitors and output capacitors.
B4, B5, D4, D6, D7, E2, E3, E4, E5, E6, E7 F2, F3, F4, F5 F7, G2, G3, G4, H3 H5, H6, H7, J7 J8	SGND	Signal ground pads. The small-signal ground is common to all control circuitry and all voltage levels are measured with respect to this pin. Tie SGND to a solid low noise GND plane.
C1	PMSCL	Serial clock signal pin for the SMBus interface.
C3	VCCS	Internally generated 1.2V LDO logic supply from V3P3. Decouple with a capacitor of 4.7µF or greater (preferably MLCC type X5R or better).
C4	V3P3	Output of 3.3V LDO. Place a 2.2µF capacitor from this pin to GND.
C5	ADDRESS	SMBus/PMBus address selection pin.
D1	PMSDA	Serial data signal pin for the SMBus interface.
D2, F8	PWM	PWM output of digital controller, and Gate driver input of SPS. Because the PWM pins are connected inside the power module, no external routing is required for PWM connection.
F1	nVRHOT	Thermal warning indicator. This open-drain output is pulled low if a sensed over-temperature event occurs.
F6	VSEN0	Positive differential voltage sense input. Connect to a positive remote sensing point.
D3	nPMALERT	Open-drain output pin for alerting the SMBus host.
D5	CONFIG	Configuration ID selection pin. Attach a resistor from this pin to GND.
E1	CFP	Catastrophic fault protection output. This active-high, logic signal can be configured to alert the host to major fault events.
E8	FAULT	Open-drain output pin. Any fault of the SPS (overcurrent, over-temperature, shorted HFET, or V_{CC} UVLO) pulls this pin to ground. This pin can be connected to EN pin or used to signal a fault at the system level.
G1	EN	Input pin used for enable control of output.
G5	RGND0	Negative differential voltage sense input for output. Connect to a negative remote sensing point. Inside the module, RGND0 is connected to SGND using a 100Ω resistor.

Pin Number	Pin Name	Description
G6	CS0	The CS0 and CSRTN0 pins are current-sense inputs to the differential amplifier of the digital controller. CSRTN0 is also the input for the external reference voltage for the SPS IMON signal. Connect CSRTN0 to VCCS using a 100Ω resistor. Place the resistor close to CSRTN0.
G7	CSRTN0	
G8	IMON	SPS current monitor output, referenced to CSRTN0. IMON is pulled high to indicate an HFET shorted or overcurrent fault.
H2	PG	Open-drain, power-good indicator.
H4	VMON	Input voltage sense pin for driver supply voltage. Leave unconnected.
H8	TMON	Input pin for Smart Power Stage (SPS) temperature. Leave unconnected.
H9	VCC	+5V logic bias supply of SPS. Connect it to PVCC and place a high quality low ESR ceramic capacitor (~1µF/X7R) in close proximity from this pin to GND.
J3	VINSEN	Input voltage sense pin for the V_{IN} supply voltage. Connect to input voltage of power train.
J9	PVCC	Output of the 5V LDO, and +5V bias supply of SPS driver circuit.
K7	VDD2	Input of 5V LDO, place a 4.7µF capacitor from this pin to GND.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Input voltage to PGND	-0.3	28	V
VCC to SGND, PVCC to PGND	-0.3	6	V
VIN - PHASE Voltage for 5ns	-0.3	32	V
SW Voltage to PGND	-0.3	28	V
SW Voltage to PGND for 5ns	-10	32	V
V_{OUT} to PGND	-0.3	V3P3 + 0.3V	V
V3P3	-0.3	4.3	V
VCCS		1.6	V
VINSEN	-0.3	18	V
VDD1/VDD2 to SGND	-0.3	+20	V
PWM,CFP, nVRHOT, EN, PG, CSRTN, CS, RGND, VSEN, TMON,CONFIG, ADDRESS, nPMALERT, PMSCL, PMSDA to SGND	-0.3	V3P3 + 0.3V	V
FAULT, TMON, IMON to SGND	-0.3	+6.0	V

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JS-001-2017)	2.5	kV
Charged Device Model (Tested per JS-002-2018)	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JB} (°C/W)[2]
130 PIN 13x10 BGA Package	12	4.2

1. θ_{JA} is measured in free air with the module mounted on a 6-layer 3.8x3.5 inch evaluation board with significant coverage of 2oz copper on all layers. See TB379 for general metric information.
2. θ_{JB} is based on the board temperature (T_{board}) being taken at the location adjacent to the Module body near ball #H13.

Parameter	Minimum	Maximum	Unit
Junction Temperature	-55	+150	°C
Storage Temperature Range	-55	+150	°C
Pb-Free Reflow Profile	see TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Supply Voltage VIN, VDD1,VDD2	4.75	15	V
Output Voltage Range, V_{OUT}	0.45	3.3	V
Operating Junction Temperature Range, T_J	-40	+125	°C
Ambient Temperature Range, T_A	-40	+105	°C
3.3V (V3P3) Supply Total Supplied Current[1]			mA
PVCC Supply Total Supplied Current			mA

1. Total of current used by pull-ups to SDA, SCL, SALRT, DDC, EN, and PG (including Push-Pull configuration).

3.5 Electrical Specifications

V_{IN} = 12V, V_{3P3} = 3.3V, PV_{CC} = V_{CC} = 5V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A = -40°C to +85°C.**

Parameter	Test Conditions	Min[1]	Typ	Max[1]	Unit
V_{IN} Supply					
Input Voltage V_{IN} Range	V_{IN}, V_{DD1}, V_{DD2}	**4.75**		**15**	V
V_{IN} Supply Current					
Input Supply Current in PWM mode Operation	PWM mode, V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A		21		mA
Input Supply Current in Shutdown	Shutdown		224		µA
3.3V V_{3P3} LDO Supply					
V_{DD1} Range		**4.75**		**15**	V
I_{DD1} Nominal Current	PWM mode, V_{IN} = V_{DD} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, 600kHz frequency, PGOOD is floating		28		mA
I_{DD1} Shutdown Current	V_{3P3} = 3.3V; EN = 0V, no switching		20		mA
V_{3P3} Output voltage	PWM mode, V_{IN} = V_{DD} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, 600kHz frequency, PGOOD is floating	**3.136**	3.283	**3.431**	V
5V VCC and PVCC LDO Supply					
V_{DD2} Range		**4.75**		**15**	V
Logic Standby Current I_{VCC}	PWM = Open		5.0		mA
Gate Drive Standby Current I_{PVCC}	PWM = Open		10		µA
Logic Operational Current I_{VCC}	PWM = 300kHz		5.0		mA
Gate Drive Operational Current I_{PVCC}	PWM = 300kHz		10.3		mA
PVCC Output Voltage	PWM mode, V_{IN} = V_{DD1} = V_{DD2} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, 600kHz frequency, PGOOD is floating	**4.772**	4.997	**5.223**	V
1.22V VCCS LDO Supply					
Output Voltage			1.22		V
VCCS Maximum Current Capability	Excluding internal load		20		mA

V_{IN} = 12V, V_{3P3} = 3.3V, PV_{CC} = V_{CC} = 5V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A = -40°C to +85°C.** (Cont.)

Parameter	Test Conditions	Min[1]	Typ	Max[1]	Unit
Controller Power-On Reset (POR)					
V_{3P3} Brownout Threshold			2.95		V
VCCS Rising POR Threshold			1		V
VCCS Falling POR Threshold			0.9		V
Enable Input High Level (V_{IH})		**2**			V
Enable Input Low Level (V_{IL})				**0.8**	V
Controller POR to Initialization					
POR to Initialization Complete Time			15		ms
SPS Power-On Reset (POR) and Enable					
V_{CC} Rising POR Threshold			3.86	**4.20**	V
V_{CC} Falling POR Threshold		**3.20**	3.58		V
V_{CC} POR Delay to Operation			210		µs
V_{IN} Rising POR Threshold			2.4		V
V_{IN} Falling POR Threshold			2.1		V
Output Regulation and Characteristic					
Output Continuous Current Range		0		30	A
Output Voltage Adjustment Range	V_{IN} > V_{OUT} + 1.1V	0.45		3.3	V
Output Voltage Set-Point Accuracy[2]	Across line, load and temperature variation V_{OUT} set-point = 1.00V to 3.05V	**-0.7**		**0.7**	%
	Across line, load and temperature variation V_{OUT} set-point = 0.8V to 0.999V	**-8**		**8**	mV
	Across line, load and temperature variation V_{OUT} set-point = 0.45V to 0.799V	**-8**		**+8**	mV
Configurations Stored in Memory					
Maximum Number of Configurations Stored				28	
Maximum Number of Unique Configurations Stored				16	
Voltage Sense Amplifier					
Open Sense Current	Only at VSEN open detection during initialization period		220		µA
Input Impedance (VSEN - RGND)			140		kΩ
Maximum Common-Mode Input			V_{3P3} - 0.2		V
Differential Input Range (VSEN - RGND)				**3.05**	V
Output Current-Sense and Overcurrent Protection					
Current-Sense Accuracy		**-1**		**1**	%
Average Overcurrent Threshold Resolution			0.1		A

V_{IN} = 12V, V_{3P3} = 3.3V, PV_{CC} = V_{CC} = 5V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A = -40°C to +85°C.** (Cont.)

Parameter	Test Conditions	Min[1]	Typ	Max[1]	Unit
Cycle-by-Cycle Current Limiting Threshold Resolution			0.4		A
Digital Droop					
Droop Resolution			0.01		mV/A
Oscillators					
Accuracy of Switching Frequency Setting			±2		%
Switching Frequency Range		**0.2**		**1.25**	MHz
Soft-Start and V_{OUT} Transition Rates					
Minimum Soft-Start Ramp Time	Programmable minimum time		0.1		ms
Maximum Soft-Start Ramp Time	Programmable maximum time		10		ms
Soft-Start Ramp Rate Accuracy			±2		%
Minimum V_{OUT} Transition Rate	Programmable minimum rate		0.1		mV/µs
Maximum Fast V_{OUT} Transition Rate	Programmable maximum rate		5		mV/µs
V_{OUT} Transition Rate Accuracy		**-4**		**4**	%
Thermal Monitoring and Protection					
Temperature Sensor Range		**-50**		**150**	°C
Temperature Sensor Accuracy			±4.5		%
nVRHOT Output Low Impedance			9		Ω
Power-Good and Protection Monitors					
PG Output Low Voltage	I_{OUT} = 4mA load			**0.2**	V
PG Leakage Current	With pull-up resistor externally connected to VCC		5		µA
Overvoltage Protection Threshold Resolution			1		mV
Undervoltage Protection Threshold Resolution			1		mV
Input Voltage-Sense and Catastrophic Failure Protection (CFP) Output					
Input Voltage Accuracy	VINSEN to ADC accuracy		±2.5		%
Input Overvoltage Threshold Resolution			16		mV
CFP Output High Voltage	I_{OUT} = 8mA	**V_{CC} - 0.4**			V
CFP Output Low Voltage	I_{OUT} = 8mA			**0.4**	V
PMBus					
nPMALERT, PMSDA Output Low Level	I_{OUT} = 20mA			**0.4**	V
PMSCL, PMSDA Input High Level		**1.35**			V
PMSCL, PMSDA Input Low Level				**0.8**	V
PMSCL, PMSDA Input Hysteresis			80		mV

V_{IN} = 12V, V_{3P3} = 3.3V, PV_{CC} = V_{CC} = 5V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A = -40°C to +85°C.** (Cont.)

Parameter	Test Conditions	Min[1]	Typ	Max[1]	Unit
PMSCL Frequency Range		**0.01**		**2.00**	MHz
SPS Current Monitor					
CSRTN Voltage Range		**0.8**	1.2	**1.6**	V
I_{OUT} Current Gain Accuracy	≥10A, T_J = +0°C to +125°C, V_{CC} = 5V		±3		%
	≥10A, T_J = -40°C to +0°C,V_{CC} = 5V		±5		%
HFET Overcurrent Trip			100		A
IMON-REFIN at OCP		**1.1**	1.2	**1.3**	V
Temperature Monitor					
Over-Temperature Rising Threshold			145		°C
Over-Temperature Falling Threshold			130		°C
Over-Temperature Hysteresis			15		°C
Temperature Coefficient			8		mV/K
TMON Voltage at +25°C Temperature	$V(T_J) = 0.6V + (8mV \times T_J)$		0.80		V
TMON High at Over-Temperature		**2.3**	2.5	**2.7**	V
FAULT Pin					
Output Low Voltage			0.18	**0.26**	V
Overcurrent					
Default Overcurrent			40		A

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. V_{OUT} measured at the termination of the VSENP and VSENN sense points.

4. Typical Performance Graphs

V_{IN} = V_{DD1} = V_{DD2} = 12V, T_A = +25°C, unless otherwise stated.

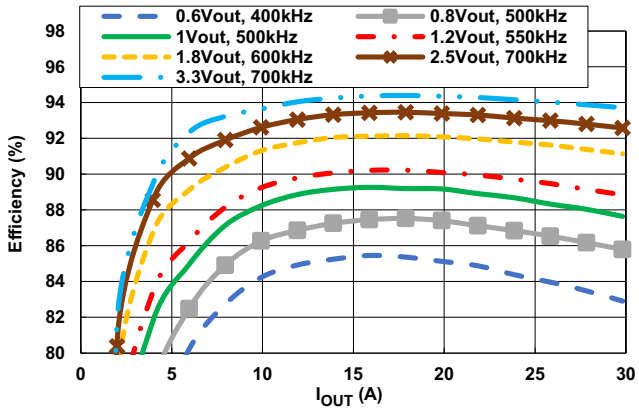


Figure 6. Efficiency vs Load Current at V_{IN} = 12V, with Internal 5V and 3.3V Supply

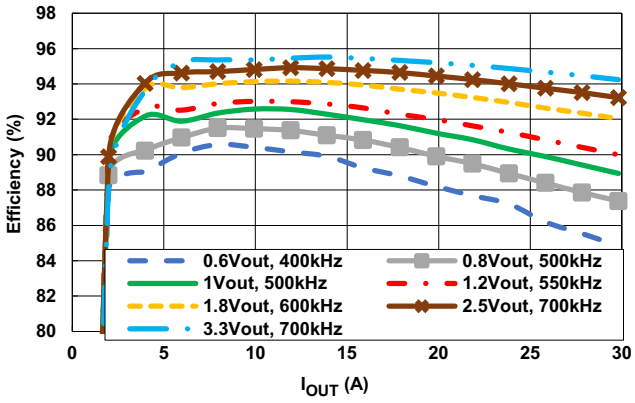


Figure 7. Efficiency vs Load Current at V_{IN} = 12V, with External 5V and 3.3V Supply

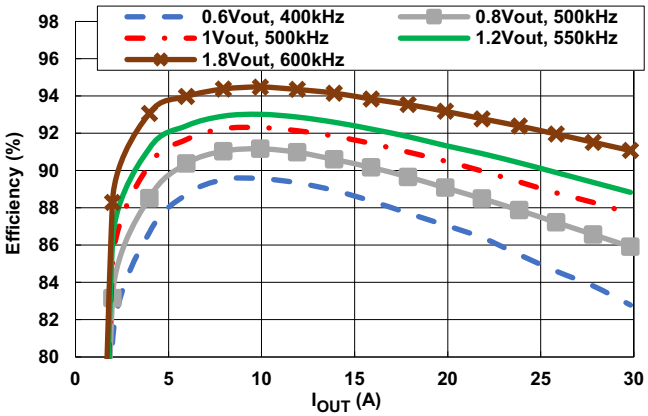


Figure 8. Efficiency vs Load Current at V_{IN} = 5V, with Internal 5V and 3.3V Supply

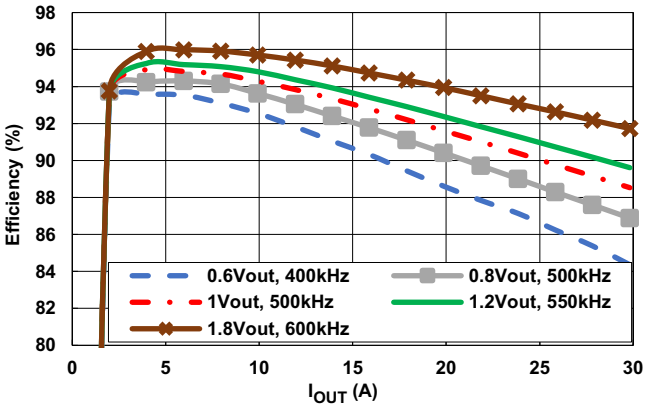


Figure 9. Efficiency vs Load Current at V_{IN} = 5V, with External 5V and 3.3V Supply

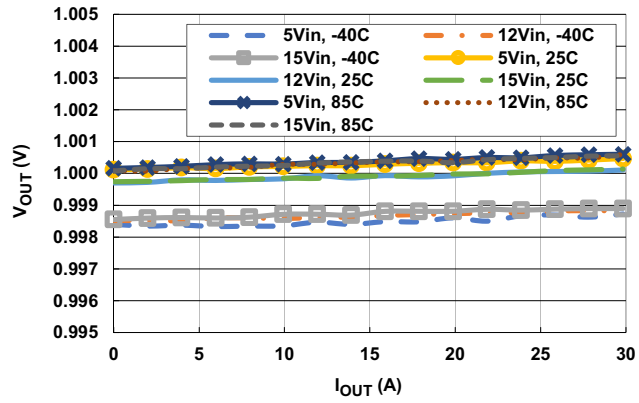


Figure 10. Load Regulation over V_{IN} and Temperature V_{OUT} = 1V, V_{IN} = 5V, 12V, 15V, Temperature = -40, 25, 85°C

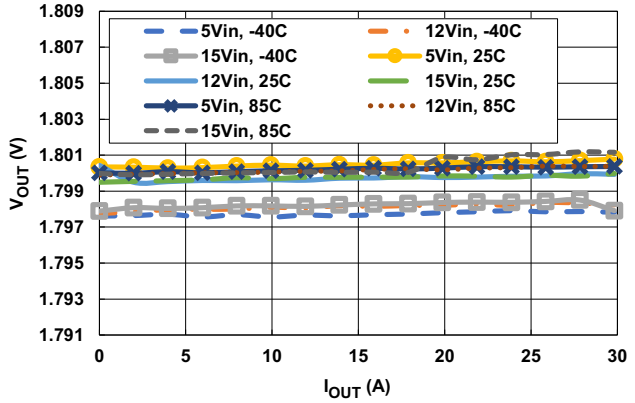


Figure 11. Load Regulation over V_{IN} and Temperature V_{OUT} = 1.8V, V_{IN} = 5V, 12V, 15V, Temperature = -40, 25, 85°C

V_{IN} = V_{DD1} = V_{DD2} = 12V, T_A = +25°C, unless otherwise stated. (Cont.)

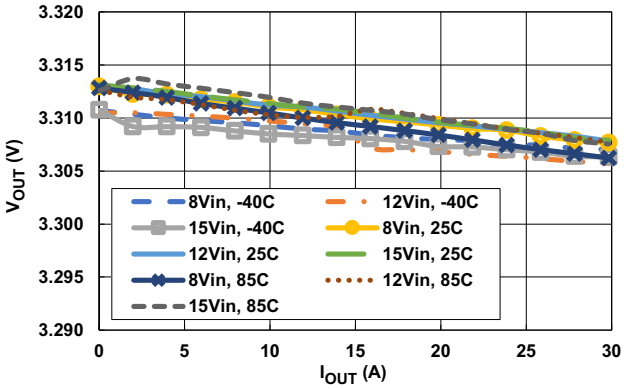


Figure 12. Load Regulation over V_{IN} and Temperature V_{OUT} = 3.3V, V_{IN} = 8V, 12V, 15V, Temperature = -40, 25, 85°C

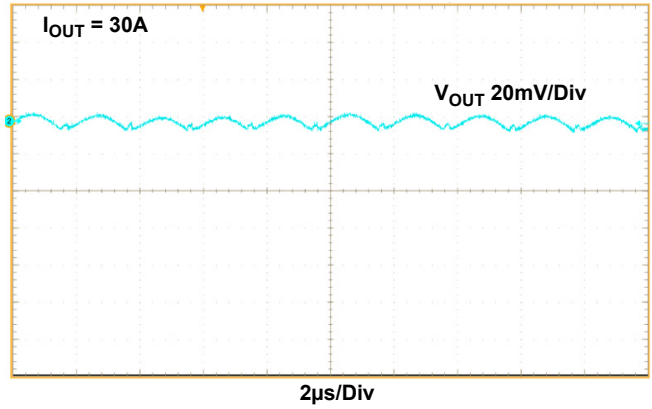


Figure 13. Output Ripple, V_{IN} = 12V, V_{OUT} = 0.8V, C_{OUT} = 10×47µF Ceramic + 2×470µF Polymer Capacitor

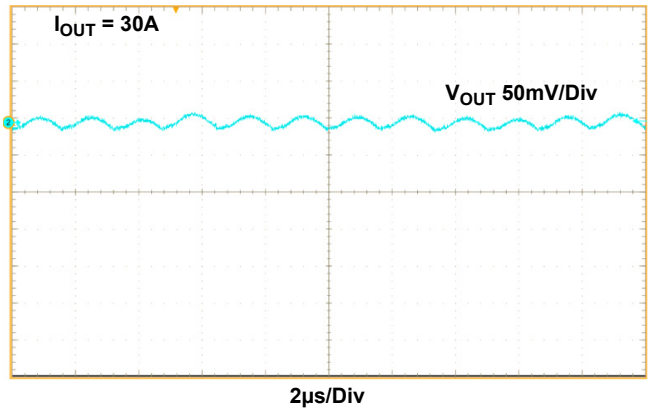


Figure 14. Output Ripple, V_{IN} = 12V, V_{OUT} = 1.8V, C_{OUT} = 7×47µF Ceramic + 2×470µF Polymer Capacitor

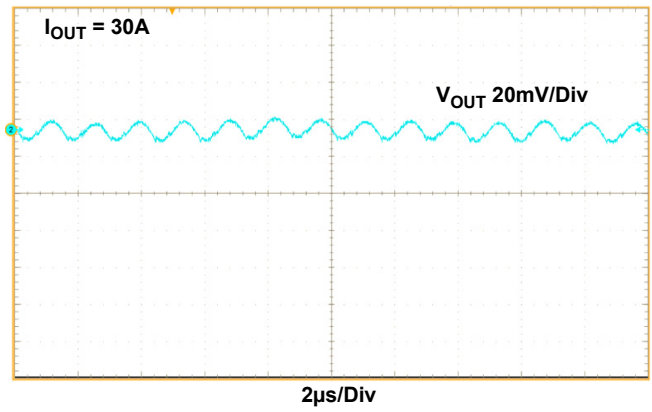


Figure 15. Output Ripple, V_{IN} = 12V, V_{OUT} = 3.3V, C_{OUT} = 15×47µF Ceramic + 2×470µF Polymer Capacitor

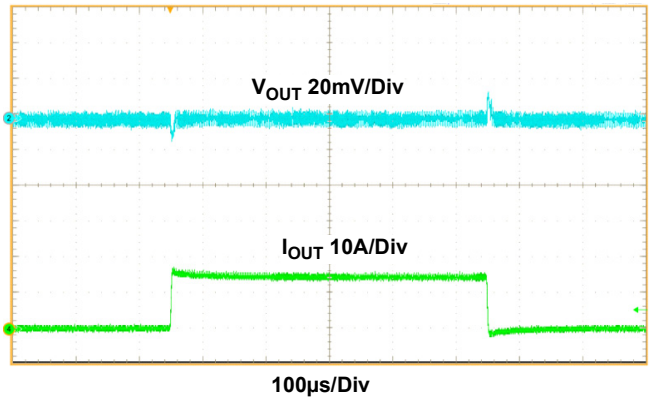


Figure 16. Transient Response, V_{IN} = 12V, V_{OUT} = 0.8V, 0A to 15A to 0A, 5A/µs Step Load, C_{OUT} = 10×47µF Ceramic + 2×470µF Polymer Capacitor

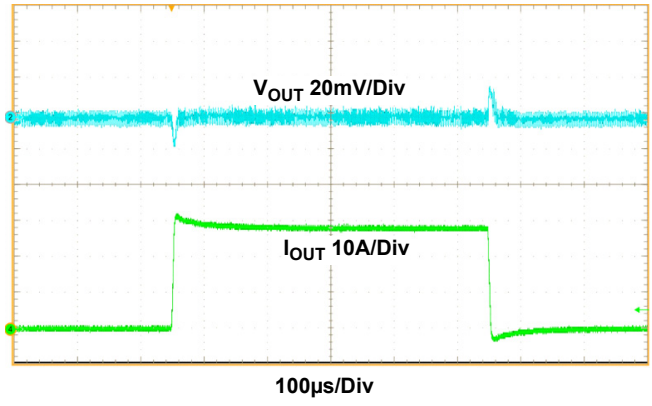


Figure 17. Transient Response, V_{IN} = 12V, V_{OUT} = 0.8V, 0A to 30A to 0A, 5A/µs Step Load, C_{OUT} = 10×47µF Ceramic + 2×470µF Polymer Capacitor

V_{IN} = V_{DD1} = V_{DD2} = 12V, T_A = +25°C, unless otherwise stated. (Cont.)

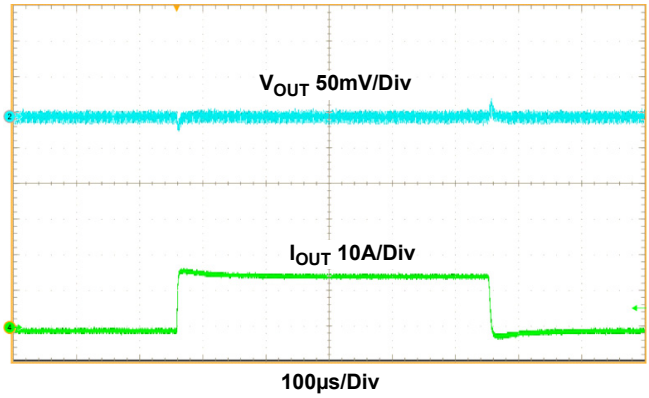


Figure 18. Transient Response, V_{IN} = 12V, V_{OUT} = 1.2V, 0A to 15A to 0A, 5A/µs Step Load, C_{OUT} = 7×47µF Ceramic + 2×470µF Polymer Capacitor

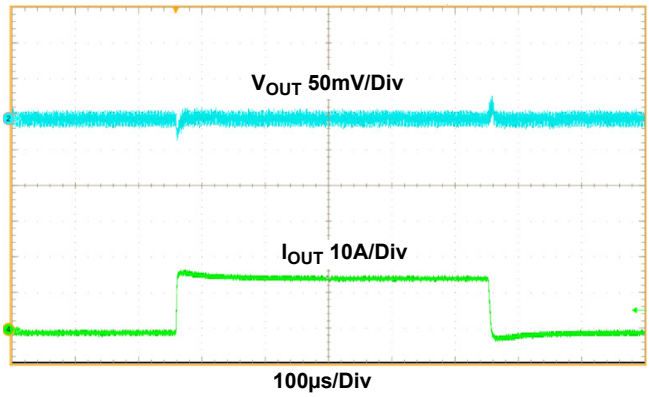


Figure 19. Transient Response, V_{OUT} = 1.8V, 0A to 15A, 5A/µs Step Load, C_{OUT} = 7×47µF Ceramic + 2×470µF Polymer Capacitor

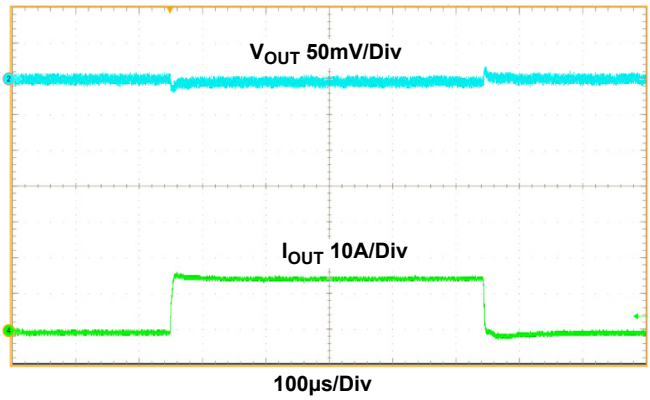


Figure 20. Transient Response, V_{OUT} = 3.3V, 0A to 15A, 5A/µs Step Load, C_{OUT} = 15×47µF Ceramic + 2×470µF Polymer Capacitor

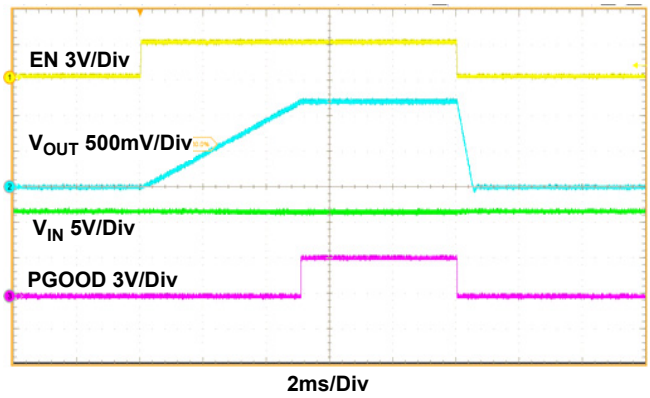


Figure 21. Start-Up and Shutdown Waveform by Pin Enable, V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 30A.

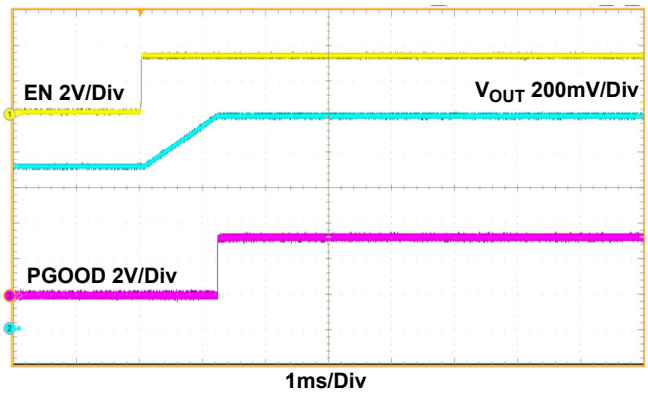


Figure 22. Pre-Biased Startup Waveform, V_{IN} = 12V, Pre-Biased Voltage = 0.9V, V_{OUT} = 1.2V, I_{OUT} = 0A

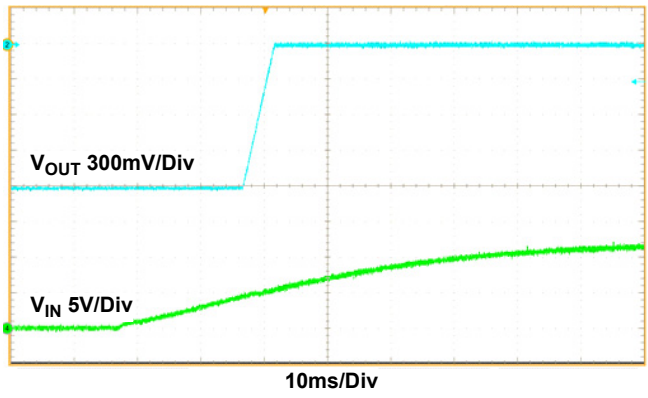


Figure 23. Startup by V_{IN}, V_{IN} = 0V to 12V, V_{OUT} = 1.2V, I_{OUT} = 30A

V_{IN} = V_{DD1} = V_{DD2} = 12V, T_A = +25°C, unless otherwise stated. (Cont.)

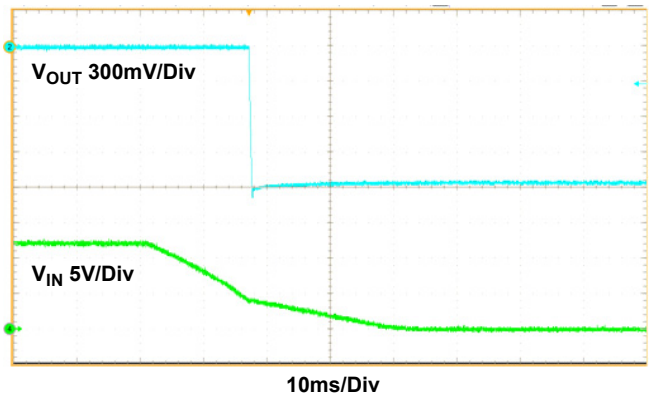


Figure 24. Shutdown by V_{IN}, V_{IN} = 12V to 0V, V_{OUT} = 1.2V, I_{OUT} = 15A

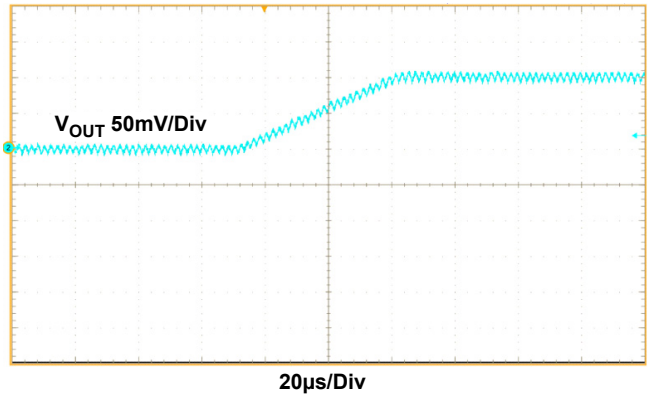


Figure 25. V_{OUT} Transition, V_{OUT} = 0.8V to 0.9V, Rate = 2mV/µs

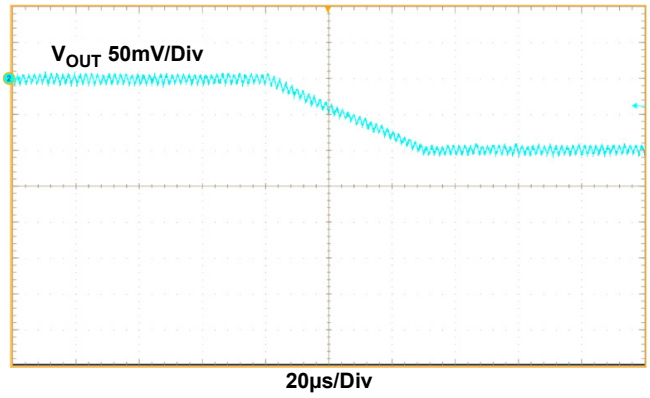


Figure 26. V_{OUT} Transition, V_{OUT} = 1.2V to 1.1V, Rate = -2mV/µs

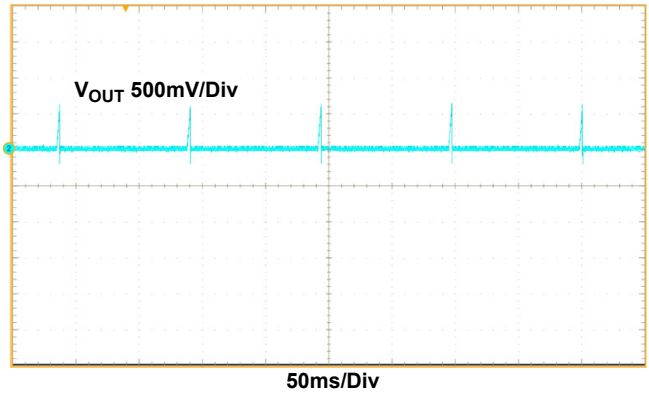


Figure 27. Short Output in Retry Mode, V_{IN} = 12V, V_{OUT} = 1.2V

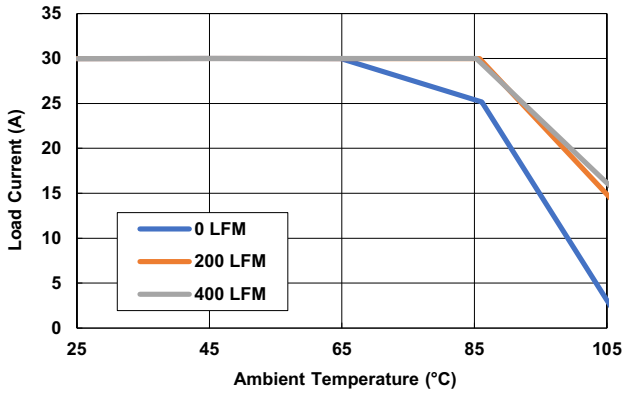


Figure 28. Thermal Derating Curve, V_{IN} = 12V, V_{OUT} = 0.8V, f_{SW} = 500kHz[1]

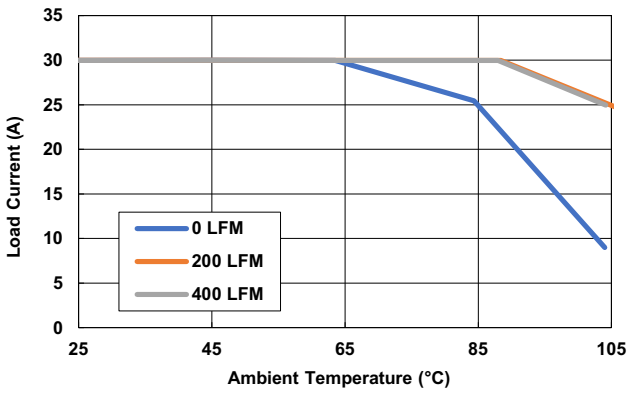


Figure 29. Thermal Derating Curve, V_{IN} = 5V, V_{OUT} = 0.8V, f_{SW} = 500kHz[1]

V_{IN} = V_{DD1} = V_{DD2} = 12V, T_A = +25°C, unless otherwise stated. (Cont.)

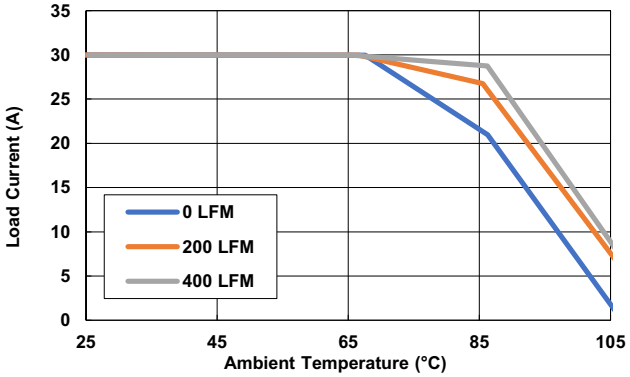


Figure 30. Thermal Derating Curve, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 600kHz[1]

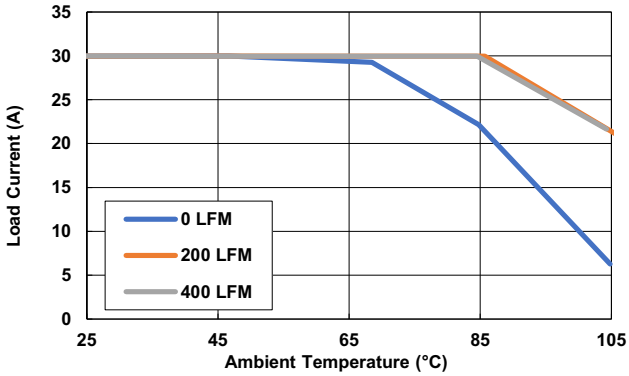


Figure 31. Thermal Derating Curve, V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 600kHz[1]

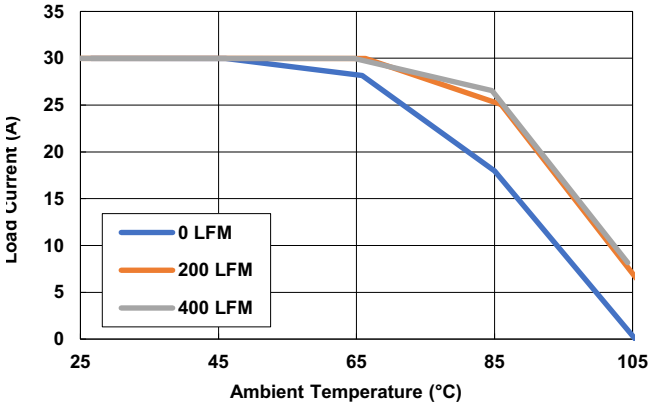


Figure 32. Thermal Derating Curve, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 700kHz[1]

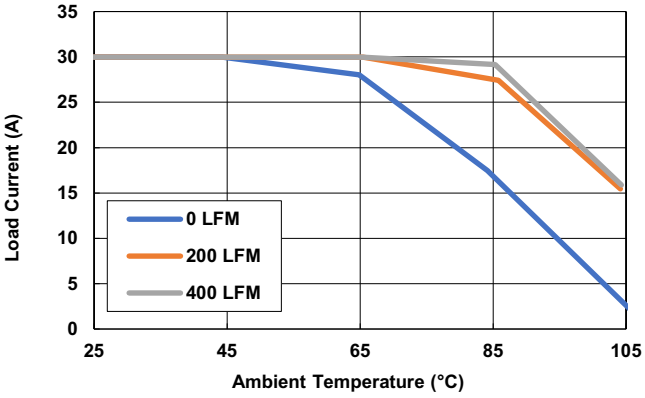


Figure 33. Thermal Derating Curve, V_{IN} = 8V, V_{OUT} = 3.3V, f_{SW} = 700kHz[1]

1. The thermal derating curves are obtained by measuring temperatures of hotspots of the module for various ambient temperatures in a temperature controlled chamber. When any of the hotspots reaches a temperature of 115C before 30A is reached, the current is recorded. When 30A is reached before 115C is reached, the maximum current for that ambient temperature would be 30A.

5. Initializing the Power Module

The RAA210130 is an innovative single-channel step-down power supply that provides up to 30A continuous load current. Inside the module, there is a full digital controller and a Smart Power Stage (SPS) with both high side and low side MOSFET. The full digital control loop of the RAA210130 achieves precise control of the entire power conversion process, resulting in a flexible and easy-to-use device. An advanced linear digital modulation scheme is implemented to achieve the industry-best combination of transient response, ease of tuning, and efficiency across the full load range. This achieves a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

An extensive set of power management functions is fully integrated and configured through the PowerNavigator software tool and using simple pin connections according to the tables provided in the following sections. The user configuration can be saved in an internal Nonvolatile Memory (NVM). All functions can be configured and monitored through the SMBus hardware interface using standard PMBus commands, allowing excellent flexibility.

5.1 Power-On Reset (POR)

The RAA210130 initialization begins after V_{3P3} crosses its rising POR threshold. When POR conditions are met, basic digital subsystem integrity checks begin. During this process, the controller starts the telemetry subsystem, configures its PMBus address according to the ADDRESS pin resistor value, loads the selected user configuration from NVM as indicated by the CONFIG pin resistor value, checks fault status, and prepares for regulation. The PWM pins are held in tri-state until the device is commanded to regulate. Figure 34 shows the device initialization sequence.

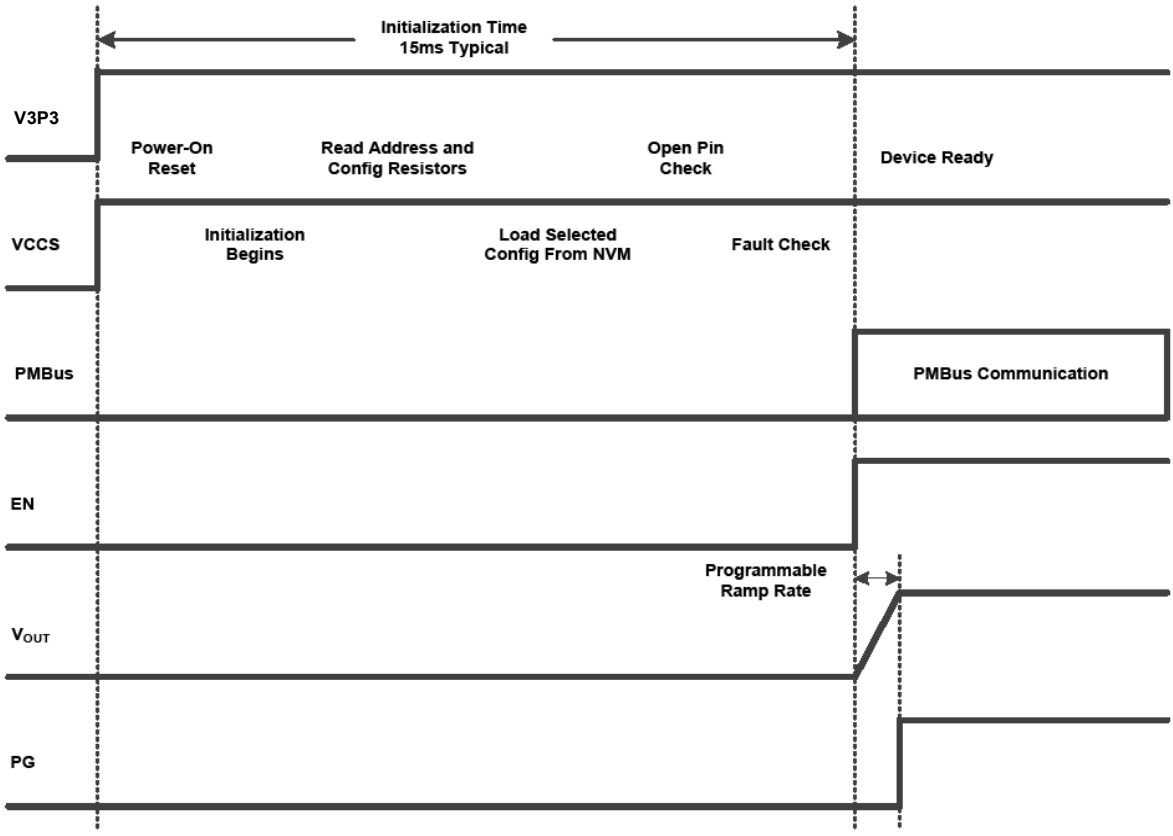


Figure 34. Simplified PMBus Initialization Timing Diagram

5.2 Selecting the PMBus Address

A resistor reader selects the PMBus slave address. The ADDRESS pin reads the value of a resistor connected to GND to determine the PMBus address to use during host communication. Table 2 shows the $R_{ADDRESS}$ values to specify the PMBus slave addresses (7-bit).

Table 2. Resistor Value to PMBus Address Map

R Value (Ω)	PMBus Address	R Value (Ω)	PMBus Address
0	60	5230	51
162	61	5900	52
316	62	6650	53
487	63	7500	54
681	64	8450	55
887	65	9530	56
1130	66	10700	57
1370	67	12100	58
1650	45	13700	59
1960	46	15400	5A
2320	47	17400	5B
2670	4C	19600	5C
3090	4D	22100	5D
3570	4E	24300	5E
4120	4F	27400	5F
4640	50	30100	68

5.3 Selecting the User Configurations

At power-up, a user configuration is loaded for operation. The CONFIG pin reads the value of a resistor connected to GND to determine which user configuration is loaded. The RAA210130 supports 15 preloaded distinct configuration identifiers with one configuration ID left open. Table 3 provides the R_{CONFIG} value corresponding to each configuration identifier that stores a particular V_{OUT} configuration. A total of 28 one-time programmable non-volatile memory locations exist in the controller, therefore another 13 locations are available to store new user configurations or overwrite existing ones. Only the most recent configuration for a given configuration ID is loaded. When all 28 memory locations have been written, RAA210130 no longer accepts attempts to write to NVM. PowerNavigator provides a simple interface to store and load configurations.

Table 3. Resistor Value to CONFIG ID Map

R Value (Ω)	Configuration ID	Output Voltage (V)	R Value (Ω)	Configuration ID	Output Voltage (V)
0	0	3.30	1650	8	1.00[1]
162	1	3.00	1960	9	0.90[1]
316	2	2.50	2320	10	0.85
487	3	1.80	2670	11	0.84[1]
681	4	1.70	3090	12	0.82[1]
887	5	1.35	3570	13	0.80[1]

Table 3. Resistor Value to CONFIG ID Map (Cont.)

R Value (Ω)	Configuration ID	Output Voltage (V)	R Value (Ω)	Configuration ID	Output Voltage (V)
1130	6	1.20	4120	14	0.95
1370	7	1.05	4640	15	Open

1. When these configuration IDs and output voltages are selected, use EEF-GX0D471R, which is 2V rated instead of T55D477M004C0008, which is 4V rated.

5.4 Configuring the Device

You can configure the RAA210130 to generate a configuration file using PowerNavigator and either directly load to the device RAM or program to the device NVM. During device initialization, the controller attempts to load a configuration from NVM. If no configuration is found, the device remains in a wait state with the PWM pins tri-stated. The device ignores attempts to enable and waits until a configuration is directly loaded using PowerNavigator. The features and functions of the RAA210130 described in this datasheet are all configured using PowerNavigator. The datasheet provides a fundamental understanding of device behavior and design information. Additional details regarding the configuration process are provided in the PowerNavigator GUI.

6. Operating the Device

After the RAA210130 initializes and a configuration is loaded, it is ready for operation.

The RAA210130 has several performance enhancing features that enable it to meet the most stringent voltage regulation and efficiency demands. The synthetic current modulator provides excellent transient response to support the latest generation of ASICs and CPUs. Smart Power Stage (SPS) current sense enables optimal design of the RAA210130. The power module also supports a full complement of high resolution telemetry including the temperature sense. The following sections provide more detail about these features.

6.1 Input Voltage Sensing

Input voltage is monitored using the VINSEN pin. Connect the VINSEN pin to input voltage of the module. Input voltage is monitored continuously and regulation is stopped anytime the sensed input voltage falls outside the boundaries established by configuration settings associated with the parameters V_{IN} ON, V_{IN} OFF, V_{IN} Overvoltage Fault Limit, and V_{IN} Undervoltage Fault Limit.

6.2 Lossless Input Current and Power Sensing

Input current telemetry is provided using an input current synthesizer. By using the ability of the RAA210130 to precisely determine its operational conditions, the input current can be synthesized to a high degree of accuracy without the need for a lossy sense resistor. With a precise knowledge of the input current and voltage, the input power can be computed.

6.3 VMON Voltage Sensing

The bias supply voltage of the SPS, PVCC, is monitored by the VMON pin with programmable voltage ranges. The VMON input pin can be used to inhibit rail operation when the sensed voltage falls outside the boundary established by the configuration settings that are associated with the parameters VMON_ON and VMON_OFF. If the RAA210130 is prevented from operating because of a VMON excursion, it restarts if the sensed voltage returns to the specified range.

6.4 Enabling and Soft-Starting the Device

The output of the RAA210130 is enabled using the enable pin or PMBus. The enable method selection is configured in PowerNavigator. When the device is commanded to regulate an output, it begins its soft-start

sequence. Soft-start moves V_{OUT} smoothly to the programmed voltage. Soft-start timing is programmed using the TON_DELAY (60h) and TON_RISE (61h) PMBus commands.

If a pre-existing voltage bias exists on the output, the PWM signals are held in tri-state until the soft-start ramp reaches the pre-bias level. The tri-state prevents the converter from sinking current and pulling the pre-bias down. No special configuration is required to enable this operation.

6.5 Disabling the Device

Similar to the enabling process, output can be disabled using the EN pin or PMBus. The RAA210130 is configured to disable in two ways:

- **Immediate OFF**: Immediately ceases regulation and tri-states the PWM pins.
- **Soft OFF**: Actively ramps the output voltage down to 0V before ceasing activity as programmed in TOFF_DELAY (64h) and TOFF_FALL (65h) PMBus commands.

6.6 Diode Braking

Applications that support loads with large transient current demands often have significant output voltage overshoot when the load current demand drops suddenly. In some cases, diode braking can allow overshoot reduction at the expense of thermal dissipation in the low-side MOSFET. When enabled, the controller automatically turns off the low-side FETs during load release resulting in decreased V_{OUT} overshoot. With diode braking enabled, the feedback signal is monitored and if it exceeds a user-set value, the LFET body diode braking comes into action. Braking turn-on/turn-off thresholds, duration, and blanking time are available to modify with the use of the PowerNavigator.

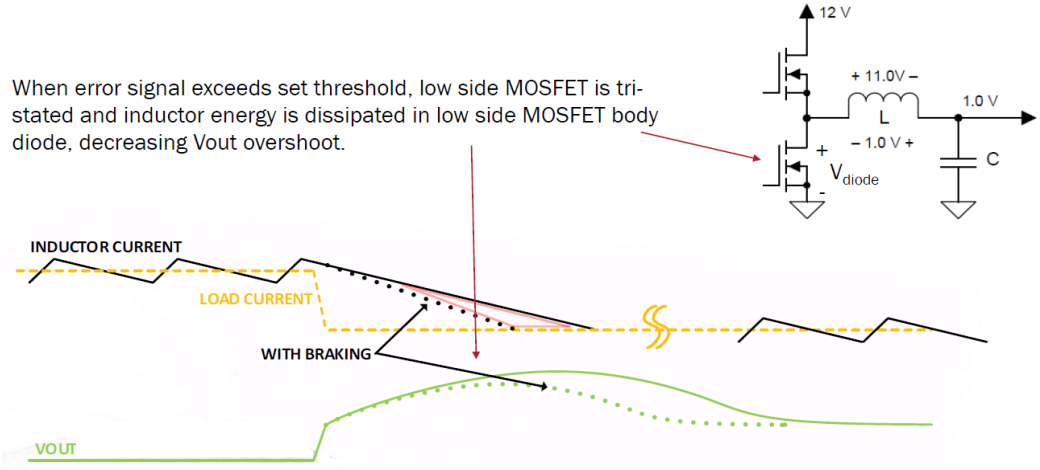


Figure 35. Body Diode Braking Operation

6.7 Switching Frequency

Switching frequency is independently programmable from 200kHz to 1.25MHz.

6.8 Output Current Sensing

The RAA210130 uses smart power stage current sensing. Inside the module, the differential input CS0 and CSRTN0 pins of the digital controller are connected to the SPS current sense pins.

6.9 Temperature Sensing

The RAA210130 monitors the controller temperature and the SPS temperature using the TMON pin.

7. Fault Monitoring and Protection

The RAA210130 includes an extensive fault management system that integrates with high performance host controllers, supporting unprecedented remote system management and debugging capability. If a fault condition occurs, the controller de-asserts the PG pin and alerts the host using the nPMALERT pin. You can optionally configure the Catastrophic Failure Protection (CFP) to assert on select faults for additional protection measures at the system level. The RAA210130 also provides a Black Box, which is a recorder with extensive fault logging to support system level debug.

Fault controls are independently enabled and associated fault responses are user configurable. Response type is independently configurable by fault type. Response types supported are:

- **Alert only**: The rail continues to operate.
- **Shut down immediately**: The rail is latched off until commanded on.
- **Shut down and retry with variable retry delay**: The rail attempts to retry indefinitely until the condition clears or the rail is commanded off.

If a fault condition has been declared, clear the fault by issuing a CLEAR_FAULTS (03h) command or by cycling the EN pin.

7.1 Power-Good Signal

The PG pin is an open-drain, power-good output that indicates completion of the soft-start sequence and output voltage is within the expected regulation range. If a fault occurs, the PG pin is pulled low. PG is also pulled low immediately on the rail disable.

7.2 Overvoltage/Undervoltage Protection

Output voltage is measured at the load sensing points differentially for regulation, and the same measurement is used for OVP and UVP. Figure 36 shows a simplified OVP/UVP block diagram. The output voltage comparisons are done in the digital domain.

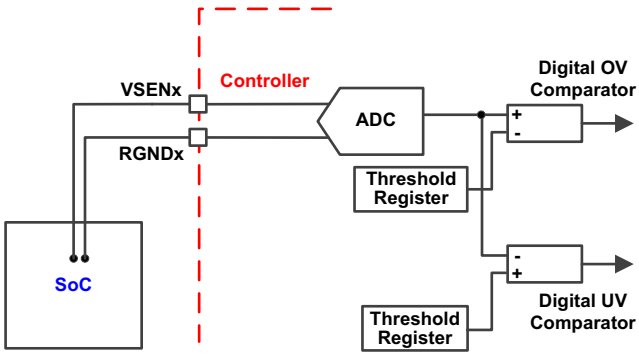


Figure 36. OV/UV Comparators

The device responds to an output overvoltage condition by disabling the output, declaring a fault, setting the nPMALERT pin, pulling the PG pin low, and then pulsing the LFET until the output voltage drops below the threshold. Similarly, the device responds to an output undervoltage condition by disabling the output, declaring a fault, setting the nPMALERT pin, and pulling the PG pin low. The output does not restart until the EN pin is cycled (unless the device is configured to retry).

The RAA210130 also features open-pin sensing protection to detect an open of the output voltage sensing circuit. If this condition is detected, module operation is suspended.

7.3 Output Overcurrent Protection

The RAA210130 offers a comprehensive overcurrent protection scheme that monitors peak phase current and the valley phase current. The scheme allows you to avoid inductor saturation. The RAA210130 supports shutdown and retry response types for OC faults. The response configuration applies to the output current fault mechanisms such as phase peak overcurrent and phase negative current limit.

The module is protected from both overcurrent and undercurrent using a pulse-by-pulse scheme that acts instantly on a PWM signal if a detected inductor current reaches its threshold. The undercurrent limit is the negative inductor current limit for the converter. Thresholds for overcurrent and undercurrent allow you to precisely limit the phase current. Current limiting behavior can be configured to shut down the device after a user-determined number of consecutive events. Figure 37 and Figure 38 show the OC and UC current limiting when the device is configured to shut down after a finite number of consecutive events.

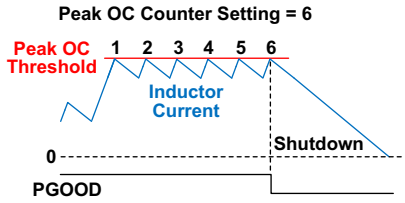


Figure 37. Peak OC Operation

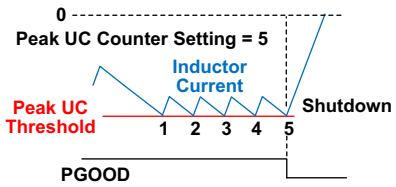


Figure 38. Peak UC Operation

7.4 Smart Power Stage OC Fault Detect

Renesas Smart Power Stage (SPS) device outputs a large signal on the IMON line if peak current exceeds the preprogrammed threshold. The RAA210130 detects this fault flag by sensing the signals that exceed the current-sense ADC full scale range and immediately shuts down.

7.5 Thermal Protection and nVRHOT

The RAA210130 supports a comprehensive scheme for thermal alerting and protection. It monitors SPS temperature and supports over-temperature and under-temperature faults in addition to over-temperature warning.

The controller temperature is monitored to support telemetry and thermal shutdown. Shutdown occurs at approximately +130°C.

The nVRHOT pin is used at the system level to inform the powered device to reduce its power consumption. nVRHOT is an open-drain output; an external pull-up resistor is required. This signal is valid only after the controller is enabled. nVRHOT is pulled low when the sensed temperature reaches the PMBus OT_WARN threshold, providing the powered device with an advance warning of the controller thermal status.

Figure 39 shows the behavior of nVRHOT and an over-temperature fault shutdown.

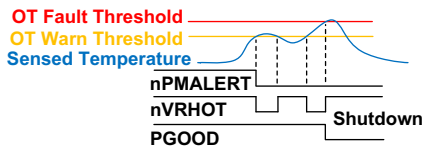


Figure 39. nVRHOT and Over-Temperature Shutdown

7.6 Catastrophic Failure Protection

The CFP pin supports Catastrophic Failure Protection (CFP) functionality. The pin can be configured to activate in the event of a catastrophic fault detection. The function is typically used to immediately disable the input supply to

protect the entire system. The CFP function can be configured to respond to output overvoltage, input overvoltage, and/or output overcurrent faults.

7.7 Black Box Recorder

Black Box is a powerful diagnostic tool that captures all telemetry and status information when any fault occurs. The RAA210130 continuously monitors rail information along with the time duration for which the rail has been regulating, and the tool captures that data when a fault is registered. The tool reports the first fault bit that occurred to cause the shutdown. This diagnostic data is stored in the RAM. The Black Box can be configured to additionally write to the NVM for retrieval when the system loses input power and a fault occurs. The RAM record is updated every time a fault occurs. The Black Box can write to the NVM up to 10 times and provides an option to limit NVM writing to once per power cycle to avoid filling up the available NVM space inadvertently.

7.8 Configuring for 3.3V Output

See Figure 5 for the typical application circuit with V_{OUT} = 3.3V.

For hardware settings, place a 499Ω resistor between VSEN and RGND and remove the 2Ω resistor between VSEN and VOUT. This resistor forms a divider with the 100Ω resistor between VSEN and VOUT, which is internal to the module. For PMBus settings and telemetry, the PMBUS register VOUT_COMMAND (21h) for 3.3V needs to be set to 2.75V. Because of the divider effect, the READ_VOUT (8Bh) command is a 1.2mV/bit weight vs the standard 1mV/bit weight. PowerNavigator therefore shows V_{OUT} as 2.75V in the monitor view.

Note: When measured across the VOUT and GND on the hardware side, 3.3V is observed.

7.9 Thermal Considerations and Internal 5V and 3.3V Supplies

The RAA210130 has integrated 5V and 3.3V supplies for powering the internal circuitry of the module. If external 5V and 3.3V supplies are available, the internal LDOs can be bypassed, which can help in increasing the efficiency and lowering the overall power dissipation of the module.

If the 5V and 3.3V supplies that are internal to the module are used, no additional 5V and 3.3V supplies are required. However, because they are additional heat sources to the module, especially when the module is used in an environment with higher ambient temperature, to help lower the overall power dissipation of the module, a 100Ω resistor can be added between the 12V input and VDD1/VDD2. VDD1 is the input to the 3.3V internal LDO and VDD2 is the input to the 5V internal LDO. A 100Ω resistor with power rating greater than 0.25W can be used.

8. Layout and Design Considerations

The following layout and design strategies help minimize noise coupling and the impact of board parasitic impedances on converter performance, and they optimize the heat dissipating capabilities of the Printed Circuit Board (PCB). Follow these practices during the layout and design process.

8.1 Pin Noise Sensitivity, Design, and Layout Considerations

Table 4 provides general guidance on best practices related to pin noise sensitivity. Use of good engineering judgment is required to implement designs based on criteria specific to the situation.

Table 4. Pin Design and/or Layout Considerations

Pin Name	Noise Sensitive	Description
VINSEN	Yes	Connect to power train input directly. A 100nF capacitor decoupling capacitor is placed inside module.
RGND0 VSEN0	Yes	The remote voltage sense pair should be routed as a pair of differential signals in the PCB layout. Route them side by side on the same layer. Do not route them in proximity to noisy signals like PWM or Phase.
PG	No	Open-drain. Avoid setting its pull-up higher than V3P3. Tie it to ground when not used.
PMSCL, PMSDA, nPMALERT	Yes	The 50kHz to 2MHz signals should pair up with nPMALERT and routed carefully between devices and back to the host. Provide 20 mils of spacing within PMSDA, nPMALERT and PMSCL, and more than 30 mils to all other signals. See the SMBus design guidelines and place proper terminated (pull-up) resistance for impedance matching. Tie to ground when not used. Pull up to 3.3V max.
TMON	Yes	Leave this pin floating.
nVRHOT	No	Open drain. Avoid setting its pull-up rail higher than V3P3.
V3P3	Yes	A 1µF MLCC decoupling capacitor is placed inside the module. Place a 2.2µF MLCC (X5R or better) directly between the pin and GND.
VCCS	Yes	Place a 4.7µF MLCC decoupling capacitor (X5R or better) directly between the pin and GND.
PWM	No	Leave both PWM pins floating.
SW	Yes	Connect all SW pins together on the board.
CS0 CSRTN0	Yes	The current sense pair should be routed as a differential signal in the PCB layout. Route them side by side on the same layer. **Note:** Do not route them in close proximity to noisy signals like PWM or Phase. Proper routing of current sense is perhaps the most critical of all the layout tasks.
General Comments		The layer next to the top or bottom layer should be a ground layer. The signal layers should be sandwiched between the ground layers if possible.

8.2 Layout Guidelines

Careful attention to layout requirements is necessary for a successful implementation of the RAA210130 power module. The RAA210130 switches at a high frequency. Therefore, the switching times are short. At these switching frequencies, even the shortest trace has significant impedance. The peak gate drive current also rises significantly in an extremely short time. Current transition from one MOSFET to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, generate EMI, and increase MOSFET voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes. Use the RTKA210130E0020BU as an example and reference for the PCB layout.

The following are layout considerations:

- Renesas recommends using a six-layer PCB board. Use the top and bottom layer to route VIN and VOUT. Use a full ground plane in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. Use another full ground plane directly above the bottom layer. Use the other internal layers to route the remote sense, PG, PMSCL, PMSDA, and nPMALERT signals.
- Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND as close to the module as possible. The loop formed by the input capacitors, VIN, and PGND must be as small as possible to minimize high frequency noise. Place the output ceramic capacitors close to VOUT. Use a copper plane to connect the output ceramic capacitors to the load to minimize any parasitic inductances and resistances. An example layout is illustrated in Figure 40.

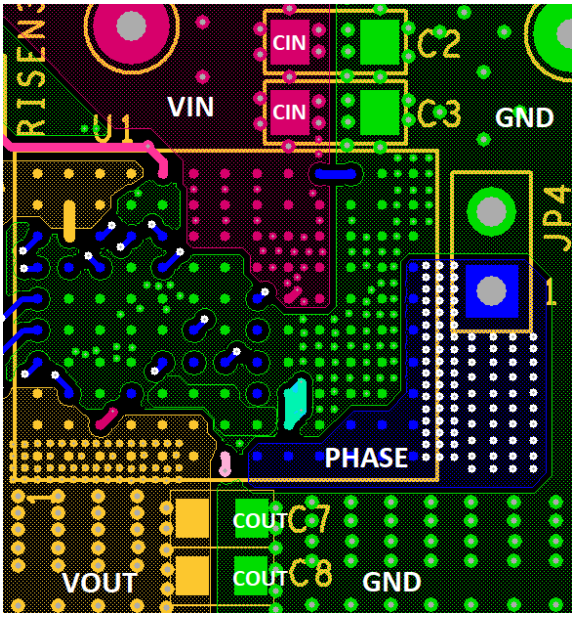


Figure 40. Layout Example - Top Layer, Showing Location of VIN and VOUT Capacitors

- Use large copper planes for power paths (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.

- Use full ground planes in the second layer (underneath the module) and in the fifth layer, which is the layer above the bottom layer which contains components such as input caps, output caps and other passive components. Use the inner layers 3 and 4 to route the other signals. A layout example of a large area ground plane is shown in Figure 41.

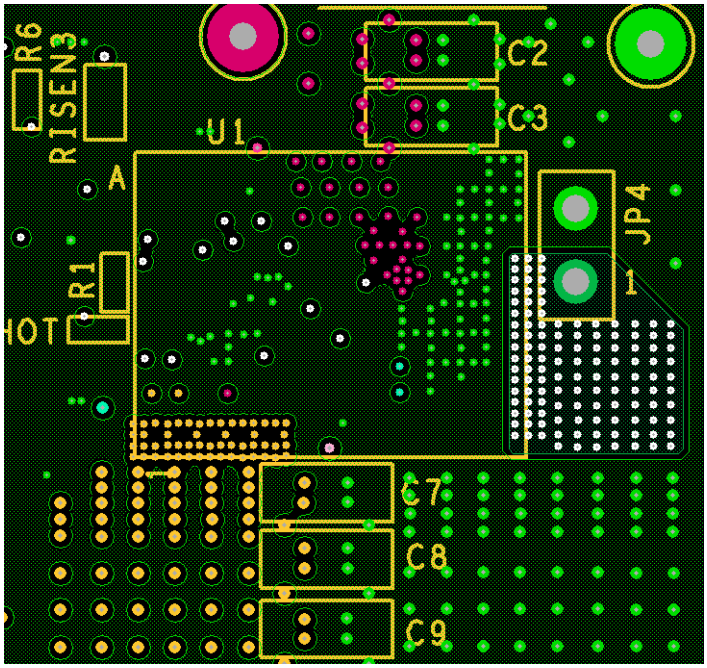


Figure 41. Layout Example - Large Area Ground Planes in Layer 2 and Layer 5.

- Do not oversize the copper planes for the SW planes. Because the SW planes are subjected to high dv/dt, the parasitic capacitor formed between these planes and the surrounding circuitry tends to couple the switching noise. Ensure that none of the sensitive signal traces are routed close to the SW plane.
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation. Route the remote sensing traces in parallel underneath the PGND layer and avoid routing the sensing trace near noisy planes such as SW. Place 2Ω resistors close to VSEN0 and RGND0, respectively, to dampen the noise on the traces.

- Place the VDD1, VDD2_2, CVCC, CCCS, C3P3 bypass capacitors on the bottom side of the board, underneath the module close to their respective pins for optimum decoupling. A layout example is shown in Figure 42.

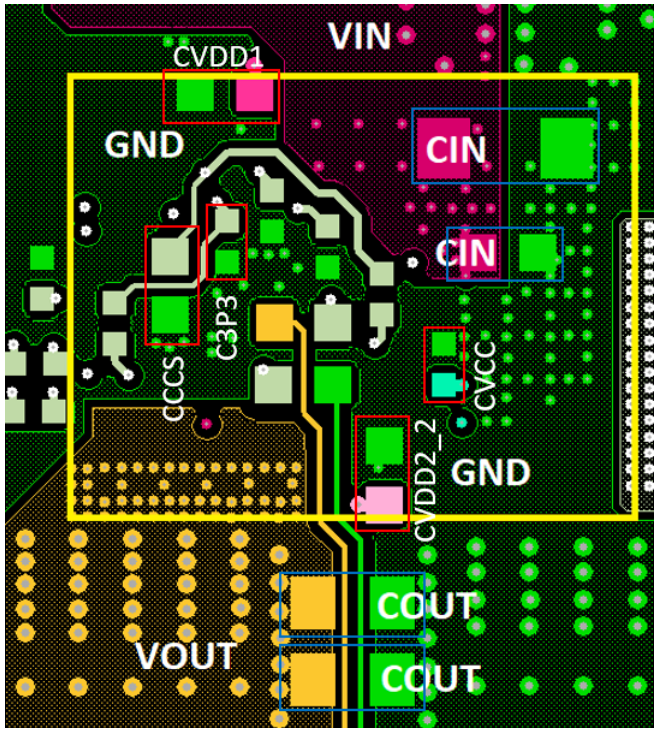


Figure 42. Layout Example - Bottom Layer

This example shows location of VIN and VOUT capacitors in blue boxes and location of the other decoupling capacitors CVDD1, CVDD2_2, CVCC, CCCS, C3P3 are shown in the red boxes.

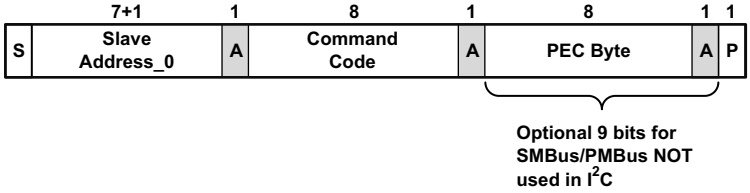
9. PMBus Protocol

The PMBus Protocol includes the Send Byte, the Write Byte/Word, Read Byte/Word, Group Command, and Alert Response Address protocols.

PMBus Protocol Legend

S: Start Condition
A: Acknowledge (“0”)
N: Not Acknowledge (“1”)
W: Write (“0”)
RS: Repeated Start Condition
R: Read (“1”)
PEC: Packet Error Checking
P: Stop Condition
Acknowledge or DATA from Slave, Controller

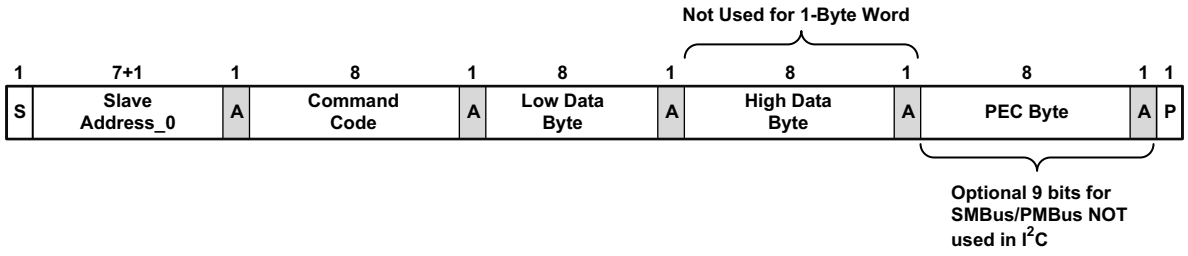
9.1 Send Byte Protocol



Example command: 03h Clear Faults
(This clears all of the bits in Status Byte for the rail)

Figure 43. Send Byte Protocol

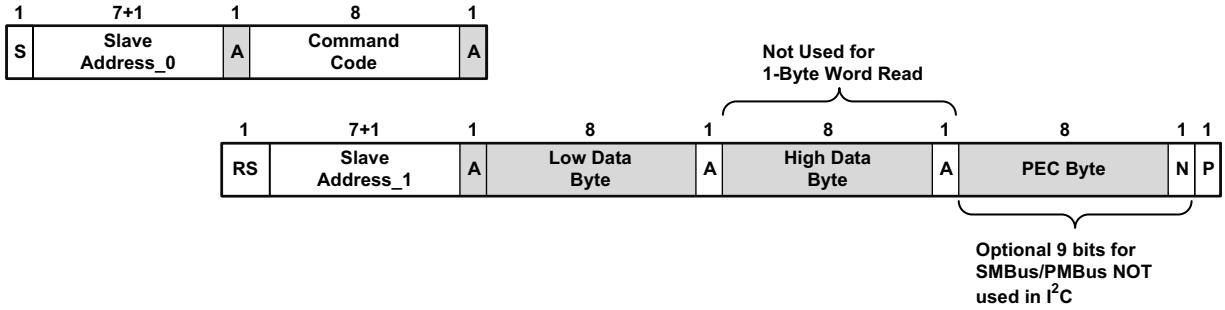
9.2 Write Byte/Word Protocol



Example command: 21h VOUT_COMMAND

Figure 44. Write Byte/Word Protocol

9.3 Read Byte/Word Protocol

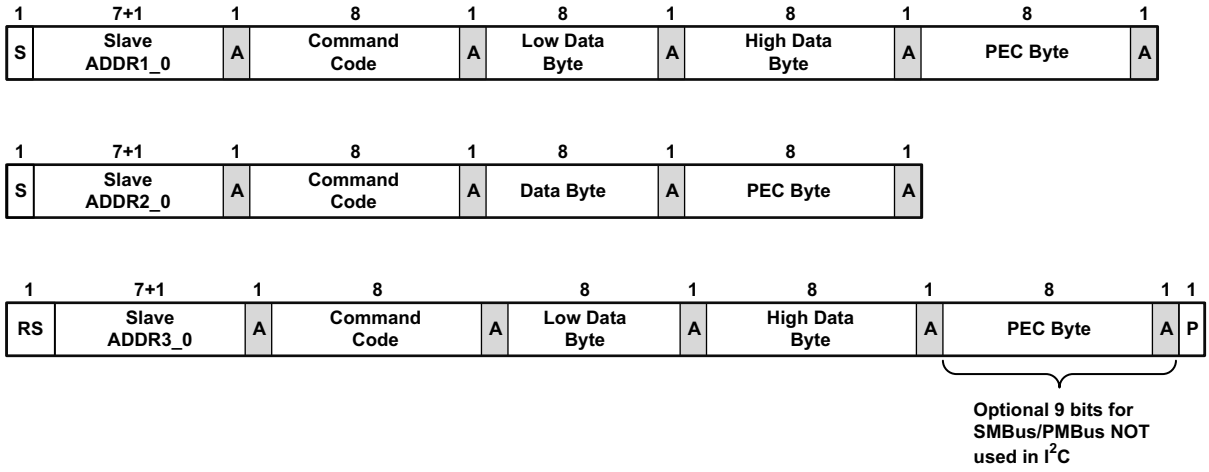


Example command: 8B READ_VOUT (Two words, read voltage of the rail).

Note: The STOP (P) bit is NOT allowed before the repeated START condition when reading contents of a register.

Figure 45. Read Byte/Word Protocol

9.4 Group Command Protocol



Note: No more than one command can be sent to the same Address

Figure 46. Group Command Protocol

9.5 Alert Response Address

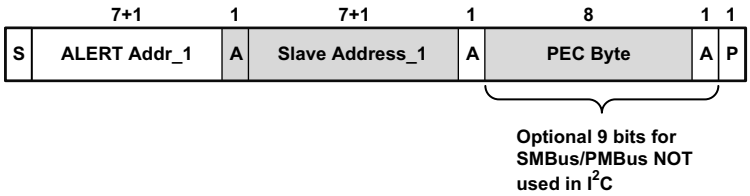


Figure 47. Alert Response Address (ARA, 0001_1001, 25h) for SMBus and PMBus

10. PMBus Commands Summary

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
00h	PAGE (00h)	Rail Selector	R/W	Bit	00h	Page 0
01h	OPERATION (01h)	Enable/disable, VOUT source	R/W	Bit	48h	Immediate off, act on fault
02h	ON_OFF_CONFIG (02h)	On/off configuration settings	R/W	Bit	16h	ENABLE pin control, active high, immediate off
03h	CLEAR_FAULTS (03h)	Clears all fault bits in all registers and releases the nPMALERT pin	Write	N/A	N/A	N/A
04h	PHASE (04h)	Phase Selector	R/W	Direct	00h	Phase 0
05h	PAGE_PLUS_WRITE (05h)	Allows page and command write in single transaction	Block Write	Bit	N/A	N/A
06h	PAGE_PLUS_READ (06h)	Allows page and command read in single transaction	Block Write/read /process call	N/A	N/A	N/A
10h	WRITE_PROTECT (10h)	Write protection to sets of commands	R/W	Bit	00h	No write protection
19h	CAPABILITY (19h)	Reports PMBus capability	Read	Bit	D0h	See detail
1Bh	SMBALERT_MASK (1Bh)	Mask status bits from SMBALERT signal	Block R/W	Bit	00h	No bits masked
20h	VOUT_MODE (20h)	Defines format for output voltage related commands	Read	Bit	40h	Direct format
21h	VOUT_COMMAND (21h)	Output voltage set by PMBus	R/W	Direct	ABEh	2750mV
22h	VOUT_TRIM (22h)	Applies trim voltage to V_{OUT} set-point	R/W	Direct	0000h	0mV
23h	VOUT_CAL_OFFSET (23h)	Applies offset voltage to V_{OUT} set-point	R/W	Direct	0000h	0mV
24h	VOUT_MAX (24h)	Absolute maximum voltage setting	R/W	Direct	0BEAh	3050mV
25h	VOUT_MARGIN_HIGH (25h)	Sets voltage target during margin high	R/W	Direct	0B47h	2887mV
26h	VOUT_MARGIN_LOW (26h)	Sets voltage target during margin low	R/W	Direct	0A34h	2612mV
27h	VOUT_TRANSITION_RATE (27h)	Slew rate setting for V_{OUT} ramp	R/W	Direct	0C8h	2mV/µs
28h	VOUT_DROOP (28h)	Sets the load-line (V/I slope) resistance for the output	R/W	Direct	0000h	0µV/A
2Bh	VOUT_MIN (2Bh)	Absolute minimum voltage setting	R/W	Direct	0000h	0mV
33h	FREQUENCY_SWITCH (33h)	Sets PWM switching frequency	R/W	Direct	02BCh	700kHz

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
34h	POWER_MODE (34h)	Sets the power conversion mode	R/W	Bit	03h	Maximum power
35h	VIN_ON (35h)	Sets the V_{IN} startup threshold	R/W	Direct	030Ch	7800mV
36h	VIN_OFF (36h)	Sets the V_{IN} shutdown threshold	R/W	Direct	0000h	0mV
40h	VOUT_OV_FAULT_LIMIT (40h)	Sets the V_{OUT} OV fault limit	R/W	Direct	0C1Ch	3100mV
41h	VOUT_OV_FAULT_RESPONSE (41h)	Configures the V_{OUT} OV fault response	R/W	Bit	84h	Latch off
44h	VOUT_UV_FAULT_LIMIT (44h)	Sets the V_{OUT} UV fault limit	R/W	Direct	0921h	2337mV
45h	VOUT_UV_FAULT_RESPONSE (45h)	Configures the V_{OUT} UV fault response	R/W	Bit	84h	Latch off
46h	IOUT_OC_FAULT_LIMIT (46h)	Sets the I_{OUT} OC fault limit	R/W	Direct	01F4h	50A
47h	IOUT_OC_FAULT_RESPONSE (47h)	Configures the I_{OUT} OC fault response	R/W	Bit	FCh	Latch off
4Fh	OT_FAULT_LIMIT (4Fh)	Sets the OT fault limit	R/W	Direct	007Dh	125°C
50h	OT_FAULT_RESPONSE (50h)	Configures the OT fault response	R/W	Bit	BCh	Retry
51h	OT_WARN_LIMIT (51h)	Sets the OT warning limit	R/W	Direct	006Eh	110°C
53h	UT_FAULT_LIMIT (53h)	Sets the UT fault limit	R/W	Direct	FFD8h	-40°C
54h	UT_FAULT_RESPONSE (54h)	Configures the UT fault response	R/W	Bit	80h	Latch off
55h	VIN_OV_FAULT_LIMIT (55h)	Sets the V_{IN} OV fault limit	R/W	Direct	640h	16000mV
56h	VIN_OV_FAULT_RESPONSE (56h)	Configures the V_{IN} OV fault response	R/W	Bit	84h	Latch off
57h	VIN_OV_WARN_LIMIT (57h)	Sets the V_{IN} OV warning limit	R/W	Direct	0708h	18V
58h	VIN_UV_WARN_LIMIT (58h)	Sets the V_{IN} UV warning limit	R/W	Direct	0000h	0mV
59h	VIN_UV_FAULT_LIMIT (59h)	Sets the V_{IN} UV fault limit	R/W	Direct	02D0h	7200mV
5Ah	VIN_UV_FAULT_RESPONSE (5Ah)	Configures the V_{IN} UV fault response	R/W	Bit	BCh	Retry
5Bh	IIN_OC_FAULT_LIMIT (5Bh)	Sets the I_{IN} OC fault limit	R/W	Direct	03E8h	10A
5Ch	IIN_OC_FAULT_RESPONSE (5Ch)	Configures the I_{IN} OC fault response	R/W	Bit	04h	Ignore
5Dh	IIN_OC_WARN_LIMIT (5Dh)	Sets the I_{IN} OC warning limit	R/W	Direct	3A98h	150A
60h	TON_DELAY (60h)	Sets turn-on delay time	R/W	Direct	0000h	0µs
61h	TON_RISE (61h)	Sets turn-on rise time	R/W	Direct	1388h	5000µs
64h	TOFF_DELAY (64h)	Sets turn-off delay time	R/W	Direct	0000h	0µs
65h	TOFF_FALL (65h)	Sets turn-off fall time	R/W	Direct	1388h	5000µs
78h	STATUS_BYTE (78h)	First byte of STATUS_WORD	Read	Bit	N/A	N/A
79h	STATUS_WORD (79h)	Summary of critical faults	Read	Bit	N/A	N/A

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
7Ah	STATUS_VOUT (7Ah)	Reports V_{OUT} warnings/faults	Read	Bit	N/A	N/A
7Bh	STATUS_IOUT (7Bh)	Reports I_{OUT} warnings/faults	Read	Bit	N/A	N/A
7Ch	STATUS_INPUT (7Ch)	Reports input warnings/faults	Read	Bit	N/A	N/A
7Dh	STATUS_TEMPERATURE (7Dh)	Reports temperature warnings/faults	Read	Bit	N/A	N/A
7Eh	STATUS_CML (7Eh)	Reports communication, memory, logic errors	Read	Bit	N/A	N/A
80h	STATUS_MFR_SPECIFIC (80h)	Reports other specific faults	Read	Bit	N/A	N/A
88h	READ_VIN (88h)	Reports input voltage measurement	Read	Direct	N/A	mV
89h	READ_IIN (89h)	Reports input current measurement	Read	Direct	N/A	A
8Bh	READ_VOUT (8Bh)	Reports output voltage measurement	Read	Direct	N/A	mV
8Ch	READ_IOUT (8Ch)	Reports output current measurement	Read	Direct	N/A	A
8Dh	READ_TEMPERATURE_1 (8Dh)	Reports power stage temperature measurement	Read	Direct	N/A	°C
8Eh	READ_TEMPERATURE_2 (8Eh)	Reports internal temperature measurement	Read	Direct	N/A	°C
8Fh	READ_TEMPERATURE_3 (8Fh)	Reports TEMP pin temperature measurement	Read	Direct	N/A	°C
96h	READ_POUT (96h)	Reports output power	Read	Direct	N/A	W
97h	READ_PIN (97h)	Reports input power	Read	Direct	N/A	W
98h	PMBUS_REVISION (98h)	Reports the PMBus revision used	Read	Bit	33h	P1 R1.3, P2 R1.3
99h	MFR_ID (99h)	Stores inventory information	Block R/W	Bit	00000000h	Empty
9Ah	MFR_MODEL (9Ah)	Stores inventory information	Block R/W	Bit	00000000h	Empty
9Bh	MFR_REVISION (9Bh)	Stores inventory information	Block R/W	Bit	00000000h	Empty
9Dh	MFR_DATE (9Dh)	Stores inventory information	Block R/W	Bit	00000000h	Empty
ADh	IC_DEVICE_ID (ADh)	Reports device identification information	Block Read	Bit	49D2B000h	RAA210130
AEh	IC_DEVICE_REV (AEh)	Reports device revision information	Block Read	Bit		Release revision
C5h	DMAFIX (C5h)	Fixed DMA transactions	R/W	Bit	0000h	0
C6h	DMASEQ (C6h)	Sequential DMA transaction	R/W	Bit	0000h	0
C7h	DMAADDR (C7h)	Sets the address for DMA transactions	R/W	Bit	0000h	0
CDh	PEAK_OC_LIMIT (CDh)	Sets peak per phase OC limit	R/W	Direct	01F4h	50A
CEh	PEAK_UC_LIMIT (CEh)	Sets peak per phase UC limit	R/W	Direct	FE0C	-50A

Code	Command Name	Description	Type	Data Format	Default Value	Default Setting
D0h	VMON_ON (D0h)	Sets the VMON startup threshold	R/W	Direct	1C2h	4500mV
D1h	VMON_OFF (D1h)	Sets the VMON shutdown threshold	R/W	Direct	190h	4000mV
DDh	COMPPROP (DDh)	Configures proportional gain	R/W	Bit	D80189C4h	See detail
DEh	COMPINTEG (DEh)	Configures integral gain	R/W	Bit	A8h	See detail
DFh	COMPDIFF (DFh)	Configures differential gain	R/W	Bit	0020h	See detail
E0h	COMPCFB (E0h)	Configures AC current feedback	R/W	Bit	6840h	See detail
E3h	HS_BUS_CURRENT_SCALE (E3h)	Sets the high speed bus current scaling	R/W	Bit	4000h	1.0
E4h	PHASE_CURRENT (E4h)	Reports per-phase current	Read	Direct	N/A	A
E5h	PHASE_TEMPERATURE (E5h)	Reports per-phase temperature	Read	Direct	N/A	°C
E9h	PEAK_OCUC_COUNT (E9h)	Sets the count limit before fault	R/W	Bit	606h	6 cycles for OC & UC
EAh	SLOW_IOUT_OC_LIMIT (EAh)	Sets the slow I_{OUT} OC limit	R/W	Direct	01F4h	50A
EBh	FAST_OC_FILT_COUNT (EBh)	Configures the fast OC filter	R/W	Bit	0696h	Filter = 10.7µs, Delay = 100µs
ECh	SLOW_OC_FILT_COUNT (ECh)	Configures the slow OC filter	R/W	Bit	0606h	Filter = 10.7µs, Delay = 1024µs
F0h	LOOPCFG (F0h)	Defines rail operating configuration	R/W	Bit	002371B6h	See detail
F2h	RESTORE_CFG (F2h)	Identifies configuration to be restored from NVM	R/W	Bit	00h	

10.1 PMBus Use Guidelines

All commands can be read at any time.

10.2 PMBus Data Formats

10.2.1 Direct

The Direct data format is a 2-byte binary integer.

10.2.2 Linear 16 Unsigned (L16U)

The L16u data format uses a fixed exponent (hard-coded to N = -9h) and a 16-bit unsigned integer mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-9}$.

10.2.3 Linear 16 Signed (L16S)

The L16S data format uses a fixed exponent (hard-coded to N = -9h) and a 16-bit signed integer mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-9}$.

10.2.4 Linear 11 (L11)

The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent the real world decimal value (X).

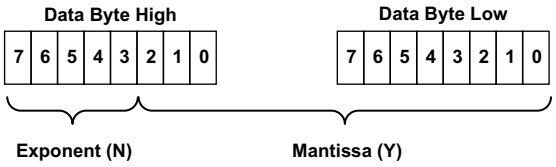


Figure 48. Linear 11 Data Format

The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{N}$.

10.2.5 Bit Field (Bit)

A description of Bit Field is provided in the PMBus Command Detail.

10.2.6 Custom (Cus)

Custom format

11. PMBus Command Detail

11.1 PAGE (00h)

Definition: Selects the communication path to Rail 0. All paged commands following this command are received and acted on by the selected destination path. Paged commands that can be written globally, but can only be read on a specific page unless otherwise specified. Global commands remain global regardless of the value of this command.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h

Command	PAGE (00h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Value	Setting
00h	Page 0 (Rail 0)
01h	Reserved
80h	Reserved
FFh	Reserved

11.2 OPERATION (01h)

Definition: Sets Enable/Disable state when configured for PMBus enable. Sets the source of the target V_{OUT}. The following table reflects the valid settings for the device.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 48h (Immediate off, Act on fault)

Command	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	1	0	0	0

Bit Number	Purpose	Bit Value	Meaning
7	Enable/Disable Output	0	Disable
		1	Enable
6	Disable by PMBus Behavior	0	Immediate off (decay with PWM tri-state)
		1	Soft off (Use TOFF_DELAY and TOFF_FALL)
5:4	V_{OUT} Source	00	VOUT_COMMAND
		01	VOUT_MARGIN_LOW
		10	VOUT_MARGIN_HIGH
		11	Not used
3:2	Margin Response	01	Ignore V_{OUT} OV, UV faults when margined.
		10	Act on V_{OUT} OV, UV faults when margined.
1	Not Supported	0	Not supported
0	Not Supported	X	Not supported

11.3 ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 16h (ENABLE pin control)

Command	ON_OFF_CONFIG (02h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	0

Bit Number	Purpose	Bit Value	Meaning
7:5	Not Supported	000	Not supported
4:2	Sets the source of enable	0XX	Output enables any time power is present regardless of pin or OPERATION command state.
		101	Output enables from the enable pin only.
		110	Output enables from the OPERATION command only.
		111	Output enables from the enable pin AND the OPERATION command. Both must be set to enable.
1	Polarity of ENABLE pin	0	Active low
		1	Active high
0	ENABLE pin action when commanding the unit to turn off	0	Use the configured TOFF_DELAY and TOFF_FALL settings.
		1	Turn off the output immediately (decay with PWM tri-state).

11.4 CLEAR_FAULTS (03h)

Definition: Clears all fault status bits in all registers and releases the nPMALERT pin (if asserted) simultaneously. If a fault condition still exists, the bit(s) reasserts immediately. This command does not restart a device if it is shut down, it only clears the faults.

Access: Paged (always set to 0x00)

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

11.5 PHASE (04h)

Definition: Sets the individual phase address for reading from PHASE_CURRENT (E4h) and PHASE_TEMPERATURE (E5h). The PAGE command must also be set to access phase information.

Access: Global

Data Length in Bytes: 1

Data Format: Direct

Type: R/W

Default Value: 00h (phase 0)

Equation: PHASE = (direct value)

Command	PHASE (04h)							
Format	Direct							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer							
Default Value	0	0	0	0	0	0	0	0

11.6 PAGE_PLUS_WRITE (05h)

Definition: Sets the page within a device, sends a command, and sends the data for the command in one packet.

Access: Global

Data Format: Bit Field

Type: Block Write

The PAGE_PLUS_WRITE command uses the WRITE BLOCK protocol.

Figure 49 shows an example of the PAGE_PLUS command being used to send a command that has two data bytes to be written and a PEC byte.

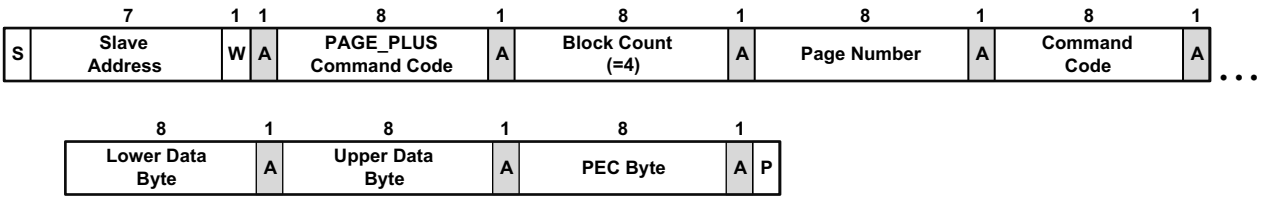


Figure 49. PAGE_PLUS_WRITE Command with a PEC Byte

11.7 PAGE_PLUS_READ (06h)

Definition: Sets the page within a device, sends a command, and reads the data returned by the command in one packet.

Access: Paged (always set to 0x00)

Data Format: Bit Field

Type: Block Read

The PAGE_PLUS_READ command uses the BLOCK WRITE – BLOCK READ PROCESS CALL protocol.

Figure 50 shows an example of the PAGE_PLUS command being used to send a command that has two data bytes to be read and a PEC byte.

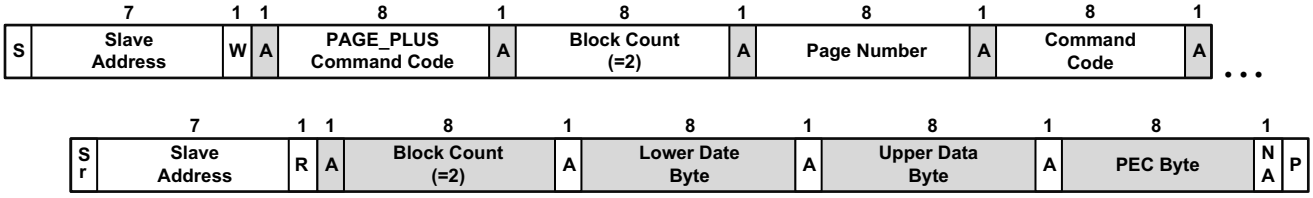


Figure 50. PAGE_PLUS_READ Command with a PEC Byte

11.8 WRITE_PROTECT (10h)

Definition: Sets the write protection of certain configuration commands.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h (enable all writes)

Command	WRITE_PROTECT (10h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bits 7:0[1]	Protection
1000 0000	Disable all writes except to WRITE_PROTECT command.
0100 0000	Disable all writes except to WRITE_PROTECT, OPERATION, and PAGE.
0010 0000	Disable all writes except to WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND.
0000 0010	Disable all writes except to WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, VOUT_COMMAND, and DMA.
0000 0000	Enable all writes

1. Any settings other than the five shown results in an invalid data fault.

11.9 CAPABILITY (19h)

Definition: Reports PMBus capabilities of the device.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: D0h (PEC supported, bus speed 1MHz, SMBALERT supported, Linear/Direct numeric data)

Command	CAPABILITY (19h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	1	1	0	1	0	0	0	0

Bit Number	Purpose	Bit Value	Meaning
7	PEC Support	1	PEC supported
		0	PEC not supported
6:5	Maximum Bus Speed	11	Not supported
		10	1MHz
		01	400kHz
		00	100kHz
4	SMBALERT Support	1	SMBALERT pin and response protocol is supported.
		0	SMBALERT pin and response protocol is not supported.
3	Numeric Format	1	Numeric data, IEEE half precision floating point format
		0	Numeric data, Linear/Direct
2	Not Supported	0	Not supported
1:0	Not Supported	00	Not supported

11.10 SMBALERT_MASK (1Bh)

Definition: Prevents a warning or fault condition from asserting the SMBALERT# signal. Can be used on the following PMBus status commands: STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, and STATUS_MFR_SPECIFIC.

Access: Paged (always set to 0x00)

Data Format: Bit Field

Type: Block R/W

The command format used to block a status bit or bits from causing the SMBALERT# signal to be asserted is shown in Figure 51 and Figure 52. The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS_TEMPERATURE command code is sent with the mask byte 01000000b, an over-temperature warning condition would be blocked from asserting SMBALERT#.
Note: Figure 51 shows the command format used by the host to determine the SMBALERT_MASK setting for a given status register.

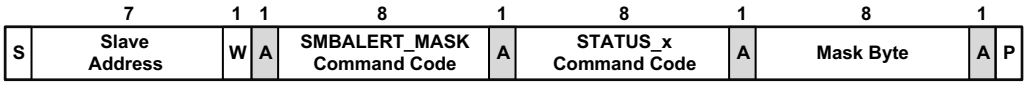


Figure 51. SMBALERT_MASK Command Packet Format

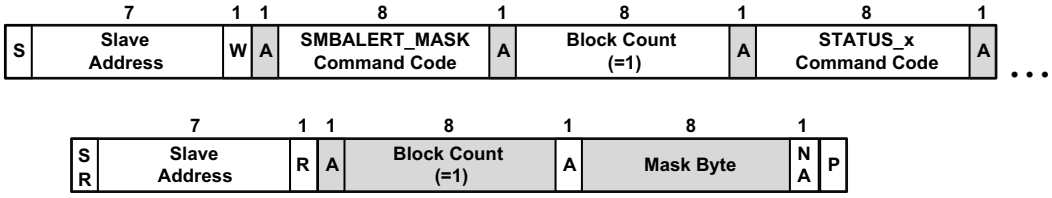


Figure 52. Retrieving the SMBALERT_MASK Setting for a Given Status Register

11.11 VOUT_MODE (20h)

Definition: Returns the supported V_{OUT} mode. Direct mode, 1mV per LSB.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: 40h

Command	VOUT_MODE (20h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Mode			Exponent				
Default Value	0	1	0	0	0	0	0	0

11.12 VOUT_COMMAND (21h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for PMBus nominal operation. 1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0ABEh (2750mV) for config ID 0

Units: mV

Equation: V_{OUT} Command = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_COMMAND (21h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	1	0	1	0	1	0	1	1	1	1	1	0

11.13 VOUT_TRIM (22h)

Definition: Applies a fixed trim voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit. 1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h

Units: mV

Equation: V_{OUT} Trim = (Direct value)

Range: Any value that results in the V_{OUT} target being between 0V and VOUT_MAX

Command	VOUT_TRIM (22h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.14 VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit. 1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h

Units: mV

Equation: V_{OUT} Cal Offset = (Direct value)

Range: Any value that results in the V_{OUT} target being between 0V and VOUT_MAX

Command	VOUT_CAL_OFFSET (23h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.15 VOUT_MAX (24h)

Definition: Sets the absolute maximum V_{OUT} regulation value regardless of any other commands or combinations.1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0BEAh (3050mV)

Units: mV

Equation: V_{OUT} Max = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_MAX (24h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1	0

11.16 VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for margin high. 1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0B47h (2887mV)

Units: mV

Equation: V_{OUT} Margin High = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_MARGIN_HIGH (25h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	1	0	1	1	0	1	0	0	0	1	1	1

11.17 VOUT_MARGIN_LOW (26h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for margin low. 1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0A34h (2612mV)

Units: mV

Equation: V_{OUT} Margin Low = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_MARGIN_LOW (26h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	1	0	1	0	0	0	1	1	0	1	0	0

11.18 VOUT_TRANSITION_RATE (27h)

Definition: Defines the output voltage rate of change during regulation. 0.01mV/µs per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0C8h (2mV/µs)

Units: mV/µs

Equation: V_{OUT} Transition Rate = (Direct value) / 100

Range: 10µV/µs to 100mV/µs

Command	VOUT_TRANSITION_RATE (27h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0

11.19 VOUT_DROOP (28h)

Definition: Sets the rate at which the output voltage changes relative to output current during regulation. 10µV/A per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0µV/A)

Units: µV/A

Equation: V_{OUT} Droop = (Direct value) × 10

Range: 0µV/A to 16000µV/A

Command	VOUT_DROOP (28h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.20 VOUT_MIN (2Bh)

Definition: Sets the absolute minimum voltage that is delivered to the output during regulation. 1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h

Units: mV

Equation: V_{OUT} Min = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_MIN (2Bh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.21 FREQUENCY_SWITCH (33h)

Definition: Sets the PWM switching frequency during regulation. 1kHz per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 02BCh (700kHz)

Units: kHz

Equation: Frequency Switch = (Direct value)

Range: 200kHz to 1.25MHz

Command	FREQUENCY_SWITCH (33h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0

11.22 POWER_MODE (34h)

Definition: Sets the power conversion mode.

Maximum Efficiency Mode (0) default setting:

- Voltage down transitions happen immediately with decay (PWM tri-state).

Maximum Power Mode (3) default setting:

- Voltage down transitions happen as programmed in the TOFF_DELAY and TOFF_FALL commands.

MFR Defined Mode (4) default setting:

- Voltage down transitions happen immediately with decay (PWM tri-state).

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 03h, Maximum Power

Command	POWER_MODE (34h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	1	1

Bit Value	Setting
04h	MFR defined
03h	Maximum Power
00h	Maximum Efficiency

11.23 VIN_ON (35h)

Definition: Sets the input voltage rising threshold at which the output can be enabled. 10mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 030Ch (7800mV)

Units: mV

Equation: V_{IN} On = (Direct value) × 10

Range: -327680mV to 327670mV

Command	VIN_ON (35h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0

11.24 VIN_OFF (36h)

Definition: Sets the input voltage falling threshold at which the output disables. 10mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000 (0mV)

Units: mV

Equation: V_{IN} Off = (Direct value) × 10

Range: -327680mV to 327670mV

Command	VIN_OFF (36h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.25 VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the output overvoltage threshold. 1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0C1Ch (3100mV)

Units: mV

Equation: V_{OUT} OV Fault Limit = (Direct value)

Range: 0mV to 3050mV

Command	VOUT_OV_FAULT_LIMIT (40h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	1	1	0	0	0	0	0	1	1	1	0	0

11.26 VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the output overvoltage fault response. For a fault to be considered cleared, the output must drop by 100mV.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

Command	VOUT_OV_FAULT_RESPONSE (41h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	1	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption.
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the rail is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	0ms delay (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.27 VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the output undervoltage fault threshold. 1mV per LSB. This fault is masked during ramp or when disabled.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0921h (2337mV)

Units: mV

Equation: V_{OUT} UV Fault Limit = (Direct value)

Range: 0V to 3050mV

Command	VOUT_UV_FAULT_LIMIT (44h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	1

11.28 VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the output undervoltage fault response. This fault is masked during ramp or when disabled.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

Command	VOUT_UV_FAULT_RESPONSE (45h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	1	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption.
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the rail is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.29 IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the fast sum output overcurrent fault threshold. 0.1A per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4h (50A)

Units: A

Equation: I_{OUT} OC Fault Limit = (Direct value) / 10

Range: 0A to 3276.7A

Command	IOUT_OC_FAULT_LIMIT (46h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

11.30 IOUT_OC_FAULT_RESPONSE (47h)

Definition: Configures the output overcurrent fault response for all I_{OUT} OC detection methods. This response setting is also applied to output undercurrent faults.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: FCh (latch off)

Command	IOUT_OC_FAULT_RESPONSE (47h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	1	1	1	1	1	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption.
		01-10	Not supported
		11	Disable and retry as set in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the rail is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.31 OT_FAULT_LIMIT (4Fh)

Definition: Sets the power stage over-temperature fault limit. 1°C per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 007Dh (125°C)

Units: °C

Equation: OT Fault Limit = (Direct value)

Range: 0°C to +150°C

Command	OT_FAULT_LIMIT (4Fh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

11.32 OT_FAULT_RESPONSE (50h)

Definition: Configures the power stage over-temperature fault response. For a fault to be considered cleared, the temperature must drop 5°C below the OT fault threshold value.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: BCh (retry)

Command	OT_FAULT_RESPONSE (50h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption.
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the rail is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.33 OT_WARN_LIMIT (51h)

Definition: Sets the power stage over-temperature warning limit. 1°C per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 006Eh (110°C)

Units: °C

Equation: OT Warn Limit = (Direct value)

Range: 0°C to 150°C

Command	OT_WARN_LIMIT (51h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0

11.34 UT_FAULT_LIMIT (53h)

Definition: Sets the power stage under-temperature fault limit. 1°C per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: FFD8h (-40°C)

Units: °C

Equation: UT Fault Limit = (Direct value)

Range: -50°C to 150°C

Command	UT_FAULT_LIMIT (53h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0

11.35 UT_FAULT_RESPONSE (54h)

Definition: Configures the power stage under-temperature fault response. For the fault to be considered cleared, the temperature must rise 5°C above the UT fault threshold value.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 80h (latch off)

Command	UT_FAULT_RESPONSE (54h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption.
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not supported
		111	Attempts to restart continuously without limitation until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.36 VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold. 10mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 640h (16000mV)

Units: mV

Equation: V_{IN} OV Fault Limit = (Direct value) × 10

Range: 0mV to 327670mV

Command	VIN_OV_FAULT_LIMIT (55h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0

11.37 VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the input overvoltage fault response. For a fault to be considered cleared, the input voltage must drop by 1/16th of the OV fault threshold value.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

Command	VIN_OV_FAULT_RESPONSE (56h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	1	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption.
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not supported
		111	Attempts to restart continuously without limitation until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.38 VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} overvoltage fault threshold. 10mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 708h (18000mV)

Units: mV

Equation: V_{IN} OV Warn Limit = (Direct value) × 10

Range: 0mV to 327670mV

Command	VIN_OV_WARN_LIMIT (57h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0

11.39 VIN_UV_WARN_LIMIT (58h)

Definition: Sets the V_{IN} undervoltage warning threshold. 10mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0V)

Units: mV

Equation: V_{IN} UV Warn Limit = (Direct value) × 10

Range: 0mV to 327670mV

Command	VIN_UV_WARN_LIMIT (58h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.40 VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold. 10mV per LSB. If using VIN_ON and VIN_OFF commands, this command should be set to 0V.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 02D0h (7200mV)

Units: mV

Equation: V_{IN} UV Fault Limit = (Direct value) × 10

Range: -327680mV to 327670mV

Command	VIN_UV_FAULT_LIMIT (59h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two’s Complement Integer															
Default Value	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0

11.41 VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the input undervoltage fault response. For a fault to be considered cleared, the input voltage must rise by 1/16th of the UV fault threshold value.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: BCh (retry)

Command	VIN_UV_FAULT_RESPONSE (5Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption.
		01	Not supported
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not supported
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.42 IIN_OC_FAULT_LIMIT (5Bh)

Definition: Sets the input overcurrent fault threshold for the synthesized input current reading at READ_IIN. 10mA per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 03E8h (10A)

Units: A

Equation: I_{IN} OC Fault Limit = (Direct value) / 100

Range: -327.68A to 327.67A

Command	IIN_OC_FAULT_LIMIT (5Bh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two’s Complement Integer															
Default Value	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0

11.43 IIN_OC_FAULT_RESPONSE (5Ch)

Definition: Configures the input overcurrent fault response for the synthesized input current reading at READ_IIN.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 04h (ignore)

Command	IIN_OC_FAULT_RESPONSE (5Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	1	0	0

Bit	Field Name	Value	Description
7:6	Response Behavior During a fault, the device: ▪ Pulls PMALRT low ▪ Sets the related fault bit in the status registers.	00	Continue without interruption.
		01-10	Not supported
		11	Disable and retry as set in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted
		001-110	Not supported
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0].
2:0	Delay Time before Retry	000	Delay 0ms (not recommended)
		001-110	Delay 25ms per LSB
		111	Delay 175ms

11.44 IIN_OC_WARN_LIMIT (5Dh)

Definition: Sets the input overcurrent warning threshold. 10mA per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 3A98h (150A)

Units: A

Equation: I_{IN} OC Warn Limit = (Direct value) / 100

Range: -327.68A to 327.67A

Command	IIN_OC_WARN_LIMIT (5Dh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

11.45 TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise. 10µs per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0µs)

Units: µs

Equation: t_{ON} Delay = (Direct value) × 10

Range: 0µs to 655534µs

Command	TON_DELAY (60h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.46 TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} during enable. 1µs per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 1388h (5000µs)

Units: µs

Equation: t_{ON} Rise = (Direct value)

Range: 0µs to 10000µs

Command	TON_RISE (61h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0

11.47 TOFF_DELAY (64h)

Definition: Sets the delay time of V_{OUT} during disable when configured for soft off. 10µs per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0µs)

Units: µs

Equation: t_{OFF} Delay = (Direct value) × 10

Range: 0µs to 655534µs

Command	TOFF_DELAY (64h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.48 TOFF_FALL (65h)

Definition: Sets the fall time of V_{OUT} during disable when configured for soft off. 1µs per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 1388h (5000µs)

Units: µs

Equation: t_{OFF} Fall = (Direct value)

Range: 0µs to 10000µs

Command	TOFF_FALL (65h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0

11.49 STATUS_BYTE (78h)

Definition: Returns a summary of the device status. Based on the information in this byte, the host can get more information by reading the appropriate status registers.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Command	STATUS_BYTE (78h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault occurred.
4	IOUT_OC_FAULT	An output overcurrent fault occurred.
3	VIN_UV_FAULT	An input undervoltage fault occurred.
2	TEMPERATURE	A temperature fault or warning occurred.
1	CML	A communications, memory, or logic fault occurred.
0	None of the Above	A fault other than those listed above occurred.

11.50 STATUS_WORD (79h)

Definition: Returns a summary of the device status. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same as the STATUS_BYTE (78h) command.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Command	STATUS_WORD (79h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															

Bit Number	Status Bit Name	Meaning
15	V_{OUT}	An output voltage fault or warning occurred.
14	IOUT	An output current fault occurred.
13	INPUT	An input voltage fault or warning occurred.
12	MFR_SPECIFIC	A manufacturer specific fault or warning occurred.
11	POWER_GOOD #	The POWER_GOOD signal is negated.[1]
10:9	Not Supported	Not supported
8	Unknown	A fault other than those described in Bits 15:9 occurred.
7	Busy	Device busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault occurred.
4	IOUT_OC_FAULT	An output overcurrent fault occurred.
3	VIN_UV_FAULT	An input undervoltage fault occurred.
2	TEMPERATURE	A temperature fault or warning occurred.
1	CML	A communications, memory, or logic fault occurred.
0	None of the Above	A status change other than those listed above occurred.

1. If the POWER_GOOD# Bit is set, this indicates that the POWER_GOOD signal is signaling that the output power is not good.

11.51 STATUS_VOUT (7Ah)

Definition: Returns a summary of output voltage status.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_VOUT (7Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT	Indicates an output overvoltage fault occurred.
6:5	Not Supported	Not supported
4	VOUT_UV_FAULT	Indicates an output undervoltage fault occurred.
3	VOUT_MAX Warning	Indicates an output voltage maximum warning occurred.
2:0	Not Supported	Not supported

11.52 STATUS_IOUT (7Bh)

Definition: Returns a summary of output current status.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_IOUT (7Bh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT	An output overcurrent fault occurred.
6	Not Supported	Not supported
5	Not supported	Not supported
4	IOUT_UC_FAULT	An output undercurrent fault occurred.
3	Reserved	Reserved
2:0	Not Supported	Not supported

11.53 STATUS_INPUT (7Ch)

Definition: Returns a summary of input status.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_INPUT (7Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	VIN_OV_FAULT	An input overvoltage fault occurred.
6	VIN_OV_WARN	An input overvoltage warning occurred.
5	VIN_UV_WARN	An input undervoltage warning occurred.
4	VIN_UV_FAULT	An input undervoltage fault occurred.
3	VIN_ON/OFF	Disabled because of insufficient input voltage. This could be VIN or VMON.
2	IIN_OC_FAULT	An input overcurrent fault occurred.
1	IIN_OC_WARN	An input overcurrent warning occurred.
0	Not Supported	Not supported

11.54 STATUS_TEMPERATURE (7Dh)

Definition: Returns a summary of temperature status.

Access: Paged (always set to 0x00)

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_TEMPERATURE (7Dh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	OT_FAULT	An over-temperature fault occurred.
6	OT_WARN	An over-temperature warning occurred.
5	Not Supported	Not supported
4	UT_FAULT	An under-temperature fault occurred.
3:0	Not Supported	Not supported

11.55 STATUS_CML (7Eh)

Definition: Returns a summary of any communications, logic, and/or memory errors.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_CML (7Eh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit Number	Status Bit Name	Meaning
7	IUCR	Invalid or unsupported PMBus command was received. This bit sets during device discovery when using PowerNavigator.
6	IUDR	The PMBus command was sent with invalid or unsupported data.
5	PECF	A packet error check failure was detected in the PMBus command.
4	MFD	Memory fault detected. This bit sets if the selected NVM configuration location is empty or invalid.
3	PFD	Processor fault detected
2	Not Supported	Not supported
1	OCF	A communication fault other than the ones listed in this table occurred.
0	OMLF	A memory or logical fault not listed previously was detected.

11.56 STATUS_MFR_SPECIFIC (80h)

Definition: Returns a summary of the manufacturer specific status.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Command	STATUS_MFR_SPECIFIC (80h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							

Bit	Status Bit Name	Meaning
7	ADCUNLOCK	ADC clock unlock detected.
6	Not Supported	Not supported
5	CFP Fault	A CFP fault occurred.
4	Internal Temperature Fault	The controller internal temperature exceeded 130 °C.
3	BBEVENT	A Black Box event occurred.
2	LMS Event	A Last Man Standing event occurred.
1	SPS Fault	An SPS overcurrent and/or over-temperature event occurred.
0	Not Supported	Not supported

11.57 READ_VIN (88h)

Definition: Returns the input voltage reading, scaled at 10mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: mV

Equation: Read V_{IN} = (Direct value) × 10

Command	READ_VIN (88h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.58 READ_IIN (89h)

Definition: Returns the synthesized input current reading. 10mA per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Read I_{IN} = (Direct value) / 100

Command	READ_IIN (89h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.59 READ_VOUT (8Bh)

Definition: Returns the output voltage reading. 1mV per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: mV

Equation: Read V_{OUT} = (Direct value)

Command	READ_VOUT (8Bh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Unsigned Integer															

11.60 READ_IOUT (8Ch)

Definition: Returns the output current reading. 0.1A per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Read I_{OUT} = (Direct value) / 10

Command	READ_IOUT (8Ch)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.61 READ_TEMPERATURE_1 (8Dh)

Definition: Returns the temperature reading of the smart power stage. 1°C per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Read Temperature 1 = (Direct value)

Command	READ_TEMPERATURE_1 (8Dh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.62 READ_TEMPERATURE_2 (8Eh)

Definition: Returns the internal controller temperature reading. 1°C per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Read Temperature 2 = (Direct value)

Command	READ_TEMPERATURE_2 (8Eh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.63 READ_TEMPERATURE_3 (8Fh)

Definition: Returns the temperature reading from the TEMP pins. 1°C per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Read Temperature 3 = (Direct value)

Command	READ_TEMPERATURE_3 (8Fh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.64 READ_POUT (96h)

Definition: Returns the output power. 1W per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: W

Equation: Read P_{OUT} = (Direct value)

Command	READ_POUT (96h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.65 READ_PIN (97h)

Definition: Returns the input power. 1W per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: W

Equation: READ_PIN = (Direct value)

Command	READ_PIN (97h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.66 PMBUS_REVISION (98h)

Definition: Returns the revision of the PMBus specification to which the device is compliant.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

Command	PMBUS_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	1	1	0	0	1	1

Bits 7:4	Part 1 Revision	Bits 3:0	Part 2 Revision
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2
0011	1.3	0011	1.3

11.67 MFR_ID (99h)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h (empty)

11.68 MFR_MODEL (9Ah)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h (empty)

11.69 MFR_REVISION (9Bh)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h (empty)

11.70 MFR_DATE (9Dh)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h (empty)

11.71 IC_DEVICE_ID (ADh)

Definition: Reports device identification information.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block Read

Default Value: 49D2B000h

Command	IC_DEVICE_ID (ADh)			
Format	Bit Field			
Byte Position	3	2	1	0
Function	MFR Code	ID High Byte	ID Low Byte	Reserved
Default Value	49h	D2h	B0h	00h

11.72 IC_DEVICE_REV (AEh)

Definition: Reports device revision information.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block Read

Default Value: Based on the revision released

Command	IC_DEVICE_REV (AEh)		
Format	Bit Field		
Bit Position	31:24	23:8	7:0
Function	Hardware Revision	Reserved	Firmware Revision

11.73 DMAFIX (C5h)

Definition: Location for DMA access when performing a fixed address memory access. There is no physical storage for this register.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Units: N/A

11.74 DMASEQ (C6h)

Definition: Location for DMA access when performing a auto-increment address memory access. A series of reads or writes accesses sequential memory locations, with the value of DMAADDR incremented with each access. The reads or writes can be singular 32-bit transfers or unlimited bursts. There is no physical storage for this register.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Units: N/A

11.75 DMAADDR (C7h)

Definition: Specifies the target address of a DMA read or write to system memory. This command is used for indirect access to any system memory.

Access: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Units: N/A

Command	DMAADDR (C7h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Field Name	Meaning
15:13	REGION	000 - RAM
12:0	DMAADDR	The 13-bit target address

11.76 PEAK_OC_LIMIT (CDh)

Definition: Sets the peak overcurrent limit thresholds for each phase within the rail. 0.1A per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Equation: Peak Phase OC Limit = (Direct value) / 10

Units: A

Default Value: 01F4h (50A)

Range: Depends on configuration

Command	PEAK_OC_LIMIT (CDh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two’s Complement Integer															
Default Value	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

11.77 PEAK_UC_LIMIT (CEh)

Definition: Sets the peak undercurrent limit thresholds for each phase within the rail. 0.1A per LSB.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Equation: Peak Phase UC Limit = (Direct value) / 10

Units: A

Default Value: FE0C (-50A)

Range: Depends on configuration

Command	PEAK_UC_LIMIT (CEh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	0

11.78 VMON_ON (D0h)

Definition: Sets the VMON pin input voltage rising threshold at which the output can be enabled. 10mV per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 1C2h (4.5V)

Units: mV

Equation: VMON On = (Direct value) × 10

Range: 0mV to 32767mV

Command	VMON_ON (D0h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0

11.79 VMON_OFF (D1h)

Definition: Sets the VMON pin input voltage falling threshold at which the output disables. 10mV per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 190h (4V)

Units: mV

Equation: VMON_OFF = (Direct value) × 10

Range: 0mV to 32767mV

Command	VMON_OFF (D1h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

11.80 COMPPROP (DDh)

Definition: Sets the proportional gain of the compensation loop.

Access: Paged (always set to 0x00)

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: D80189C4h

Command	COMPPROP (DDh)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	1	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0

Bit Position	Function
31:28	Proportional gain mantissa >8 phase override, use normal P gain if value = 0 and shift = 0
27:25	Proportional gain exponent >8 phase override, use normal P gain if value = 0 and shift = 0
24:21	Proportional gain mantissa 2-phase override, use normal P gain if value = 0 and shift = 0
20	Not Used
19:17	Proportional gain exponent 2-phase override, use normal P gain if value = 0 and shift = 0
16:13	Proportional gain mantissa 1-phase override, use normal P gain if value = 0 and shift = 0
12	Not Used
11:9	Proportional gain exponent 1-phase override, use normal P gain if value = 0 and shift = 0
8	FIR filter length, 0 = none or 1 = ON Must be set if using D term for PID, optional if not using D term
7:4	Proportional gain mantissa is (value/8), all phase counts, if value = 0 gain is 0
3	Not Used
2:0	Proportional gain exponent is 2^(shift-3), all phase counts, if value = 0 and shift = 0 gain is 0

11.81 COMPINTEG (DEh)

Definition: Sets the integral gain of the compensation loop.

Access: Paged (always set to 0x00)

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 00A8h

Command	COMPINTEG (DEh)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0

Bit Position	Function
31:16	Not Used
15:12	Delay time for stepping down gain towards shift. DCM when in DCM, in 16×clkTs per gain step
11:8	Gain when in DCM for a while
7:4	Maximum gain used when Integral movement detected Gain is 2^(-shift-1)
3:0	Gain is 2^(-shift-1)

11.82 COMPDIFF (DFh)

Definition: Sets the differential gain of the compensation loop.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0020h

Command	COMPDIFF (DFh)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit Number	Setting
15:13	Reserved
12	FIR filter length 0 or 1
11:8	Differentiator gain mantissa 1-phase override, use normal P gain if value = 0 and shift = 0
7:6	Differentiator gain exponent 1-phase override, use normal P gain if value = 0 and shift = 0
5:2	Differentiator gain mantissa (value/8)
1:0	Differentiator gain exponent 2^(shift+1 + P-shift) range 0:3

11.83 COMPCFB (E0h)

Definition: Sets the AC current feedback gain of the compensation loop.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 6840h

Command	COMPCFB (E0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0	0

Bit Number	Function
15:8	High-pass filter coefficient for current feedback
7:0	Current feedback gain, low droop cases

11.84 HS_BUS_CURRENT_SCALE (E3h)

Definition: Sets the scaling value for the high speed bus output current reporting. 16 bits with 14 fractional bits. A value of 0x4000 is a scale factor of 1.0. A value of 0x0000 is also interpreted as a scale factor of 1.0.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 4000h (1.0)

Units: Scale Factor

Equation: HS Bus Current Scale = (Direct value) × 2^{-14}

Range: 0 to 4.0

Command	HS_BUS_CURRENT_SCALE (E3h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Unsigned Integer															
Default Value	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.85 PHASE_CURRENT (E4h)

Definition: Returns the individual phase current reading for the phase selected in PHASE (04h). 0.1A per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Phase current = (Direct value) / 10

Command	PHASE_CURRENT (E4h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.86 PHASE_TEMPERATURE (E5h)

Definition: Returns the individual phase temperature reading for the phase selected in PHASE (04h). 1°C per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Phase Temperature = (Direct value)

Command	PHASE_TEMPERATURE (E5h)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Two's Complement Integer															

11.87 PEAK_OCUC_COUNT (E9h)

Definition: Sets the number of consecutive switch cycles that can exceed the peak per-phase overcurrent limit threshold before generating a fault within the rail. A value of 0 disables the fault shutdown and produces a constant current effect.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Equation: Peak UC Count = (Direct value [15:8]), Peak OC Count = (Direct value [7:0])

Units: Cycles

Default Value: 0606h (6 cycles OC and 6 cycles UC)

Range: 1 cycle - 255 cycles

Command	PEAK_OCUC_COUNT (E9h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0

Bit Number	Meaning
15:8	Number of consecutive switch cycles exceeding peak UC limit before fault.
7:0	Number of consecutive switch cycles exceeding peak OC limit before fault.

11.88 SLOW_IOUT_OC_LIMIT (EAh)

Definition: Sets the slow sum output overcurrent fault threshold. 100mA per LSB. A value of 0 disables this function.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4h (50A)

Units: A

Equation: Slow I_{OUT} OC Limit = (Direct value) / 10

Range: 0A to 3276A

Command	SLOW_IOUT_OC_LIMIT (EAh)															
Format	Direct															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Two's Complement Integer															
Default Value	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

11.89 FAST_OC_FILT_COUNT (EBh)

Definition: Sets the fast sum output overcurrent fault filter settings.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0696h (Filter = 10.7µs, Delay = 100µs)

Command	FAST_OC_FILT_COUNT (EBh)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0

Bit Number	Purpose	Setting
15:12	Not Used	Not used
11:8	Filter Setting	Time constant = 166.7ns × 2^direct value. Range is 167ns to 5.46ms.
7:0	Delay Setting	Delay 0.667µs × direct value before a fault is generated. Range is 0µs to 170µs.

11.90 SLOW_OC_FILT_COUNT (ECh)

Definition: Sets the slow sum output overcurrent fault filter settings.

Access: Paged (always set to 0x00)

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0606h (Filter = 10.7µs, Delay = 1024µs)

Command	SLOW_OC_FILT_COUNT (EBh)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0

Bit Number	Purpose	Setting
15:12	Not Used	Not used
11:8	Filter Setting	Time constant = 166.7ns × 2^direct value. Range is 167ns to 5.46ms.
7:0	Delay Setting	Delay 170.7µs × direct value before a fault is generated. Range is 0µs to 43.5ms.

11.91 LOOPCFG (F0h)

Definition: Configures various rail settings. To make a change, read the value, modify only the desired bits, and write the value while preserving the bit settings.

Access: Paged (always set to 0x00)

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 002371B6h

Command	LOOPCFG (F0h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	1	1	1	0	0	0	1	1	0	1	1	0	1	1	0

Bit Position	Field	Function
31	Not Used	Not used
30:29	Reserved	Reserved
28	Reserved	Reserved
27:12	Reserved	Reserved
11:8	Minimum Phase Count	Minimum phase count, 0-2
7	Reserved	Reserved
6	Reserved	Reserved
5:4	Reserved	Reserved
3:1	Reserved	Reserved
0	Reserved	Reserved

11.92 RESTORE_CFG (F2h)

Definition: Identifies the user configuration ID to be restored from NVM and loads the stored settings into the active memory of the device. This command should only be used while the output is disabled. Restore takes 3ms to complete.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h

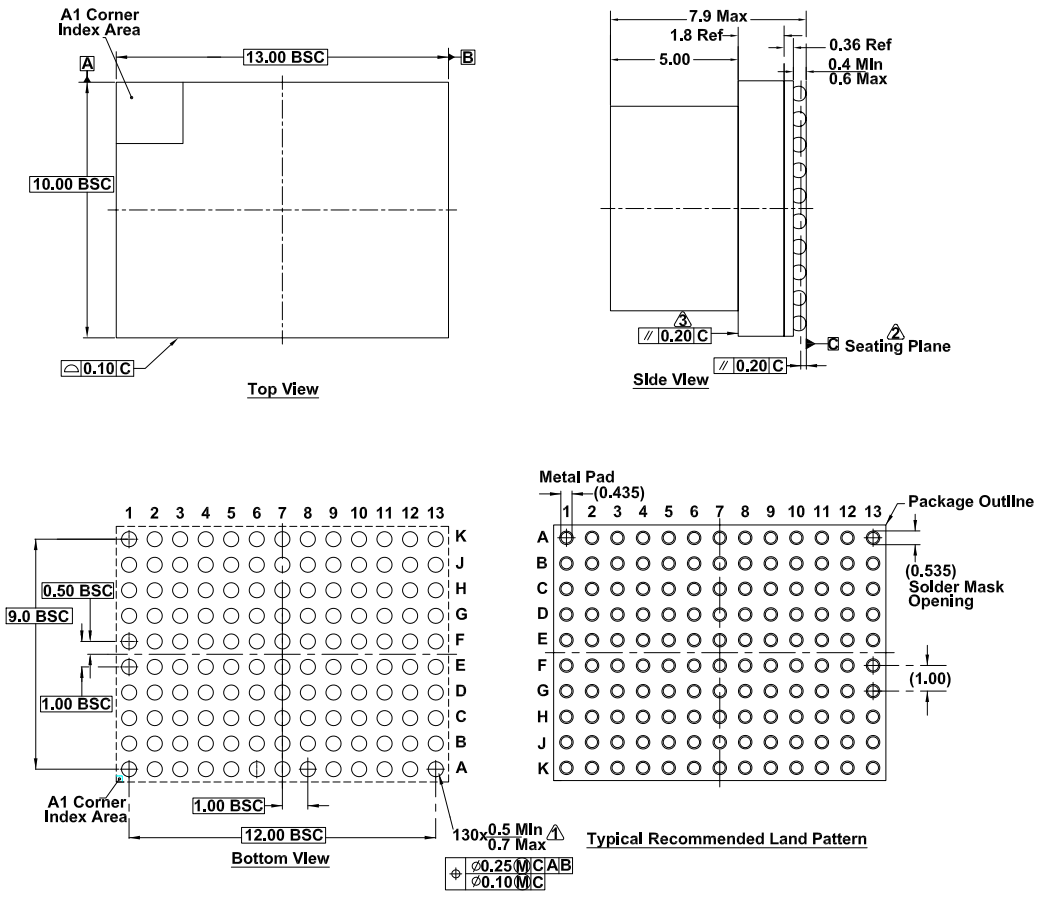
Command	RESTORE_CFG (F2h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Meaning
7:4	Reserved	Reserved
3:0	CONFIG	Selected user configuration ID to restore, 0-15.

12. Package Outline Drawing

For the most recent package outline drawing, see V130.10x13.

V130.10x13
130 Ball Plastic Ball Grid Array Package (POP)
Rev 0, 6/2021



Notes:

1. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
2. Datum C (seating plane) is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of the mark on the top surface of the package.
4. All dimensions and tolerances conform to ASME Y14.5M.
5. Units: mm

13. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	PKG. Dwg.#	Carrier Type	Junction Temp. Range
RAA210130GBG#AD0	RAA210130	130 Ball BGA+POP	V130.10X13	Tray	-40 to +125°C
RTKA210130DE0020BU	Evaluation Board				

1. These Pb-free BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu-e6 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA210130 product information page. For more information about MSL, see TB363.

14. Revision History

Rev.	Date	Description
1.02	Oct 6, 2022	Footnote 3 removed from Ordering Information.
1.01	Jun 8, 2022	Updated Table 1 Note. Updated Table 3 by adding Note and references.
1.00	May 16, 2022	Initial release.

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