Evaluating the LT3097 Dual 500mA, Positive/Negative, Ultra-Low Noise, Ultra-High PSRR, Low Dropout Linear Regulator

FEATURES

- Input voltage range: ±3.8 V to ±20 V
- Resistor programmed ±3.32 V output
- Maximum output current: 500 mA
- BNC Connectors for noise and PSRR measurement
- Resistor programmed power good
- Resistor-programmable current limit and UVLO
- Positive-channel current monitoring
- Thermally enhanced 22-lead, 6 mm × 3 mm, Plastic DFN package

EVALUATION KIT CONTENTS

- EVAL-LT3097-AZ evaluation board

DOCUMENTS NEEDED

- LT3097 data sheet

EQUIPMENT NEEDED

- DC power supplies
- Multimeters for voltage and current measurements
- Electronic or resistive loads

EVALUATION BOARD PHOTOGRAPH

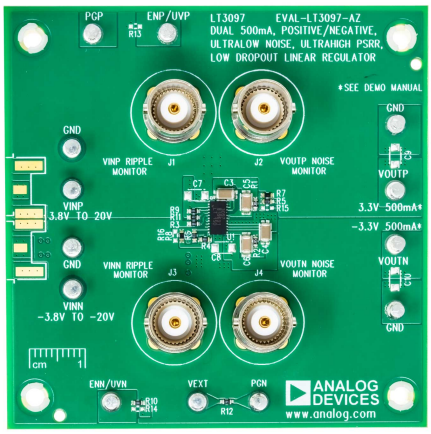

Figure 1. EVAL-LT3097-AZ Evaluation Board Photograph

GENERAL DESCRIPTION

The EVAL-LT3097-AZ evaluation board features the LT3097, a dual 500mA, positive/negative, ultra-low noise, and ultra-high power supply rejection ratio (PSRR), low-dropout (LDO) linear regulator.

The EVAL-LT3097-AZ operates over an input voltage range of 3.8 V to 20 V for the positive channel and an input voltage range of -3.8V to -20V for the negative channel. The LT3097 delivers maximum output currents of 500mA. In addition to featuring ultra-low noise and ultra-high PSRR, each channel of the regulator offers programmable power good functionality and a programmable current limit. Current monitoring is also achieved for the positive channel by sensing the ILIMP pin voltage. ILIMN architecture does not allow output current monitoring for the negative channel. The negative channel enable function (ENN/UVN pin) is bidirectional and can be controlled with either a positive or a negative voltage.

Built-in protection for the positive channel includes reverse-battery protection and reverse current protection. Built-in protection for both channels includes an internal current limit with foldback and a thermal limit with hysteresis.

For full details on the LT3097, refer to the LT3097 datasheet, which must be consulted with this user guide when using the EVAL-LT3097-AZ evaluation board.

The LT3097 of the EVAL-LT3097-AZ features a 22-lead, 6 mm x 3 mm Plastic dual-flat no-leads (DFN) package with exposed pads on the bottom side of the IC. Proper board layout is essential for maximum thermal performance.

Design files are available on the EVAL-LT3097-AZ evaluation board page.

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REVISION HISTORY

3/2023—Revision 0: Initial Version

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Table 1. Performance Summary

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POSITIVE INPUT VOLTAGE	V_{INP}					
Minimum					3.8	V
Maximum		V_{INP} = $\lvert V_{INN}\rvert$, Positive output current (I_{OUTP}) = Negative output current (I_{OUTN}) = 100 mA, V_{OUTP} = 3.32 V, V_{OUTN} = –3.32 V	20			V
		V_{INP} =$\lvert V_{INN}\rvert$, I_{OUTP} = I_{OUTN} = 500 mA, V_{OUTP} = 3.32 V, V_{OUTN} = –3.32 V	6.5[1]			V
NEGATIVE INPUT VOLTAGE	V_{INN}					
Minimum			–3.8			V
Maximum		V_{INP} =$\lvert V_{INN}\rvert$, I_{OUTP} = I_{OUTN} = 100 mA, V_{OUTP} = 3.32 V, V_{OUTN} = -3.32 V			–20	V
		V_{INP} =$\lvert V_{INN}\rvert$, I_{OUTP} = I_{OUTN} = 500 mA, V_{OUTP} = 3.32 V, V_{OUTN} = -3.32 V			–6.5[1]	V
POSITIVE OUTPUT VOLTAGE	V_{OUTP}	V_{INP} = 5 V, I_{OUTP} = 500 mA, R1 = 33.2 KΩ	3.25	3.32	3.39	V
NEGATIVE OUTPUT VOLTAGE	V_{OUTN}	V_{INN} = -5 V, I_{OUTN} = 500 mA, R2 = 33.2 KΩ	–3.39	-3.32	–3.25	V
POSITIVE SHUTDOWN INPUT CURRENT	I_{INP}	$V_{ENP/UVP}$ = 0 V, V_{INP} = 5V, R9 = OPEN		0.3		µA
NEGATIVE SHUTDOWN INPUT CURRENT	I_{INN}	$V_{ENN/UVN}$ = 0 V, V_{INN} = -5V, R10 = OPEN		3		µA

[1] The maximum power dissipation and, consequently, the maximum input voltage for 500mA load current is set by the 60°C temperature rise of the LT3097 on the evaluation board. Higher input voltages can be reached if a larger copper area or forced-air cooling is applied. In addition, consider the effect of ambient temperature and the maximum junction temperature that can occur. The LT3097 limits output current at higher input to output voltage differentials. Refer to the LT3097 datasheet for more information.

QUICK START PROCEDURE

The EVAL-LT3097-AZ evaluation board is simple to set up to evaluate the performance of the LT3097. See Figure 2 for proper measurement equipment setup and use the following procedure:

1. Connect loads between the VOUTP and GND terminals and between the VOUTN and GND terminals.
2. With power off, connect the input power supplies to the VINP and GND terminals and to the VINN and GND terminals.
3. With the loads turned down, turn the input power supplies on, and ensure that the voltage between the VINP and GND terminals is between 3.8 V and 20 V and the voltage between the VINN and GND terminals is between –3.8 V and –20 V.
4. Vary VINP from 3.8V to 20V and vary VINN from –3.8V to –20V. Vary the load currents from 0 mA to 500 mA. Note the following when setting VINP, VINN, and the load currents:
   - An input voltage too close to the programmed output voltage (too low) can cause dropout operation and a loss of output-voltage regulation.
   - The amount of output current combined with an input voltage that is too high above the output can increase power dissipation to an unacceptable level.
   - The LT3097 limits output current at higher input-to-output voltage differentials. Refer to the LT3097 data sheet for more information.
5. Refer to Application Note AN83 and Application Note AN-159 for measuring output noise and PSRR. Note: J1, J2, J3, and J4 are Bayonet Neill-Concelman (BNC) connectors used for noise and PSRR measurements.
6. R13 and R14 can be used to set an accurate undervoltage lockout (UVLO) threshold.
7. Change to a suitable ILIMP resistor (R3) or ILIMN resistor (R4) to program a current limit. Output current monitoring is provided at the ILIMP resistor or pin. ILIMN architecture does not allow output current monitoring for the negative channel.
8. In addition, change the PGFBP divider resistors (R5 and R7) or the PGFBN divider resistors (R6 and R8) if the SETP resistor (R1) or SETN resistor (R2) is changed. Monitor power good for the positive channel at the PGP terminal. Apply a power source at VEXT and monitor power good for the negative channel at the PGN terminal.

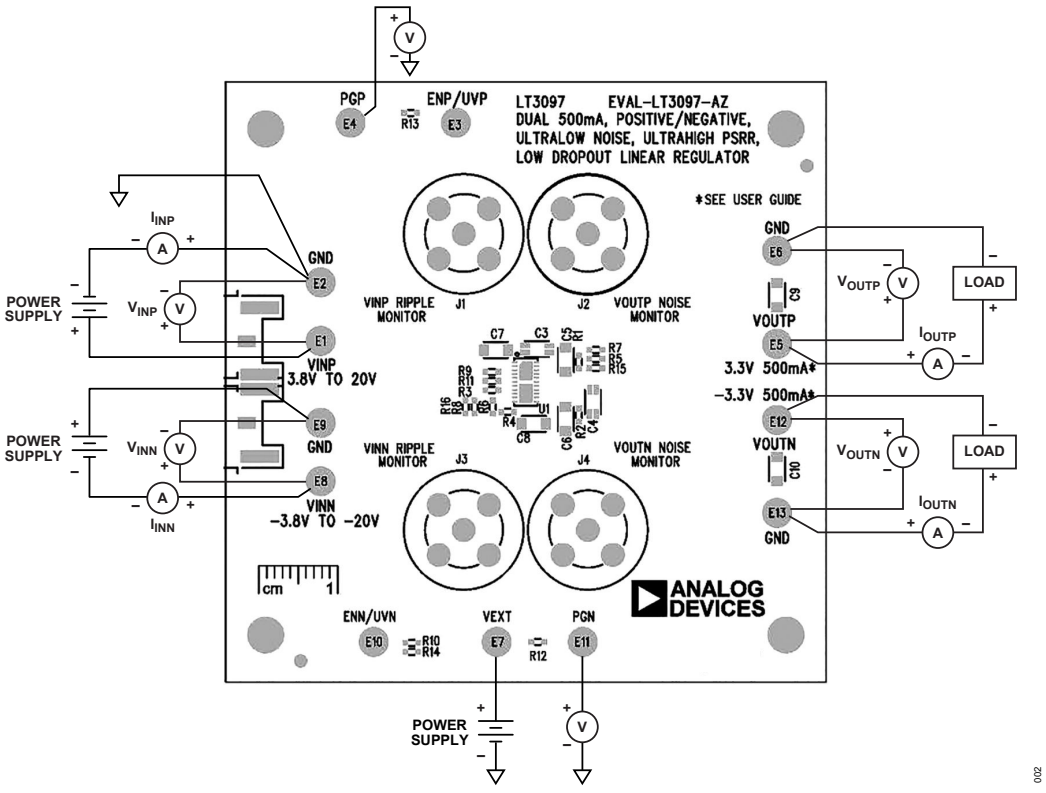

Figure 2. Proper Measurement Equipment Setup for EVAL-LT3097-AZ

PRINTED CIRCUIT BOARD (PCB) LAYOUT

BEST PSRR PERFORMANCE: PCB LAYOUT FOR INPUT TRACES

For applications using the LT3097 for post-regulating switching converters, placing a capacitor directly at the LT3097 input results in AC current (at the switching frequency) flowing near theLT3097. Without careful attention to PCB layout, the high-frequency switching current generates an electromagnetic field (EMF) that couples to the LT3097 output, degrading its effective PSRR. Highly dependent on the PCB, the switching preregulator, and the input capacitor size, among other factors, the PSRR degradation can easily be 30 dB at 1 MHz. This degradation is present even if the LT3097 is desoldered from the board because it effectively degrades the PSRR of the PC board itself. While negligible for conventional low PSRR LDOs, the LT3097's ultra-high PSRR requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The LT3097 evaluation board alleviates this degradation in PSRR by using a specialized layout technique. The VINP input trace and its corresponding return path (GND) are highlighted in red in Figure 3 and Figure 4. Similarly, the VINN input trace and its corresponding return path (GND) are highlighted in blue in Figure 3 and Figure 4. Figure 4 also shows the location of input capacitors C1 and C2. Normally when AC voltages are applied to the inputs of the board, AC current flows on the input and return paths, thus generating EMF. This EMF couples to output capacitors C3 and C4 and the related traces, making the PSRR appear worse than it is. With the input traces directly above the return paths, the EMFs are in opposite directions and consequently, cancel each other out. Making sure that these traces overlap each other exactly maximizes the cancellation effect and thus provides the maximum PSRR offered by the regulator.

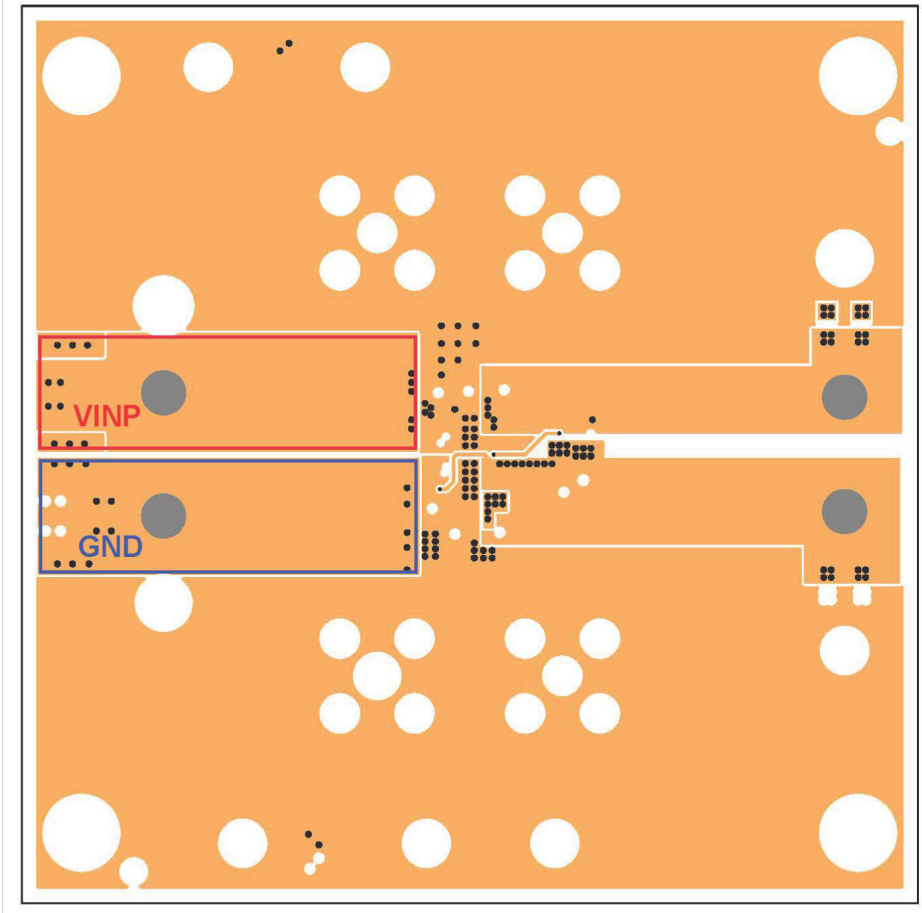

Figure 3. Layer 3 of EVAL-LT3097-AZ

PRINTED CIRCUIT BOARD (PCB) LAYOUT

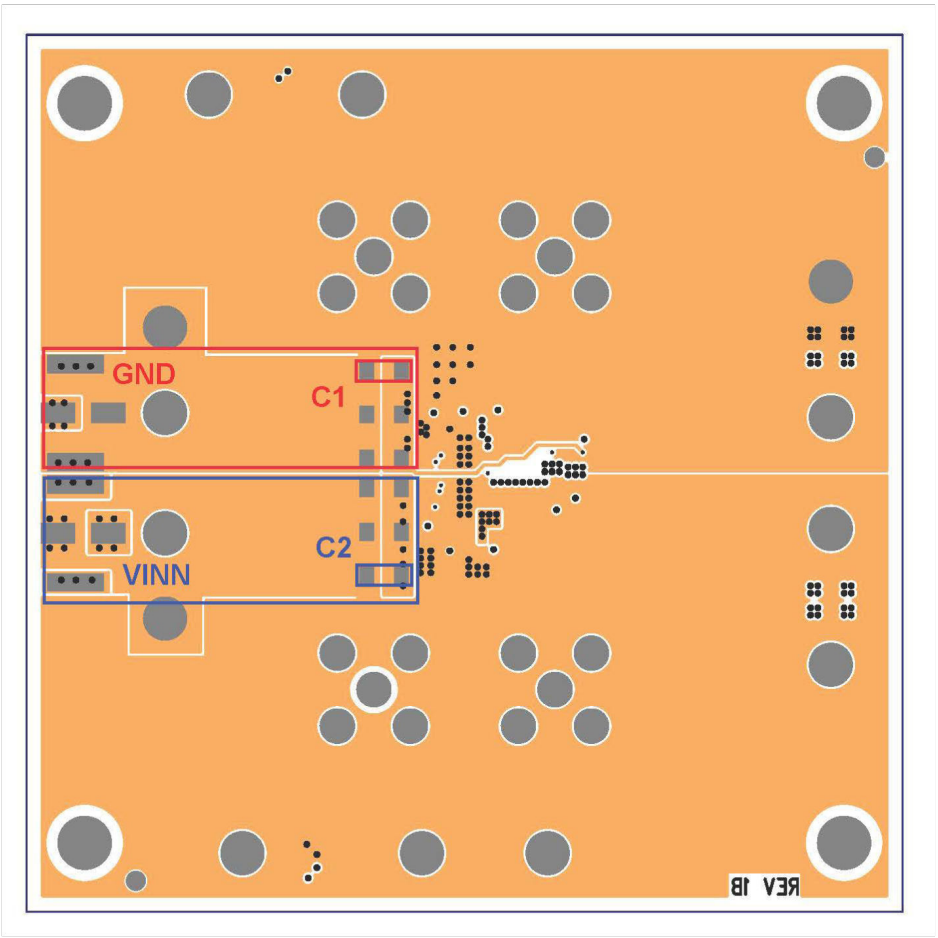

Figure 4. Layer 4 of EVAL-LT3097-AZ

PRINTED CIRCUIT BOARD (PCB) LAYOUT

BEST AC PERFORMANCE: PCB LAYOUT FOR OUTPUT CAPACITORS C3 AND C4

For ultra-high PSRR performance, the LT3097 bandwidth is quite high (~1 MHz), making it very close to the output capacitor's self-resonance frequency (~1.6 MHz). Therefore, avoiding adding extra impedance ((effective-series inductance (ESL) and effective-series resistance (ESR)) outside the feedback loop is very important. To achieve this avoidance, minimize the effects of PCB trace and solder inductance by Kelvin connecting output sense (OUTSP and OUTSN) and SET pin capacitor (C_{SETP} and C_{SETN}) GND directly to the terminals of output capacitors (C3 and C4) using a split capacitor technique as shown in Figure 5 and Figure 6. With only a small AC current flowing through these connections, the impact of solder joint/PCB trace inductance on stability is eliminated. While the LT3097 is robust enough not to oscillate, if the recommended layout is not followed, phase/gain margin and stability degrades.

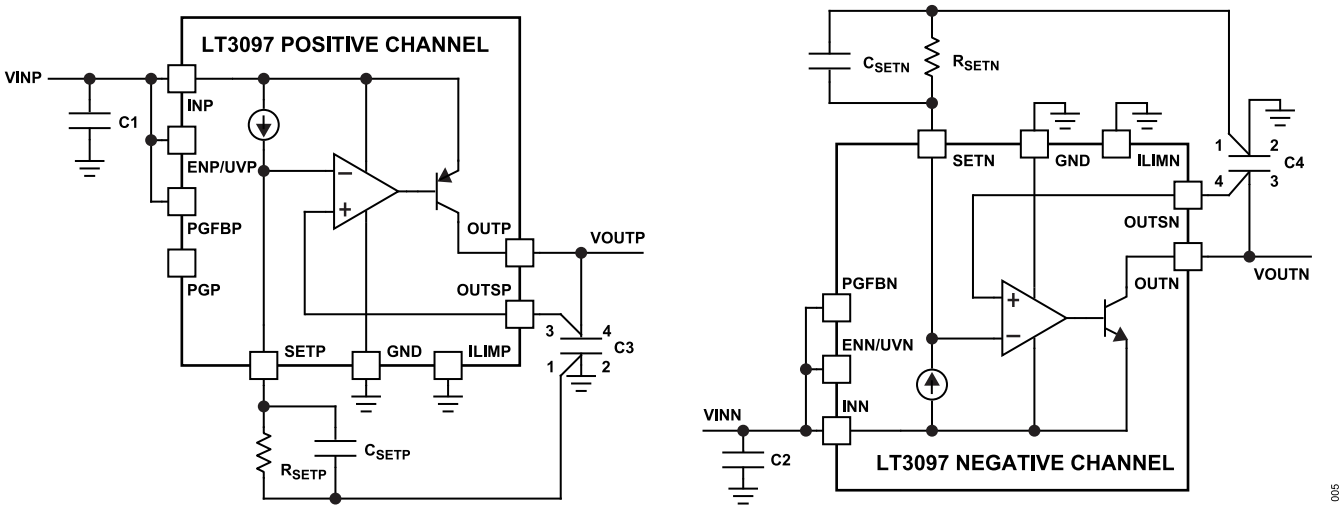

Figure 5. C3, C4, C_{SETP}, and C_{SETN} Connections for Best Performance

PRINTED CIRCUIT BOARD (PCB) LAYOUT

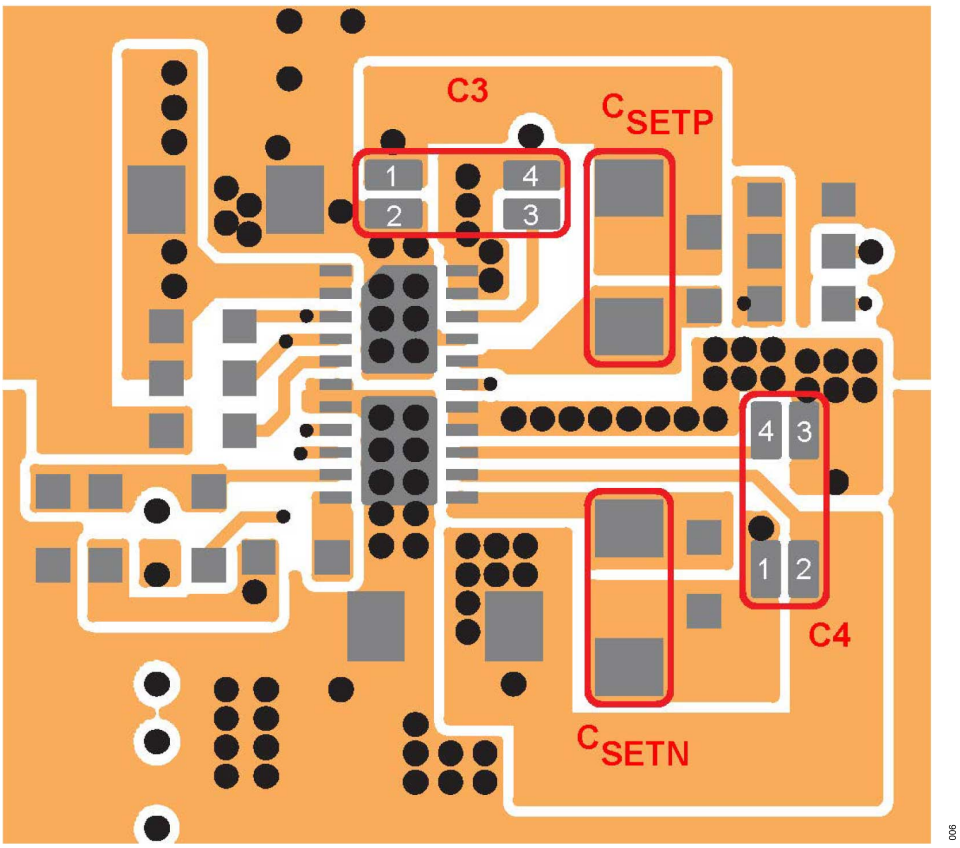

Figure 6. Split Pads for C3 and C4 on the Top Layer of EVAL-LT3097-AZ

EVALUATION BOARD SCHEMATIC

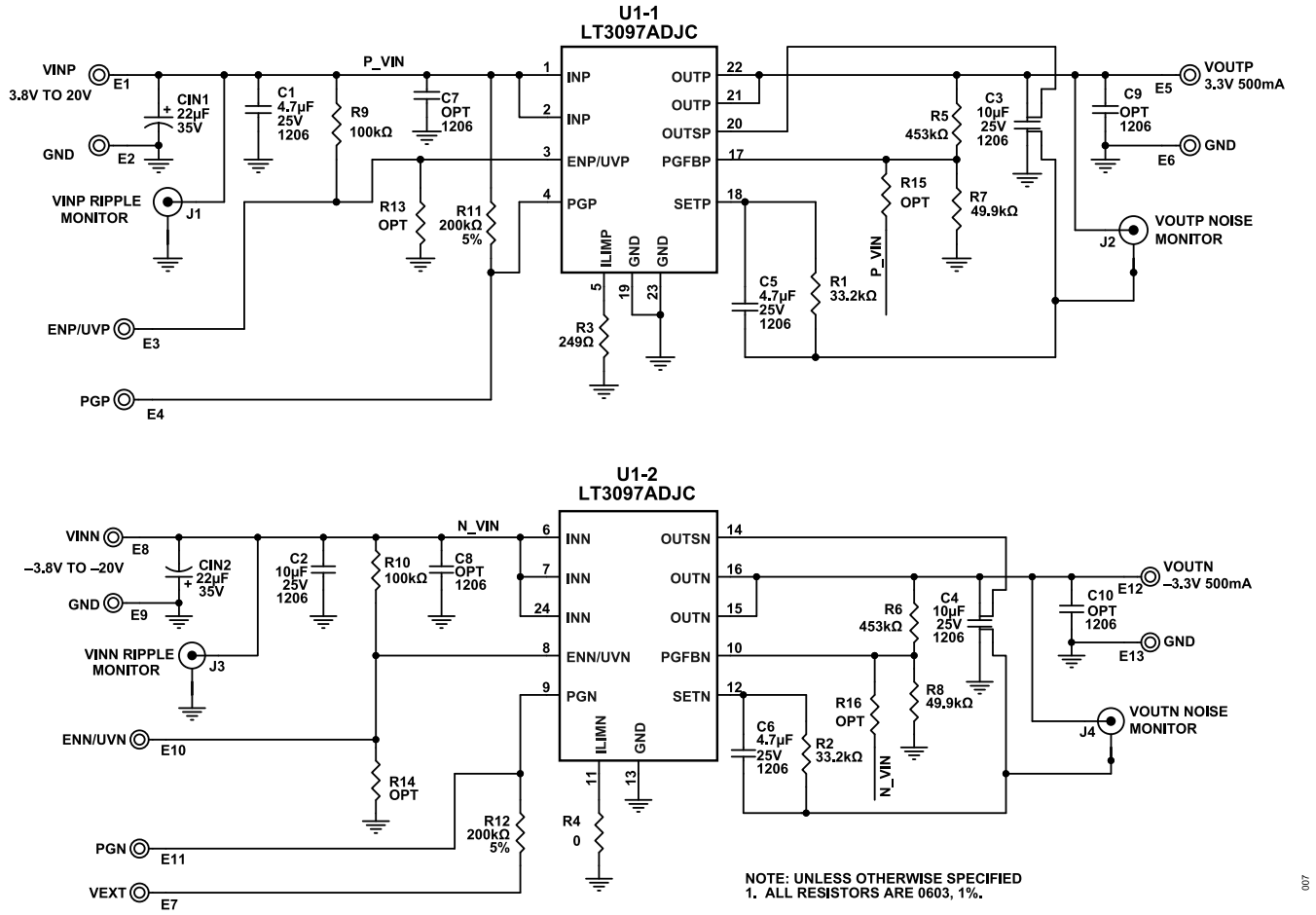

Figure 7. EVAL-LT3097-AZ Evaluation Board Schematic

ORDERING GUIDE

BILL OF MATERIALS

Table 2. Bill of Materials

Item	Quantity[1]	Reference Designator	Part Description	Manufacturer, Part Number
Required Circuit Components				
1	1	C1	4.7 µF capacitor, X7R, 25 V, 10%, 1206	AVX, 12063C475KAT2A
2	1	C2	10 µF capacitor, X7R, 25 V, 10%, 1206	AVX, 12063C106KAT2A
3	2	C3, C4	10 µF capacitor, X7S, 25 V, 10%, 1206	MURATA, GCM31CC71E106KA03L
4	2	C5, C6	4.7 µF capacitor, X7R, 25 V, 10%, 1206, soft termination	MURATA, GCJ31CR71E475KA12L
5	2	R1, R2	33.2 kΩ resistor, 1%, 1/10 W, 0603	Vishay, CRCW060333K2FKEA
6	1	U1	Dual 500mA, positive/negative, ultra-low noise, ultra-high PSRR, low dropout linear regulator	Analog Devices, Inc., LT3097ADJC#PBF
Optional Evaluation Board Components				
1	2	CIN1, CIN2	22 µF capacitor, 35 V, 20%, 5 mm × 5.4 mm	Sun Electronic Industries, 35CE22BSS
2		C7 to C10	Capacitors, 1206, optional	
3	1	R3	249 Ω resistor, 1%, 1/10 W, 0603	Vishay, CRCW0603249RFKEA
4	1	R4	0 Ω, 1/10 W, 0603, AEC-Q200	Vishay, CRCW06030000Z0EA
5	2	R5, R6	453 kΩ resistor, 1%, 1/10 W, 0603	Vishay, CRCW0603453KFKEA
6	2	R7, R8	49.9 kΩ resistor, 1%, 1/10 W, 0603	Vishay, CRCW060349K9FKEA
7	2	R9, R10	100 kΩ resistor, 1%, 1/10 W, 0603	Vishay, CRCW0603100KFKEA
8	2	R11, R12	200 kΩ resistor, 5%, 1/10 W, 0603	Vishay, CRCW0603200KJNEA
9		R13 to R16	Resistor, 0603, optional	
Hardware				
1	13	E1 to E13	Test points, turret, 0.094" PBF	Mill-Max, 2501-2-00-80-00-00-07-0
2	4	J1 to J4	Connector, RF, BNC, receptacle, jack, 5-pin, straight, through-hole, 50 Ω	Amphenol RF, 112404
3	4	MP1 to MP4	Standoff, nylon, snap-on, 6.4 mm	Würth Elektronik, 702931000

[1] Blank cell is for optional components.

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.