Description

The 5P35023 is a VersaClock programmable clock generator and is designed for low-power, consumer, and high-performance PCI Express applications. The 5P35023 device is a three PLL architecture design, and each PLL is individually programmable and allowing for up to six unique frequency outputs.

The 5P35023 has built-in unique features such as Proactive Power Saving (PPS), Performance-Power Balancing (PPB), Overshot Reduction Technology (ORT) and Extreme Low Power DCO. An internal OTP memory allows the user to store the configuration in the device. After power up, the user can change the device register settings through the I2C interface when I2C mode is selected.

The device has programmable VCO and PLL source selection to allow the user to do power-performance optimization based on the application requirements. It also supports three single-ended outputs and two pair of differential outputs that support LVCMOS, LVPECL, LVDS and LP-HCSL. A Low Power 32.768kHz clock is supported with only less than 2µA current consumption for system RTC reference clock.

Typical Applications

- PCIe Gen1–3 clock generator
- Consumer application crystal replacements
- SmartDevice, Handheld
- Computing and consumer applications
- Automotive applications (infotainment, dashboard, camera/vision, computing, networking)

Key Specifications

- PCIe clocks phase jitter: PCIe Gen3
- Differential clocks < 1.5ps rms jitter integer range 12kHz–20MHz

Features

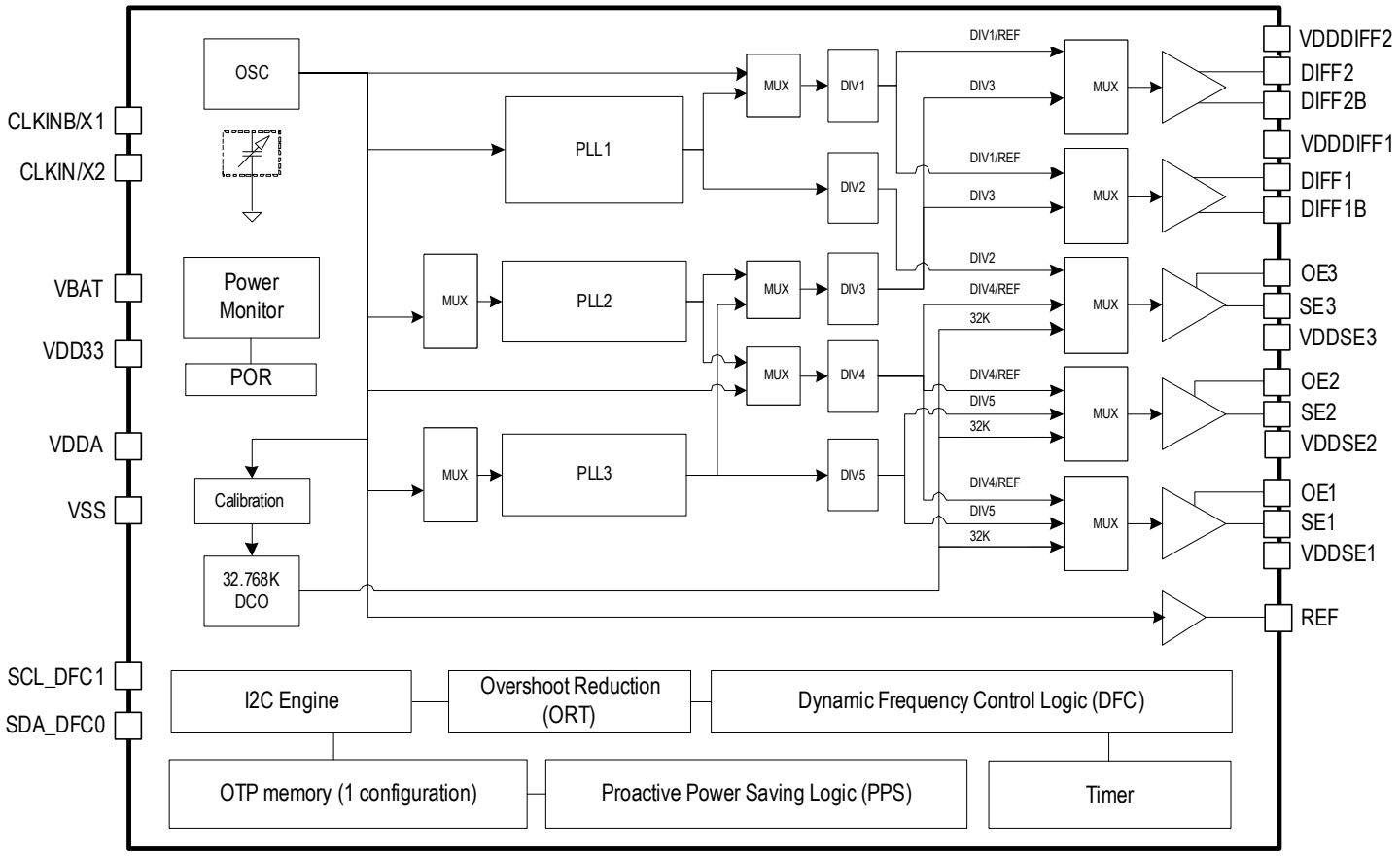
- Configurable OE pin function as OE, PD#, PPS or DFC control function
- Configurable PLL bandwidth; minimizes jitter peaking
- PPS: Proactive Power Saving features save power during the end device power down mode
- PPB: Performance Power Balancing feature allows minimum power consumption based on required performance
- DFC: Dynamic Frequency Control feature allows user to dynamically switch between and up to 4 different frequencies smoothly
- Two PLLs support independent spread spectrum clocks to lower system EMI
- Store user configuration into OTP memory
- I^2C interface
- Available in Automotive Grade 2 (-40°C to +105°C) or industrial (-40° to +85°) temperature ranges

Output Features

- 2 DIFF outputs with configurable LP-HSCL, LVDS, LVPECL, LVCMOS output pairs. 1MHz–500MHz (160MHz with LVCMOS mode)
- 3 LVCMOS outputs: 1MHz–160MHz
- Maximum 8 LVCMOS outputs as REF + 3 × SE + 2 × DIFF_T/C as LVCMOS
- Low power 32.768kHz clock supported for all SE1–SE3

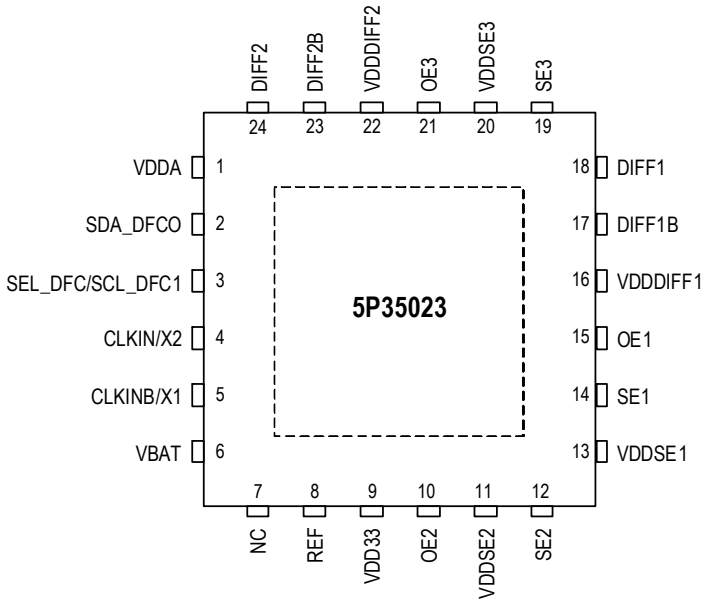
Contents

Block Diagram



Pin Assignments

Figure 1. Pin Assignments for 4 x 4 mm 24-VFQFPN Package – Top View



24-VFQFPN

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	V_{DDA}	Power	V_{DD} 3.3V
2	SDA_DFC0	I/O	I^2C data pin. The pin can be DFC0 function by pin 3 SEL_DFC power-on latch status.
3	SEL_DFC/ SCL_DFC1	Input	I^2C CLK pin. SEL_DFC is a latch input pin during the power-up. High on power-on: I^2C mode as SCLK function. Low on power-on: SCL and SDA as DFC function control pins.
4	CLKIN/X2	I/O	Crystal oscillator interface output or differential clock input pin (CLKIN).
5	CLKINB/X1	Input	Crystal oscillator interface input or differential clock input pin (CLKINB) or single-ended clock input.
6	V_{BAT}	Power	Power supply pin for 32.768kHz DCO; usually connect to coin cell battery, 3.0V–3.3V.
7	NC	—	No connect.
8	REF	Output	3.3V reference clock output.
9	V_{DD33}	Power	V_{DD} 3.3V.
10	OE2	Input	Output enable control 2, multi-function pin. Refer to OE Pin Functions table.
11	V_{DDSE2}	Power	Output power supply. Connect to 1.8 –3.3V. Sets output voltage levels for SE2.
12	SE2	Output	Output clock SE2.
13	V_{DDSE1}	Power	Output power supply. Connect to 1.8V–3.3V. Sets output voltage levels for SE1.
14	SE1	Output	Output clock SE1.
15	OE1	Input	OE1's function selected from OTP pre-programmed register bits. OE1 pull to 6.5V when burn OTP registers. Refer to OE Pin Functions table for details.
16	$V_{DDDIFF1}$	Power	Output power supply. Connect to 2.5V–3.3V. Sets output voltage levels for DIFF1.
17	DIFF1B	Output	Differential clock output 1_Complement; can be OTP pre-programmed to LVCMOS/LPHCSL/LVDS/LVPECL output type.
18	DIFF1	Output	Differential clock output 1_True; can be OTP pre-programmed to LVCMOS/LP-HCSL/LVDS/LVPECL output type.
19	SE3	Output	Output clock SE3.
20	V_{DDSE3}	Power	Output power supply. Connect to 1.8V–3.3V. Sets output voltage levels for SE3.
21	OE3	Input	Output enable control 3, multi-function pin. Refer to OE Pin Functions table.
22	$V_{DDDIFF2}$	Power	Output power supply. Connect to 2.5V–3.3V. Sets output voltage levels for DIFF2.
23	DIFF2B	Output	Differential clock output 2_Complement; can be OTP pre-programmed to LVCMOS/LP-HCSL/LVDS/LVPECL output type.
24	DIFF2	Output	Differential clock output 2_True; can be OTP pre-programmed to LVCMOS/LP-HCSL/LVDS/LVPECL output type.
	EPAD	Power	Connect to ground pad.

Power Group

Table 2. Power Group

Power Supply	SE	DIFF	DIV	MUX	PLL	DCO	REF	Xtal
V_{DDSE1}	SE1 [1]							
V_{DDSE2}	SE2 [1]							
V_{DDSE3}	SE3 [1]							
$V_{DDDIFF1}$		DIFF1	DIV3/4	MUXPLL2	PLL2			
$V_{DDDIFF2}$		DIFF2	DIV1	MUXPLL1				
V_{DD33}			DIV5		PLL3	DCO	REF	Xtal
V_{BAT}						DCO		Xtal
V_{DDA}			DIV2		PLL1			

[1] V_{DDSEx} for non-32kHz outputs should be OFF when V_{DDA}/V_{DD33} turns OFF; V_{BAT} mode only supports 32.768kHz outputs from SE1–3.

Output Sources

Table 3. Output Source

Source	Outputs					
	REF	SE1	SE2	SE3	DIFF1	DIFF2
Xtal REF	Xtal REF	Xtal REF	Xtal REF	Xtal REF		
32.768kHz		32.768kHz	32.768kHz	32.768kHz		
PLL1				PLL1	PLL1	PLL1
PLL2		PLL2	PLL2	PLL2	PLL2	PLL2
PLL3		PLL3	PLL3		PLL3	PLL3

Table 4. Output Source Selection Register Settings

SE1	B36<4>	B36<3>	B31<1>	B29<3>
From 32kHz	0	1	0	0
From PLL3 + Divider 5	1	0	0	0
From PLL2 + Divider 4	1	1	1	0
From REF + Divider 4	1	1	0	1

Table 5. Output Source Selection Register Settings

SE2	B31<7>	B31<6>	B36<0>	B31<1>	B29<3>
From 32kHz	0	0	0	0	0
From PLL3 + Divider 5	1	0	0	0	0
From PLL2 + Divider 4	1	1	1	1	0
From REF + Divider 4	1	1	1	0	1

Table 6. Output Source Selection Register Settings

SE3	B33<7>	B33<6>	B7<5>	B29<3>	B36<1>	B31<1>
From 32kHz	0	0	0	0	0	0
From PLL3 + Divider 5	1	0	1	0	0	0
From PLL2 + Divider 4	1	1	0	0	1	1
From REF + Divider 4	1	1	0	1	1	0

Table 7. DIFF1 Output

DIFF1	B34<7>	B0<3>
From PLL1 + Divider 1	0	0
From PLL2/3 + Divider 3	1	0
From REF + Divider 1	0	1

Table 8. DIFF2 Output

DIFF2	B35<7>	B0<3>
From PLL1 + Divider 1	0	0
From PLL2/3 + Divider 3	1	0
From REF + Divider 1	0	1

Device Features and Functions

DFC – Dynamic Frequency Control

- OTP programmable – 4 different feedback fractional dividers (4 VCO frequencies) that apply to PLL2.
- ORT (overshoot reduction) function will be applied automatically during the VCO frequency change.
- Smooth frequency incremental or decremental from current VCO to targeted VCO based on DFC hardware pins selection.

Figure 2. DFC Function Block Diagram

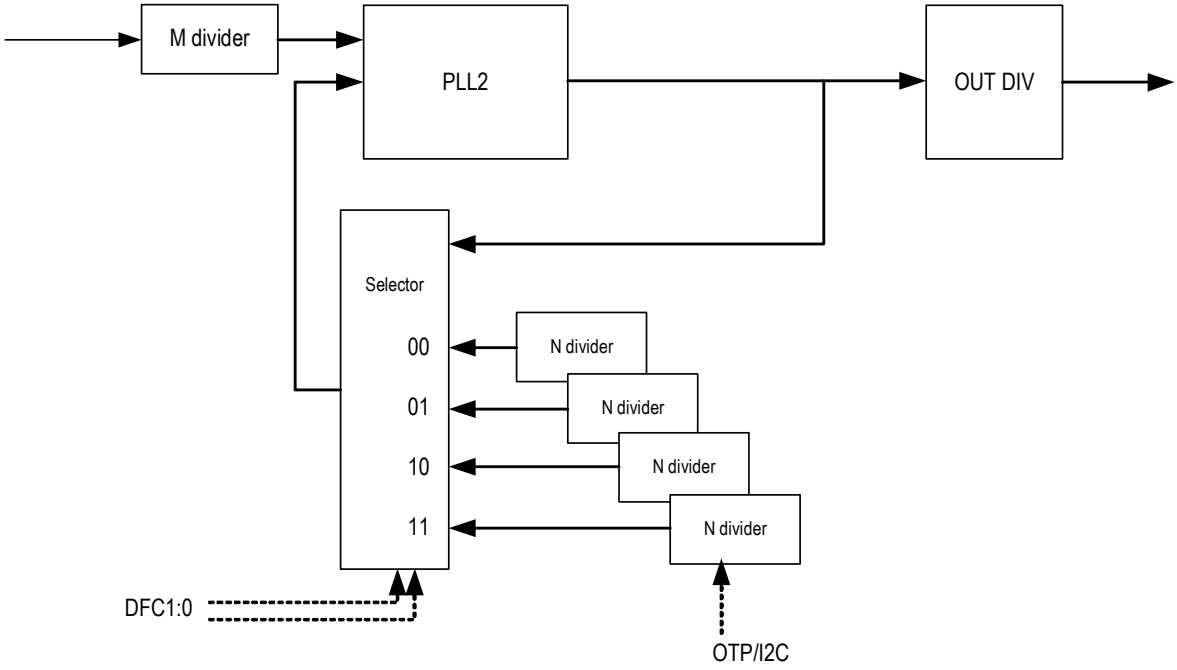


Table 9. DFC Function Priority

DFC_EN bit (W32[4])	OE1_fun_sel (W30[6:5])	OE3_fun_sel (W30[3:2])	SCL_DFC1	DFC[1:0]	Notes
0	x	x	x	0	DFC disable
1	11 (DFC)	00–10 (DFC)	x	[0,OE1]	One-pin DFC–OE1
1	11 (DFC)	11 (DFC)	x	[OE3,OE1]	Two-pin DFC–OE3, OE1
1	00–10	11	x	Not permitted	Not supported
1	00–10	00–10	0	[SCL_DFC1, SDA_DFC0]	I^2C pin as DFC control pins mode
1	00–10	00–10	1	W30[1:0]	I^2C control DFC mode

DFC Function Programming

- Register B63b3:2 selects DFC00–DFC11 configuration.
- Byte16–19 are the registers for PLL2 VCO setting, based on B63b3:2 configuration selection, the data write to B16–19 will be stored in selected configuration OTP memory.
- Refer to DFC Function Priority table. Select proper control pin(s) to activate DFC function.
- Note the DFC function can also be controlled by I^2C access.

PPS – Proactive Power Saving Function

PPS (Proactive Power Saving) is an IDT patented unique design for the clock generator that proactively detects end device power down state and then switches output clocks between normal operation clock frequency and low power mode 32kHz clock that only consumes < 2µA current. The system could save power when the device goes into power down or sleep mode. The PPS function diagram is shown as below.

Figure 3. PPS Function Block Diagram

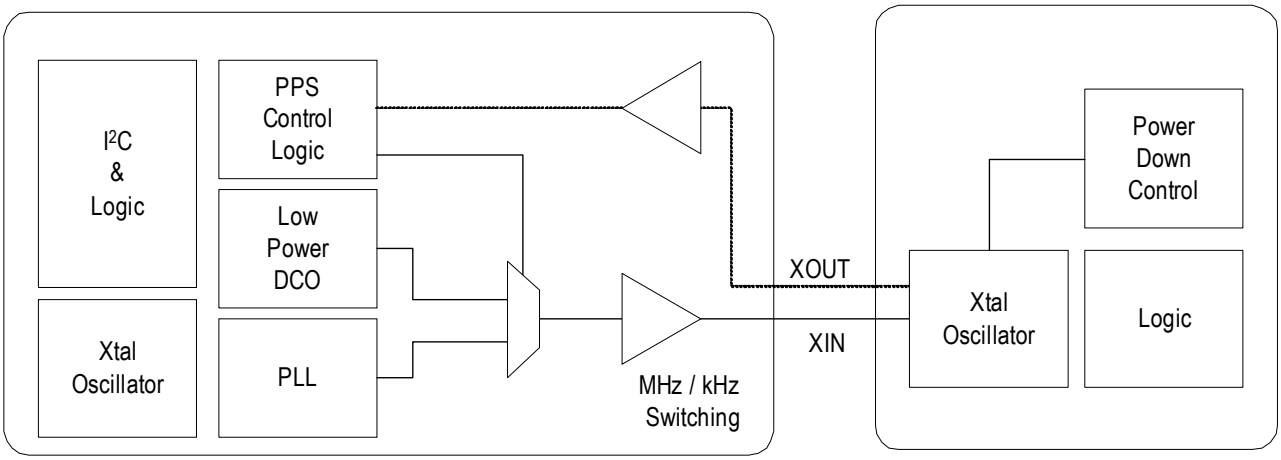
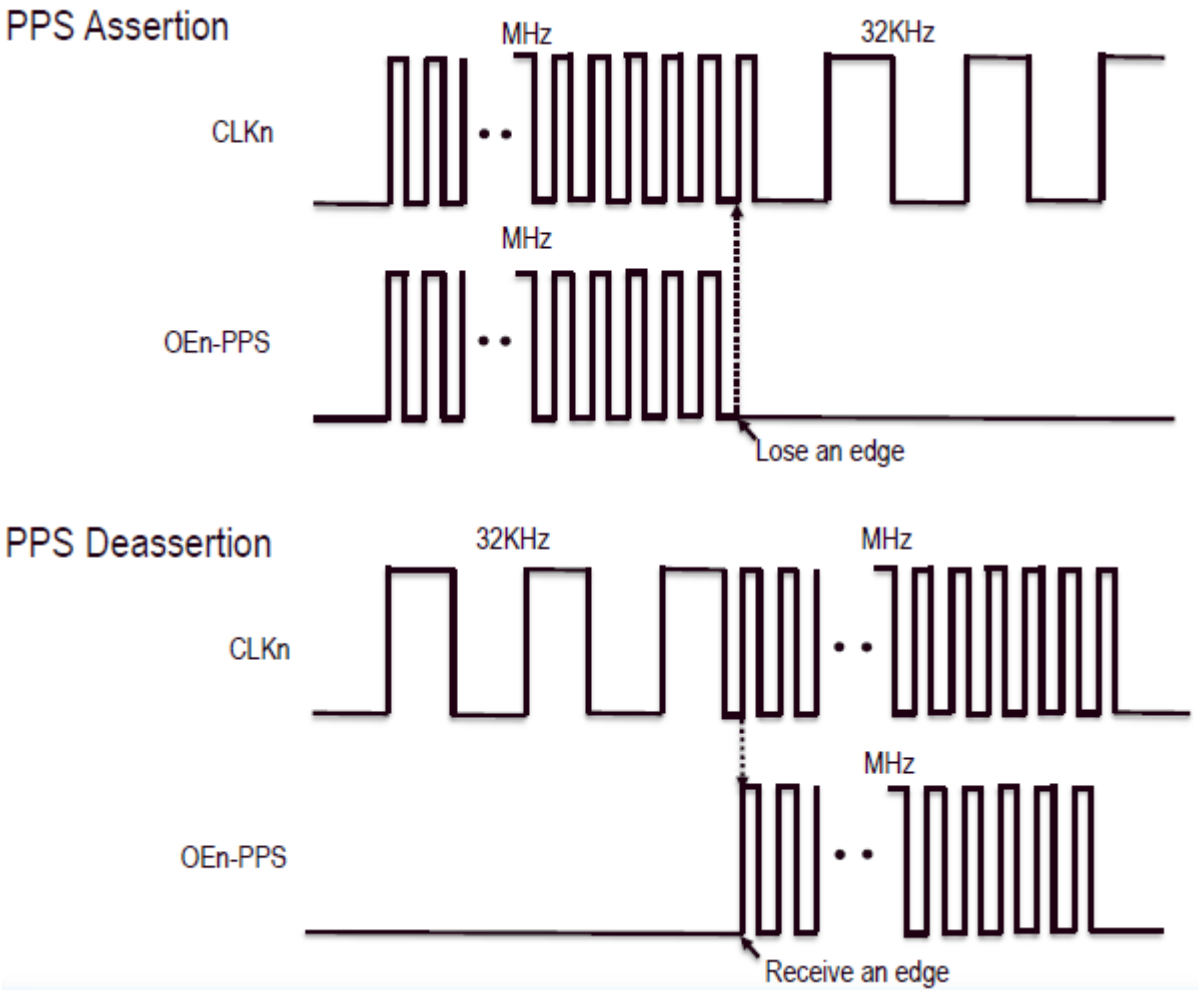


Figure 4. PPS Assertion/Deassertion Timing Chart



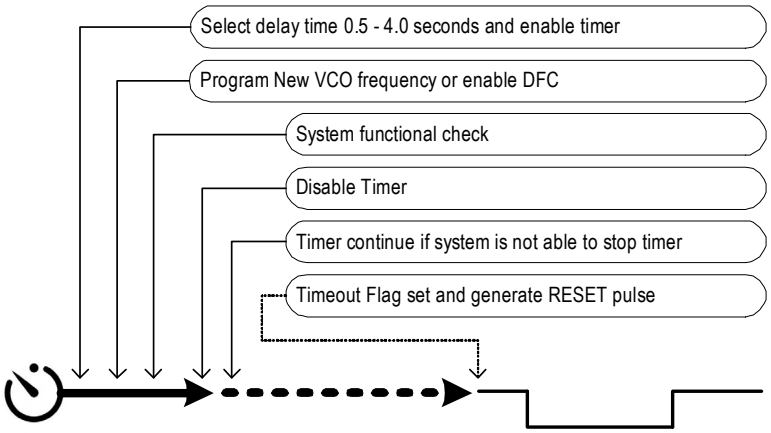
PPS Function Programming

- Refer to the OE Pin Functions table to have the proper PPS function selected for OE pin(s). Note that the register default is set to Output enable (OE) function for OE pins.
- Have proper setup to Byte 30 and 32 for OE1–OE3 function selection; for PPS function, select 10 to control register bits.

Timer Function Description

1. The timer function can be used together with the DFC -Dynamic Frequency Control function or with another PLL frequency programming.
2. The timer provides 4 different delay times by two bits selection: 0.5 sec – 1 sec – 2 sec – 4 sec.
3. The timeout flag will be set when timer times out and the flag can be cleared by writing 0 to timer enable bit.
4. When timer times out, RESET pin can generate a 250ms pulse signal if RESET control bit is enabled.
5. When timer times out, DFC stage will switch back to DFC00 setting if DFC function is enabled, and DFC function will be disabled after RESET.

Figure 5. Timer Functions



OE Pin Function

The OE pins in the 5P35023 have multiple functions. The OE pins can be configured as output enable control (OE) or chip power-down control (PD#) or Proactive Power Saving function (PPS). Furthermore, the OE pins can be configured as a single or two-pin Dynamic Frequency Control (DFC), or the RESET out function that is associated with the Timer function.

Table 10. OE Pin Functions

Function	Pin		
	OE1	OE2	OE3
SE Output Enable/Disable	SE1 (default)	SE2 (default)	SE3 (default)
DIFF Output Enable/Disable	—	DIFF1/DIFF2	—
Global Power Down (PD#)	PD#	—	—
Proactive Power Saving Input	SE1_PPS	SE2_PPS	SE3_PPS
DOC Control (Only PLL2)	DFC0	—	DFC1
RESET OUT	—	RESET OUT	—

Table 11. OE Pin Function Summary

OE Pin	Description
OE1: SE1	OE1 only control SE1 enable/disable; other outputs are not affected by this pin status.
OE2: SE2	OE2 only control SE2 enable/disable; other outputs are not affected by this pin status.
OE3: SE3	OE3 only control SE3 enable/disable; other outputs are not affected by this pin status.
OE2: DIFF1/DIFF2	OE2 control differential outputs 1 and 2 only. Other SE outputs are not affected by this pin status.
OE1: PD#	OE1 control chip global power down (PD#) except 32.768kHz on OE1 (when 32kHz is enabled). When the PD# pin is active low, the chip goes to lowest power down mode and all outputs are disabled except 32kHz output and only keep 32k/Xtal calibration.
OE1: SE1_PPS	Configure OE1 as SE1_PPS (Proactive Power Saving) function pin.
OE2: SE2_PPS	Configure OE2 as SE2_PPS (Proactive Power Saving) function pin.
OE3: SE3_PPS	Configure OE3 as SE3_PPS (Proactive Power Saving) function pin.
OE1: DFC0	Configure OE1 as DFC0 control pin 0.
OE3: DFC1	Configure OE3 as DFC1 control pin 1.

Table 12. PD# Priority

PD#	I2C_OE_EN_bit	SE1/2/3, DIFF1/DIFF2, SEx_PPS	Output	Notes
0	x	x	Stop	32kHz free run
1	0	x	Stop	
1	1	0	Stop	
1	1	1	Running	

Reference Input and Selection

When programming, the 5P35023 accepts 8MHz–40MHz crystal input, 8MHz to 125MHz differential clocks input or 1MHz–125MHz LVCMOS (to X1) input. See below reference circuit for details.

Crystal Input (X1/X2)

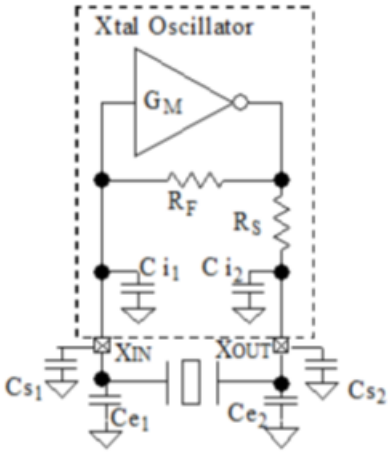
The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 40MHz maximum.

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate as 0 PPM. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal. In order to get an accurate oscillation frequency, the matching the oscillator load capacitance with the crystal load capacitance is required.

To set the oscillator load capacitance, 5P35023 has built-in two programmable tuning capacitors inside the chip, one at XIN and one at XOUT. They can be adjusted independently. The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[7:0] register. Adjustment of the crystal tuning capacitors allows for maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

Table 13. Programmable Tuning Caps

Parameter	Bits	Range	Minimum (pF)	Maximum (pF)
Xtal [7:0]	4 × 2	+1 / +2 / +4 / +8pF	0	15pF



XTAL[4:0] = (XTAL C_L - 7pF) × 2 (Eq.1)

Equation 1 and the table of XTAL[7:0] tuning capacitor characteristics show that the parallel tuning capacitance can be set between 4.5pF to 12.5pF with a resolution of 0.25pF.

For a crystal C_L = 8pF, where C_L is the parallel capacity specified by the crystal vendor that sets the crystal frequency to the nominal value. Under the assumptions that the stray capacity between the crystal leads on the circuit board is zero and that no external tuning caps are placed on the crystal leads, then the internal parallel tuning capacity is equal to the load capacity presented to the crystal by the device.

The internal load capacitors are true parallel-plate capacitors for ultra-linear performance. Parallel-plate capacitors were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. External non-linear crystal load capacitors should not be used for applications that are sensitive to absolute frequency requirements.

Spread Spectrum

The 5P35023 supports spread spectrum clocks from PLL1 and PLL2; the PLL1 built-in with analog spread spectrum and PLL2 has digital spread spectrum.

Analog Spread Spectrum

Refer to the programming guide.

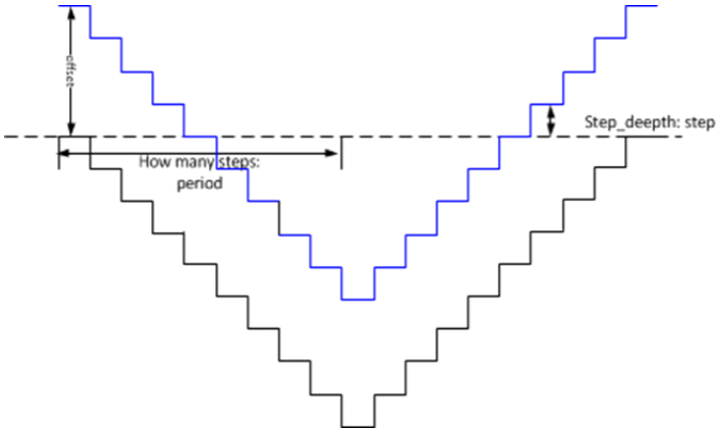
Digital Spread Spectrum

Figure 6. Digital Spread Spectrum

$$N = \frac{Fvco}{2 * Fout}$$

$$period = \frac{Fpfd}{2 * Fss}$$

$$step = \frac{N * SSamount}{period}$$



Down spread or spread off

N = Fvco/Fpfd
Center Spread
N = Nssoff + N × SSamount/2
N: include integer and fraction
Fvco: VCOs frequency
Fpfd: PLLs pfd frequency
Fss: spread modulation rate
SSamount: spread percentage

The black line is for the down spread; N will decrease to make the center frequency is lower than spread off.

The blue line is for the center spread; there is an offset put on divider ratio to make the center frequency keep same as spread off.

Example: 0.5% down spread at 32kHz modulation rate.

V_{BAT}

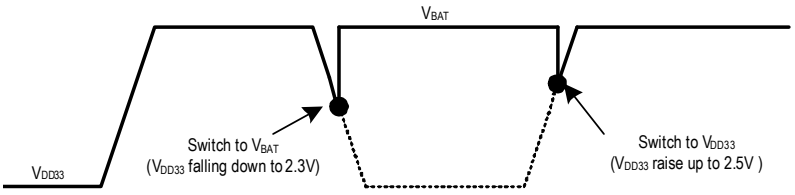
The 5P35023 supports a low-power operation 32.768kHz RTC clock with only a coin cell battery supply. The coin cell battery power capacitance is usually 170mAhr or higher, with less than 2µA* low-power DCO operation mode will support application up to few years clock source for date/time keeping circuit (RTC).

When main power exists (for example, V_{DD33} and V_{DDA}), the 5P35023 will switch DCO power source to main power to save battery power.

Table 14. V_{BAT} Switching Threshold

V_{DD33}	V_{BAT}	DCO Power Source
> 2.5V	—	V_{DD33}
< 2.3V	—	V_{BAT}

VBAT needs to be 3.0V–3.3V.



ORT–VCO Overshoot Reduction Technology

The 5P35023 supports the VCO overshoot reduction technology (ORT) to prevent an output clock frequency spike when the device is changing frequency on the fly or doing DFC (Dynamic Frequency Control) function. The VCO frequency changes are under control instead of free-run to targeted frequency.

PLL Features and Descriptions

Table 15. Output 1 Divider

Output Divider bits <1:0>	Output Divider bits <3:2>			
	00	**01**	**10**	**11**
00	1	2	4	8
01	4	8	16	32
10	5	10	20	40
11	6	12	24	48

Table 16. Output 2, 4, and 5 Divider

Output Divider bits <1:0>	Output Divider bits <3:2>			
	00	**01**	**10**	**11**
00	1	2	4	5
01	3	6	12	15
10	5	10	20	25
11	10	20	40	50

Table 17. Output 3 Divider

Output Divider bits <1:0>	Output Divider bits <3:2>			
	00	**01**	**10**	**11**
00	1	2	4	8
01	3	6	12	24
10	5	10	20	40
11	10	20	40	80

Output Clock Test Conditions

Figure 7. LVCMOS Output Test Conditions

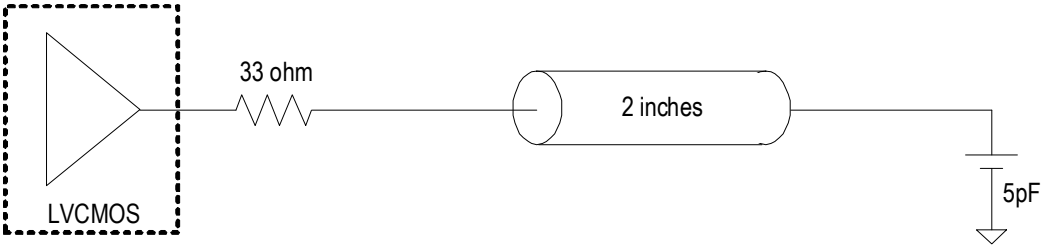
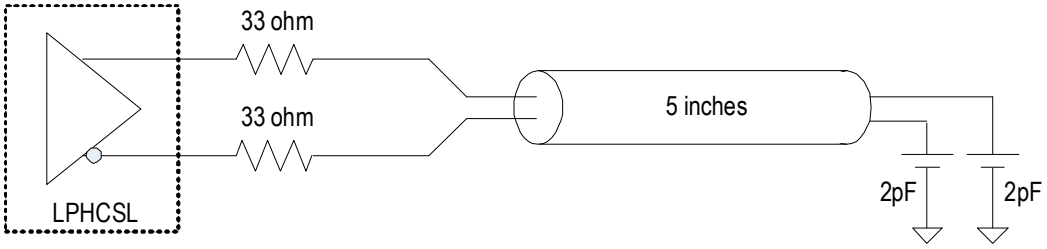


Figure 8. LP-HCSL Output Test Conditions



Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 5P35023 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 18. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DDA}, V_{DD33}, V_{DDSE},V_{DDDIFF}	3.6V
Supply Voltage, V_{BAT}	3.6V
Inputs	
XIN/CLKIN	0V to 3.3V voltage swing for both LVCMOS or DIFF CLK
Other Inputs	-0.5V to V_{DD33} or V_{DDSEx}
Outputs, V_{DDSEx} (LVCMOS)	-0.5V to V_{DDSEx} or V_{DDDIFF}
Outputs, IO (SDA)	10mA
Package Thermal Impedance, Θ_{JA}	50.1°C/W (0mps)
Package Thermal Impedance, Θ_{JC}	61.68°C/W (0mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
ESD Charge Device Model	1000V
Junction Temperature	125°C

Recommended Operating Conditions

Table 19. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{DDSEx}	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V	
	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625		
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465		
V_{DD33}	Power supply voltage for core logic functions.	3.135	3.3	3.465	V	1,2,3
V_{DDA}	Analog power supply voltage. Use filtered analog power supply if available.	2.375		3.465	V	
V_{BAT}	Battery power supply voltage.	2.8	3	3.465	V	1,2,3
T_A	Operating temperature, ambient (industrial).	-40		85	°C	
	Operating temperature, ambient (automotive).	-40		105	°C	
C_{LOAD_OUT}	Maximum load capacitance (LVCMOS only).		5		pF	

Table 19. Recommended Operating Conditions (Cont.)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
F_{IN}	External reference crystal.	8		40	MHz	
	External reference crystal with DCO used.	12		38		
	External single-ended reference clock CLKINB.	1		125		
	External differential reference clock CLKIN, CLKINB.	8		125		
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic).	0.05		3	ms	

[1] Power-up sequence conditions.

[2] V_{DDSEx} for non-32kHz outputs should be OFF when V_{DDA}/V_{DD33} turn off, V_{BAT} mode only supports 32.768kHz outputs from SE1–3.

[3] When using a single-ended clock to CLKINB pin within differential clocking mode, CLKIN pin needs to be grounded and minimum input frequency should be higher than 8MHz.

Electrical Characteristics

Supply voltage: all V_{DD} ±5%, unless otherwise stated.

Table 20. Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance
(T_A = +25°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance (CLKIN, CLKINB, OE, SDA, SCL, DFC1:0)		3	7	pF
Pull-down Resistor	OE		200		kΩ
R_{OUT}	LVCMOS Output Driver Impedance (V_{DDSE} = 1.8V)		22		Ω
	LVCMOS Output Driver Impedance (V_{DDSE} = 2.5V)		22		Ω
	LVCMOS Output Driver Impedance (V_{DDSE} = 3.3V)		22		Ω
X1, X2	Programmable Input Capacitance at X1 or X2	0		15	pF

Table 21. Crystal Characteristics

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Mode of Oscillation	—	Fundamental			
Frequency	—	8		40	MHz
Frequency when 32.768kHz DCO is used	—	12		38	MHz
Equivalent Series Resistance (ESR)	—		10	100	Ω
Shunt Capacitance	—		2	7	pF
Load Capacitance (C_L)	—	6	8	10	pF
Maximum Crystal Drive Level (C_L = 8pF)	—			100	µW

Table 22. DC Electrical Characteristics (Industrial)[1,2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDCORE}	Core Supply Current	V_{DD} = V_{DDSE} = V_{DD33}= 3.3; XTAL = 25MHz, PLL2/3 off, no output, PLLs disabled.		5		mA
I_{DD_PLL1} [3]	PLL1 Supply Current	V_{DD} = V_{DDSE} = V_{DD33} = 3.3V; XTAL = 25MHz, PLL2/3 off, no output, PLL1 = 600MHz.		13		mA
		V_{DD} = V_{DDSE} = V_{DD33} = 2.5V; XTAL = 25MHz, PLL2/3 off, no output, PLL1 = 600MHz.		13		mA
I_{DD_PLL2} [3]	PLL2 Supply Current	V_{DD} = V_{DDSE} = V_{DD33} = 3.3V; XTAL = 25MHz, PLL1/3 off, no output, PLL2 = 1GHz.		11		mA
		V_{DD} = V_{DDSE} = V_{DD33} = 2.5V; XTAL = 25MHz, PLL1/3 off, no output, PLL2 = 1GHz.		11		mA
I_{DD_PLL3} [3]	PLL3 Supply Current	V_{DD} = V_{DDSE} = V_{DD33} = 3.3V; XTAL = 25MHz, PLL1/2 off, no output, PLL3 = 480MHz.		4		mA
I_{DDOx}	Output Buffer Supply Current	LVPECL, 500MHz, 3.3V V_{DDDIFF} (DIFF1,2).		39		mA
		LVPECL, 156.25MHz, 2.5V V_{DDDIFF} (DIFF1,2).		33		mA
		LVDS, 500MHz, 3.3V V_{DDDIFF} (DIFF1,2).		13		mA
		LVDS, 250MHz, 2.5V V_{DDDIFF} (DIFF1,2).		8		mA
		LPHCSL, 125MHz, 3.3V V_{DDDIFF}, 2pF load (DIFF1,2).		7		mA
		LPHCSL, 100MHz, 2.5V V_{DDDIFF}, 2pF load (DIFF1,2).		8		mA
		LVCMOS, 8MHz, 3.3V, V_{DDSE} [1,2] (SE1).		1		mA
		LVCMOS, 8MHz, 2.5V V_{DDSEx} [1,2] (SE1).		1		mA
		LVCMOS, 8MHz, 1.8V V_{DDSEx} [1,2] (SE1).		1		mA
		LVCMOS, 160MHz, 3.3V V_{DDSEx} [1] (SE1).		9.5		mA
		LVCMOS, 160MHz, 2.5V V_{DDSEx} [1,2] (SE1).		5.0		mA
		LVCMOS, 160MHz, 1.8V V_{DDSEx} [1,2] (SE1).		6.0		mA
I_{DDPD}	Power Down Current	PD asserted with V_{DDA}, V_{DD33} and V_{DDSE} on, I^2C programming, 32kHz running.		3.5		mA
$I_{DDSUSPEND}$ – V_{DD33}	$I_{DDSUSPEND}$ – V_{BAT}	Only V_{BAT} = 3.3V and V_{DDSEn} is powered.		1.1		µA
$I_{DDSUSPEND}$ – SEn 3.3V	$I_{DDSUSPEND}$ – V_{DDSEn} 3.3V	Only V_{BAT} = 3.3V and V_{DDSEn} is powered with 3.3V.		3.4		µA
$I_{DDSUSPEND}$ – SEn 2.5V	$I_{DDSUSPEND}$ – V_{DDSEn} 2.5V	Only V_{BAT} = 3.3V and V_{DDSEn} is powered with 2.5V.		2.5		µA
$I_{DDSUSPEND}$ – SEn 1.8V	$I_{DDSUSPEND}$ – V_{DDSEn} 1.8V	Only V_{BAT} = 3.3V and V_{DDSEn} is powered with 1.8V.		1.8		µA

[1] Single CMOS driver active.

[2] SE1–3 current measured with 2 inches transmission line and 5pF load, DIFF clock current measured with 5 inches transmission line with 2pF loads.

[3] I_{DDCORE} = I_{DDA}+ I_{DDD}, no loads.

Table 23. DC Electrical Characteristics (Automotive)[1,2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDCORE}	Core Supply Current	V_{DD} = V_{DDSE} = V_{DD33}= 3.3; XTAL = 25MHz, PLL2/3 off, no output, PLLs disabled.		5		mA
I_{DD_PLL1} [3]	PLL1 Supply Current	V_{DD} = V_{DDSE} = V_{DD33} = 3.3V; XTAL = 25MHz, PLL2/3 off, no output, PLL1 = 600MHz.		13		mA
		V_{DD} = V_{DDSE} = V_{DD33} = 2.5V; XTAL = 25MHz, PLL2/3 off, no output, PLL1 = 600MHz.		13		mA
I_{DD_PLL2} [3]	PLL2 Supply Current	V_{DD} = V_{DDSE} = V_{DD33} = 3.3V; XTAL = 25MHz, PLL1/3 off, no output, PLL2 = 1GHz.		11		mA
		V_{DD} = V_{DDSE} = V_{DD33} = 2.5V; XTAL = 25MHz, PLL1/3 off, no output, PLL2 = 1GHz.		11		mA
I_{DD_PLL3} [3]	PLL3 Supply Current	V_{DD} = V_{DDSE} = V_{DD33} = 3.3V; XTAL = 25MHz, PLL1/2 off, no output, PLL3 = 480MHz.		4.7		mA
I_{DDOx}	Output Buffer Supply Current	LVPECL, 500MHz, 3.3V V_{DDDIFF} (DIFF1,2).		39		mA
		LVPECL, 156.25MHz, 2.5V V_{DDDIFF} (DIFF1,2).		33		mA
		LVDS, 500MHz, 3.3V V_{DDDIFF} (DIFF1,2).		15		mA
		LVDS, 250MHz, 2.5V V_{DDDIFF} (DIFF1,2).		9		mA
		LPHCSL, 125MHz, 3.3V V_{DDDIFF}, 2pF load (DIFF1,2).		9		mA
		LPHCSL, 100MHz, 2.5V V_{DDDIFF}, 2pF load (DIFF1,2).		7		mA
		LVCMOS, 8MHz, 3.3V, V_{DDSE} [1,2] (SE1).		1		mA
		LVCMOS, 8MHz, 2.5V V_{DDSEx} [1,2] (SE1).		1		mA
		LVCMOS, 8MHz, 1.8V V_{DDSEx} [1,2] (SE1).		1		mA
		LVCMOS, 160MHz, 3.3V V_{DDSEx} [1] (SE1).		9.5		mA
		LVCMOS, 160MHz, 2.5V V_{DDSEx} [1,2] (SE1).		9		mA
		LVCMOS, 160MHz, 1.8V V_{DDSEx} [1,2] (SE1).		6		mA
I_{DDPD}	Power Down Current	PD asserted with V_{DDA}, V_{DD33} and V_{DDSE} on, I^2C programming, 32kHz running.		3.5		mA
$I_{DDSUSPEND}$ – V_{DD33}	$I_{DDSUSPEND}$ – V_{BAT}	Only V_{BAT} = 3.3V and V_{DDSEn} is powered.		1.1		µA
$I_{DDSUSPEND}$ – SEn 3.3V	$I_{DDSUSPEND}$ – V_{DDSEn} 3.3V	Only V_{BAT} = 3.3V and V_{DDSEn} is powered with 3.3V.		3.4		µA
$I_{DDSUSPEND}$ – SEn 2.5V	$I_{DDSUSPEND}$ – V_{DDSEn} 2.5V	Only V_{BAT} = 3.3V and V_{DDSEn} is powered with 2.5V.		2.5		µA
$I_{DDSUSPEND}$ – SEn 1.8V	$I_{DDSUSPEND}$ – V_{DDSEn} 1.8V	Only V_{BAT} = 3.3V and V_{DDSEn} is powered with 1.8V.		1.8		µA

[1] Single CMOS driver active.

[2] SE1–3 current measured with 2 inches transmission line and 5pF load, DIFF clock current measured with 5 inches transmission line with 2pF loads.

[3] I_{DDCORE} = I_{DDA}+ I_{DDD}, no loads.

Table 24. Input Parameters[1,2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage – CLKIN	Single-ended inputs.	2.4		3.465	V
V_{IL}	Input Low Voltage – CLKIN	Single-ended inputs.	GND - 0.3		0.8	V
V_{SWING}	Input Amplitude – CLKIN	Differential input.	325		3300	mV
dV/dt	Input Slew Rate – CLKIN	Differential input.	0.4		8	V/ns
VCM	Input Common Mode Voltage	Differential input.	200		2500	mV
I_{IL}	Input Leakage Low Current for OE1	V_{IN} = GND	-150		5	µA
	Input Leakage Low Current for OE2/3	V_{IN} = GND.			5	µA
I_{IH}	Input Leakage High Current for OE1/2/3	V_{IN} = 3.465V (industrial).			20	µA
I_{IH}	Input Leakage High Current for OE1/2/3	V_{IN} = 3.465V (automotive).			35	µA
d_{TIN}	Input Duty Cycle	Measurement from differential waveform.	45		55	%

[1] Confirmed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 25. Power Consumption of 32.768kHz Output Only Operation

Supply voltage V_{DDSE} = 1.8V–3.3V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_V_{BAT}	V_{BAT} = 3.3V Power Input Current			1.1		µA
I_V_{DDSEx}	V_{DDSEx} = 1.8V Current	0.5 inch, no load, one output.		0.4		µA
	V_{DDSEx} = 1.8V Current	2.0 inch, no load, one output.		1.0		µA
	V_{DDSEx} = 1.8V Current	5.0 inch, no load, one output.		2.3		µA
	V_{DDSEx} = 2.5V Current	0.5 inch, no load, one output.		0.6		µA
	V_{DDSEx} = 2.5V Current	2.0 inch, no load, one output.		1.5		µA
	V_{DDSEx} = 2.5V Current	5.0 inch, no load, one output.		3.1		µA
	V_{DDSEx} = 3.3V Current	0.5 inch, no load, one output.		0.8		µA
	V_{DDSEx} = 3.3V Current	2.0 inch, no load, one output.		1.9		µA
	V_{DDSEx} = 3.3V Current	5.0 inch, no load, one output.		4.2		µA

Table 26. DC Electrical Characteristics – 3.3V LVCMOS

V_{DDSE} = 3.3V ±5%, T_A = -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	I_{OH} = -15mA.	2.4		V_{DDSE}	V
V_{OL}	Output Low Voltage	I_{OL} = 15mA.			0.4 (industrial) 0.5 (automotive)	V
I_{OZDD}	Output Leakage Current	Tri-state outputs, V_{DDSE} = 3.465V.			3	µA
		Tri-state outputs, V_{DDSE} = 0V.	-3			µA
V_{IH}	Input High Voltage	Single-ended inputs – OE, SDA, SCL.	2		V_{DDSE}	V
V_{IL}	Input Low Voltage	Single-ended inputs – OE, SDA, SCL.	GND - 0.3		0.8	V
V_{IH}	Input High Voltage	Single-ended input – XIN/CLKIN	2.4		V_{DD33}	V
V_{IL}	Input Low Voltage	Single-ended input – XIN/CLKIN	GND - 0.3		0.8	V

Table 27. DC Electrical Characteristics – 2.5V LVCMOS

V_{DDSE} = 2.5V ±5%, T_A = -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	I_{OH} = -12mA.	0.7 × V_{DDSE}		V_{DDSE}	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA.			0.4 (industrial) 0.45 (automotive)	V
I_{OZDD}	Output Leakage Current	Tri-state outputs, V_{DDSE} = 2.625V.			3	µA
		Tri-state outputs, V_{DDSE} = 0V.	-3			µA
V_{IH}	Input High Voltage	Single-ended inputs – OE, SDA, SCL.	1.7		V_{DDSE}	V
V_{IL}	Input Low Voltage	Single-ended inputs – OE, SDA, SCL.	GND - 0.3		0.2 × V_{DDSE}	V

Table 28. DC Electrical Characteristics – 1.8V LVCMOS

V_{DDSE} = 1.8V ±5%, T_A = -40°C to +105°C, unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	I_{OH} = -8mA.	0.7 × V_{DDSE}		V_{DDSE}	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA.			0.25 × V_{DDSE}	V
I_{OZDD}	Output Leakage Current	Tri-state outputs, V_{DDSE} = 1.89V.			3	µA
		Tri-state outputs, V_{DDSE} = 0V.	-3			µA
V_{IH}	Input High Voltage	Single-ended inputs.	0.65 × V_{DDSE}		V_{DDSE}	V
V_{IL}	Input Low Voltage	Single-ended inputs.	GND - 0.3		0.35 × V_{DDSE} (industrial) 0.2 × V_{DDSE} (automotive)	V

Table 29. Electrical Characteristics – DIF 0.7V LPHCSL Differential Outputs

V_{DDDIFF} = 3.3 V ±5% or 2.5V ±5%, T_A = -40° to +105°C.

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
dV/dt	Slew Rate	1	2.5	4	V/ns	1,2,3,8
ΔdV/dt	Slew Rate Mismatch			20	%	1,2,3,8 at < = 200MHz
V_{HIGH}	Voltage High	660	800	1150	mV	1,6,7,8
V_{LOW}	Voltage Low	-150	0	150	mV	1,6
V_{MAX}	Maximum Voltage			1150	mV	1
V_{MIN}	Minimum Voltage	-300			mV	1
V_{SWING}	Voltage Swing	300			mV	1,2
V_{CROSS}	Crossing Voltage Value	250	360	550	mV	1,4,6
ΔV_{CROSS}	Crossing Voltage Variation			140	mV	1,5
Jitter-Cy/Cy	Cycle to Cycle Jitter		10		ps	1,2
Jitter-STJ	Short Term Period Jitter		70		ps	1,2
T_{DC}	Duty Cycle	45		55	%	1,2
Measured Frequency	LPHCSL at Differential Output			500	MHz	1,2

[1] Confirmed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the V_{SWING} voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

[4] V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[5] The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of V_{CROSS} min/max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting ΔV_{CROSS} to be smaller than V_{CROSS} absolute.

[6] Measured from single-ended waveform.

[7] Measured with scope averaging off, using statistics function. Variation is the difference between minimum and maximum.

[8] Scope average on.

[9] Differential clock amplitude setting = 01.

Table 30. Electrical Characteristics – LVDS

V_{DDDIFF} = 3.3 V ±5% or 2.5V ±5%, T_A = -40° to +105°C.

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
VOT (+)	Differential Output Voltage for the TRUE Binary State	247		454	mV	
VOT (-)	Differential Output Voltage for the FALSE Binary State	-454		-247	mV	
ΔVOT	Change in VOT between Complimentary Output States			50	mV	
VOS	Output Common Mode Voltage (Offset Voltage) at 3.3V ±5%, 2.5V ±5%	1.125	1.25	1.375	V	
	Output Common Mode Voltage (Offset Voltage) at 1.8 V ±5%	0.8	0.875	0.95		
ΔVOS	Change in VOS between Complimentary Output States			50	mV	
IOS	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT}- = 0V or V_{DDDIFF}		9	24	mA	
IOSD	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT}-		6	12	mA	
Jitter-Cy/Cy	Cycle to Cycle Jitter		20		ps	1,2
Jitter-STJ	Short Term Period Jitter		100		ps	1,2
T_{DC}	Duty Cycle	45		55	%	1,2
Measured Frequency	LVDS at Differential Output			500	MHz	1,2

[1] Confirmed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Differential clock amplitude setting = 01.

Table 31. Electrical Characteristics – LVPECL

V_{DDDIFF} = 3.3 V ±5% or 2.5V ±5%, T_A = -40° to +105°C.

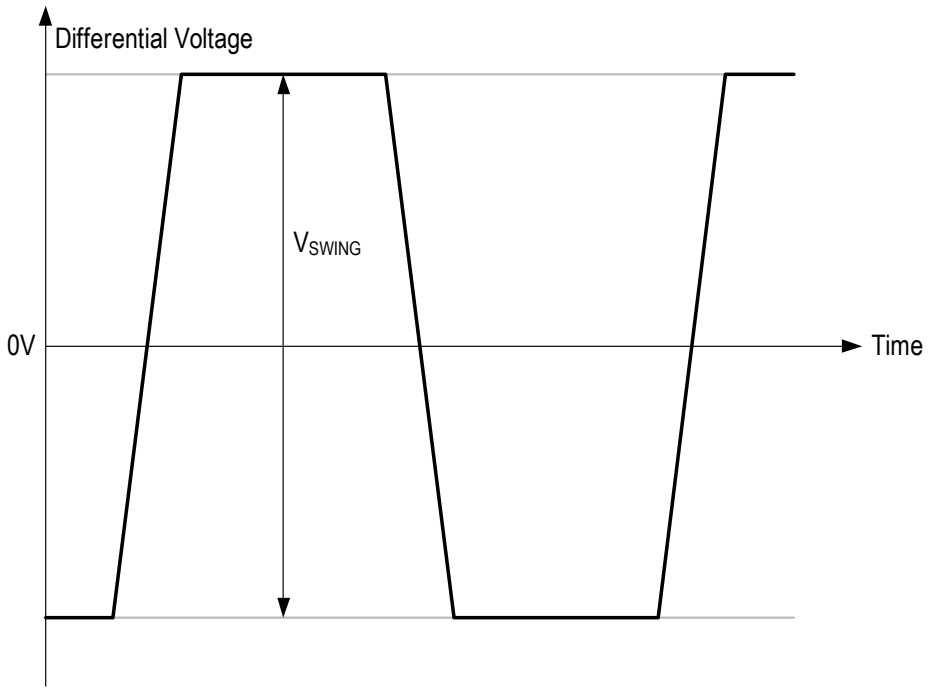
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{OH}	Output Voltage HIGH, terminated through 50Ω tied to V_{DDDIFF} - 2V	V_{DDDIFF} - 1.19		V_{DDDIFF} - 0.69	V	
V_{OL}	Output Voltage LOW, terminated through 50Ω tied to V_{DDDIFF} - 2V	V_{DDDIFF} - 1.94		V_{DDDIFF} - 1.4	V	
V_{SWING}	Output Differential Voltage Swing (see Figure 9)	1.1		2	V	2,3
Jitter-Cy/Cy	Cycle to Cycle Jitter		20		ps	1,2
Jitter-STJ	Short Term Period Jitter		100		ps	1,2
T_{DC}	Duty Cycle	45		55	%	1,2
Measured Frequency	LVPECL at Differential Output			500	MHz	1,2

[1] Confirmed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Differential clock amplitude setting = 01.

Figure 9. Output Differential Voltage Swing



AC Electrical Characteristics

V_{DDSE} = 3.3V ±5% or 2.5V ±5% or 1.8V ±5%, T_A = -40°C to +105°C (spread spectrum off), unless stated otherwise.

Table 32. AC Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{IN} [1]	Input Frequency	Input frequency limit (XIN).	8		40	MHz
		Input frequency limit (XIN) when enable DCO.	12		38	MHz
		Input frequency limit (differential CLKIN).	8		125	MHz
		Input frequency limit (LVCMOS to X1).	1		125	MHz
f_{OUT}	Output Frequency	Single-ended clock output limit (LVCMOS).	1	< 125	160	MHz
		Differential clock output limit (LPHCSL).	1	< 333	500	MHz
		Differential clock output limit (LVDS).	1	< 333	500	MHz
		Differential clock output limit (LVPECL).	1		500	MHz
f_{VCO1}	VCO Frequency Range of PLL1	VCO operating frequency range.	300		600	MHz
f_{VCO2}	VCO Frequency Range of PLL2	VCO operating frequency range.	400		1200	MHz
f_{VCO3}	VCO Frequency Range of PLL3	VCO operating frequency range.	300		800	MHz
t2	Input Duty Cycle	Duty cycle.	45		55	%
t3	Output Duty Cycle	LVCMOS, Single-ended.	45		55	%
		DIFF1 / DIFF2 configured as a pair of LVCMOS outputs, 180° out of phase (crossing point measurements).	40		60	%
	Output Duty Cycle – REF	Reference clock output or SE1–3 fan out clock.	40		60	%
t4 [4]	Rise/Fall, SLEW[0] = 1	Single-ended LVCMOS output clock rise and fall time, 20% to 80% of V_{DDSE}1.8V–3.3V.		1.0		ns
	Rise/Fall, SLEW[0] = 0	Single-ended LVCMOS output clock rise and fall time, 20% to 80% of V_{DDSE}1.8V–3.3V.		1.1		
t5 [5]	Rise Time	LVDS, 20% to 80%.		300		ps
	Fall Time	LVDS, 80% to 20%.		300		
	Rise Time	LVPECL, 20% to 80%.		300		
	Fall Time	LVPECL, 80% to 20%.		300		

Table 32. AC Electrical Characteristics (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t6	Clock Jitter	Cycle-to-cycle jitter (peak-to-peak), multiple output frequencies switching, differential outputs (1.8V to 3.3V nominal output voltage). SE1 = 25MHz SE2 = 100MHz SE3 = 100MHz DIFF1/2 = 100MHz		50		ps
		RMS phase jitter (12kHz to 20MHz integration range) differential output, V_{DDSE} = 3.465V, 25MHz crystal. SE1 = 25MHz SE2 = 100MHz SE3 = 100MHz DIFF1/2 = 100MHz		1.1 (industrial) 1.5 (automotive)		ps
		RMS phase jitter (12kHz to 20 MHz integration rage) REF output.		0.3		ps
t7	Output Skew	Skew between the same frequencies, with outputs using the same driver format.		75		ps
t8 [2]	Lock Time	PLL lock time from power-up.			20	ms
t9	Lock Time	32.768kHz clock low power power-up time.		10	100	ms
t9 [3]	Lock Time	PLL lock time from shutdown mode.		0.1	2	ms

[1] Practical lower frequency is determined by loop filter settings.

[2] Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.

[3] Actual PLL lock time depends on the loop configuration.

[4] t4 Rise/Fall time measurements are based on 5pF load.

[5] t5 Rise/Fall time measurements are based on 2pF load.

PCI Express Jitter Specifications

V_{DDDIFF} = 3.3V ±5% or 2.5V ±5%, T_A = -40°C to +105°C.

Table 33. PCI Express Jitter Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Industry Specification	Unit	Notes
t_J (PCIe Gen1)	Phase Jitter Peak-to-Peak	f = 100MHz/125MHz, 25MHz crystal input. Evaluation band: 0Hz – Nyquist (clock frequency/2).		30		86	ps	1,4
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen2)	Phase Jitter RMS	f = 100MHz/125MHz, 25MHz crystal input. High band: 1.5MHz – Nyquist (clock frequency/2).		2.56		3.10	ps	2,4
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen2)	Phase Jitter RMS	f = 100MHz/125MHz, 25MHz crystal input. Low band: 10kHz – 1.5MHz.		0.7		3.0	ps	2,4
t_{REFCLK_RMS} (PCIe Gen3)	Phase Jitter RMS	f = 100MHz/125MHz, 25MHz crystal input. Evaluation band: 0Hz – Nyquist (clock frequency/2).		0.8		1.0	ps	3,4

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[1] Peak-to-peak jitter after applying system transfer function for the common clock architecture. Maximum limit for PCI Express Gen1.

[2] RMS jitter after applying the two evaluation bands to the two transfer functions defined in the common clock architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Gen2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (high band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (low band).

[3] RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI_Express_Base_r3.0 10 Nov. 2010 specification, and is subject to change pending the final release version of the specification.

[4] This parameter is confirmed by characterization. Not tested in production.

Spread Spectrum Generation Specifications

Table 34. Spread Spectrum Generation Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	Output frequency range.	1		350	MHz
f_{MOD} [1]	Modulation Frequency	Modulation frequency.	30 to 63			kHz
f_{SPREAD}	Spread Value	Amount of spread value (programmable) – down spread.	-0.5% to -2%			$\%f_{OUT}$
%tolerance [2]	Spread% Value	Variation of spread range.		±15		%

[1] Input frequency dependent (see programming guide).

[2] Design target.

I²C Bus Characteristics

Table 35. I²C Bus DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Level		0.7 × V_{DD33}			V
V_{IL}	Input Low Level				0.3 × V_{DD33}	V
V_{HYS}	Hysteresis of Inputs		0.05 × V_{DD33}			V
I_{IN}	Input Leakage Current				±1	µA
V_{OL}	Output Low Voltage	I_{OL} = 3mA.			0.4	V

Table 36. I²C Bus AC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
F_{SCLK}	Serial Clock Frequency (SCL)			100	400	kHz
t_{BUF}	Bus Free Time between STOP and START		1.3			µs
$t_{SU:START}$	Setup Time, START		0.6			µs
$t_{HD:START}$	Hold Time, START		0.6			µs
$t_{SU:DATA}$	Setup Time, Data Input (SDA)		100			ns
$t_{HD:DATA}$	Hold Time, Data Input (SDA) [1]		0			µs
t_{OVD}	Output Data Valid from Clock				0.9	µs
C_B	Capacitive Load for Each Bus Line				400	pF
t_R	Rise Time, Data and Clock (SDA, SCL)		20 + 0.1 × C_B		300	ns
t_F	Fall Time, Data and Clock (SDA, SCL)		20 + 0.1 × C_B		300	ns
t_{HIGH}	High Time, Clock (SCL)		0.6			µs
t_{LOW}	Low Time, Clock (SCL)		1.3			µs
$t_{SU:STOP}$	Setup Time, STOP		0.6			µs

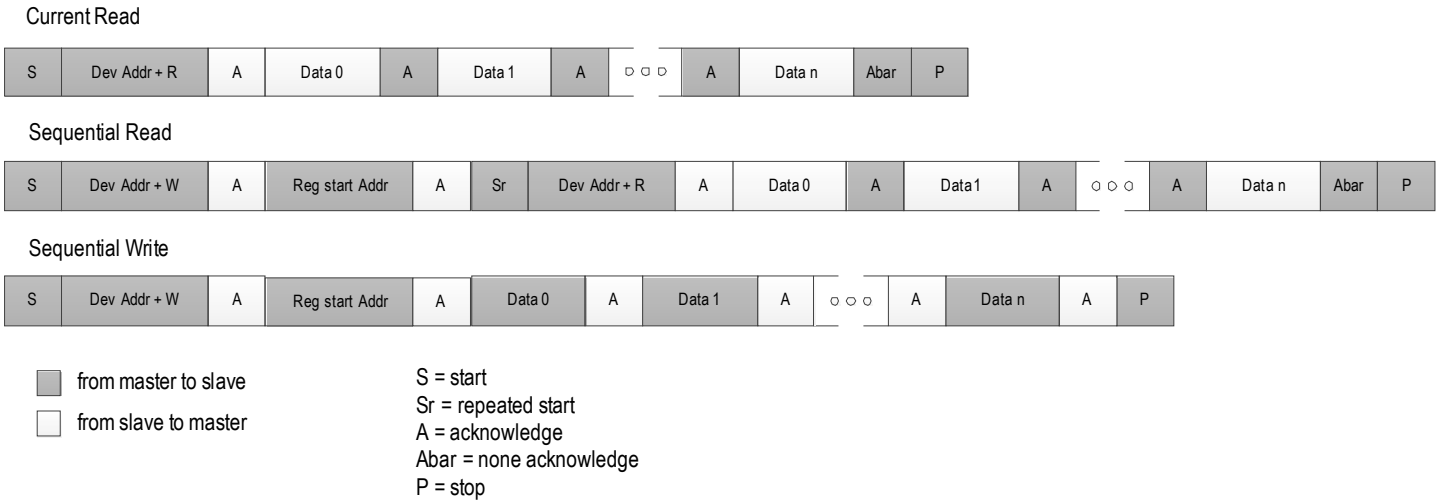
[1] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

I²C Mode Operations

The device acts as a slave device on the I²C bus using one of the four I²C addresses (0xD0, 0xD2, 0xD4, or 0xD6) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-down resistors have a size of 100kΩ typical.

Figure 10. I²C Slave Read and Write Cycle Sequencing



Byte 0: General Control

Byte 00h	Name	Control Function	Type	0	1	PWD
Bit 7	OTP_Burned	OTP memory programming indication	R/W	OTP memory non-programmed	OTP memory programmed	0
Bit 6	I²C_addr[1]	I²C address select bit 1	R/W	00: D0 / 01: D2 10: D4 / 11: D6		0
Bit 5	I²C_addr[0]	I²C address select bit 0	R/W			0
Bit 4	PLL1_SSEN	PLL1 Spread Spectrum enable	R/W	disable	enable	0
Bit 3	DIV1_src_sel	Divider 1 source clock select	R/W	PLL1	Xtal	0
Bit 2	PLL3_refin_sel	PLL3 source selection	R/W	Xtal	Seed (DIV2)	0
Bit 1	EN_CLKIN	Enable CLKIN	R/W	disable	enable	0
Bit 0	OTP_protect	OTP memory protection	R/W	read/write	write locked	0

Byte 1: Dash Code ID (optional)

Byte 01h	Name	Control Function	Type	0	1	PWD
Bit 7	DashCode ID[7]	Dash code ID	R/W	—	—	0
Bit 6	DashCode ID[6]	Dash code ID	R/W	—	—	0
Bit 5	DashCode ID[5]	Dash code ID	R/W	—	—	0
Bit 4	DashCode ID[4]	Dash code ID	R/W	—	—	0
Bit 3	DashCode ID[3]	Dash code ID	R/W	—	—	0
Bit 2	DashCode ID[2]	Dash code ID	R/W	—	—	0
Bit 1	DashCode ID[1]	Dash code ID	R/W	—	—	0
Bit 0	DashCode ID[0]	Dash code ID	R/W	—	—	0

Byte 2: Crystal Cap Setting

Byte 02h	Name	Control Function	Type	0	1	PWD
Bit 7	Xtal_Cap[7]	Xtal cap load trimming bits	R/W	x1 x2 x4 x8 total 15pf		0
Bit 6	Xtal_Cap[6]	Xtal cap load trimming bits	R/W			0
Bit 5	Xtal_Cap[5]	Xtal cap load trimming bits	R/W			0
Bit 4	Xtal_Cap[4]	Xtal cap load trimming bits	R/W			1
Bit 3	Xtal_Cap[3]	Xtal cap load trimming bits	R/W			0
Bit 2	Xtal_Cap[2]	Xtal cap load trimming bits	R/W			0
Bit 1	Xtal_Cap[1]	Xtal cap load trimming bits	R/W			0
Bit 0	Xtal_Cap[0]	Xtal cap load trimming bits	R/W			1

Byte 3: PLL3 M Divider

Byte 03h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL3_MDIV1	PLL3 source clock divider	R/W	disable M DIV1	bypadd divider (/1)	0
Bit 6	PLL3_MDIV2	PLL3 source clock divider	R/W	disable M DIV2	bypadd divider (/2)	0
Bit 5	PLL3 M_DIV[5]	PLL3 reference integer divider	R/W	3–64	default 25	0
Bit 4	PLL3 M_DIV[4]	PLL3 reference integer divider	R/W	—	—	1
Bit 3	PLL3 M_DIV[3]	PLL3 reference integer divider	R/W	—	—	1
Bit 2	PLL3 M_DIV[2]	PLL3 reference integer divider	R/W	—	—	0
Bit 1	PLL3 M_DIV[1]	PLL3 reference integer divider	R/W	—	—	0
Bit 0	PLL3 M_DIV[0]	PLL3 reference integer divider	R/W	—	—	1

Byte 4: PLL3 N Divider

Byte 04h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL3 N_DIV[7]	PLL3 VCO feedback integer divider bit7	R/W	12–2048, default VCO setting is 480MHz		1
Bit 6	PLL3 N_DIV[6]	PLL3 VCO feedback integer divider bit6	R/W			1
Bit 5	PLL3 N_DIV[5]	PLL3 VCO feedback integer divider bit5	R/W			1
Bit 4	PLL3 N_DIV[4]	PLL3 VCO feedback integer divider bit4	R/W			0
Bit 3	PLL3 N_DIV[3]	PLL3 VCO feedback integer divider bit3	R/W			0
Bit 2	PLL3 N_DIV[2]	PLL3 VCO feedback integer divider bit2	R/W			0
Bit 1	PLL3 N_DIV[1]	PLL3 VCO feedback integer divider bit1	R/W			0
Bit 0	PLL3 N_DIV[0]	PLL3 VCO feedback integer divider bit0	R/W			0

Byte 5: PLL3 Loop Filter Setting and N Divider 10:8

Byte 05h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL3_R100K	PLL3 Loop filter resister 100kohm	R/W	bypass	plus 100kohm	0
Bit 6	PLL3_R50K	PLL3 Loop filter resister 50kohm	R/W	bypass	plus 50kohm	0
Bit 5	PLL3_R25K	PLL3 Loop filter resister 25kohm	R/W	bypass	plus 25kohm	0
Bit 4	PLL3_R12.5K	PLL3 Loop filter resister 12.5kohm	R/W	bypass	plus 12.5kohm	1
Bit 3	PLL3_R6K	PLL3 Loop filter resister 6kohm	R/W	bypass	only 6kohm applied	0
Bit 2	PLL3 N_DIV[10]	PLL3 VCO feedback integer divider bit10	R/W	12–2048, default VCO setting is 480MHz		0
Bit 1	PLL3 N_DIV[9]	PLL3 VCO feedback integer divider bit9	R/W			0
Bit 0	PLL3 N_DIV[8]	PLL3 VCO feedback integer divider bit8	R/W			1

Byte 6: PLL3 Charge Pump Control

Byte 06h	Name	Control Function	Type	0	1	PWD
Bit 7	OUTDIV 3 Source	Output divider 3 source clock selection	R/W	PLL2	PLL3	0
Bit 6	PLL3_CP_8X	PLL3 charge pump control	R/W	—	x8	1
Bit 5	PLL3_CP_4X	PLL3 charge pump control	R/W	—	x4	1
Bit 4	PLL3_CP_2X	PLL3 charge pump control	R/W	—	x2	0
Bit 3	PLL3_CP_1X	PLL3 charge pump control	R/W	—	x1	1
Bit 2	PLL3_CP_/24	PLL3 charge pump control	R/W	—	/24	1
Bit 1	PLL3_CP_/3	PLL3 charge pump control	R/W	—	/3	0
Bit 0	PLL3_SIREF	PLL3 SiRef current selection	R/W	10µA	20µA	0

Formula: (iRef (10µA) × (1 + SIREF) × (1 × 1X + 2 × 2X + 4 × 4X + 8 × 8X + 16 × 16X))/((24 × /24) + (3 × /3))

Byte 7: PLL1 Control and OUTDIV5 Divider

Byte 07h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL1_MDIV_Doubler	PLL1 reference clock doubler	R/W	disable	enable	0
Bit 6	PLL1_SIREF	PLL1 SiRef current selection	R/W	10.8µA	21.6µA	0
Bit 5	PLL1_EN_CH2	PLL1 output Channel 2 control	R/W	disable	enable	1
Bit 4	PLL1_EN_3rdpole	PLL1 3rd Pole control	R/W	disable	enable	0
Bit 3	OUTDIV5[3]	Output divider5 control bit 3	R/W	—	—	0
Bit 2	OUTDIV5[2]	Output divider5 control bit 2	R/W	—	—	0
Bit 1	OUTDIV5[1]	Output divider5 control bit 1	R/W	—	—	1
Bit 0	OUTDIV5[0]	Output divider5 control bit 0	R/W	—	—	1

Byte 8: PLL1 M Divider

Byte 08h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL1_MDIV1	PLL3 VCO reference clock divider 1	R/W	disable M DIV1	bypass divider (/1)	0
Bit 6	PLL1_MDIV2	PLL3 VCO reference clock divider 2	R/W	disable M DIV2	bypass divider (/2)	0
Bit 5	PLL1 M_DIV[5]	PLL1 reference clock divider control bit 5	R/W	3–64, default is 25		0
Bit 4	PLL1 M_DIV[4]	PLL1 reference clock divider control bit 4	R/W			1
Bit 3	PLL1 M_DIV[3]	PLL1 reference clock divider control bit 3	R/W			1
Bit 2	PLL1 M_DIV[2]	PLL1 reference clock divider control bit 2	R/W			0
Bit 1	PLL1 M_DIV[1]	PLL1 reference clock divider control bit 1	R/W			0
Bit 0	PLL1 M_DIV[0]	PLL1 reference clock divider control bit 0	R/W			1

Byte 9: PLL1 VCO N Divider

Byte 09h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL1 N_DIV[7]	PLL1 VCO feedback divider control bit 7	R/W	12–2048, default is 600		0
Bit 6	PLL1 N_DIV[6]	PLL1 VCO feedback divider control bit 6	R/W			1
Bit 5	PLL1 N_DIV[5]	PLL1 VCO feedback divider control bit 5	R/W			0
Bit 4	PLL1 N_DIV[4]	PLL1 VCO feedback divider control bit 4	R/W			1
Bit 3	PLL1 N_DIV[3]	PLL1 VCO feedback divider control bit 3	R/W			1
Bit 2	PLL1 N_DIV[2]	PLL1 VCO feedback divider control bit 2	R/W			0
Bit 1	PLL1 N_DIV[1]	PLL1 VCO feedback divider control bit 1	R/W			0
Bit 0	PLL1 N_DIV[0]	PLL1 VCO feedback divider control bit 0	R/W			0

Byte 10: PLL Loop Filter and N Divider

Byte 0Ah	Name	Control Function	Type	0	1	PWD
Bit 7	PLL1_R100K	PLL1 Loop filter resister 100kohm	R/W	bypass	plus 100kohm	1
Bit 6	PLL1_R50K	PLL1 Loop filter resister 50kohm	R/W	bypass	plus 50kohm	0
Bit 5	PLL1_R25K	PLL1 Loop filter resister 25kohm	R/W	bypass	plus 25kohm	1
Bit 4	PLL1_R12.5K	PLL1 Loop filter resister 12.5kohm	R/W	bypass	plus 12.5kohm	1
Bit 3	PLL1_R1.0K	PLL1 Loop filter resister 1kohm	R/W	bypass	only 1.0kohm applied	0
Bit 2	PLL1 N_DIV[10]	PLL1 VCO feedback integer divider bit10	R/W	12–2048, default is 600		0
Bit 1	PLL1 N_DIV[9]	PLL1 VCO feedback integer divider bit9	R/W			1
Bit 0	PLL1 N_DIV[8]	PLL1 VCO feedback integer divider bit8	R/W			0

Byte 11: PLL1 Charge Pump

Byte 0Bh	Name	Control Function	Type	0	1	PWD
Bit 7	PLL1_CP_32X	PLL1 charge pump control	R/W	—	x32	0
Bit 6	PLL1_CP_16X	PLL1 charge pump control	R/W	—	x16	0
Bit 5	PLL1_CP_8X	PLL1 charge pump control	R/W	—	x8	0
Bit 4	PLL1_CP_4X	PLL1 charge pump control	R/W	—	x4	0
Bit 3	PLL1_CP_2X	PLL1 charge pump control	R/W	—	x2	0
Bit 2	PLL1_CP_1X	PLL1 charge pump control	R/W	—	x1	1
Bit 1	PLL1_CP_/24	PLL1 charge pump control	R/W	—	/24	1
Bit 0	PLL1_CP_/3	PLL1 charge pump control	R/W	—	/3	0

Byte 12: PLL1 Spread Spectrum Control

Byte 0Ch	Name	Control Function	Type	0	1	PWD
Bit 7	PLL1_SS_REFDIV23	PLL1 Spread Spectrum control - Ref divider 23	R/W	—	—	0
Bit 6	PLL1_SS_REFDIV[6]	PLL1 Spread Spectrum control - Ref divider 6	R/W	—	—	0
Bit 5	PLL1_SS_REFDIV[5]	PLL1 Spread Spectrum control - Ref divider 5	R/W	—	—	0
Bit 4	PLL1_SS_REFDIV[4]	PLL1 Spread Spectrum control - Ref divider 4	R/W	—	—	0
Bit 3	PLL1_SS_REFDIV[3]	PLL1 Spread Spectrum control - Ref divider 3	R/W	—	—	0
Bit 2	PLL1_SS_REFDIV[2]	PLL1 Spread Spectrum control - Ref divider 2	R/W	—	—	0
Bit 1	PLL1_SS_REFDIV[1]	PLL1 Spread Spectrum control - Ref divider 1	R/W	—	—	0
Bit 0	PLL1_SS_REFDIV[0]	PLL1 Spread Spectrum control - Ref divider 0	R/W	—	—	0

Byte 13: PLL1 Spread Spectrum Control

Byte 0Dh	Name	Control Function	Type	0	1	PWD
Bit 7	PLL1_SS_FBDIV[7]	PLL1 Spread Spectrum - feedback divider 7	R/W	—	—	0
Bit 6	PLL1_SS_FBDIV[6]	PLL1 Spread Spectrum - feedback divider 6	R/W	—	—	0
Bit 5	PLL1_SS_FBDIV[5]	PLL1 Spread Spectrum - feedback divider 5	R/W	—	—	0
Bit 4	PLL1_SS_FBDIV[4]	PLL1 Spread Spectrum - feedback divider 4	R/W	—	—	0
Bit 3	PLL1_SS_FBDIV[3]	PLL1 Spread Spectrum - feedback divider 3	R/W	—	—	0
Bit 2	PLL1_SS_FBDIV[2]	PLL1 Spread Spectrum - feedback divider 2	R/W	—	—	0
Bit 1	PLL1_SS_FBDIV[1]	PLL1 Spread Spectrum - feedback divider 1	R/W	—	—	0
Bit 0	PLL1_SS_FBDIV[0]	PLL1 Spread Spectrum - feedback divider 0	R/W	—	—	0

Byte 14: PLL1 Spread Spectrum Control

Byte 0Eh	Name	Control Function	Type	0	1	PWD
Bit 7	PLL1_SS_FBDIV[15]	PLL1 Spread Spectrum - feedback divider 15	R/W	—	—	0
Bit 6	PLL1_SS_FBDIV[14]	PLL1 Spread Spectrum - feedback divider 14	R/W	—	—	0
Bit 5	PLL1_SS_FBDIV[13]	PLL1 Spread Spectrum - feedback divider 13	R/W	—	—	0
Bit 4	PLL1_SS_FBDIV[12]	PLL1 Spread Spectrum - feedback divider 12	R/W	—	—	0
Bit 3	PLL1_SS_FBDIV[11]	PLL1 Spread Spectrum - feedback divider 11	R/W	—	—	0
Bit 2	PLL1_SS_FBDIV[10]	PLL1 Spread Spectrum - feedback divider 10	R/W	—	—	0
Bit 1	PLL1_SS_FBDIV[09]	PLL1 Spread Spectrum - feedback divider 9	R/W	—	—	0
Bit 0	PLL1_SS_FBDIV[08]	PLL1 Spread Spectrum - feedback divider 8	R/W	—	—	0

Byte 15: Output Divider1 Control

Byte 0Fh	Name	Control Function	Type	0	1	PWD
Bit 7	OUTDIV1[3]	Output divider1 control bit 3	R/W	—	—	0
Bit 6	OUTDIV1[2]	Output divider1 control bit 2	R/W	—	—	0
Bit 5	OUTDIV1[1]	Output divider1 control bit 1	R/W	—	—	1
Bit 4	OUTDIV1[0]	Output divider1 control bit 0	R/W	—	—	1
Bit 3	OUTDIV2[3]	Output divider2 control bit 3	R/W	—	—	0
Bit 2	OUTDIV2[2]	Output divider2 control bit 2	R/W	—	—	0
Bit 1	OUTDIV2[1]	Output divider2 control bit 1	R/W	—	—	1
Bit 0	OUTDIV2[0]	Output divider2 control bit 0	R/W	—	—	1

Byte 16: PLL2 Integer Feedback Divide

Byte 10h	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	PLL2_FB_INT[10]	PLL2 feedback integer divider 10	R/W	—	—	0
Bit 1	PLL2_FB_INT[9]	PLL2 feedback integer divider 9	R/W	—	—	0
Bit 0	PLL2_FB_INT[8]	PLL2 feedback integer divider 8	R/W	—	—	0

Byte 17: PLL2 Integer Feedback Divider

Byte 11h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_FB_INT_DIV[7]	PLL2 feedback integer divider 7	R/W	—	—	0
Bit 6	PLL2_FB_INT_DIV[6]	PLL2 feedback integer divider 6	R/W	—	—	0
Bit 5	PLL2_FB_INT_DIV[5]	PLL2 feedback integer divider 5	R/W	—	—	1
Bit 4	PLL2_FB_INT_DIV[4]	PLL2 feedback integer divider 4	R/W	—	—	0
Bit 3	PLL2_FB_INT_DIV[3]	PLL2 feedback integer divider 3	R/W	—	—	1
Bit 2	PLL2_FB_INT_DIV[2]	PLL2 feedback integer divider 2	R/W	—	—	0
Bit 1	PLL2_FB_INT_DIV[1]	PLL2 feedback integer divider 1	R/W	—	—	0
Bit 0	PLL2_FB_INT_DIV[0]	PLL2 feedback integer divider 0	R/W	—	—	0

Byte 18: PLL2 Fractional Feedback Divider

Byte 12h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_FB_FRC_DIV[7]	PLL2 feedback fractional divider 7	R/W	—	—	0
Bit 6	PLL2_FB_FRC_DIV[6]	PLL2 feedback fractional divider 6	R/W	—	—	0
Bit 5	PLL2_FB_FRC_DIV[5]	PLL2 feedback fractional divider 5	R/W	—	—	0
Bit 4	PLL2_FB_FRC_DIV[4]	PLL2 feedback fractional divider 4	R/W	—	—	0
Bit 3	PLL2_FB_FRC_DIV[3]	PLL2 feedback fractional divider 3	R/W	—	—	0
Bit 2	PLL2_FB_FRC_DIV[2]	PLL2 feedback fractional divider 2	R/W	—	—	0
Bit 1	PLL2_FB_FRC_DIV[1]	PLL2 feedback fractional divider 1	R/W	—	—	0
Bit 0	PLL2_FB_FRC_DIV[0]	PLL2 feedback fractional divider 0	R/W	—	—	0

Byte 19: PLL2 Fractional Feedback Divider

Byte 13h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_FB_FRC_DIV[15]	PLL2 feedback fractional divider 15	R/W	—	—	0
Bit 6	PLL2_FB_FRC_DIV[14]	PLL2 feedback fractional divider 14	R/W	—	—	0
Bit 5	PLL2_FB_FRC_DIV[13]	PLL2 feedback fractional divider 13	R/W	—	—	0
Bit 4	PLL2_FB_FRC_DIV[12]	PLL2 feedback fractional divider 12	R/W	—	—	0
Bit 3	PLL2_FB_FRC_DIV[11]	PLL2 feedback fractional divider 11	R/W	—	—	0
Bit 2	PLL2_FB_FRC_DIV[10]	PLL2 feedback fractional divider 10	R/W	—	—	0
Bit 1	PLL2_FB_FRC_DIV[9]	PLL2 feedback fractional divider 9	R/W	—	—	0
Bit 0	PLL2_FB_FRC_DIV[8]	PLL2 feedback fractional divider 8	R/W	—	—	0

Byte 20: PLL2 Spread Spectrum Control

Byte 14h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_STEP[7]	PLL2 spread step size control bit 7	R/W	—	—	0
Bit 6	PLL2_STEP[6]	PLL2 spread step size control bit 6	R/W	—	—	0
Bit 5	PLL2_STEP[5]	PLL2 spread step size control bit 5	R/W	—	—	0
Bit 4	PLL2_STEP[4]	PLL2 spread step size control bit 4	R/W	—	—	0
Bit 3	PLL2_STEP[3]	PLL2 spread step size control bit 3	R/W	—	—	0
Bit 2	PLL2_STEP[2]	PLL2 spread step size control bit 2	R/W	—	—	0
Bit 1	PLL2_STEP[1]	PLL2 spread step size control bit 1	R/W	—	—	0
Bit 0	PLL2_STEP[0]	PLL2 spread step size control bit 0	R/W	—	—	0

Byte 21: PLL2 Spread Spectrum Control

Byte 15h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_STEP[15]	PLL2 spread step size control bit 15	R/W	—	—	0
Bit 6	PLL2_STEP[14]	PLL2 spread step size control bit 14	R/W	—	—	0
Bit 5	PLL2_STEP[13]	PLL2 spread step size control bit 13	R/W	—	—	0
Bit 4	PLL2_STEP[12]	PLL2 spread step size control bit 12	R/W	—	—	0
Bit 3	PLL2_STEP[11]	PLL2 spread step size control bit 11	R/W	—	—	0
Bit 2	PLL2_STEP[10]	PLL2 spread step size control bit 10	R/W	—	—	0
Bit 1	PLL2_STEP[9]	PLL2 spread step size control bit 9	R/W	—	—	0
Bit 0	PLL2_STEP[8]	PLL2 spread step size control bit 8	R/W	—	—	0

Byte 22: PLL2 Spread Spectrum Control

Byte 16h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_STEP_DELTA[7]	PLL2 spread step size control delta bit 7	R/W	—	—	0
Bit 6	PLL2_STEP_DELTA[6]	PLL2 spread step size control delta bit 6	R/W	—	—	0
Bit 5	PLL2_STEP_DELTA[5]	PLL2 spread step size control delta bit 5	R/W	—	—	0
Bit 4	PLL2_STEP_DELTA[4]	PLL2 spread step size control delta bit 4	R/W	—	—	0
Bit 3	PLL2_STEP_DELTA[3]	PLL2 spread step size control delta bit 3	R/W	—	—	0
Bit 2	PLL2_STEP_DELTA[2]	PLL2 spread step size control delta bit 2	R/W	—	—	0
Bit 1	PLL2_STEP_DELTA[1]	PLL2 spread step size control delta bit 1	R/W	—	—	0
Bit 0	PLL2_STEP_DELTA[0]	PLL2 spared step size control delta bit 0	R/W	—	—	0

Byte 23: PLL2 Period Control

Byte 17h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_PERIOD[7]	PLL2 period control bit 7	R/W	—	—	0
Bit 6	PLL2_PERIOD[6]	PLL2 period control bit 6	R/W	—	—	0
Bit 5	PLL2_PERIOD[5]	PLL2 period control bit 5	R/W	—	—	0
Bit 4	PLL2_PERIOD[4]	PLL2 period control bit 4	R/W	—	—	0
Bit 3	PLL2_PERIOD[3]	PLL2 period control bit 3	R/W	—	—	0
Bit 2	PLL2_PERIOD[2]	PLL2 period control bit 2	R/W	—	—	0
Bit 1	PLL2_PERIOD[1]	PLL2 period control bit 1	R/W	—	—	0
Bit 0	PLL2_PERIOD[0]	PLL2 period control bit 0	R/W	—	—	0

Byte 24: PLL2 Control Register

Byte 18h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_PERIOD[9]	PLL2 period control bit 9	R/W	—	—	0
Bit 6	PLL2_PERIOD[8]	PLL2 period control bit 8	R/W	—	—	0
Bit 5	PLL2_SSEN	PLL2 spread spectrum enable	R/W	disable	enable	0
Bit 4	PLL2_R100K	PLL2 Loop filter resister 100kohm	—	bypass	plus 100kohm	0
Bit 3	PLL2_R50K	PLL2 Loop filter resister 50kohm	—	bypass	plus 50kohm	0
Bit 2	PLL2_R25K	PLL2 Loop filter resister 25kohm	—	bypass	plus 25kohm	0
Bit 1	PLL2_R12.5K	PLL2 Loop filter resister 12.5kohm	—	bypass	plus 12.5kohm	0
Bit 0	PLL2_R6K	PLL2 Loop filter resister 6kohm	—	bypass	only 6kohm applied	0

Byte 25: PLL2 Charge Pump Control

Byte 19h	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_CP_16X	PLL2 charge pump control	R/W	—	x16	0
Bit 6	PLL2_CP_8X	PLL2 charge pump control	R/W	—	x8	0
Bit 5	PLL2_CP_4X	PLL2 charge pump control	R/W	—	x4	1
Bit 4	PLL2_CP_2X	PLL2 charge pump control	R/W	—	x2	0
Bit 3	PLL2_CP_1X	PLL2 charge pump control	R/W	—	x1	0
Bit 2	PLL2_CP_/24	PLL2 charge pump control	R/W	—	/24	1
Bit 1	PLL2_CP_/3	PLL2 charge pump control	R/W	—	/3	0
Bit 0	PLL2_SIREF	PLL2 SiRef current selection	R/W	10µA	20µA	0

Byte 26: PLL2 M Divider Setting

Byte 1Ah	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_MDIV_Doubler	PLL2 reference divider - doubler	R/W	disable	enable	0
Bit 6	PLL2_MDIV1	PLL2 reference divider 1	R/W	disable M DIV1	bypadd divider (/1)	1
Bit 5	PLL2_MDIV2	PLL2 reference divider 2	R/W	disable M DIV2	bypadd divider (/2)	0
Bit 4	PLL2_MDIV[4]	PLL2 reference divider control bit 4	R/W	3–64, default is 25		0
Bit 3	PLL2_MDIV[3]	PLL2 reference divider control bit 3	R/W			0
Bit 2	PLL2_MDIV[2]	PLL2 reference divider control bit 2	R/W			0
Bit 1	PLL2_MDIV[1]	PLL2 reference divider control bit 1	R/W			0
Bit 0	PLL2_MDIV[0]	PLL2 reference divider control bit 0	R/W			0

Byte 27: Output Divider 4

Byte 1Bh	Name	Control Function	Type	0	1	PWD
Bit 7	OUTDIV3[3]	Out divider 3 control bit 3	R/W	—	—	0
Bit 6	OUTDIV3[2]	Out divider 3 control bit 2	R/W	—	—	0
Bit 5	OUTDIV3[1]	Out divider 3 control bit 1	R/W	—	—	1
Bit 4	OUTDIV3[0]	Out divider 3 control bit 0	R/W	—	—	1
Bit 3	OUTDIV4[3]	Out divider 4 control bit 3	R/W	—	—	0
Bit 2	OUTDIV4[2]	Out divider 4 control bit 2	R/W	—	—	0
Bit 1	OUTDIV4[1]	Out divider 4 control bit 1	R/W	—	—	1
Bit 0	OUTDIV4[0]	Out divider 4 control bit 0	R/W	—	—	1

Byte 28: PLL Operation Control Register

Byte 1Ch	Name	Control Function	Type	0	1	PWD
Bit 7	PLL2_HRS_EN	PLL2 spread high resolution selection enable	R/W	normal	enable (shift 4 bits)	0
Bit 6	PLL2_refin_sel	PLL2 reference clock source select	R/W	Xtal	DIV2	0
Bit 5	PLL3_PDB	PLL3 Power Down	R/W	Power Down	running	1
Bit 4	PLL3_LCKBYPSSB	PLL3 lock bypass	R/W	bypass lock	lock	1
Bit 3	PLL2_PDB	PLL2 Power Down	R/W	Power Down	running	1
Bit 2	PLL2_LCKBYPSSB	PLL2 lock bypass	R/W	bypass lock	lock	1
Bit 1	PLL1_PDB	PLL1 Power Down	R/W	Power Down	running	1
Bit 0	PLL1_LCKBYPSSB	PLL1 lock bypass	R/W	bypass lock	lock	1

Byte 29: Output Control

Byte 1Dh	Name	Control Function	Type	0	1	PWD
Bit 7	DIFF1_SEL	Differential clock 1 output OE2 control		not controlled	controlled	0
Bit 6	DIFF2_SEL	Differential clock 2 output OE2 control		not controlled	controlled	0
Bit 5	DIFF1_EN	Differential clock 1 output enable	R/W	disable	enable	1
Bit 4	DIFF2_EN	Differential clock 2 output enable	R/W	disable	enable	1
Bit 3	OUTDIV4_Source	Output divider 4 source clock selection	R/W	PLL2	Xtal	0
Bit 2	SE1_SLEW	SE 1 slew rate control	R/W	normal	strong	0
Bit 1	VDD1_SEL[1]	VDD1 level control bit 1	R/W	00/01: 3.3V 10: 2.5V 11: 1.8		0
Bit 0	VDD1_SEL[0]	VDD1 level control bit 0	R/W			0

Byte 30: OE and DFC Control

Byte 1Eh	Name	Control Function	Type	0	1	PWD
Bit 7	SE1_EN	SE1 output enable control	R/W	disable	enable	1
Bit 6	OE1_fun_sel[1]	OE1 pin function selection bit 1	R/W	11:DFC0 10: SE1_PPS 01: PD# 00: SE1 OE		0
Bit 5	OE1_fun_sel[0]	OE1 pin function selection bit 0	R/W			0
Bit 4	SE3_EN	SE3 output enable control	R/W	disable	enable	1
Bit 3	OE3_fun_sel[1]	OE3 pin function selection bit 1	R/W	11:DFC1 10: SE3_PPS 01: xx 00: SE3 OE		0
Bit 2	OE3_fun_sel[0]	OE3 pin function selection bit 0	R/W			0
Bit 1	DFC_SW_Sel[1]	DFC frequency select bit 1	R/W	00: N0 01: N1 10:N2 11:N3		0
Bit 0	DFC_SW_Sel[0]	DFC frequency select bit 0	R/W			0

Byte 31: Control Register

Byte 1Fh	Name	Control Function	Type	0	1	PWD
Bit 7	SE2_Freerun_32K	SE2 32K free run		freerun 32K	B31 bit6 control source	1
Bit 6	SE2_CLKSEL1	SE2 source clock selection		DIV5	DIV4	0
Bit 5	VDD2_SEL[1]	VDD2 level control bit 1	R/W	00/01: 3.3V 10: 2.5V 11: 1.8V		0
Bit 4	VDD2_SEL[0]	VDD2 level control bit 0	R/W			0
Bit 3	SE2_SLEW	SE2 slew rate control	R/W	normal	strong	0
Bit 2	PLL2_3rd_EN_CFG	PLL2 3rd order control		1st order	3rd order	1
Bit 1	PLL2_EN_CH2	PLL2 channel 2 enable control	R/W	disable	enable	0
Bit 0	PLL2_EN_3rdpole	PLL2 3rd Pole control	R/W	disable	enable	1

Byte 32: Control Register

Byte 20h	Name	Control Function	Type	0	1	PWD
Bit 7	SE2_EN	SE2 output enable control	R/W	disable	enable	1
Bit 6	OE2_fun_sel[1]	OE2 pin function selection bit 1	R/W	11:RESET 10: SE2_PPS 01: DIFF1/2 OE 00: SE2 OE		0
Bit 5	OE2_fun_sel[0]	OE2 pin function selection bit 0	R/W			0
Bit 4	DFC_EN	DFC function control	R/W	disable	enable	0
Bit 3	WD_EN	Watchdog timer control	R/W	disable	enable	0
Bit 2	Timer_sel<1>	Watchdog timer select bit 1	R/W	00: 250ms 01: 500ms 10: 2s 11: 4s		0
Bit 1	Timer_sel<0>	Watchdog timer select bit 0	R/W			0
Bit 0	Alarm_Flag	Alarm Status (Read Only)	R	No alarm	Alarmed	0

Byte 33: SE3 and DIFF1 Control Register

Byte 21h	Name	Control Function	Type	0	1	PWD
Bit 7	SE3_Freerun_32K	SE3 32K free run		freerun 32K	DIC2 or DIV4 selected by B33 bit6	1
Bit 6	SE3_CLKSEL1	SE3 source clock selection		DIV2	DIV4	0
Bit 5	VDD3_SEL[1]	VDD3 level control bit 1	R/W	11: 1.8V 10: 2.5V 0x: 3.3V		0
Bit 4	VDD3_SEL[0]	VDD3 level control bit 0	R/W			0
Bit 3	SE3_SLEW	SE3 slew rate control	R/W	normal	strong	0
Bit 2	DIFF_PDBHiZEN	Differential output high-Z at power down	R/W	TBD	output tri-state, bias off	0
Bit 1	DIFF1_CMOS2_FLIP	Differential 1/2 LVCMOS output control	R/W	DIFF1_B inverted	DIFF1_B non-inverted	0
Bit 0	DIFF2_CMOS2_FLIP	Differential 1/2 LVCMOS output control	R/W	DIFF2_B inverted	DIFF2_B non-inverted	0

Byte 34: DIFF1 Control Register

Byte 22h	Name	Control Function	Type	0	1	PWD
Bit 7	DIFF1_CLK_SEL	Differential clock 1 source selection	R/W	DIV1	DIV3	1
Bit 6	DIFF1_io_pwr_sel	Differential clock 1 output power	R/W	2.5V	3.3V	1
Bit 5	DIFF1_OUTPUT_TYPE[1]	Differential clock 1 type select bit 1	R/W	00: LVMOS 01: LVDS 10: LVPECL 11: LPHCSL		1
Bit 4	DIFF1_OUTPUT_TYPE[0]	Differential clock 1 type select bit 0	R/W			1
Bit 3	DIFF1_AMP[1]	Differential clock 1 amplitude control bit 1	R/W	LPHCSL: 00 = 740mV, 01 = 800mV, 10 = 855mV, 11 = 910mV LVPECL: 00 = 710mV, 01 = 810mV, 10 = 875mV, 11 = 920mV LVDS: 00 = 311mV, 01 = 344mV, 10 = 376mV, 11 = 408mV		0
Bit 2	DIFF1_AMP[0]	Differential clock 1 amplitude control bit 0	R/W			1

Byte 22h	Name	Control Function	Type	0	1	PWD
Bit 1	DIFF1_CMOS_SLEW	Differential clock 1 LVCMOS slew rate control	R/W	normal	strong	0
Bit 0	D1FF1_CMOS2_EN	Differential clock 1 LVCMOS output_B control	R/W	disable	enable	0

Byte 35: DIFF2 Control Register

Byte 23h	Name	Control Function	Type	0	1	PWD
Bit 7	DIFF2_CLK_SEL	Differential clock 2 source selection	R/W	DIV1	DIV3	0
Bit 6	DIFF2_IO_PWR_SEL	Differential clock 2 output power	R/W	2.5V	3.3V	1
Bit 5	DIFF2_OUTPUT_TYPE[1]	Differential clock 2 type select bit 1	R/W	00: LVMOS 01: LVDS 10: LVPECL 11: LPHCSL		1
Bit 4	DIFF2_OUTPUT_TYPE[0]	Differential clock 2 type select bit 0	R/W			1
Bit 3	DIFF2_AMP[1]	Differential clock 2 amplitude control bit 1	R/W	LPHCSL: 00 = 740mV, 01 = 800mV, 10 = 855mV, 11 = 910mV LVPECL: 00 = 710mV, 01 = 810mV, 10 = 875mV, 11 = 920mV LVDS: 00 = 311mV, 01 = 344mV, 10 = 376mV, 11 = 408mV		0
Bit 2	DIFF2_AMP[0]	Differential clock 2 amplitude control bit 0	R/W			1
Bit 1	DIFF2_CMOS_SLEW	Differential clock 2 LVCMOS slew rate control	R/W	normal	strong	0
Bit 0	DIFF2_CMOS2_EN	Differential clock 2 LVCMOS output_B control	R/W	disable	enable	0

Byte 36: SE1 and DIV4 control

Byte 24h	Name	Control Function	Type	0	1	PWD
Bit 7	I2C_PDB	chip power down control bit	R/W	power down	normal	1
Bit 6	Ref_free_run	Reference clock output (SE2/SE3)	R/W	stop	free run	0
Bit 5	free_run_output_config	SE clocks free run control	R/W	SE2 free run	SE2/3 free run	0
Bit 4	SE1_Freerun_32K	SE1 clock output default	R/W	32k free run	B36bit3 control	0
Bit 3	SE1_CLKSEL1	SEL1 output select	R/W	DIV5	DIV4	1
Bit 2	REF_EN	REF output enable	R/W	disable	enable	1
Bit 1	DIV4_CH3_EN	DIV4 channel 3 output control	R/W	disable	enable	0
Bit 0	DIV4_CH2_EN	DIV4 channel 2 output control	R/W	disable	enable	0

Glossary of Features

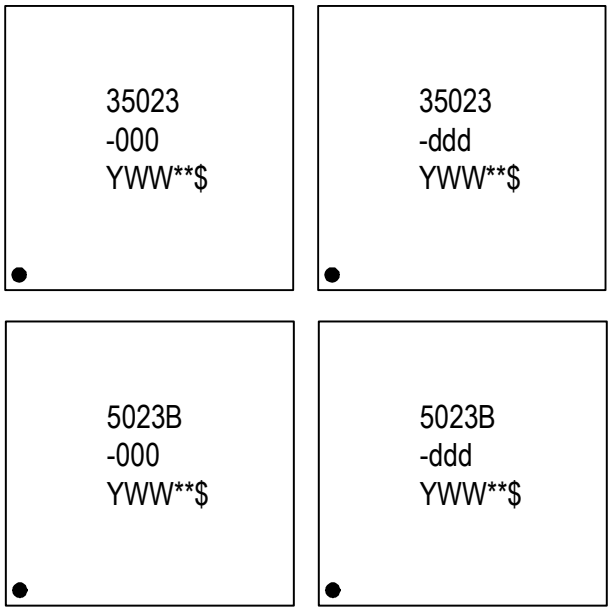
Table 37. Glossary of Features

Term	Function Description	Apply to
DFC	Dynamic Frequency Control; from selected PLL to support four VCO frequencies; means two different output frequencies by assigned H/W pin state changes (H-L or L-H) needs to have frequency change Glitch-Free function in order to not crash application system.	PLL2
ORT	Overshoot Reduction; when the DFC dynamic frequency change is functional, the VCO changes frequencies smoothly to target frequency without overshoot or undershoot.	PLL2
OE	Output enable function; each output can be controlled by assigned OE pin and the dedicated OE pin can be OTP programmable as global Power Down function (PD#) or Output Enable (OE) or Proactive Power Saving function (PPS) or RESET pin function.	OE1–3
SS	Spread spectrum clock.	PLL1/PLL2
Slew Rate	LVCMOS outputs with slew rate control – slow and fast.	LVCMOS
PPS	Proactive Power Saving; utilize OE pin as monitor pin for end device X2 clock status. See PPS – Proactive Power Saving Function description for details.	SE1–3

Package Outline Drawings

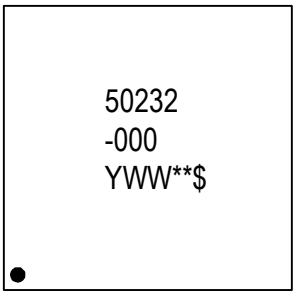
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagrams (industrial)



- Line 1 and 2 is the truncated part number.
  - "-000" denotes the blank part.
  - "-ddd" denotes the dash code.
- "YWW" is the last digit of the year and work week that the part was assembled.
- "**" denotes lot sequence number.
- "$" denotes mark code.

Marking Diagrams (automotive)



- Line 1 and 2 is the truncated part number.
  - "-000" denotes the blank part.
  - "-ddd" denotes the dash code.
- "YWW" is the last digit of the year and work week that the part was assembled.
- "**" denotes lot sequence number.
- "$" denotes mark code.

Ordering Information

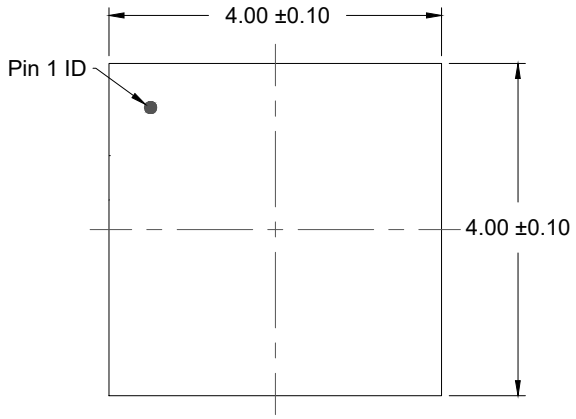
Orderable Part Number	Package	Carrier Type	Temperature
5P35023-000NLGI	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Trays	-40 to +85°C, Industrial
5P35023-000NLGI8	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tape and Reel	-40 to +85°C, Industrial
5P35023-dddNLGI	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Trays	-40 to +85°C, Industrial
5P35023-dddNLGI8	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tape and Reel	-40 to +85°C, Industrial
5P35023B-000NLGI	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Trays	-40 to +85°C, Industrial
5P35023B-000NLGI8	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tape and Reel	-40 to +85°C, Industrial
5P35023B-dddNLGI	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Trays	-40 to +85°C, Industrial
5P35023B-dddNLGI8	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tape and Reel	-40 to +85°C, Industrial
5P35023-000NLG2	4 × 4 mm, 0.5mm pitch 24-VFQFPN, Wettable Flank	Trays	-40 to +105°C, Automotive Grade 2
5P35023-000NLG28	4 × 4 mm, 0.5mm pitch 24-VFQFPN, Wettable Flank	Tape and Reel	-40 to +105°C, Automotive Grade 2
5P35023-dddNLG2	4 × 4 mm, 0.5mm pitch 24-VFQFPN, Wettable Flank	Trays	-40 to +105°C, Automotive Grade 2
5P35023-dddNLG28	4 × 4 mm, 0.5mm pitch 24-VFQFPN, Wettable Flank	Tape and Reel	-40 to +105°C, Automotive Grade 2

Revision History

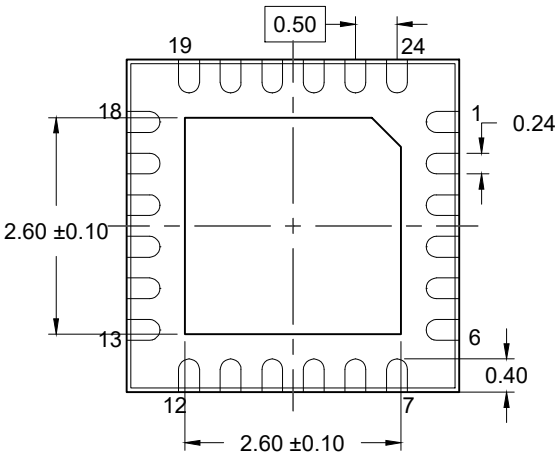
Revision Date	Description of Change
November 30, 2022	Updated 24-VFQFPN POD link in Ordering Information.
May 17, 2022	▪ Updated Supply Voltage ratings in Absolute Maximum Ratings table. ▪ Updated VIH maximum ratings in Table 26, Table 27, and Table 28 (3.3V, 2.5V, 1.8V).
October 4, 2019	Removed comment “VBAT power ramp-up should be same or earlier time than other VDD power rail.” from Power Group table, Recommended Operating Conditions and VBAT description section.
September 27, 2019	▪ Added revision “B” orderable part numbers (non-automotive) and marking diagrams.
August 19, 2019	▪ Updated Figure 4 PPS Assertion/Deassertion Timing Chart. ▪ Updated LVCMOS 3.3V VOL maximum and 2.5V VIL maximum. ▪ Updated LVDS VOS specifications.
May 15, 2019	▪ Added information for automotive parts. ▪ Corrected error in thermal impedance values. ▪ Corrected error in LVCMOS test load.
November 30, 2017	Updated I2C section.
January 25, 2017	▪ Updates/corrected typos in Byte 27. ▪ Updated package outline drawings.
May 26, 2016	Initial release.

Package Outline Drawing

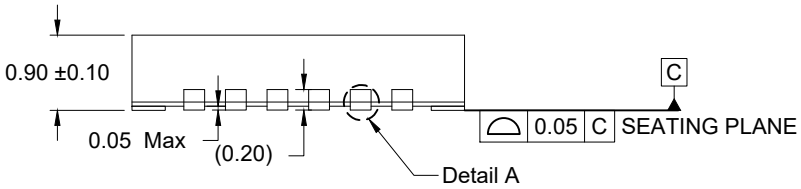
Package Code:NLG24S3
24-VFQFPN 4.0 x 4.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4192-07, Revision: 06, Date Created: Aug 1, 2022



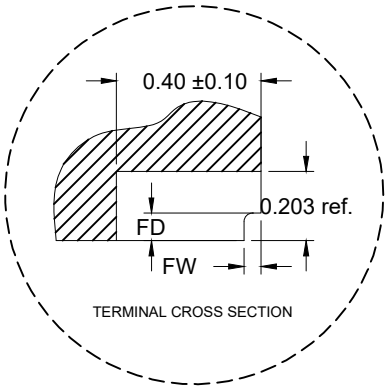
TOP VIEW



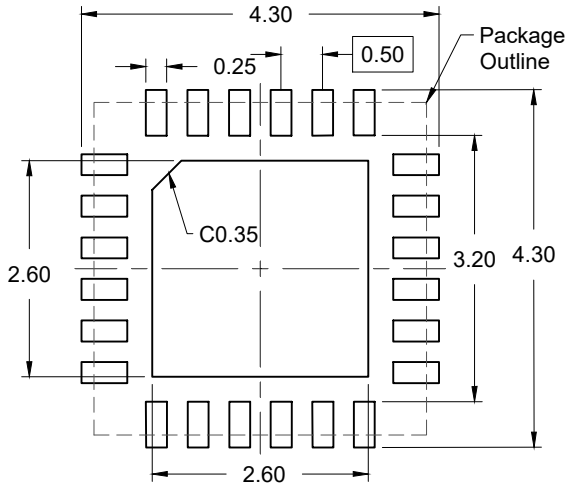
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

Table 1: Dimensions of wettable flank (DETAIL A)

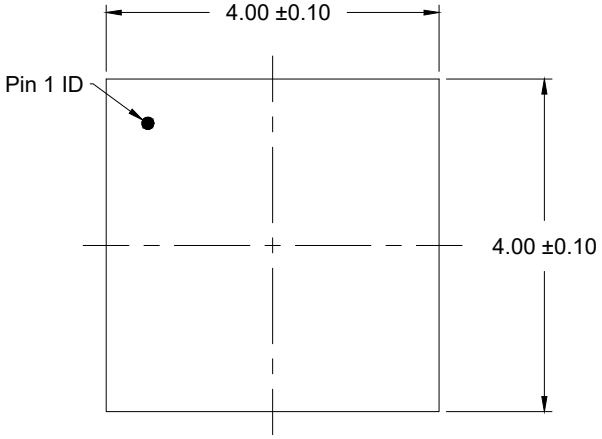
Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	-
FW	0.001	0.075

NOTES:

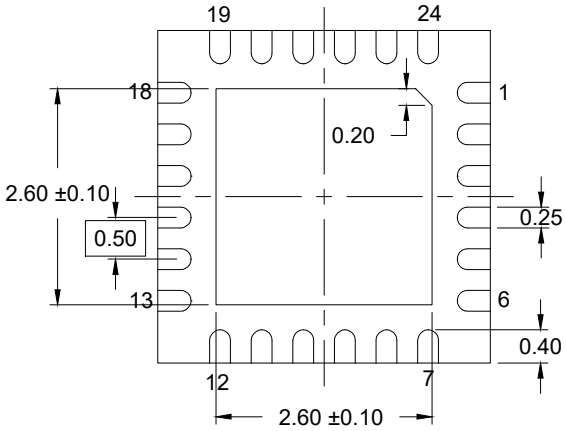
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Wettable flank (step cut).

Package Outline Drawing

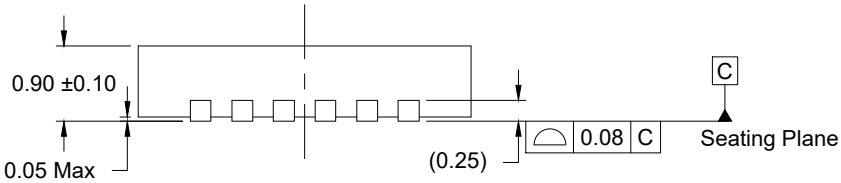
Package Code: NLG24P3
24-VFQFPN 4.0 x 4.0 x 0.90 mm Body, 0.5mm Pitch, Epad 2.60 x 2.60 mm
PSC-4192-03, Revision: 05, Date Created: July 13, 2022



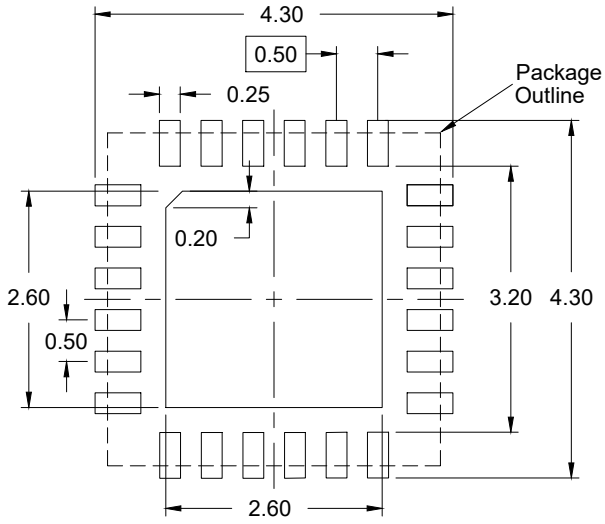
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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