MPQ4253A

36V, Step-Down Converter Supports One Type-A, One Type-C Dual USB Charging Ports for Automotive, AEC-Q100 Qualified

DESCRIPTION

The MPQ4253A integrates a monolithic, step-down, switch-mode converter with two USB current-limit switches and charging port identification circuitry for each port. The MPQ4253A achieves 6A of output current, with excellent load and line regulation over a wide input supply range.

The USB outputs are fixed as one Type-A port and one Type-C port. Each USB switch is current-limited. The USB1 port supports USB Type-C 5V @ 3A DFP mode. The USB2 port supports DCP schemes for battery charging specification (BC1.2), Apple divider 3 mode, and 1.2V/1.2V mode, eliminating the need for outside user interaction.

The MPQ4253A buck and USB2 output is always on if EN is high. The USB1 port capability automatically changes to 1.5A when USB2 detects a device is plugged in.

The step-down converter uses peak current mode control to regulate the output voltage. Under light-load conditions, it enters PFM mode to get high light-load efficiency.

Full protection features include hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown. The device supports load-shedding mode for the USB1 port. When entering load-shedding, the Type-C advertised current capability changes to 1.5A.

The MPQ4253A requires a minimal number of readily available, standard external components, and is available in a QFN-26 (5mmx5mm) package.

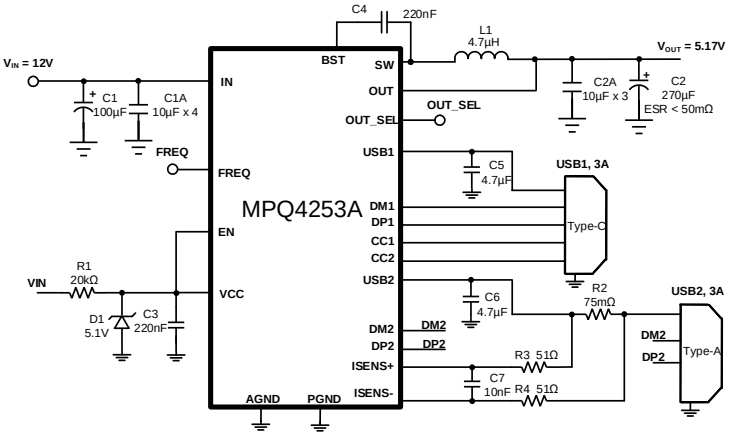
FEATURES

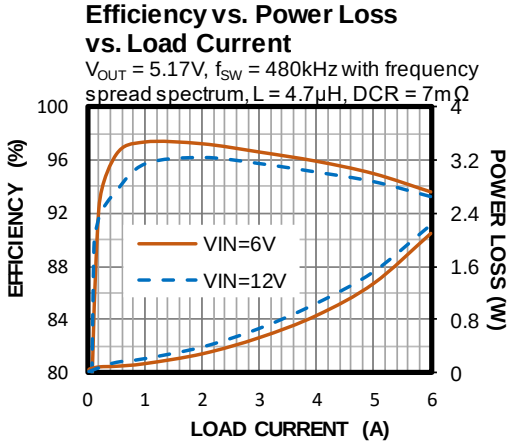
- All-In-One Type-C + Type-A Solution
- Type-C Auto-Enters 1.5A Load Capability when the Type-A Port Detects a Device Is Plugged In
- Default Frequency Spread Spectrum Based on 480kHz (FREQ = Float)
- Auto-PFM/PWM Operation
- Wide 6V to 36V Operating V_{IN} Range
- Selectable Output Voltage: 5.1V, 5.17V, or 5.3V
- 90mV Line Drop Compensation
- Accurate USB1/USB2 Output Current Limit
- 18mΩ/15mΩ Low Internal $R_{DS(ON)}$ Buck Power MOSFETs
- 18mΩ/18mΩ Low Internal $R_{DS(ON)}$ USB1/USB2 Power MOSFETs
- 250kHz to 1MHz Adjustable Frequency
- Hiccup Current Limit for Both Buck and USB
- Supports DCP Schemes for BC1.2, Apple Divider 3 Mode, and 1.2V/1.2V Mode
- Supports USB Type-C 5V @ 3A DFP Mode
- Available in a QFN-26 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB Dedicated Charging Ports (DCPs)
- USB Type-C + Type-A Hybrid Charging Ports

TYPICAL APPLICATION (1)





Note:

1) R1 and D1 must be added to power VCC before the buck output builds up.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4253AGU-AEC1	QFN-26 (5mmx5mm)	*See Below*	1

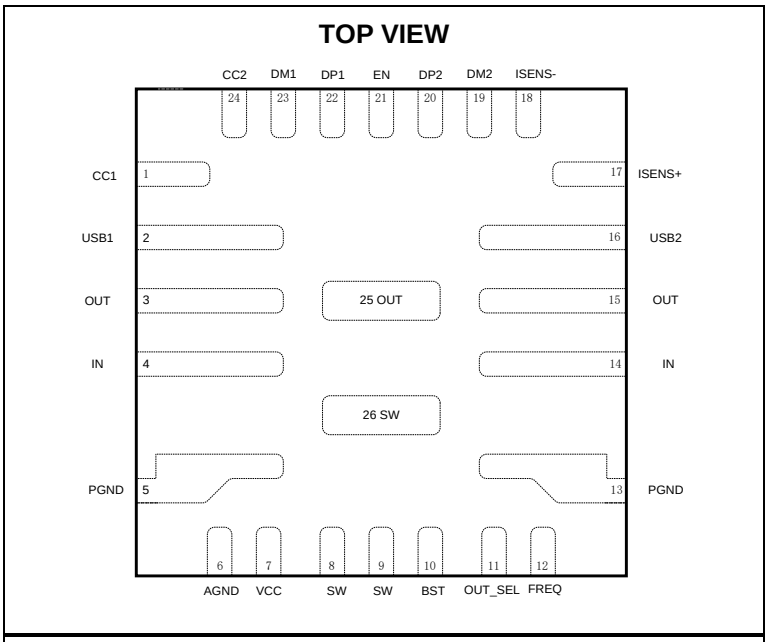
* For Tape & Reel, add suffix –Z (e.g. MPQ4253AGU-AEC1–Z).

TOP MARKING

MPSYYWW
MP4253A
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4253A: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE



QFN-26 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
2	USB1	**USB1 output.**
3, 15, 25	OUT	**Buck output.** OUT is the input for USB1 and USB2.
4, 14	IN	**Supply voltage.** IN is the drain of the internal power device, and provides the power supply for the entire chip. The MPQ4253A operates from a 6V to 36V input voltage. A capacitor (C_{IN}) prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
5, 13	PGND	**Power ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during PCB layout. Connect PGND with copper traces and vias.
6	AGND	**Analog ground.** Connect AGND to PGND.
7	VCC	**Internal 4.6V LDO regulator output.** Decouple VCC with a 220nF capacitor. This pin requires an external power supply for initial power-up.
8, 9, 26	SW	**Switch output.** Use a wide PCB trace to make the connection.
10	BST	**Bootstrap.** A 0.22µF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
11	OUT_SEL	**Buck output voltage set.** Setting OUT_SEL to either a low, floating, or high connection can set three different output voltages (5.1V, 5.17V, and 5.3V, respectively).
12	FREQ	**Switching frequency program input.** Connect a resistor from FREQ to GND to set the switching frequency. Float FREQ to achieve 480kHz with frequency spread spectrum. Connect FREQ to ground to achieve a 250kHz internal frequency.
16	USB2	**USB2 output.**
17	ISENS+	**Current-sense input positive terminal.** ISENS+ and ISENS- are used for detecting the USB2 current through an external resistor. Once the USB2 current exceeds a certain level, the USB1 port's CC pin pull-up resistance (R_P) changes to 22kΩ to indicate that its source capability has changed to 1.5A.
18	ISENS-	**Current-sense input negative terminal.** ISENS+ and ISENS- are used for detecting the USB2 current through an external resistor. Once the USB2 current exceeds a certain level, the USB1 port's CC pin pull-up resistance (R_P) changes to 22kΩ to indicate that its source capability has changed to 1.5A.
19	DM2	**D- data line to USB2 connector.** This input/output is used for handshaking with portable devices.
20	DP2	**D+ data line to USB2 connector.** This input/output is used for handshaking with portable devices.
21	EN	**On/off control input enable pin.** Apply a logic high voltage to EN to enable the IC; pull EN to logic low to disable the IC. This pin cannot be floated.
22	DP1	**D+ data line to USB1 connector.** This input/output is used for handshaking with portable devices.
23	DM1	**D- data line to USB1 connector.** This input/output is used for handshaking with portable devices.
24	CC2	**Configuration channel.** CC2 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.4V to +40V
V_{SW}.....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN}.....-0.3V to +10V (2)
V_{OUT}, V_{USB}.....-0.3V to +6.5V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = +25°C) (3) (7)
QFN-26 (5mmx5mm)..... 4.8W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Rating (4)

CC1/CC2 (HBM) (5) .....±6KV
DP1/DP2/DM1/DM2/ USB1/USB2 (HBM) (5).....±8KV
All other pins (HBM).....±1.8KV
All pins (CDM).....±1KV

Recommended Operating Conditions (6)

Operation input voltage range .....6V to 36V
Output current..... 3A for USB1, USB2
Operating junction temp (T_J) -40°C to +125°C (7)

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-26 (5mmx5mm)			
EVQ4253A-U-00A (8)	26	4	°C/W
JESD51-7 (9)	44	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS Max rating, see the Enable (EN) Control section on page 14.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114. CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
5) HBM with regard to GND.
6) The device is not guaranteed to function outside of its operating conditions.
7) Operating devices at junction temperatures greater than 125°C is possible. Contact MPS for details.
8) Measured on EVQ4253A-U-00A, 4-layer PCB, 50mmx50mm.
9) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, CC1 to ground with a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V, V_{CC} = 0V			10	μA
V_{IN} supply current (quiescent)	I_{Q1}	CC1 = 5.1kΩ, buck V_{OUT} = 5.4V, EN = high		540	1000	μA
	I_{Q2}	CC floating, buck V_{OUT} = 5.4V, EN = high		340	700	μA
EN rising threshold	V_{EN_RISING}		-3%	1.235	+3%	V
EN hysteresis	V_{EN_HYS}			230		mV
Thermal shutdown (10)	T_{TSD}			165		°C
Thermal hysteresis (10)	T_{TSD_HYS}			20		°C
VCC enable threshold	V_{CC_EN}			2.3	3	V
VCC internal regulator	V_{CC}		4.3	4.6	4.9	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO}		4.6	5.0	5.4	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			700		mV
HS switch on resistance	R_{DSON_HS}			18	40	mΩ
LS switch on resistance	R_{DSON_LS}			15	30	mΩ
Output voltage	V_{OUT}	OUT_SEL = low	-2%	5.10	+2%	V
		OUT_SEL = float, T_J = 25°C	-1%	5.17	+1%	
		OUT_SEL = float, T_J = -40°C to +125°C	-2%	5.17	+2%	
		OUT_SEL = high	-2%	5.30	+2%	
Output OVP	V_{OVP_R}		5.45	5.9	6.25	V
Output OVP recovery	V_{OVP_F}		5.3	5.7	6.1	V
Low-side current limit	I_{LS_LIMIT}			-2		A
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +125°C			5	
High-side current limit	I_{LIMIT}	V_{OUT} = 0V	8	12	16	A
Oscillator frequency	f_{SW1}	Pull R_{FREQ} to GND	185	250	315	kHz
	f_{SW2}	R_{FREQ} = 66.5kΩ	250	350	450	
Frequency spread spectrum span	f_{SS}	R_{FREQ} = float, based on 480kHz		±10		%
Maximum duty cycle	D_{MAX}	FREQ = 480kHz	91	95	99	%
Minimum off time	t_{OFF_MIN}			110		ns
Minimum on time (10)	t_{ON_MIN}			130		ns
Soft-start time	t_{SS}	Output from 10% to 90%	0.5	1	1.7	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 to ground with 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Switch (USB1 and USB2)						
Under-voltage lockout rising threshold	V_{USB_UVR}		3.7	4	4.3	V
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}			200		mV
Switch on resistance	R_{DSON_SW}			18	35	mΩ
USB OVP clamp	V_{USB_OV}		5.5	5.8	6	V
Current limit	I_{LIMIT1}	V_{OUT} drops 10%, Type-C mode (USB1), T_J = 25°C	-6%	3.55	+6%	A
	I_{LIMIT2}	V_{OUT} drops 10%, Type-A mode (USB2), T_J = 25°C	-6%	3.55	+6%	
Line drop compensation	V_{DROP_COM}	I_{OUT} = 2.4A, V_{OUT} = 5.17V	40	90	140	mV
V_{BUS1} soft-start time	t_{SS1}	Output from 10% to 90%	1	2	3	ms
V_{BUS2} soft-start time	t_{SS2}	Output from 10% to 90%	0.5	1	1.5	ms
Hiccup mode on time	t_{HICP_ON2}	OC, V_{OUT} drops 10%, T_J = 25°C	3.5	5	6.5	ms
		OC, V_{OUT} drops 10%, T_J = -40°C to +125°C	3	5	7	
Hiccup mode off time	t_{HICP_OFF}	V_{OUT} connected to GND	1	2	3	s
USB2 (Type-A Mode)						
ISENS rising threshold	V_{ISENS_R}		3.75	7.5	11.25	mV
ISENS falling threshold	V_{ISENS_F}		1			mV
ISENS falling voltage debounce timer	$t_{ISENS\_DEBOUNCE}$		2.4	3	3.6	s
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_SHORT}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = 25°C		85	155	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +125°C		85	160	
Divider Mode						
DP/DM output voltage	$V_{DP/DM\_DIVIDER}$		2.55	2.7	2.85	V
DP/DM output impedance	$R_{DP/DM\_DIVIDER}$	T_J = 25°C	14	22	30	kΩ
		T_J = -40°C to +125°C	14	22	34	
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V, T_J = 25°C	1.12	1.2	1.28	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	1.1	1.2	1.3	
DP/DM output impedance	$R_{DP/DM\_1.2V}$	T_J = 25°C	70	105	140	kΩ
		T_J = -40°C to +125°C	60	105	150	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 to ground with a 5.1kΩ resistor, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Type-C 5V @ 3A Mode – CC1, CC2						
CC voltage to enable VCONN	V_{Ra}				0.75	V
CC voltage to enable V_{BUS}	V_{Rd}		0.9		2.45	V
CC detach threshold	V_{OPEN}		2.75			V
CC falling voltage debounce timer	$t_{CC\_DEBOUNCE}$	V_{BUS} enable deglitch	100	144	200	ms
CC rising voltage debounce timer	$t_{PD\_DEBOUNCE}$	V_{BUS} disable deglitch	10	15	20	ms
VCONN output power	P_{VCONN}	V_{CONN} comes from the buck output with some series resistance	100			mW

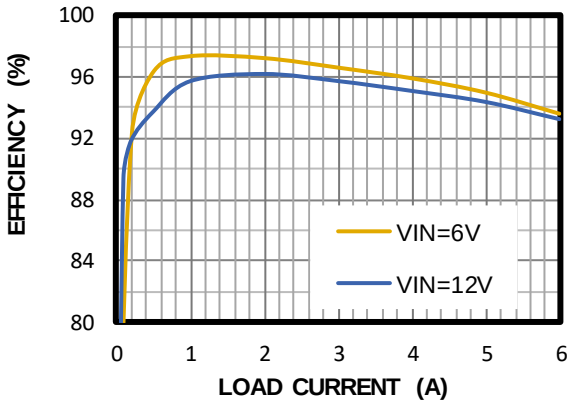
Note:

10) Guaranteed by engineering sample characterization.

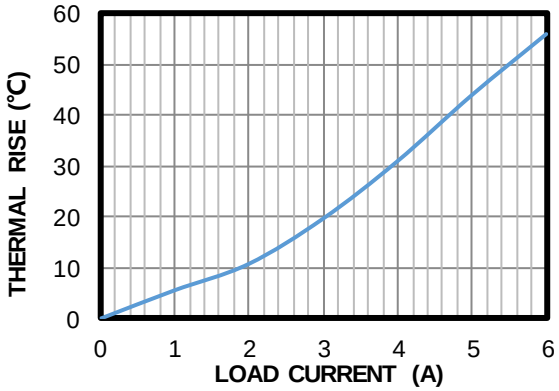
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SS} = spread spectrum based on 480kHz, L = 4.7µH, T_A = 25°C, CC1 to ground with a 5.1kΩ resistor, unless otherwise noted.

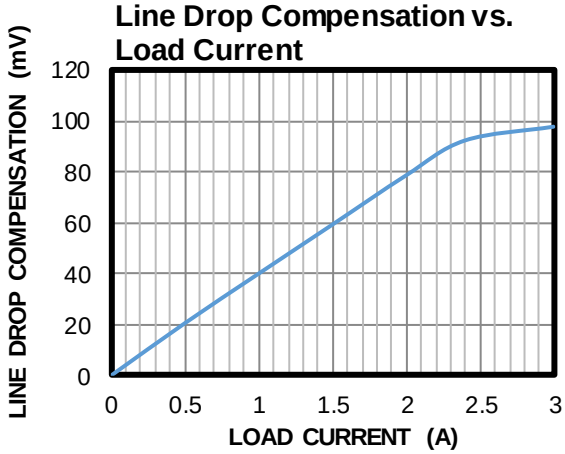
Efficiency vs. Load Current



Case Temperature Rise vs. Load Current

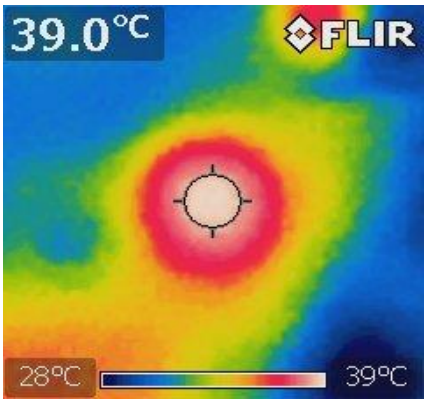


Line Drop Compensation vs. Load Current



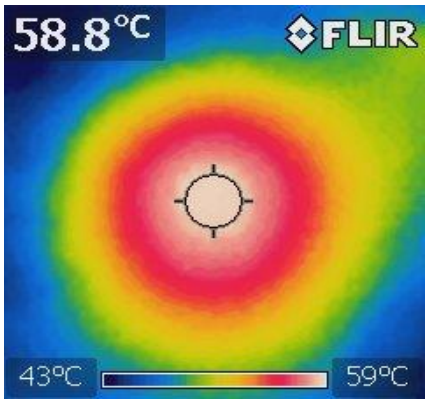
Thermal Image

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 21°C,
USB1_I_{OUT} = USB2_I_{OUT} = 1.5A



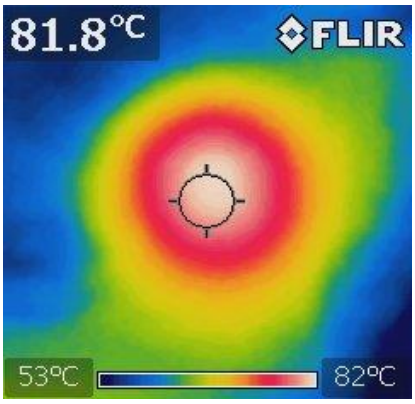
Thermal Image

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 21°C,
USB1_I_{OUT} = 1.5A, USB2_I_{OUT} = 3A



Thermal Image

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 21°C,
USB1_I_{OUT} = USB2_I_{OUT} = 3A

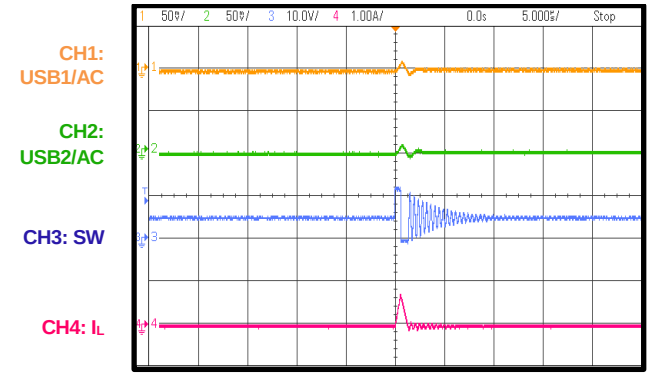


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SS} = spread spectrum based on 480kHz, L = 4.7µH, T_A = 25°C, CC1 to ground with a 5.1kΩ resistor, unless otherwise noted.

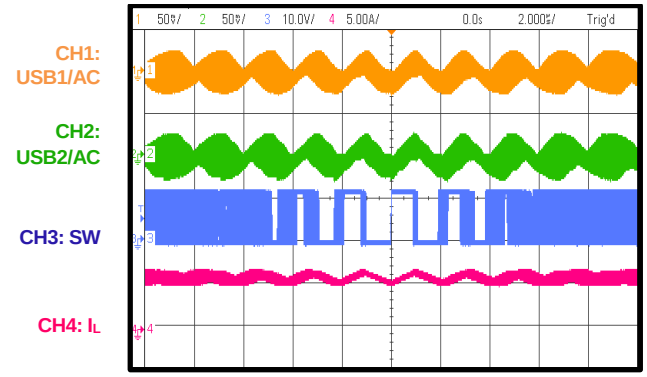
Steady State

USB1_I_{OUT} = USB2_I_{OUT} = 0A



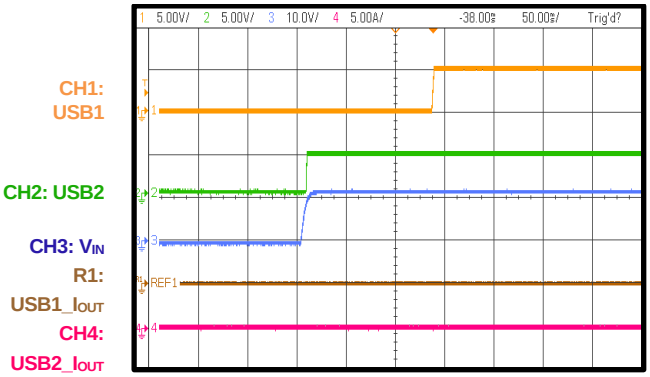
Steady State

USB1_I_{OUT} = USB2_I_{OUT} = 3A



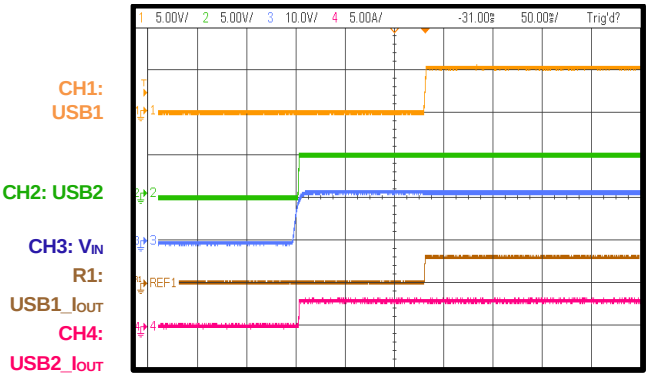
Power Start-Up

USB1_I_{OUT} = USB2_I_{OUT} = 0A



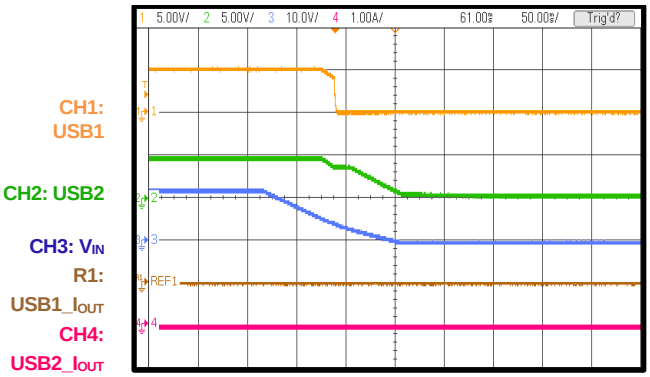
Power Start-Up

USB1_I_{OUT} = USB2_I_{OUT} = 3A



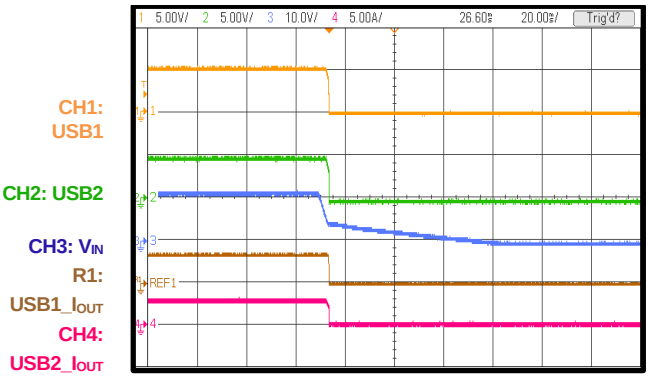
Power Shutdown

USB1_I_{OUT} = USB2_I_{OUT} = 0A



Power Shutdown

USB1_I_{OUT} = USB2_I_{OUT} = 3A

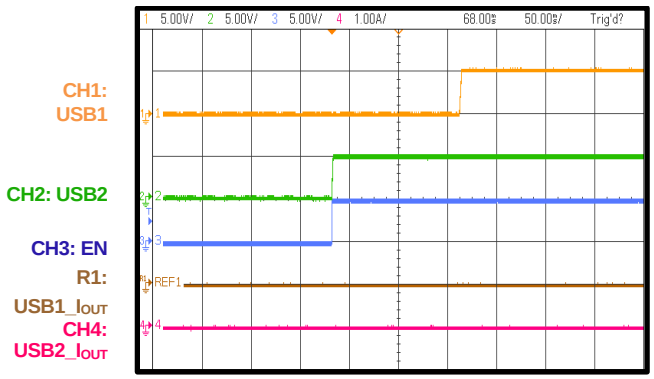


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SS} = spread spectrum based on 480kHz, L = 4.7µH, T_A = 25°C, CC1 to ground with a 5.1kΩ resistor, unless otherwise noted.

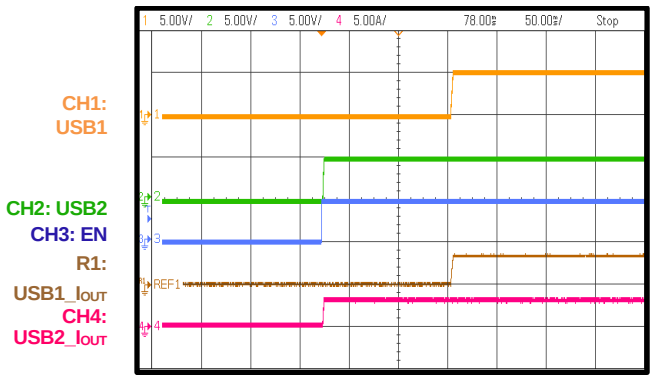
EN Start-Up

EN pin disconnected from VCC,
USB1_I_{OUT} = USB2_I_{OUT} = 0A



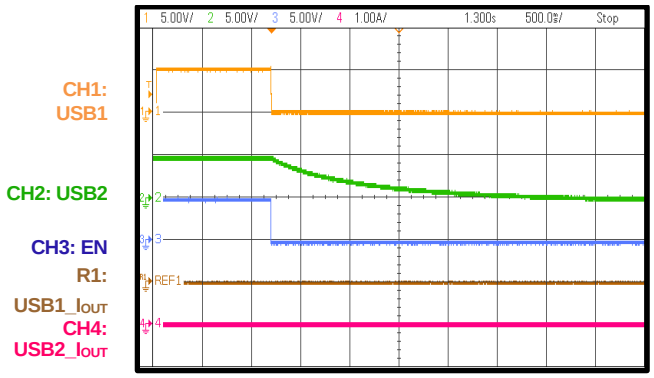
EN Start-Up

EN pin disconnected from VCC,
USB1_I_{OUT} = USB2_I_{OUT} = 3A



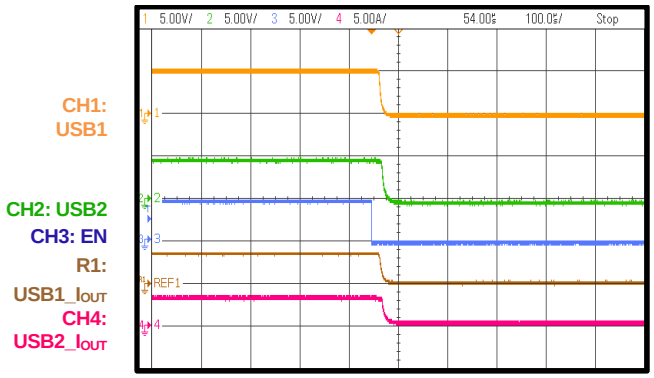
EN Shutdown

EN pin disconnected from VCC,
USB1_I_{OUT} = USB2_I_{OUT} = 0A



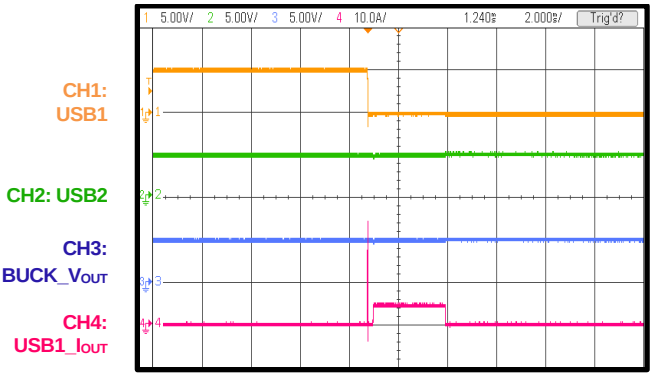
EN Shutdown

EN pin disconnected from VCC,
USB1_I_{OUT} = USB2_I_{OUT} = 3A



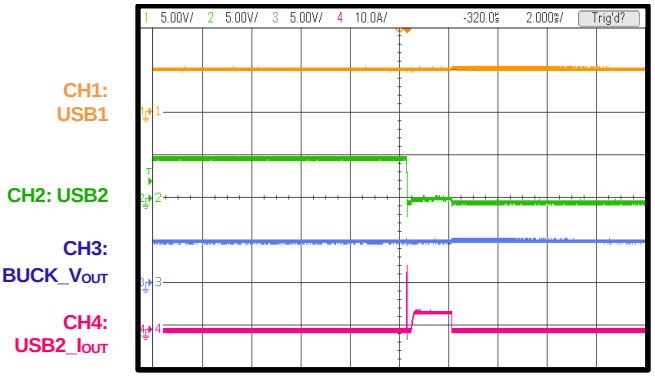
USB1 Short-to-GND Entry

USB1_I_{OUT} = USB2_I_{OUT} = 0A



USB2 Short-to-GND Entry

USB1_I_{OUT} = USB2_I_{OUT} = 0A

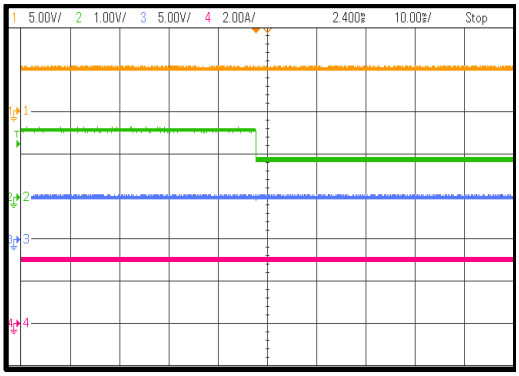


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SS} = spread spectrum based on 480kHz, L = 4.7µH, T_A = 25°C, CC1 to ground with a 5.1kΩ resistor, unless otherwise noted.

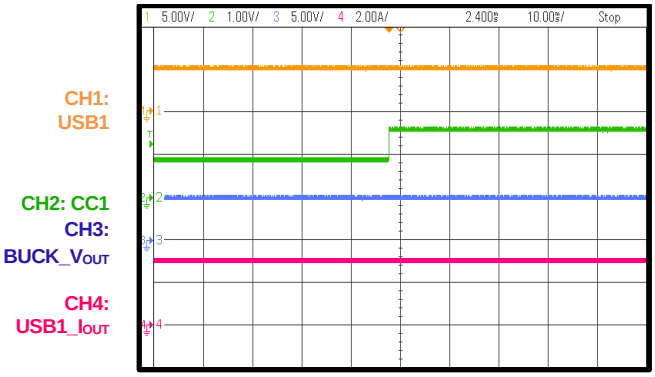
Load-Shedding Entry

USB1_I_{OUT} = 3A, USB2_I_{OUT} = 0A



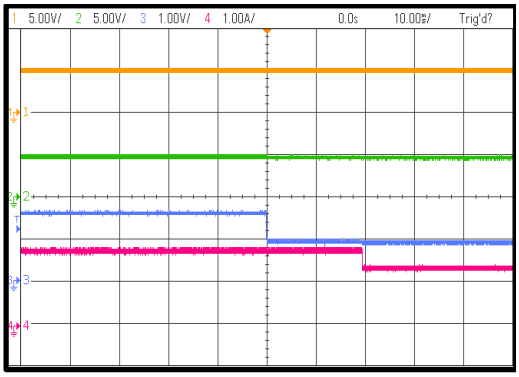
Load-Shedding Recovery

USB1_I_{OUT} = 3A, USB2_I_{OUT} = 0A



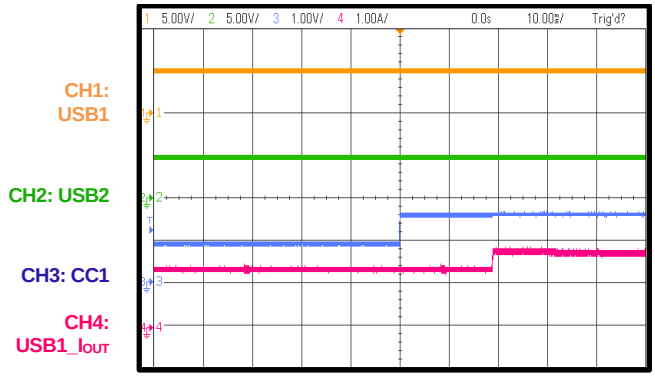
Type-C Enter 1.5A Load Capability

Remove CC1-to-ground 5.1kΩ resistor,
USB1 connected to mobile phone,
USB2 plugs into another mobile phone



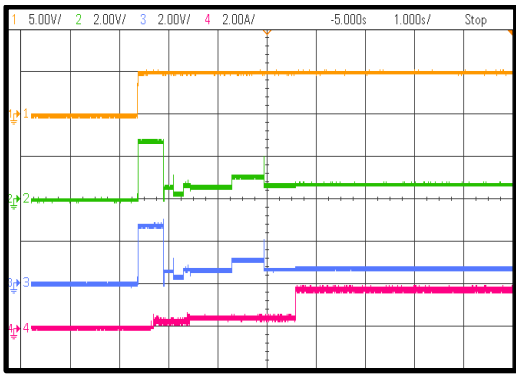
Type-C Quit 1.5A Load Capability

Remove CC1-to-ground 5.1kΩ resistor,
USB1 connected to mobile phone,
USB2 disconnects from another mobile phone

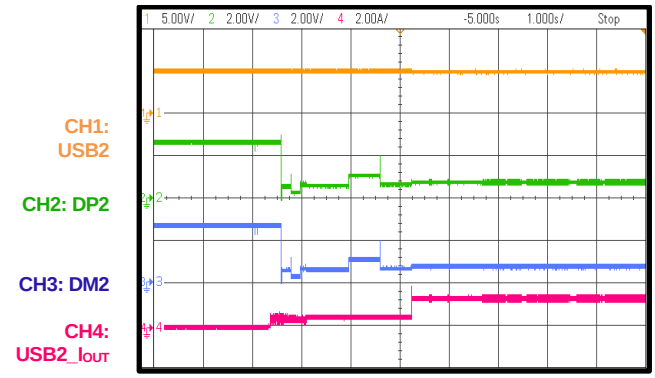


Type-C Port Device Charging Test

Remove CC1-to-ground 5.1kΩ resistor



Type-A Port Device Charging Test



FUNCTIONAL BLOCK DIAGRAM

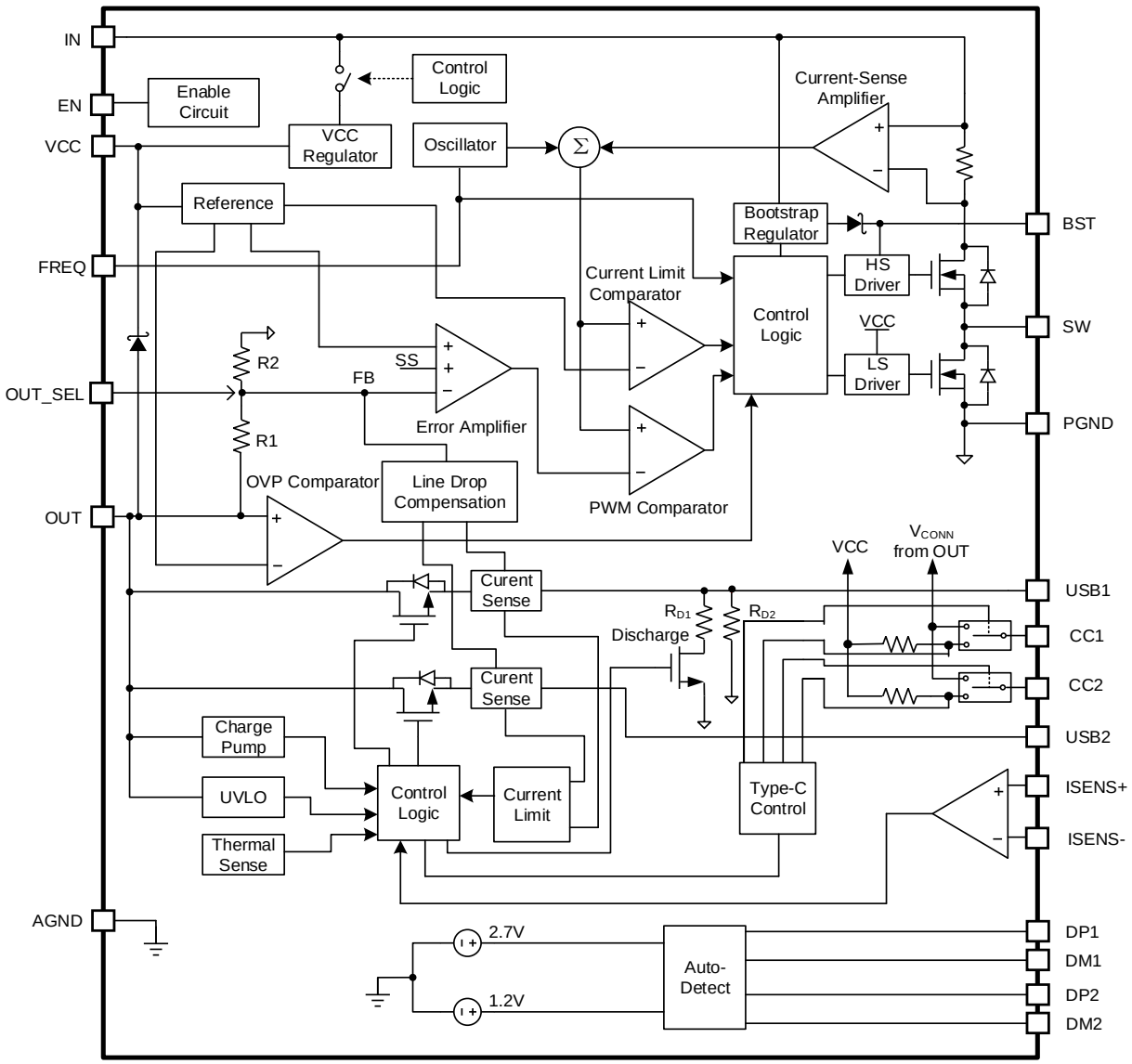


Figure 1: Functional Block Diagram

OPERATION

BUCK CONVERTER SECTION

The MPQ4253A integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with two USB current-limit switches and USB charging protocols. The MPQ4253A offers a compact solution that achieves 6A of continuous output current with excellent load and line regulation over a wide input supply range.

The MPQ4253A operates with fixed-frequency, peak current mode control to regulate the output voltage. The internal clock initiates the pulse-width modulation (PWM) cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the duty cycle reaches 95% (480kHz switching frequency) in one PWM period, the current in the power MOSFET does not reach the COMP-set current value and the power MOSFET turns off. Under light-load conditions, the device enters PFM mode to get high efficiency performance.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal reference (V_{REF}) and outputs V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Internal VCC Regulator

The MPQ4253A requires an external power supply to VCC in order to enable the chip before the converter turns on. This can be accomplished by connecting a resistor and a 5.1V Zener diode from VIN to GND (see the Typical Application Circuit section on page 23). VCC is supplied power via an external resistor and diode path. When VCC exceeds about 2.3V, the internal VCC LDO regulator starts to turn on. This regulator takes V_{IN} as the input and internally regulates the VCC voltage (V_{CC}) to 4.6V. VCC requires an external 220nF ceramic decoupling capacitor (see Figure 2).

After the buck output starts up, the internal VCC LDO output is biased by the buck output through a Schottky diode.

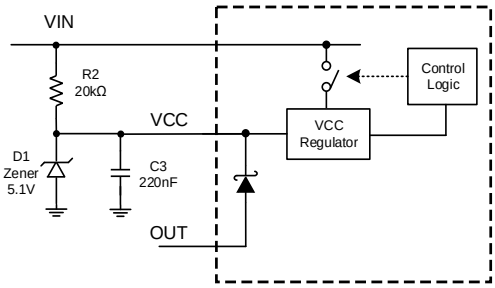


Figure 2: VCC External Connection

Enable (EN) Control

The MPQ4253A has an enable control pin (EN). Pull EN high to enable the IC; pull EN low to disable the IC (the internal VCC LDO regulator and buck can also be disabled). This pin cannot be floated. Once EN is pulled high, the buck output and USB2 are enabled.

EN is clamped internally using a 7.6V series Zener diode and a 10V breakdown voltage of the ESD cell.

It is recommended to connect EN to VCC. The IC powers up when V_{IN} exceeds the UVLO rising threshold. When selecting a pull-up resistor, ensure that it is large enough to limit the current flowing into EN below 100μA.

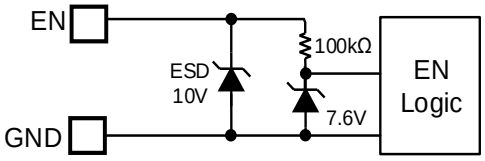


Figure 3: Zener Diode between EN and GND

Setting the Switching Frequency

Connect a resistor from FREQ to ground to set the switching frequency (see Table 1). R_{FREQ} ranges from 20kΩ to 80kΩ. The value of the frequency can be estimated with Equation (1):

$$FREQ(kHz) = \frac{1000000}{42.5 \times R_{FREQ}(k\Omega) + 53.7} \quad (1)$$

Table 1: Recommended Resistor Values for Typical Switching Frequency

R_{FREQ} (kΩ)	f_{SW} (kHz)
0	250
66.5	350
NC	Spread spectrum based on 480kHz
22	1000

Figure 4 shows the relationship between the frequency and R_{FREQ}.

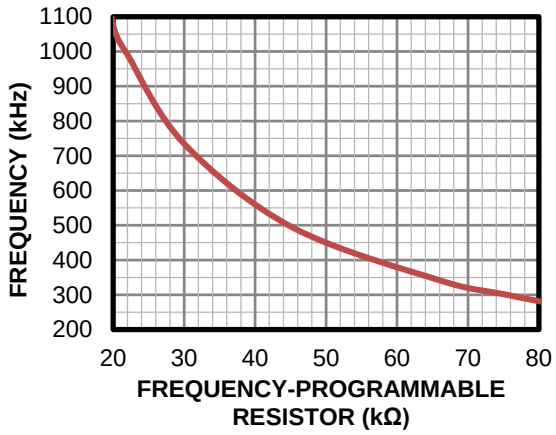


Figure 4: Switching Frequency vs. R_{FREQ}

Two internal comparators monitor FREQ's logic voltage to enable FREQ to float or short to GND. During power-up, there is another internal source current on FREQ. The frequency is locked at 480kHz when a voltage greater than 2V is sensed on FREQ for longer than 8µs. The frequency is locked at 250kHz when a voltage less than 0.1V is sensed on FREQ for longer than 8µs. Leave FREQ floating to achieve the 480kHz default switching frequency. Short FREQ to ground to achieve a 250kHz frequency (see Figure 5).

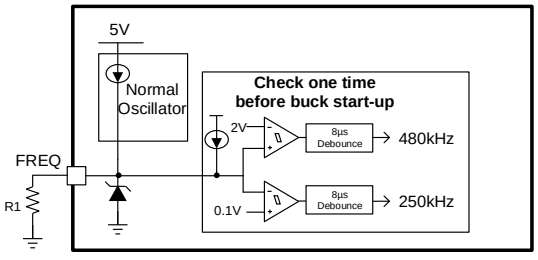


Figure 5: Switching Frequency Functional Block

Frequency Spread Spectrum

The purpose of spread spectrum is to minimize the peak emissions at certain frequencies.

The MPQ4253A uses a 4kHz triangle wave (rising 125µs, falling 125µs) to modulate the internal oscillator. The frequency span of spread spectrum operation is ±10% (see Figure 6).

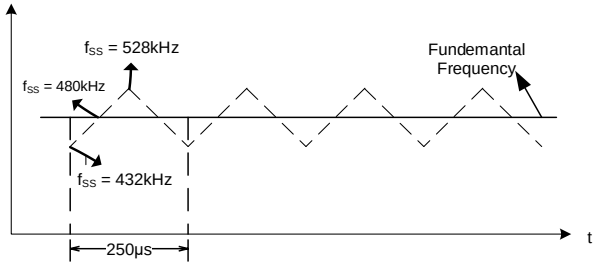


Figure 6: Frequency Spread Spectrum

The FREQ pin must be floated (480kHz) when using the spread spectrum function. The part operates without switching frequency spread spectrum when FREQ is connected to an external resistor or shorted to GND.

Light-Load Operation

As the load decreases, the MPQ4253A enters discontinuous conduction operation (DCM) and maintains a fixed frequency as long as the inductor current approaches zero.

If the load decreases further or there is no load that makes the inductor peak current lower than the AAM peak current threshold, the MPQ4253A enters sleep mode, consuming very low quiescent current to further improve the light-load efficiency. In sleep mode, the internal clock is blocked, and the MPQ4253A skips some pulses. Then the feedback voltage is less than the reference, so V_{COMP} ramps up until the inductor peak current exceeds the AAM threshold. Then the internal clock is reset, and the crossover time is taken as the benchmark for the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As the output current increases from light load, V_{COMP} increases, as does the switching frequency. If the output current exceeds the critical level set by V_{COMP}, the MPQ4253A resumes fixed-frequency PWM control (see Figure 7).

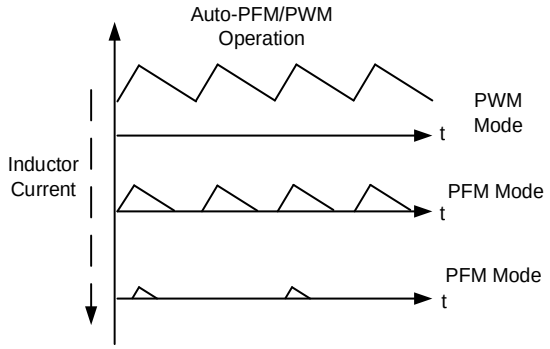


Figure 7: Auto-PFM/PWM Operation

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 5V, and its falling threshold is 4.3V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the buck converter is enabled, the internal circuitry generates a soft start voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below V_{REF}, the error amplifier uses V_{SS} as the reference. When V_{SS} is above V_{REF}, the error amplifier uses V_{REF} as the reference.

The SS time is set to 1ms internally. If the output of the MPQ4253A is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Buck Over-Current Protection (OCP)

The MPQ4253A offers over-current protection (OCP). There is a cycle-by-cycle over-current limit. When the inductor peak current exceeds the current-limit threshold and the FB voltage (V_{FB}) drops below the under-voltage (UV) threshold (typically 50% below the reference), UV is triggered. Then the MPQ4253A enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4253A exits hiccup mode once the over-current condition is removed.

Buck Output Over-Voltage Protection (OVP)

The MPQ4253A has output over-voltage protection (OVP). If the output exceeds 5.9V, the HS-FET stops turning on and the LS-FET turns on to discharge the output voltage until the output decreases to 5.7V. Then the chip resumes normal operation.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a 150mV hysteresis. The bootstrap capacitor voltage is internally regulated by VIN and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 8). The BST capacitor (C4) voltage is charged up quickly by VCC through M1. The 2.5μA input to the BST current source can also charge the BST capacitor when the LS-FET does not turn on.

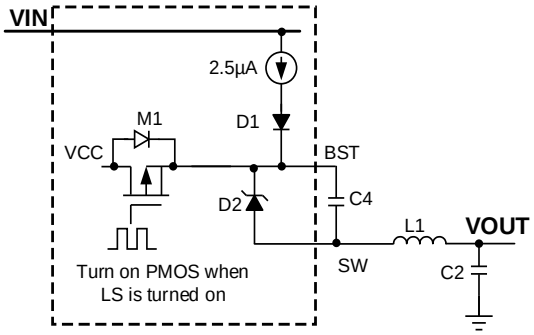


Figure 8: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If VIN and VCC exceed their respective thresholds, the internal regulator is enabled and provides a stable supply for the remaining circuitries. When EN enables the part, the buck converter and USB2 are active.

Two events can shut down the chip: EN low or VIN low. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

USB CURRENT-LIMIT SWITCH SECTION

Over-Current Protection (OCP) and Hiccup Mode

The MPQ4253A integrates two USB current-limit switches. The MPQ4253A provides built-in soft-

start circuitry that controls the rising slew rate of the output voltage to limit inrush current and voltage surges.

When the load current reaches the current-limit threshold, the USB power MOSFET works in constant current-limit mode (see Figure 9). If the over-current limit condition lasts for longer than 5ms (V_{OUT} does not drop too low), the corresponding USB channel enters hiccup mode with 5ms of on time and 2s of off time. The other USB channel still works normally.

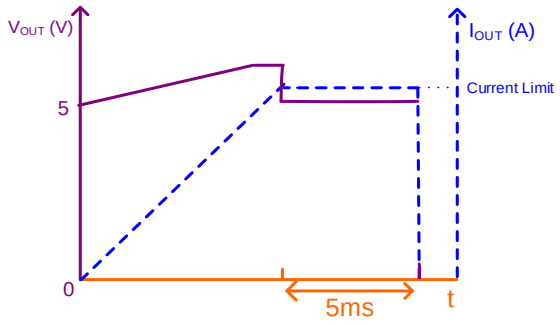


Figure 9: Over-Current Limit

After soft start finishes, if the USB output voltage is below 3.5V and lasts longer than 50µs, the MPQ4253A also enters hiccup mode without having to wait for 5ms (see Figure 10). This helps prevent an abnormal thermal rise during a constant resistor (CR) load over-current case.

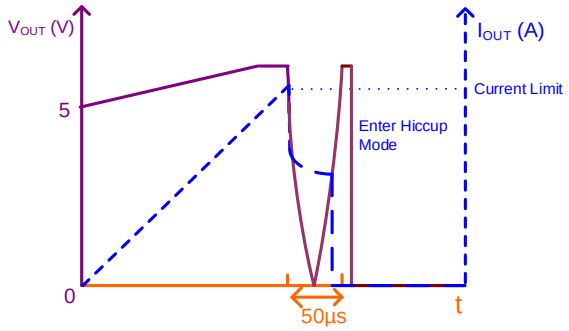


Figure 10: Over-Current Limit for CR Load

Fast Response for Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current-limit threshold before the control loop is able to respond. If the current reaches the 7A (for USB1) or 10.5A (for USB2) secondary current limit level, a fast turn-off circuit activates to turn off the power MOSFET. This helps limit the peak current through the switch, keeping the buck output voltage from dropping too much and affecting another USB channel. The total short-circuit response time is less than 1µs.

When the fast turn-off function is triggered, the MOSFET turns off for 100µs and restarts with a soft start. During the restart process, if the short still remains, the MPQ4253A regulates the gate voltage to hold the current at a normal current limit level.

Output Line Drop Compensation

The MPQ4253A can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant output voltage at the load-side voltage.

The internal comparator compares the current-sense output voltage of the two current-limit switches, and uses the larger current-sense output voltage to compensate for the line drop voltage.

The line drop compensation amplitude increases linearly as the load current increases. It also has an upper limitation. At output currents above 2.4A, the line drop compensation is 90mV.

USB Output Over-Voltage Clamp

To protect the device at the cable terminal, the USB switch output has a fixed over-voltage protection (OVP) threshold. When the input voltage exceeds the OVP threshold, the output voltage is clamped to its OVP threshold value.

USB Output Discharge and Impedance

The USB1 switch has a fast discharge path that can discharge the external output capacitor's energy quickly during power shutdown. This function is active when the CC pins are released or the part is disabled (input voltage is under UVLO or EN is off). The discharge path turns off when the USB output voltage is discharged below 50mV. After the fast discharge path turns off, there is only a high-impedance resistor (typically 500kΩ) from USB1 to ground.

USB2 has no output discharge function.

USB Port State Detection

The MPQ4253A monitors the USB2 Type-A port's state through DP2/DM2 or through the USB2 output current sensed by ISENS+ and ISENS-. If the DP2/DM2 voltage falls into the detection window or the voltage between

ISENS+ and ISENS- exceeds 7.5mV, this means a Type-A device is attached. Then the USB1 port's CC pin pull-up resistance (R_P) changes to 22kΩ to indicate that its source current capability is reduced to 1.5A.

The MPQ4253A returns to normal mode (R_P = 10kΩ) with 3 seconds when the MPQ4253A detects that there is no device plugged into the Type-A port.

If the Type-C port or Type-A port works standalone, each port can provide 3A of current.

Auto-Detection

The MPQ4253A integrates a USB dedicated charging port (DCP) auto-detect function. The USB outputs are fixed with one Type-C port for USB1 and one Type-A port for USB2. This function recognizes most mainstream portable devices and supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple divider 3 mode
- 1.2V/1.2V mode
- USB Type-C 5V @ 3A DFP mode (only for USB1)

The auto-detect function is a state machine that supports all of the DCP charging schemes listed above.

USB Type-C Mode and VCONN

For USB1 Type-C solutions, two pins (CC1 and CC2) on the connector are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and a sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up (R_P) and pull-down (R_D = 5.1kΩ) termination model is used based on a pull-up resistor and pull-down resistor (see Figure 11).

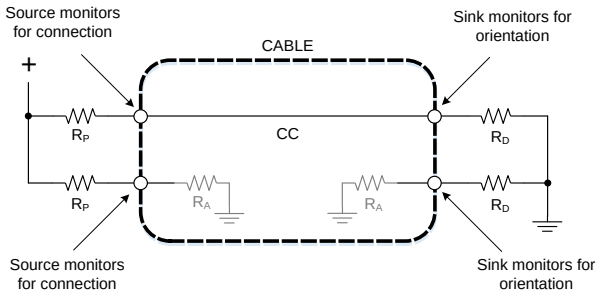


Figure 11: Current Source/Pull-Down CC Model

Initially, a source exposes independent R_P terminations on its CC1 and CC2 pins, and a sink exposes independent R_D terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage below its unterminated voltage. The choice of R_P is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Prior to the application of VCONN, a powered cable exposes R_A (typically 1kΩ) on its VCONN pin. R_A represents the load on VCONN plus any resistive elements to ground. In some cable plugs, this might be a pure resistance, and in others, it may simply be the load.

The source must be able to differentiate between the presence of R_D and R_A to know whether there is a sink attached and where to apply VCONN. The source is not required to supply to VCONN unless R_A is detected.

Two special termination combinations on the CC pins (as seen by a source) are defined for directly attached accessory modes: R_A/R_A for audio adapter accessory mode, and R_D/R_D for debug accessory mode (see Figure 12 and Table 2).

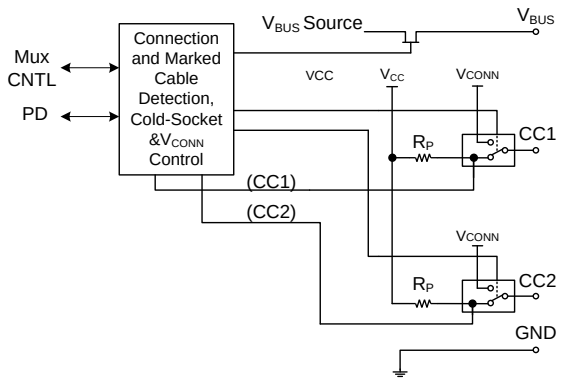


Figure 12: CC Pin Functional Block

A port that behaves as a source has the following functional characteristics:

1. The source uses a MOSFET to enable or disable the power delivery across V_{BUS}. Initially, the source is disabled.
2. The source supplies pull-up resistors (R_P) on CC1 and CC2, and monitors both to detect a sink. The presence of an R_D pull-down resistor on either CC1 or CC2 indicates that a sink is being attached. The value of R_P indicates the initial USB Type-C current level supported by the host. The MPQ4253A default R_P value is 10kΩ, which represents a 3A current level.
3. The source uses the CC pull-down characteristic to detect and determine which CC pin is intended to supply VCONN (when R_A is discovered).
4. Once a sink is detected, the source enables V_{BUS} and VCONN.
5. The source can dynamically adjust the value of R_P to indicate a change in the available USB Type-C current to a sink. For example, at high temperatures or if USB2 detects a device is attached, the MPQ4253A changes R_P to 22kΩ to indicate a 1.5A current ability.
6. The source monitors the continued presence of R_D to detect whether a sink is detached. When a detach event is detected, the source is removed, and V_{BUS} and VCONN return to step 2.

Load Shedding vs. Temperature

The MPQ4253A monitors the die temperature, and dynamically changes the USB1 output current capability.

If the die temperature exceeds 125°C, the output voltage remains unchanged, but the USB1 port's CC pin pull-up resistance (R_P) changes to 22kΩ to indicate that its source capability has changed to 1.5A.

If the die temperature is below 100°C for 16 seconds, the USB1 Type-C current capability changes back to 3A (R_P = 10kΩ). The current-limit threshold remains at 3.55A during this period.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the USB switch shuts down. When the temperature falls below its lower threshold (typically 145°C), the chip resumes normal operation.

Table 2: CC Logic Truth Table

EN	CC of USB1	USB2 Port Status	Buck	VCONN (USB1)	USB1	USB2
0	X	X	Disabled	Disabled	Disabled	Disabled
1	Audio	Attached with device	Enabled	Disabled	Disabled	Enabled
	Debug		Enabled	Disabled	Disabled	Enabled
	R_D, R_A		Enabled	Enabled	Enabled (11)	Enabled
	Open		Enabled	Disabled	Disabled	Enabled
1	Audio	Unattached	Enabled	Disabled	Disabled	Enabled
	Debug		Enabled	Disabled	Disabled	Enabled
	R_D, R_A		Enabled	Enabled	Enabled	Enabled
	Open		Enabled	Disabled	Disabled	Enabled

Note:

11) R_P changes to 22kΩ to indicate that its source capability has changed to 1.5A.

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% greater than the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. For most designs, the inductance value can be calculated with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% to 50% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Selecting Buck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimal performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. 100µF electrolytic and 40µF ceramic capacitors are recommended in automotive applications at a 480kHz switching frequency.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductance value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

A 100µF to 270µF capacitor with an ESR below 50mΩ (e.g. polymer or tantalum capacitors) and three 10µF ceramic capacitors are recommended in application (see Table 3).

Table 3: Recommended External Components

f_{SW}	Inductor	Input Capacitor	Buck Output Capacitor
250kHz	8µH	40µF ceramic capacitor + 100µF E-capacitor	30µF ceramic capacitor + 270µF polymer capacitor
480kHz	4.7µH	40µF ceramic capacitor + 100µF E-capacitor	30µF ceramic cap + 270µF polymer capacitor

ESD Protection for I/O Pins

Higher ESD levels should be considered for all USB I/O pins. The MPQ4253A features high ESD protection up to ±8kV human body model on DP1/DP2, DM1/DM2, USB1, USB2, and ±6kV human body model on CC1, CC2. The

ESD structures can withstand high ESD both in normal operation and when the device is powered off. To further extend the DP and DM pins' ESD level for covering complicated application environments, additional resistors and capacitors can be added (see Figure 13).

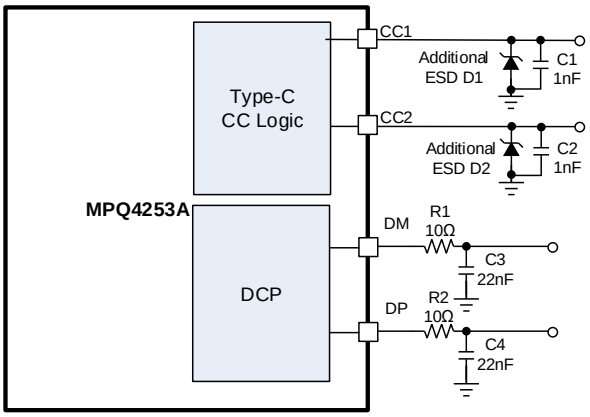


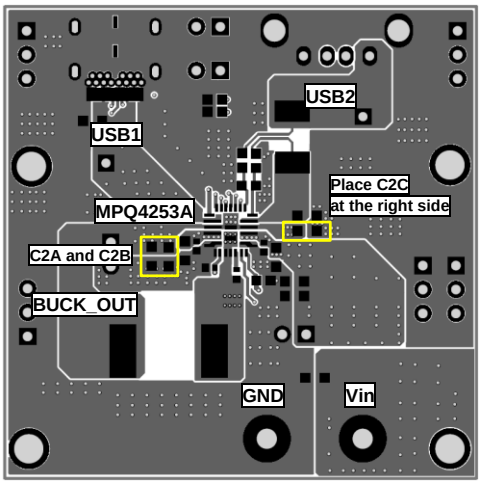
Figure 13: Recommended I/O Pins ESD Enhancing

Similar R-C networks cannot be added on the CC1 and CC2 pins since the CC line must support a 200mA current and 300kHz signaling. Additional ESD diodes can be added on CC.

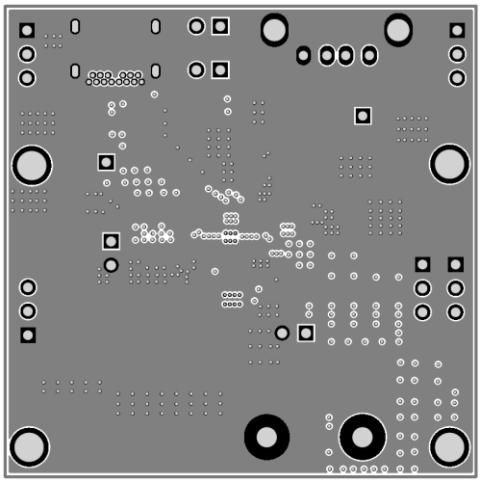
PCB Layout Guidelines (12)

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 14 and follow the guidelines below:

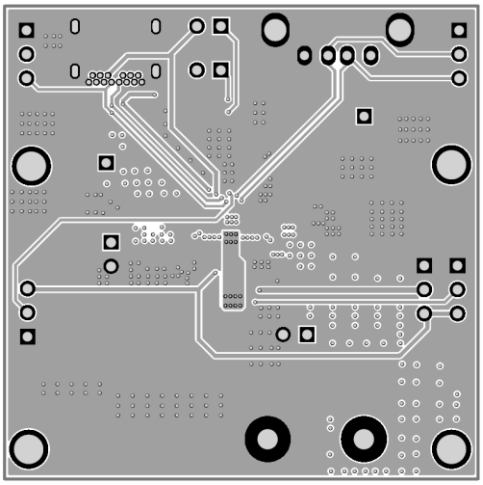
1. Use short, direct, and wide traces to connect OUT.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers.
4. Place buck output ceramic capacitors C2A and C2B on the left side, and C2C on the right side.
5. Use a large copper plane for PGND, SW, USB1, and USB2.
6. Add multiple vias to improve thermal dissipation.
7. Connect AGND to PGND.
8. Route the USB1 and USB2 trace on both PCB layers.
9. Place two ceramic input decoupling capacitors as close as possible to IN and PGND to improve EMI performance.
10. Place the symmetrical C_{IN} capacitors on each side of the IC.
11. Place the BST capacitor close to BST and SW.
12. Place the VCC decoupling capacitor as close to VCC as possible.



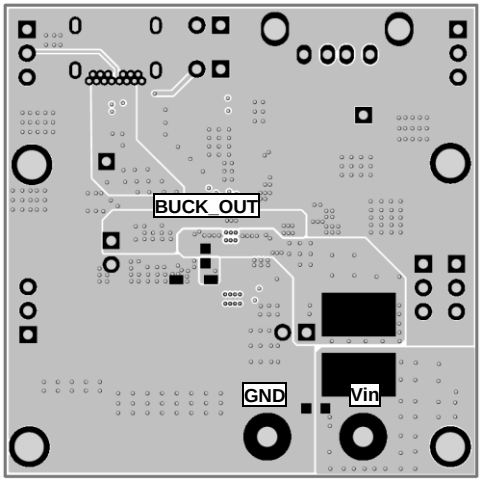
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 14: Recommended Layout

Note:

12) The recommended layout is based on the Typical Application Circuit (see Figure 15).

TYPICAL APPLICATION CIRCUIT

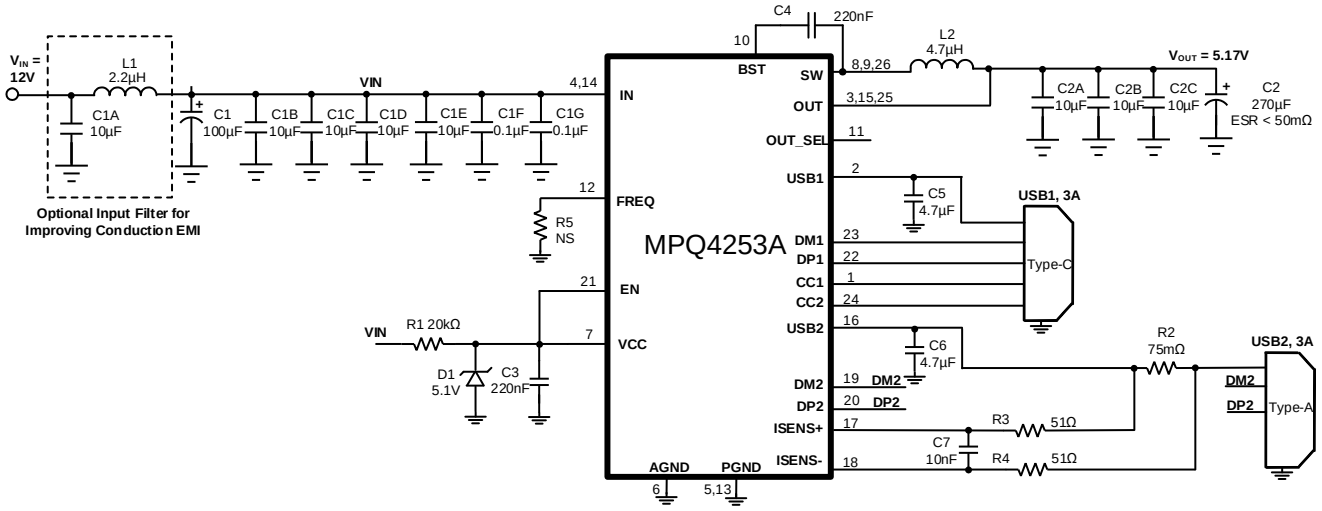


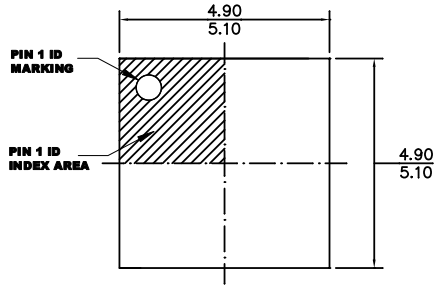
Figure 15: Type-C 5V/3A DFP Port plus Type-A 5V/3A Port Schematic (13)

Note:

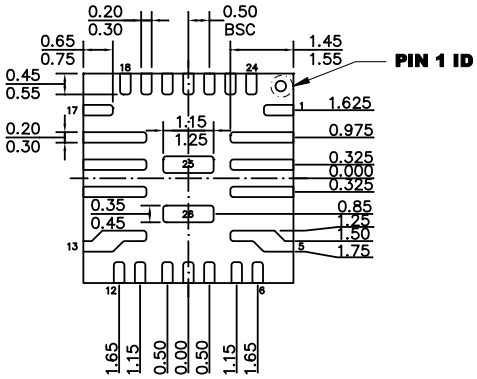
13) See Figure 13 for the I/O pins' ESD protection enhancing details.

PACKAGE INFORMATION

QFN-26 (5mmx5mm)

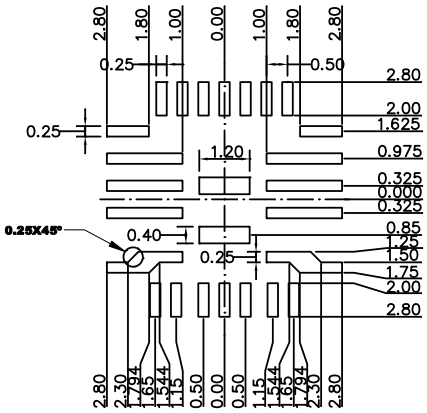


TOP VIEW



BOTTOM VIEW

SIDE VIEW

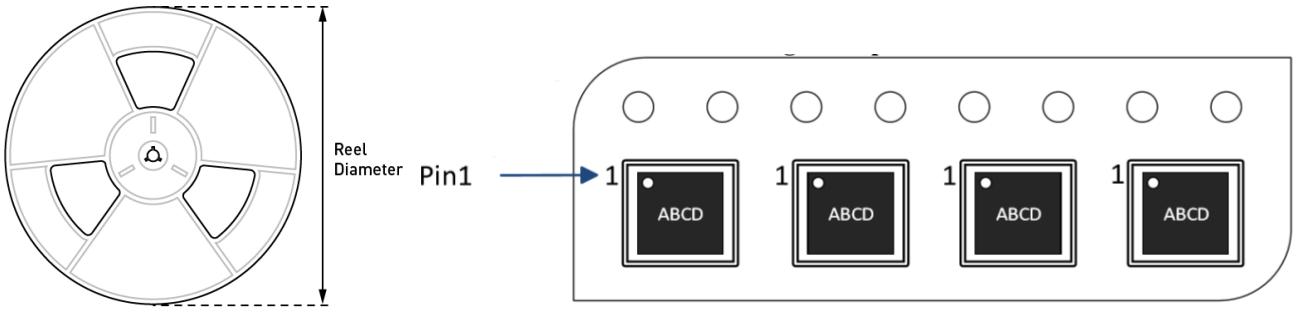


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PINS 2 TO 4 AND 14 TO 16 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN 5 AND PIN 13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) REFERENCEIS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4253AGU-AEC1–Z	QFN-26 (5mmx5mm)	5000	N/A	13in	12mm	8mm