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CONNECTIVITY

Datasheet

Lyra 24P

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	24 May 2023	Initial Release	Robert Gosewehr, Raj Khatri, Dave Drogowski	Jonathan Kaye

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1 INTRODUCTION

The Lyra 24P is a secure, high-performance wireless module optimized for the needs of battery and line powered IoT devices running on Bluetooth networks.

Based on the **Series 2 EFR32BG24 SoC**, it enables Bluetooth® Low Energy connectivity, delivering exceptional RF performance and energy efficiency, industry leading Secure Vault® technology, and future-proofing capabilities.

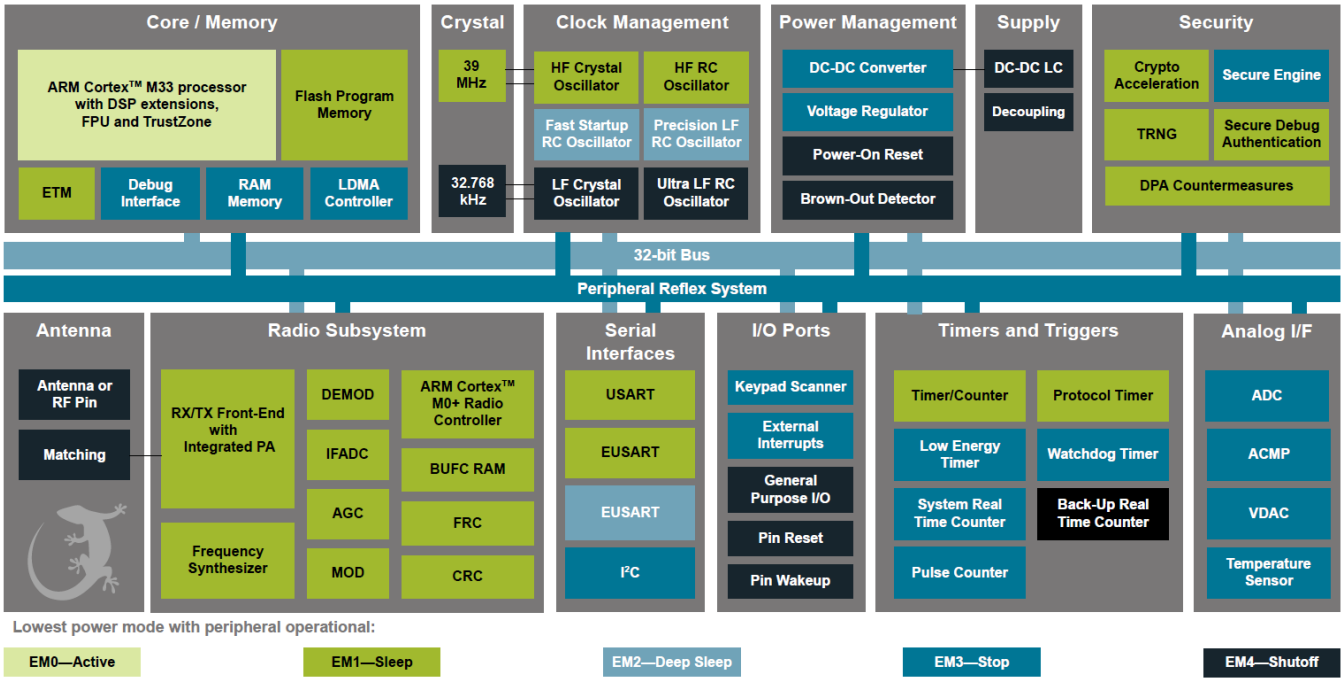
The Lyra 24P is a complete solution offered with robust and fully upgradeable software stacks, global regulatory certifications, advanced development and debugging tools, and documentation that simplifies and minimizes the development cycle of your end-product, helping to accelerate its time-to-market.

The Lyra 24P is intended for a broad range of applications, including:

- Smart Home Devices
- Lighting
- Building Automation and Security
- Gateways and Digital Assistants
- Bluetooth mesh Low Power Node

1.1 Key Features

- Bluetooth Low Energy 5.3
- Bluetooth Mesh connectivity
- Built-in antenna or RF pin
- +10 or +20 dBm TX output power (see Maximum Regulatory Certified RF TX Power per Country)
- -98.5 dBm BLE 1M RX sensitivity
- 32-bit ARM® Cortex®-M33 core at 39 MHz
- 1536/256 kB of Flash/RAM memory
- Vault High or Vault Mid security
- Rich set of analog and digital peripherals
- 26 GPIO pins
- -40 °C to 105 °C
- 12.9 mm x 15.0 mm



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1.2 Hardware Features

- **Supported Protocols**
  - Bluetooth Low Energy (BLE) 5.3
  - Bluetooth Mesh
  - Matter-ready Smart Home Connectivity
- **Wireless System-on-Chip**
  - 2.4 GHz radio
  - TX power up to +20 dBm (see Maximum Regulatory Certified RF TX Power per Country)
  - 32-bit ARM Cortex®-M33 with DSP instruction and floating- point unit for efficient signal processing
  - 1536 kB flash program memory 256 kB RAM data memory
  - Embedded Trace Macrocell (ETM) for advanced debugging
- **Receiver Sensitivity**
  - -106.5 dBm sensitivity (0.1% BER) at 125 kbps GFSK
  - -102.2 dBm sensitivity (0.1% BER) at 500 kbps GFSK
  - -98.5 dBm sensitivity (0.1% BER) at 1 Mbps GFSK
  - -95.7 dBm sensitivity (0.1% BER) at 2 Mbps GFSK
- **Current Consumption**
  - 4.5 mA RX current at 1 Mbps GFSK
  - 4.8 mA TX current at 0 dBm (BGM240Px22)
  - 18.8 mA TX current at 10 dBm (BGM240Px22)
  - 154.8 mA TX current at 19.6 dBm (BGM240Px32)
  - 33.4 µA/MHz in Active Mode (EM0) at 39.0 MHz
  - 1.3 µA EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **Regulatory Certifications**
  - CE (EU)
  - UKCA (UK)
  - FCC (USA)
  - ISED (Canada)
  - MIC (Japan)
  - KC (South Korea)
  - AS/NZ (Australia, New Zealand)
- **Operating Range**
  - 1.8 to 3.8 V
  - -40 to +105°C
- **Dimensions**
  - 12.9 mm x 15.0 mm x 2.15 mm
- **Security**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration with DPA counter-measures for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug Interface lock/unlock Secure Key Management with PUF Anti-Tamper
  - Secure Attestation
- **MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - 2 × Analog Comparator (ACMP)
  - 2 × Digital to Analog Converter (VDAC)
  - Up to 26 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 16 Channel Peripheral Reflex System (PRS)
  - 3 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 2 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 2 x 32-bit Real Time Counter (SYSRTC/BURTC)
  - 24-bit Low Energy Timer for waveform generation (LETIMER)
  - 16-bit Pulse Counter with asynchronous operation (PCNT) 2 × Watchdog Timer (WDOG)
  - 1 × Universal Synchronous/Asynchronous Receiver/Transmitter (USART), supporting UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
  - 2 × Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART) supporting UART/SPI/DALI/ IrDA
  - 2 × I2C interface with SMBus support
  - Low-Frequency RC Oscillator with precision mode to replace 32 kHz sleep crystal (LFRCO)
  - Keypad scanner supporting up to 6x8 matrix (KEYSCAN)
  - Die temperature sensor with ±1.5°C accuracy after single point calibration

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1.3 Firmware Options

The Lyra 24P series supports two different firmware options for software development:

AT Command Set – fully featured and extensible to suit any developer's needs.

- Proven over 5+ years
- Basic Bluetooth LE cable replacement
- Simplest implementation possible

C Code – Full software development with Silicon Labs SDK and Toolchain

- Native C code development
- Use Simplicity Studio IDE
- Full functionality of Silicon Labs HW / SW

2 Ordering Information

Table 1: Ordering Information

Part	Description
453-00142R	Lyra 24P Series - Bluetooth v5.3 PCB Module (10dBm) with integrated antenna (Silicon Labs EFR32BG24) - Tape / Reel
453-00142C	Lyra 24P Series - Bluetooth v5.3 PCB Module (10dBm) with integrated antenna (Silicon Labs EFR32BG24) – Cut / Tape
453-00145R	Lyra 24P Series - Bluetooth v5.3 PCB Module (20dBm) with integrated antenna (Silicon Labs EFR32BG24) - Tape / Reel
453-00145C	Lyra 24P Series - Bluetooth v5.3 PCB Module (20dBm) with integrated antenna (Silicon Labs EFR32BG24) – Cut / Tape
453-00148R	Lyra 24P Series - Bluetooth v5.3 PCB Module (20dBm) with RF Trace Pad (Silicon Labs EFR32BG24) - Tape / Reel
453-00148C	Lyra 24P Series - Bluetooth v5.3 PCB Module (20dBm) with RF Trace Pad (Silicon Labs EFR32BG24) – Cut / Tape
453-00142-K1	Lyra 24P Series - Development Kit - Bluetooth v5.3 PCB Module (10dBm) with integrated antenna
453-00145-K1	Lyra 24P Series - Development Kit - Bluetooth v5.3 PCB Module (20dBm) with integrated antenna
453-00148-K1	Lyra 24P Series - Development Kit - Bluetooth v5.3 PCB Module (20dBm) with RF Trace Pad
450-00184	Lyra 24P Series - Bluetooth v5.3 USB Adapter (20dBm) with integrated antenna (Silicon Labs EFR32BG24)

Note:

1. Lyra 24P series modules operate in the 2.4 GHz ISM frequency band.
2. The maximum RF TX power allowed by different regional regulatory authorities may differ from the maximum output power a module can produce. End-product manufacturers must then verify that the module is configured to meet the regulatory limits for each region in accordance with the local rules and the formal certification test reports.
3. See section Maximum Regulatory Certified RF TX Power per Country per Lyra 24P module part number.
4. Lyra 24P modules are pre-programmed with **Lyra 24P BGAPI UART/OTA DFU** bootloader. Lyra 24P AT firmware can be loaded by the customer (via SWD interface or via boot loader (UART or OTA)). Lyra 24P USB dongle ships with bootloader and AT firmware.

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3 System Overview

3.1 Block Diagram

The Lyra 24P module is a highly-integrated, high-performance system with all the hardware components needed to enable 2.4 GHz wireless connectivity and support robust networking capabilities via multiple wireless protocols.

Built around the **EFR32BG24** Wireless SoC, the Lyra 24P includes a built-in antenna, an RF matching network (optimized for transmit power efficiency), supply decoupling and filtering components, an LC tank for DC-DC conversion, a 39 MHz reference crystal, and an RF shield. Also, it supports the use of an external 32 kHz crystal as a low frequency reference signal via GPIO pins for use cases demanding maximum energy efficiency.

For designs where an external antenna solution may be beneficial, a module variant with a 50 Ω-matched RF pin instead of the built-in antenna is available (**for Lyra 24P, RF, 20dBm, RF Trace only**).

Because the RF matching network is optimized for transmit power efficiency, modules rated for +20 dBm will show non-optimal current consumption and performance when operated at a lower output power (i.e. +10 or 0 dBm).

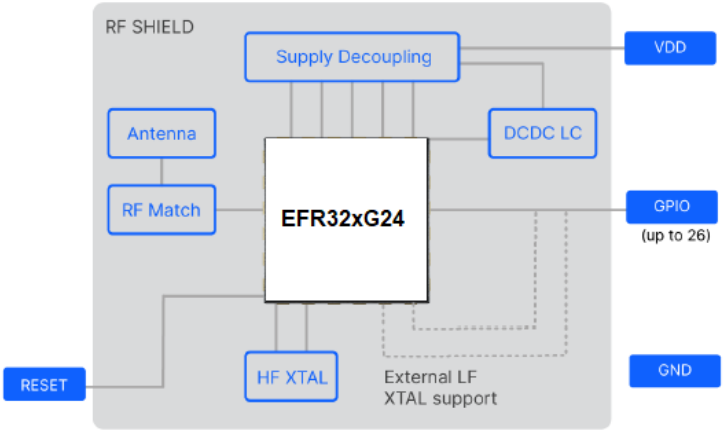

Figure 1: Lyra 24P Block Diagram – Built-in Antenna Variant

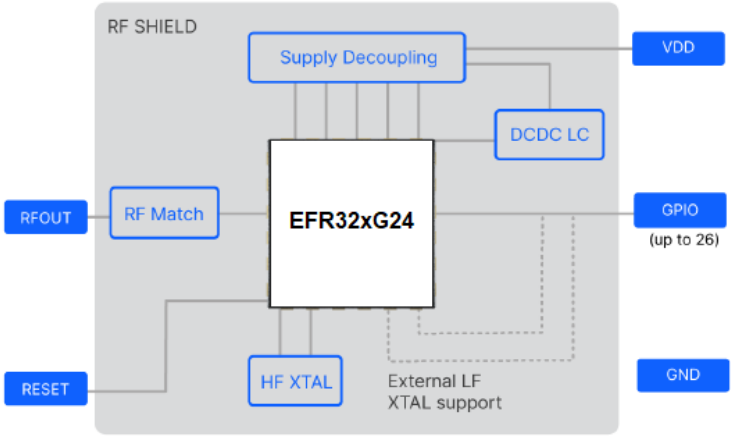

Figure 2: Lyra 24P Block Diagram – RF Pin Variant

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A simplified internal schematic for the Lyra 24P module is shown in Figure 3.

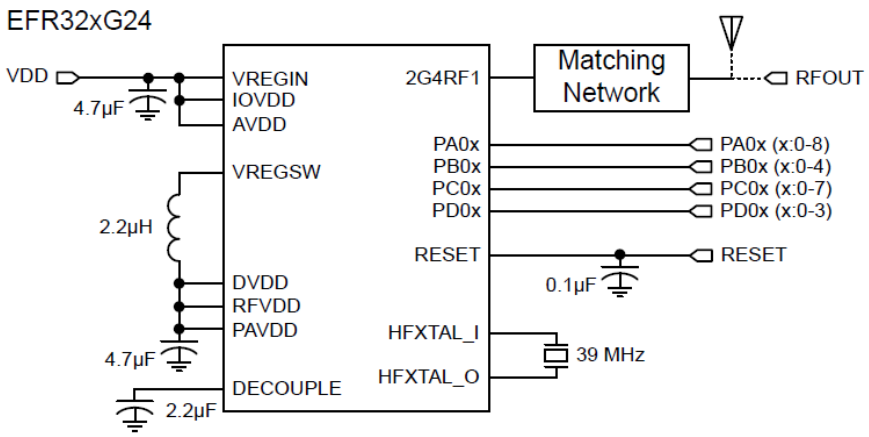

Figure 3: Lyra 24P Module Schematic

3.2 EFR32BG24 SoC

The **EFR32BG24** SoC features a 32-bit ARM Cortex M33 core, a 2.4 GHz high-performance radio, 1536 kB of Flash memory, 256 kB of RAM, a dedicated core for security, a rich set of MCU peripherals, and various clock management and serial interfacing options. See the EFR32xG24 Reference Manual and EFR32BG24 Data Sheet for details.

3.3 Integrated Antenna

Lyra 24P modules come with two antenna solutions variants: A built-in antenna or a 50 Ohms matched RF pin to support an external antenna. Typical performance characteristics of the built-in antenna are detailed in table below.

Table 2: Integrated Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 dB	Antenna efficiency, gain, and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Design Guidelines for recommendations to achieve optimal antenna performance.
Peak gain	1.82 dBi	

3.4 External Antenna

Lyra 24P module can be used with external antennas (certified by Laird Connectivity) and requires a RF 50 Ohm track (Ground Coplanar Waveguide) to be designed to run from Lyra 24P module RFOUT (pin 33) to an RF antenna connector (IPEX MHF 4) on the host PCB. The 50 ohm RF track design and length **MUST** be copied as defined in section Lyra 24P Module 50 Ohms RF Track Design for Connecting External Antenna with the Lyra 24P Module, 20dBm, RF Pad Variant (453-00148)**Error! Reference source not found.**.

The list of supported external antennas (certified by Laird Connectivity) are listed in section External Antenna Integration with the Lyra 24P Module.

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3.5 Power Supply

The Lyra 24P requires a single nominal supply level (VDD) to operate and supports an operating range of 1.8 to 3.8 V. The nominal level needed for **+10 dBm devices** (part number: 453-00142) **is 3.0 V** whereas **+20 dBm devices** (part number: 453-00145 and 453-00148) **require 3.3 V** in order to achieve higher TX output power. All necessary decoupling, filtering and DC-DC-related components are included in the module.

Note: The power amplifier for +10 dBm modules is supplied through an internal LDO, and thus is independent of the VDD supply. Respectively, the power amplifier for +20 dBm modules is supplied through the VDD pin with a target level of 3.3 V.

3.6 General Purpose Input / Output (GPIO)

The Lyra 24P has up to 26 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in Table 19: GPIO Alternate Function Table.

3.7 Security

Lyra 24P modules support one of two levels in the Security Portfolio offered by Silicon Labs: **Secure Vault Mid** or **Secure Vault High**. Lyra 24P modules support Secure Vault High.

Secure Vault is a collection of technologies that deliver state-of-the-art security and upgradability features to protect and futureproof IoT devices against costly threats, attacks, and tampering. A dedicated security CPU enables the Secure Vault functions and isolates cryptographic functions and data from the Cortex-M33 core. Lyra 24P part numbers support Secure Vault High.

Table 3: Secure Vault Features

Feature	Secure Vault Mid	Secure Vault High
True Random Number Generator (TRNG)	Yes	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes	Yes
Secure Debug with Lock/Unlock	Yes	Yes
DPA Countermeasures	Yes	Yes
Anti-Tamper		Yes
Secure Attestation		Yes
Secure Key Management		Yes

Symmetric Encryption	• AES 128 / 192 / 256 bit
	  • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC
		• AES 128 / 192 / 256 bit
		  • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC
		• ChaCha20

Public Key Encryption - ECDSA / ECDH / EdDSA	• p192 and p256	• p192, p256, p384 and p521 • Curve25519 (ECDH) • Ed25519 (EdDSA)
Key Derivation	• ECJ-PAKE p192 and p256	• ECJ-PAKE p192, p256, p384, and p521

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Feature	Secure Vault Mid	Secure Vault High
		• PBKDF2 • HKDF
Hashes	• SHA-1 • SHA-2/256	• SHA-1 • SHA-2 256, 384, and 512 • Poly1305

3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates. For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations, and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192, P-256, P-384, and P-521 for ECDH (Elliptic Curve Diffie-Hellman) key derivation, and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling) and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.7.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.
The **TRNG** is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.7.4 Secure Debug with Lock / Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, Secure Vault High also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end- user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

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3.7.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.7.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.7.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, eight external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

3.7.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

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4 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on **T_A=25 °C** and **VDD supply at 3.0 V**, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

4.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+105	°C
Voltage on VDD supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on VDD supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V/µs
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{VDD}+0.3	V
DC voltage on RESETn pin[1]	V_{RESETn}		-0.3	—	3.8	V
Absolute voltage on RFOUT pin	V_{MAX2G4}		-0.3	—	V_{VDD}+0.3	V
Total current into VDD pin	I_{VDDMAX}	Source	—	—	200	mA
Total current into GND pin	I_{GNDMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. The RESETn pin has a pull-up device to the internal DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

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4.2 General Operating Conditions

Table 5: General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A		-40	—	+105	°C
VDD operating supply voltage	V_{VDD}	10 dBm Module, DC-DC in regulation	2.2	3.0	3.8	V
		20 dBm Module, DC-DC in regulation	2.2	3.3	3.8	V
		10 dBm Module, DC-DC in bypass	1.8	3.0	3.8	V
		20 dBm Module, DC-DC in bypass	1.8	3.3	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	78	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2 or VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
EM01 Group C clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency	f_{RHCLK}	VSCALE2 or VSCALE1	—	39.0	—	MHz

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4.3 MCU Current Consumption with 3 V Supply

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. **Voltage scaling level = VSCALE1. T_A = 25 °C.** Minimum and maximum values in this table represent the worst conditions across process variation at **T_A = 25 °C**.

Table 6: MCU Current Consumption with 3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	33.3	—	µA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	32.8	—	µA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	49.1	—	µA/MHz
		39 MHz crystal, CPU running Prime from flash	—	33.9	—	µA/MHz
		39 MHz crystal, CPU running while loop from flash	—	33.4	—	µA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	49.4	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	28.1	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	22.6	—	µA/MHz
		39 MHz crystal	—	24.4	—	µA/MHz
		38 MHz HFRCO	—	19.0	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	256 kB RAM and full Radio RAM retention, RTC running from LFXO[1]	—	2.9	—	µA
		256 kB RAM and full Radio RAM retention, RTC running from LFRCO[1]	—	2.9	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO[1]	—	1.3	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO[1]	—	1.3	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO in precision mode[1]	—	1.9	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	256 kB RAM and full Radio RAM retention, RTC running from ULFRCO[1]	—	2.7	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO[1]	—	1.1	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, No LF Oscillator	—	0.27	—	µA
		BURTC with LXO	—	0.64	—	µA

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption during reset	I_{RST}	Hard pin reset held	—	467	—	µA

Note:

1. CPU cache retained, EM0/EM1 peripheral states retained.

4.4 Radio Current Consumption with 3 V Supply

RF current consumption measured with MCU in EM1 and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. **T_A = 25 °C**.

Table 7: Radio Current Consumption with 3.0 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception, VSCALE1, EM1P	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	4.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	4.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	4.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	5.2	—	mA
Current consumption in receive mode, listening for packet, VSCALE1, EM1P	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	4.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	4.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	4.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	5.2	—	mA
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm output power	—	4.8	—	mA
		f = 2.4 GHz, CW, +10 dBm output power	—	18.8	—	mA
		f = 2.4 GHz, CW, +20 dBm output power, VDD = 3.3 V[1]	—	154.8	—	mA

Note:

1. Maximum output power for Bluetooth Low Energy is limited to 19.6 dBm for compliance with the Bluetooth Core Specifications.

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4.5 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. RF center frequency **2.45 GHz. T_A=25°C**.

Table 8: RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition (Output Power)	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2402	—	2480	MHz
Maximum TX power	$POUT_{MAX}$	0 dBm	—	-0.3	—	dBm
		+10 dBm	—	10	—	dBm
		+20 dBm, VDD = 3.3 V[1]	—	19.6	—	dBm
Minimum active TX Power	$POUT_{MIN}$	0 dBm	—	-24	—	dBm
		+10 dBm	—	-30	—	dBm
		+20 dBm, VDD = 3.3 V	—	-33.7	—	dBm
Output power step size	$POUT_{STEP}$	0 dBm	0.1	0.7	9.9	dBm
		+10 dBm, -5 dBm < Output power < 0 dBm	0.6	1.1	1.8	dBm
		+10 dBm, 0 dBm < Output power < 10 dBm	0.1	0.3	0.8	dBm
		+20 dBm, VDD = 3.3 V, Output power < 0 dBm	0.9	3.6	14.4	dBm
		+20 dBm, 0 dBm < Output power < 20 dBm	0.1	0.2	1.3	dBm
Output power variation vs VDD supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	0 dBm with VDD voltage swept from 1.8 V to 3.8 V	—	0.01	—	dB
		+10 dBm with VDD voltage swept from 1.8 V to 3.8 V	—	0.05	—	dB
		+20 dBm with VDD voltage swept from 1.8 V to 3.8 V	—	5.4	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR\_T}$	0 dBm, (-40 to +105 °C)	—	1.0	—	dB
		+10 dBm, (-40 to +105 °C)	—	0.3	—	dB
		+20 dBm, VDD = 3.3 V, (-40 to +105 °C)	—	0.2	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	0 dBm	—	0.2	—	dB
		+10 dBm	—	0.2	—	dB
		+20 dBm, VDD = 3.3 V	—	0.2	—	dB

Note:

1. Maximum output power for Bluetooth Low Energy is limited to 19.6 dBm for compliance with the Bluetooth Core Specifications.

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4.6 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. RF center frequency **2.45 GHz. T_A = 25°C**.

Table 9: RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2402	—	2480	MHz

4.7 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. RF center frequency **2.45 GHz**. **T_A = 25 °C.**

Table 10: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	+10 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-98.5	—	dBm
		+10 dBm Module, Signal is reference signal, 255 byte payload[1]	—	-96.9	—	dBm
		+10 dBm Module, With non-ideal signals[2 1]	—	-96.5	—	dBm
		+20 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-97.6	—	dBm
		+20 dBm Module, Signal is reference signal, 255 byte payload[1]	—	-96	—	dBm
		+20 dBm Module, With non-ideal signals[2 1]	—	-95.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	8.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 3 4 5]	—	-5.4	—	dB
		Interferer is reference signal at -1 MHz offset[1 3 4 5]	—	-5.3	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 3 4 5]	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset[1 3 4 5]	—	-39.7	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 3 4 5]	—	-45.5	—	dB
		Interferer is reference signal at -3 MHz offset[1 3 4 5]	—	-45.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-23.3	—	dB
Selectivity to		Interferer is reference signal at image	—	-40.9	—	dB

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
image frequency ± 1 MHz	C/I_{IM_1}	frequency +1 MHz with 1 MHz precision[1 5]				
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-5.4	—	dB
Intermodulation performance	IM	n = 3 (see note[6])	—	-17.3	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -67 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. RF center frequency **2.45 GHz. T_A = 25 °C**.

Table 11: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	+10 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-95.7	—	dBm
		+10 dBm Module, Signal is reference signal, 255 byte payload[1]	—	-94.2	—	dBm
		+10 dBm Module, With non-ideal signals[2 1]	—	-93.9	—	dBm
		+20 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-94.8	—	dBm
		+20 dBm Module, Signal is reference signal, 255 byte payload[1]	—	-93.3	—	dBm
		+20 dBm Module, With non-ideal signals[2 1]	—	-93.1	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	8.6	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1 5 4 3]	—	-5.3	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 3]	—	-5.8	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1 5 4 3]	—	-42.2	—	dB
		Interferer is reference signal at -4 MHz offset[1 5 4 3]	—	-44.2	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1 5 4 3]	—	-48.1	—	dB
		Interferer is reference signal at -6 MHz offset[1 5 4 3]	—	-50.2	—	dB

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-22.8	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1 5]	—	-42.2	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1 5]	—	-5.3	—	dB
Intermodulation performance	IM	n = 3 (see note[6])	—	-18.3	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -64 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.
6. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. RF center frequency **2.45 GHz. T_A = 25 °C**.

Table 12: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	+10 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-102.2	—	dBm
		+10 dBm Module, Signal is reference signal, 255 byte payload[1]	—	-101	—	dBm
		+10 dBm Module, With non-ideal signals[2 1]	—	-100	—	dBm
		+20 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-101.4	—	dBm
		+20 dBm Module, Signal is reference signal, 255 byte payload[1]	—	-100	—	dBm
		+20 dBm Module, With non-ideal signals[2 1]	—	-99	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	2.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 3 4 5]	—	-7.1	—	dB
		Interferer is reference signal at -1 MHz offset[1 3 4 5]	—	-7.4	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 3 4 5]	—	-46.8	—	dB
		Interferer is reference signal at -2 MHz offset[1 3]	—	-49.7	—	dB

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		4 5				
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 3 4 5]	—	-49.4	—	dB
		Interferer is reference signal at -3 MHz offset[1 3 4 5]	—	-54.5	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-49	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-49.4	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-46.8	—	dB

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -72 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

4.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: **VDD = 3.0 V, DC-DC in regulation**. RF center frequency **2.45 GHz. T_A = 25 °C**.

Table 13: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	+10 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-106.5	—	dBm
		+10 dBm Module, Signal is reference signal, 255 byte payload[1]	—	-106.1	—	dBm
		+10 dBm Module, With non-ideal signals[2 1]	—	-105.7	—	dBm
		+20 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-105.6	—	dBm
		+20 dBm Module, Signal is reference signal, 255 byte payload[1]	—	-105.3	—	dBm
		+20 dBm Module, With non-ideal signals[2 1]	—	-104.8	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 3]	—	0.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 3 4 5]	—	-12.4	—	dB
		Interferer is reference signal at -1	—	-12.8	—	dB

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		MHz offset[1 3 4 5]				
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 3 4 5]	—	-52.6	—	dB
		Interferer is reference signal at -2 MHz offset[1 3 4 5]	—	-55.5	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 3 4 5]	—	-53.8	—	dB
		Interferer is reference signal at -3 MHz offset[1 3 4 5]	—	-60.0	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 5]	—	-53.0	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 5]	—	-53.8	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 5]	—	-52.6	—	dB

Note:

1. 0.017% Bit Error Rate.
2. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
3. Desired signal -79 dBm.
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
5. With allowed exceptions.

4.11 High-Frequency Crystal

Table 14: High-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	39	—	MHz
Initial calibrated accuracy	ACC_{HFXTAL}		-10	±5	10	ppm
Temperature drift	$DRIFT_{HFXTAL}$	Across specified temperature range	-20	—	20	ppm

4.12 Low-Frequency Crystal Oscillator

Table 15: Low-Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kOhms
		GAIN = 1 to 3	—	—	100	kOhms
Supported range of crystal load capacitance[1]	CL_{LFXO}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note2)	10	—	12.5	pF

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
		GAIN = 3 (see note2)	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kΩ, CL = 12.5pF, GAIN[3] = 2, AGC[4] = 1	—	294	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kΩ, CL = 7pF, GAIN[3] = 1, AGC[4] = 1	—	52	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE=0	—	5.2	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE=0x4F	—	26.2	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap, and the two caps will be seen in series by the crystal

4.13Precision Low Frequency RC Oscillator (LFRCO)

Table 16: Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	204	—	µs
		Precision mode[1]	—	11.7	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	189.9	—	nA
		Precision mode1, T = stable at 25°C [3]	—	649.8	—	nA

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ±40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.14GPIO Pins

Table 17: GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, VDD = 3.0 V	—	2.5	—	nA

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3*VDD	V
		RESETn	—	—	0.3*DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7*VDD	—	—	V
		RESETn	0.7*DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*VDD	—	—	V
		RESETn	0.05*DVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, VDD = 3.0 V	—	—	0.2*VDD	V
Output high voltage	V_{OH}	Sourcing 20mA, VDD = 3.0 V	0.8*VDD	—	—	V
GPIO rise time	T_{GPIO_RISE}	VDD = 3.0V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
GPIO fall time	T_{GPIO_FALL}	VDD = 3.0V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
Pull up/down resistance[2]	R_{PULL}	GPIO pull-up to VDD: MODEn = DISABLE, DOUT=1. GPIO pull-down to GND: MODEn = WIREDORPULLDOWN, DOUT = 0.	35	44	55	kΩ
		RESETn pin pull-up to DVDD.	35	44		kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:

1. GPIO input thresholds are proportional to the VDD pin. RESETn input thresholds are proportional to the internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.
2. GPIO pull-ups connect to VDD supply, pull-downs connect to GND. RESETn pull-up connects to internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

4.15 Microcontroller Peripherals

The MCU peripherals set available in Lyra 24P modules includes:

- ADC: 12-bit at 1 Msps, 16-bit at 76.9 ksps
- 16-bit and 32-bit Timers/Counters
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- USART (UART/SPI/SmartCards/IrDA/I2S)
- EUSART (UART/IrDA)
- I^2C peripheral interfaces
- 12 Channel Peripheral Reflex System

For details on their electrical performance and to learn which GPIO ports provide access to every peripheral, consult the relevant portions of Section 4 and Section 6 in the SoC datasheet, see EFR32BG24 SoC section for datasheet link.

To learn which GPIO ports provide access to every peripheral, consult Analog Peripheral Connectivity and Digital Peripheral Connectivity sections.

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4.16 Antenna Radiation and Efficiency for Lyra 24P Integrated Antenna

Typical performance curves indicate typical characterized performance under the stated conditions.

Typical Lyra 24P radiation patterns and efficiency for the integrated antenna under optimal operating conditions are plotted in the figures that follow. Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna.

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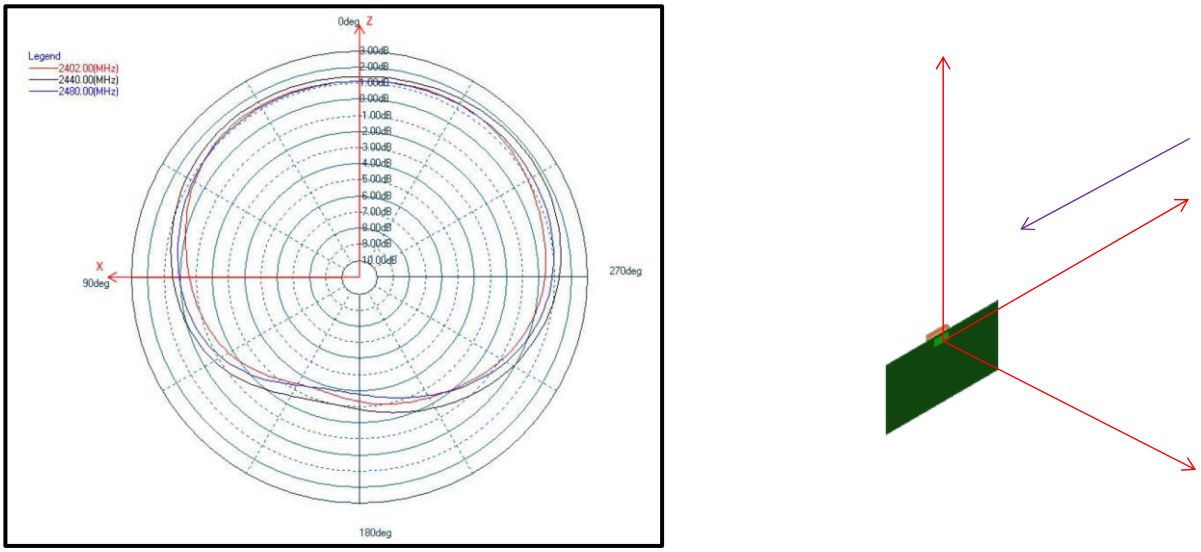

Figure 4: Lyra 24P Integrated Antenna Module Typical 2D Antenna Radiation Patterns - Phi 0º (Side View) Gain dBi

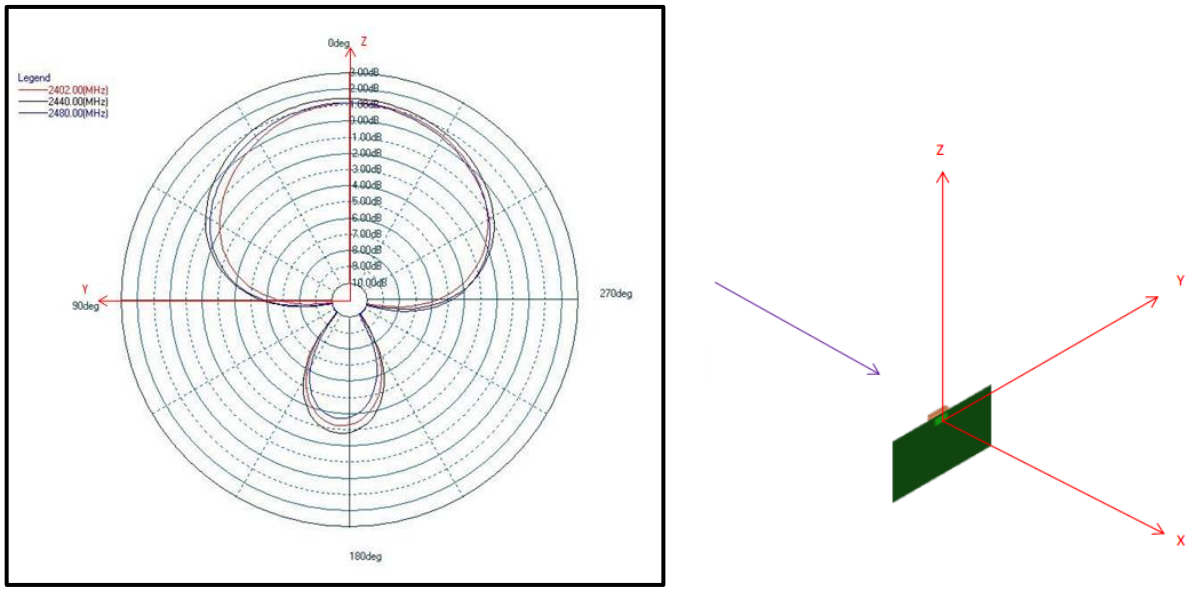

Figure 5: Lyra 24P Integrated Antenna Module Typical 2D Antenna Radiation Patterns - Phi 90º (Top View) Gain dBi

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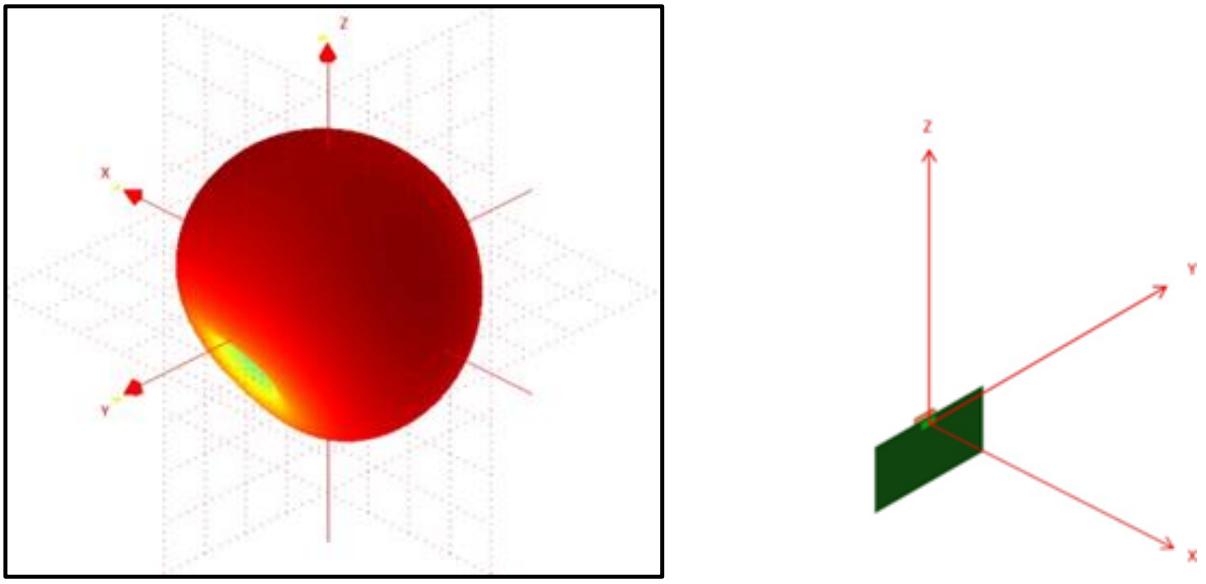

Figure 6: Lyra 24P Integrated Antenna Module Typical 2D Antenna Radiation Patterns - 3D Radiation Pattern at 2440 MHz

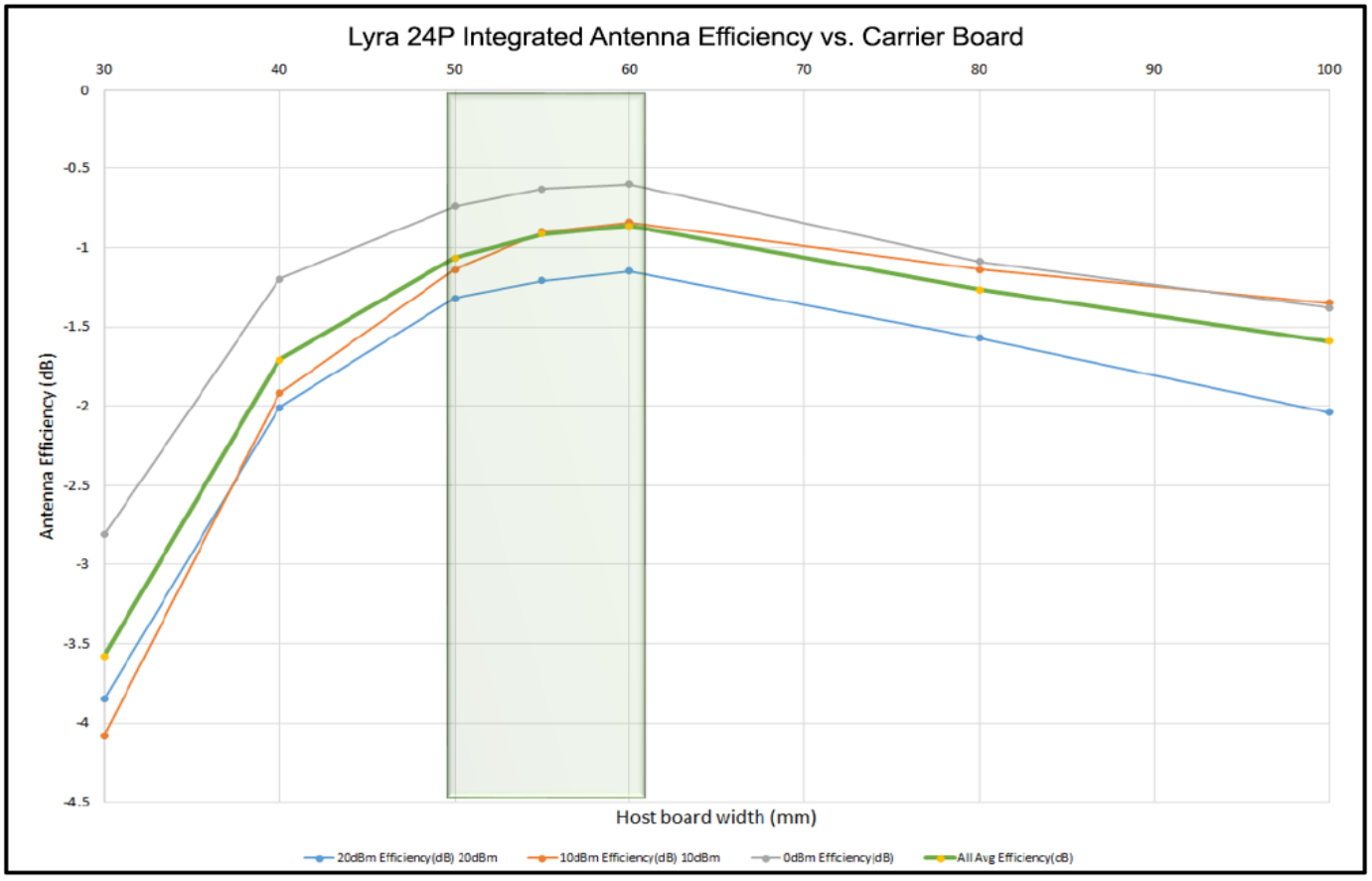

Figure 7: Radiation efficiency of the Built-in Antenna as Function of the Carrier Board Width(mm)

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5 Reference Diagrams

5.1 Network Co-Processor (NCP) Application with UART Host

The Lyra 24P can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below. For more details, see AN958: Debugging and Programming Interfaces for Custom Designs.

Note: For boot pin, see section 5.3**Error! Reference source not found.Error! Reference source not found.**.

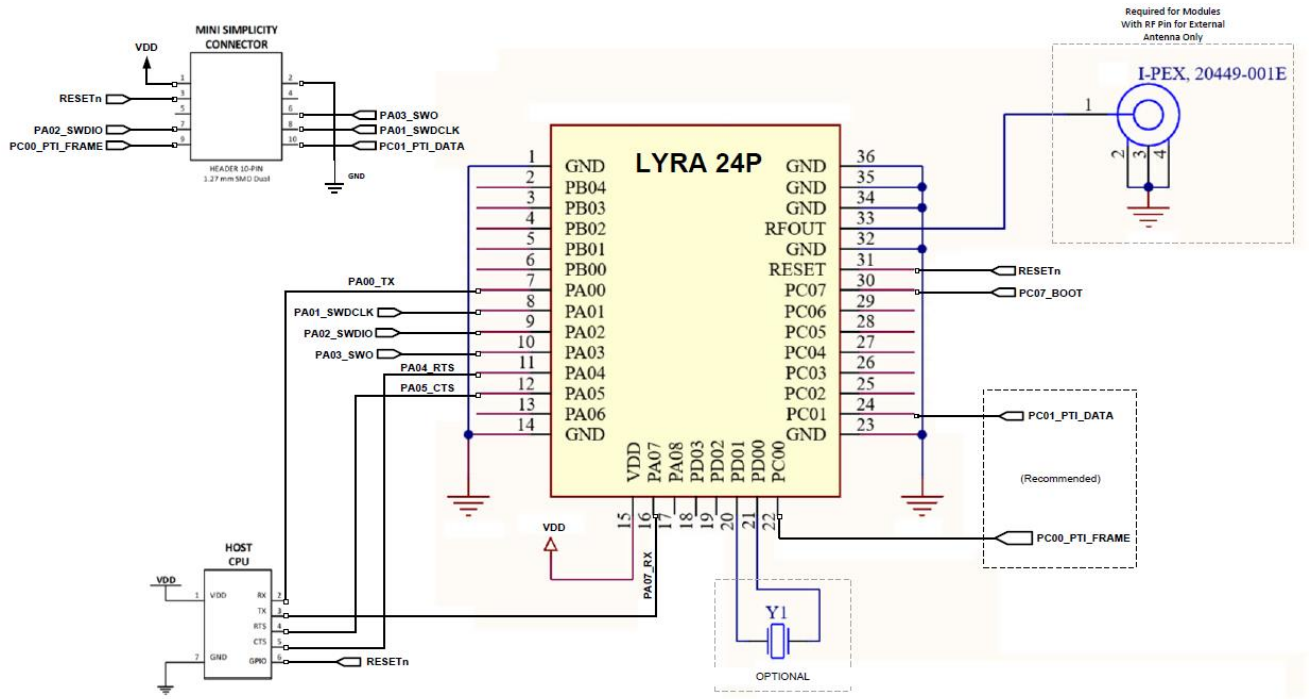

Figure 8: UART NCP Configuration (External Antenna MHF4 RF connector only required for 453-00148 Lyra 24P, RF trace pad variant module)

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5.2 SoC Application

The Lyra 24P can be used in a stand-alone SoC configuration without an external host processor. Typical power supply and programming/debug interface connections are shown in the figure below. For more details, see AN958: Debugging and Programming Interfaces for Custom Designs.

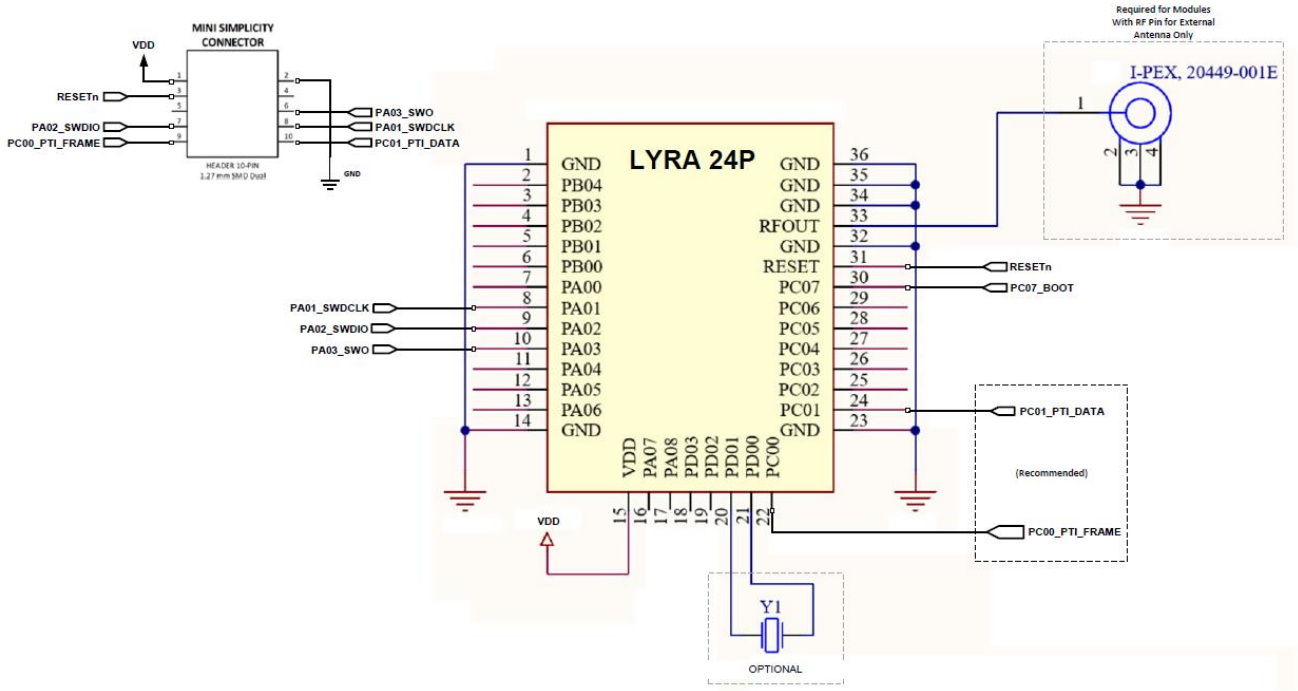

Figure 9: Stand-Alone SoC Configuration (External Antenna MHF4 RF connector only required for 453-00148 Lyra 24P, RF trace pad variant module)

5.3 Boot

The **BOOT pin is used to determine when execution of the bootloader is required**. Upon reset, execution of the bootloader begins. The **state of the BOOT pin is read immediately upon start-up of the bootloader**. If LOW, execution of the bootloader continues, facilitating firmware update via the UART. If the BOOT pin is HIGH, the bootloader will stop execution and pass control to the main application firmware.

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6 Pin Definitions

6.1 Lyra 24P 36-Pin PCB Module Pinout

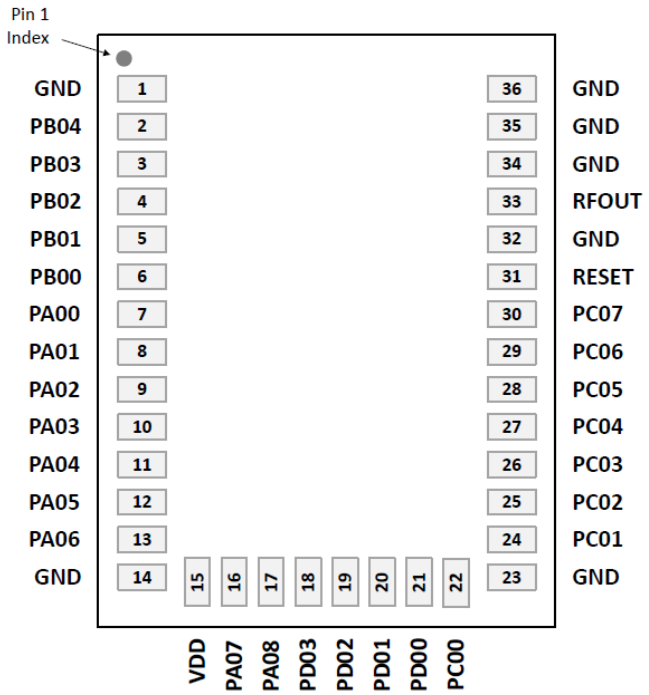

Figure 10: Lyra 24P 36-Pin PCB Module With LF Crystal Device Pinout

For GPIO pin to peripheral assignment in AT firmware, see User Guide – AT Interface Application – Lyra 24 Series.

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see Table 19: GPIO Alternate Function Table, Analog Peripheral Connectivity, and Digital Peripheral Connectivity.

Table 18: Lyra 24P Module Pin Definitions

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
GND	1	Ground	PB04	2	GPIO
PB03	3	GPIO	PB02	4	GPIO
PB01	5	GPIO	PB00	6	GPIO
PA00	7	GPIO	PA01	8	GPIO
PA02	9	GPIO	PA03	10	GPIO
PA04	11	GPIO	PA05	12	GPIO
PA06	13	GPIO	GND	14	GND
VDD	15	Power Supply	PA07	16	GPIO
PA08	17	GPIO	PD03	18	GPIO
PD02	19	GPIO	PD01	20	GPIO / LF XTAL Input (Optional)
PD00	21	GPIO / LF XTAL Output (Optional)	PC00	22	GPIO
GND	23	GPIO	PC01	24	GPIO

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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC02	25	GPIO	PC03	26	GPIO
PC04	27	GPIO	PC05	28	GPIO
PC06	29	GPIO	PC07	30	GPIO
RESETn	31	Reset Pin. The RESETn pin is pulled up to an internal DVDD supply. An external pull-up is not recommended. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. The RESETn pin can be left unconnected if no external reset switch or source is used.	GND	32	GND
RFOUT	33	RF Input/Output (External Ant.)	GND	34	GND
GND	35	GND	GND	36	GND

6.2 Alternate Function Table

Some GPIOs support alternate functions like debugging, wake-up from EM4, external low frequency crystal access, etc.. The following table shows which module pins have alternate capabilities and the functions they support. Refer to the SoC's reference manual for more details.

Table 19: GPIO Alternate Function Table

GPIO	Alternate Function		
PA00	IADC0.VREFP		
PA01	GPIO.SWCLK		
PA02	GPIO.SWDIO		
PA03	GPIO.SWV	GPIO.TDO	GPIO.TRACEDATA0
PA04	GPIO.TDI	GPIO.TRACECLK	
PA05	GPIO.TRACEDATA1	GPIO.EM4WU0	
PA06	GPIO.TRACEDATA2		
PA07	GPIO.TRACEDATA3		
PB00	VDAC0.VDAC_CH0_MAIN_OUTPUT		
PB01	GPIO.EM4WU3	VDAC0.VDAC_CH_MAIN_OUTPUT	
PB02	VDAC1.VDAC_CH0_MAIN_OUTPUT		
PB03	GPIO.EM4WU4	VDAC1.VDAC_CH1_MAIN_OUTPUT	
PC00	GPIO.EM4WU6		
PC01	GPIO.EFP_TX_SDA		
PC02	GPIO.EFP_TX_SCL		
PC05	GPIO.EFP_INT	GPIO.EM4WU7	
PC07	GPIO.EM4WU8	GPIO.THMSW_EN	GPIO.THMSW_HALFSWITCH
PD00	LFXO.LFXTAL_O		
PD01	LFXO.LFXTAL_I	LFXO.LF_EXTCLK	
PD02	GPIO.EM4WU9		

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6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. **When a differential connection is being used, positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins**. When a single ended connection is being used positive input is available on all pins. See the SoC's Reference Manual for more details on the ABUS and analog peripherals, EFR32BG24 SoC.

Table 20: ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC0	VDAC_CH0_ABUS_OUTPUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VDAC_CH1_ABUS_OUTPUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC1	VDAC_CH0_ABUS_OUTPUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VDAC_CH1_ABUS_OUTPUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

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6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

Table 21: DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT			Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1	Available	Available		
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available	Available	Available
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX			Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT	Available	Available		
HFXO0.BUFOUT_REQ_IN_ASYNC	Available	Available	Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA			Available	Available
I2C1.SCL			Available	Available
I2C1.SDA	Available	Available	Available	Available
KEYSCAN.COL_OUT_0	Available	Available	Available	Available
KEYSCAN.COL_OUT_1	Available	Available	Available	Available
KEYSCAN.COL_OUT_2	Available	Available	Available	Available
KEYSCAN.COL_OUT_3	Available	Available	Available	Available
KEYSCAN.COL_OUT_4				
KEYSCAN.COL_OUT_5	Available	Available	Available	Available
KEYSCAN.COL_OUT_6	Available	Available	Available	Available
KEYSCAN.COL_OUT_7	Available	Available	Available	Available
KEYSCAN.ROW_SENSE_0	Available	Available		
KEYSCAN.ROW_SENSE_1	Available	Available		

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Peripheral.Resource	PORT			
	PA	PB	PC	PD
KEYSCAN.ROW_SENSE_2	Available	Available		
KEYSCAN.ROW_SENSE_3	Available	Available		
KEYSCAN.ROW_SENSE_4	Available	Available		
KEYSCAN.ROW_SENSE_5	Available	Available		
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH12	Available	Available		
PRS.ASYNCH13	Available	Available		
PRS.ASYNCH14	Available	Available		
PRS.ASYNCH15	Available	Available		
PRS.SYNCH0	Available	Available	Available	Available

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Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
RAC.LNAEN	Available	Available	Available	Available
RAC.PAEN	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available

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7 Design Guidelines

7.1 Layout and Placement

For optimal performance of the Lyra 24P:

Place the module aligned to the edge of the application PCB, as illustrated in the figures below.

- Optional on the module with the RF pin.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB if you are going to use the built-in antenna.
- Antenna clearance area is not necessary if you are using an external antenna attached to the RF pin.
- RFOUT can be left floating if not used.

Antennas external to the module, either connectorized off-the-shelf antennas or PCB trace antennas, must be well-matched to 50 Ω.

- For external antenna use cases, use a 50 Ω grounded coplanar transmission line to trace the signal from the RF pin to an external MHF4 RF connector if applicable (see Figure 12).
- A general rule is to use 50 Ω transmission lines where the length of the RF trace is longer than λ/16 at the fundamental frequency, which for 2.4 GHz is approximately 3.5 mm.
- An IPEX MHF4 RF connector can be used in the host PCB for the connection to an external antenna. The use of a MHF4 connector is also recommended for conductive tests. The integrator must use a unique connector, such as a “reverse polarity SMA” or “reverse thread SMA”, if detachable antenna is offered with the host chassis. This is especially required for the FCC and ISED approvals to remain valid, and any other kind of direct connector to the antenna might require a permissive change.
- A trace length of 1.84 mm was used in the certifications host board to connect the module RF pin to the MHF4 RF connector.
- For reference, **Error! Reference source not found.**Figure 16 shows a set of parameters for a 50 Ω trace. Trace impedance should always be matched to the particular stack-up used on the host board.

Connect all ground pads directly to a solid ground plane.

Place the ground vias as close to the ground pads as possible.

Avoid plastic or any other dielectric material in contact with the antenna.

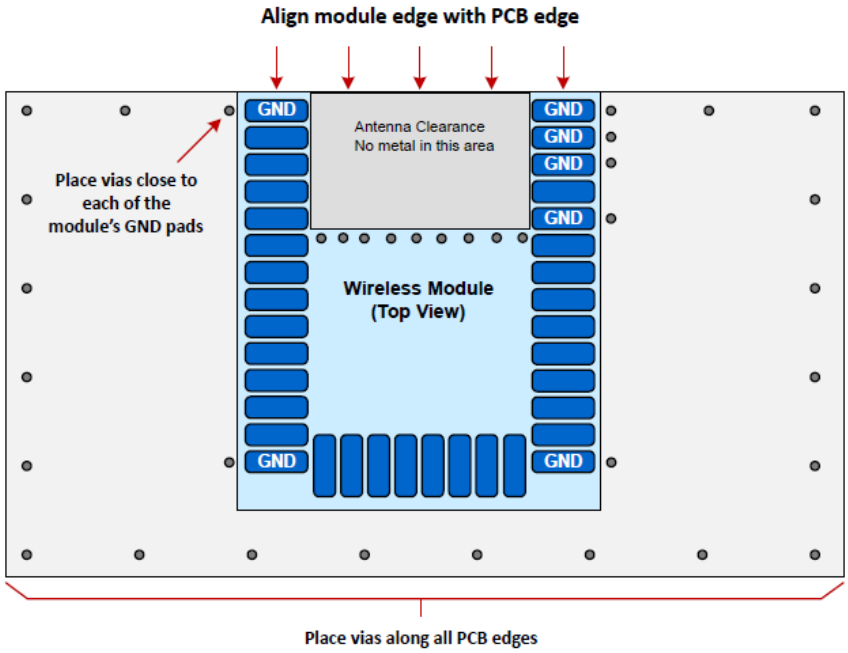

Figure 11: Recommended Layout for Lyra 24P Using Built-in Antenna

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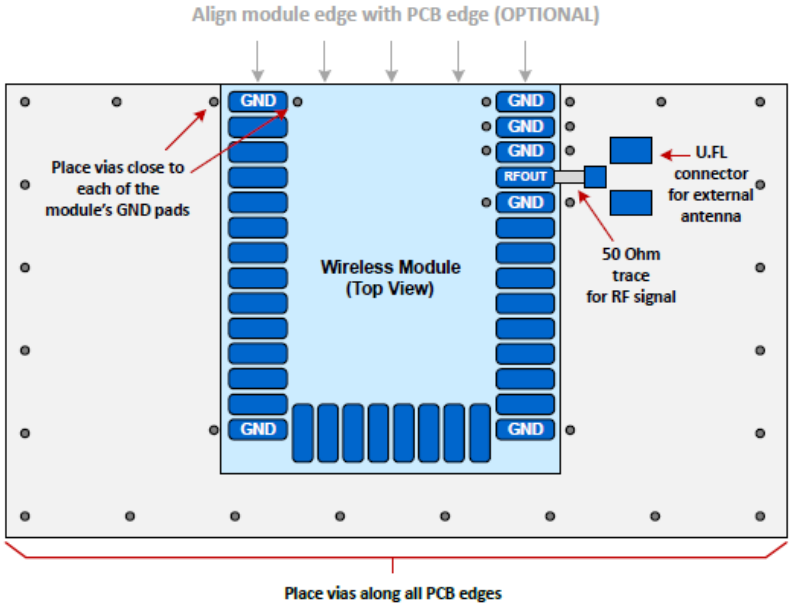

Figure 12: Recommended Layout for Lyra 24P Using External Antenna

The figure below illustrates layout scenarios that will lead to severely degraded RF performance for the module.

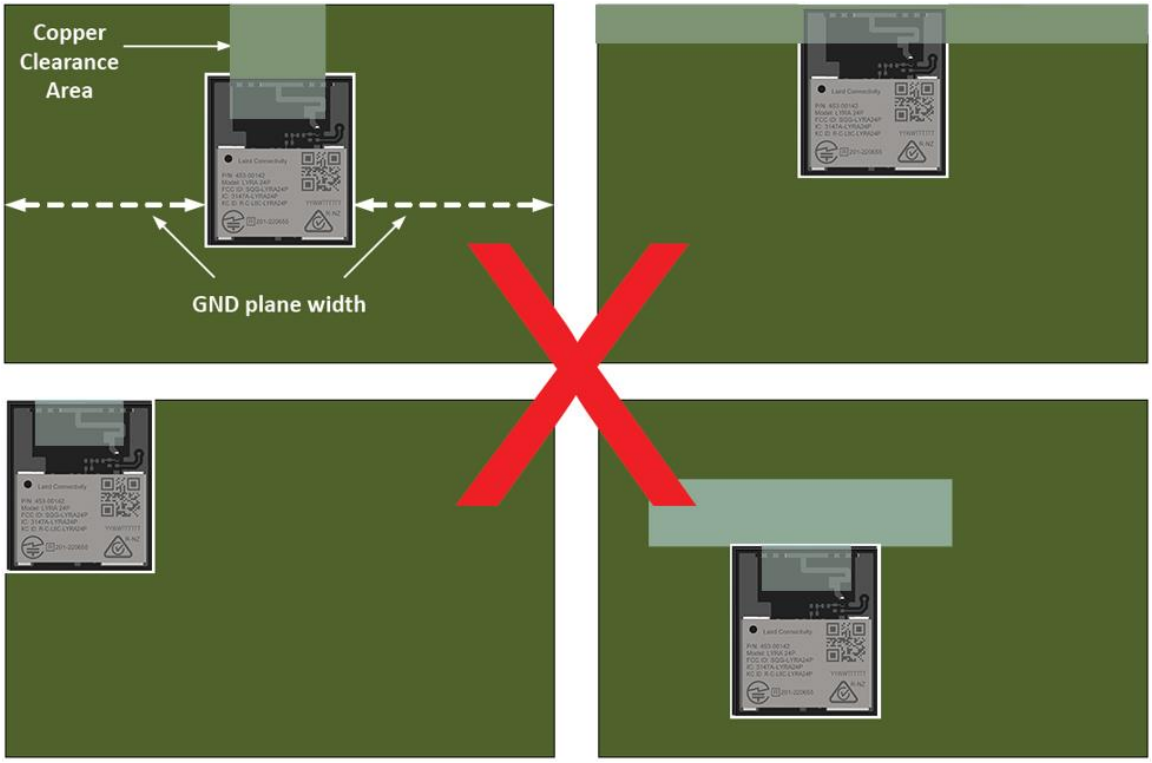

Figure 13: Non-optimal layout examples

The width of the GND plane to the sides the module will impact the efficiency of the built in antenna. **To achieve optimal performance, a GND plane width of 55-60 mm is recommended**. See Antenna Radiation and Efficiency**Error! Reference source not found.** for reference.

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7.2 Proximity to Other Materials

Avoid plastic or any other dielectric material in close contact with the antenna. Conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region, but this will also negatively impact antenna efficiency and reduce range.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

7.3 Proximity to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

7.4 Reset

The Lyra 24P can be reset by pulling the RESET line low, by the internal watchdog timer, or by software command. The reset state does not provide power saving functionality and it is not recommended as a means to conserve power.

7.5 Debug

The Lyra 24P supports hardware debugging via 4-pin JTAG or 2-pin serial-wire debug (SWD) interfaces. **It is recommended to expose the debug pins in your own hardware design for firmware update and debug purposes**. The table below lists the required pins for JTAG and SWD debug interfacing, which are also presented in Section Alternate Function Table.

If JTAG interfacing is enabled, the module must be power cycled to return to a SWD debug configuration if necessary.

Table 22: Debug Pins

Pin Name	JTAG Signal	SWD Signal	Comments
PA04	TDI	N/A	This pin is disabled after reset. Once enabled the pin has a built-in pull-up.
PA03	TDO	N/A	This pin is disabled after reset.
PA02	TMS	SWDIO	Pin is enabled after reset and has a built-in pull-up.
PA01	TCK	SWCLK	Pin is enabled after reset and has a built-in pull-down.

7.6 Packet Trace Interface (PTI)

The Lyra 24P integrates a true PHY-level packet trace interface (PTI) peripheral that can capture packets non-intrusively to monitor and log device and network traffic without burdening processing resources in the module's SoC. The PTI generates two output signals that can serve as a powerful debugging tool, especially in conjunction with other hardware and software development tools available from Silicon Labs. The **PTI_DATA** and **PTI_FRAME** signals can be accessed through any GPIO on ports C and D (see **FRC.DOUT** and **FRC.DFRAME** peripheral resources in Pin Definitions.

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7.7 Lyra 24P Module 50 Ohms RF Track Design for Connecting External Antenna with the Lyra 24P Module, 20dBm, RF Pad Variant (453-00148)

Lyra 24P module can be used with external antennas (certified by Laird Connectivity), and requires a 50 Ohm RF trace (GCPW, that Grounded Coplanar Waveguide) to be designed to run from Lyra 24P module RFOUT (pin33) to a RF antenna connector (IPEX MHF4) on host PCB. The **50 Ohms RF track design and length MUST be copied** (as specified in this section). Lyra 24P module GND pin32 and GND pin34 used to support GCPW 50Ohm RF trace.

Checklist for SCH

Lyra 24P External antenna connection SCH	Lyra 24P External antenna connection PCB

1. Fit IPEX MHF4 RF connector (20449-001E)

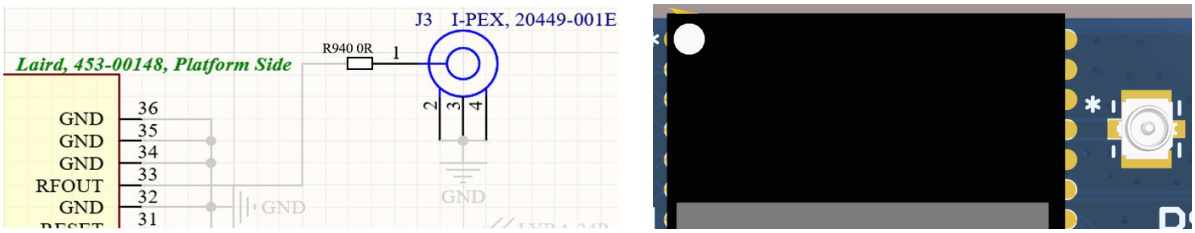
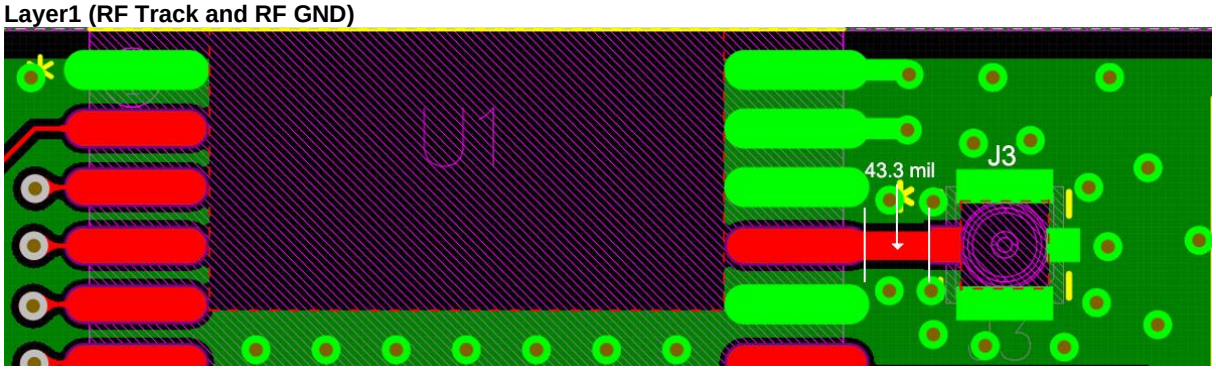


Figure 14: Lyra 24P for External antenna connection host PCB 50-Ohm RF trace schematic with MHF4 RF connector

Layer1 (RF Track and RF GND)



Layer2 (RF GND)

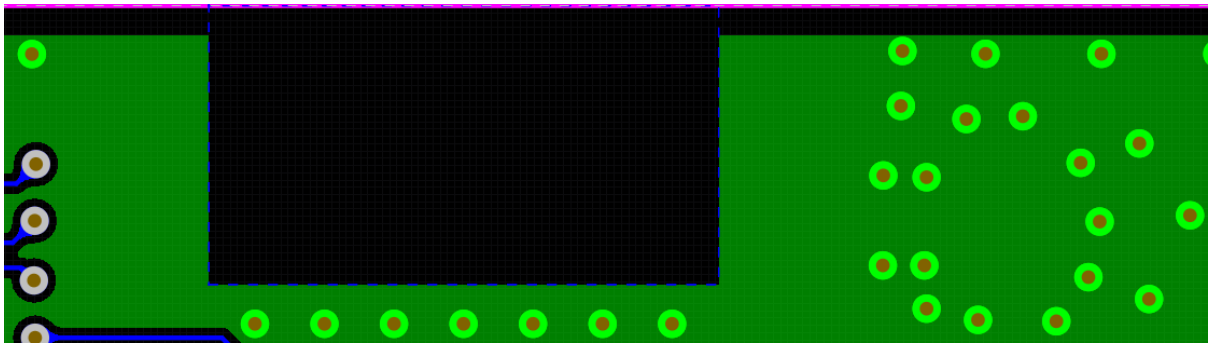


Figure 15: 50-Ohm RF trace design (Layer1 and Layer2) on DVK-Lyra 24P development board 453-00148-K1 (or host PCB) for use with Lyra 24P (453-00148) module

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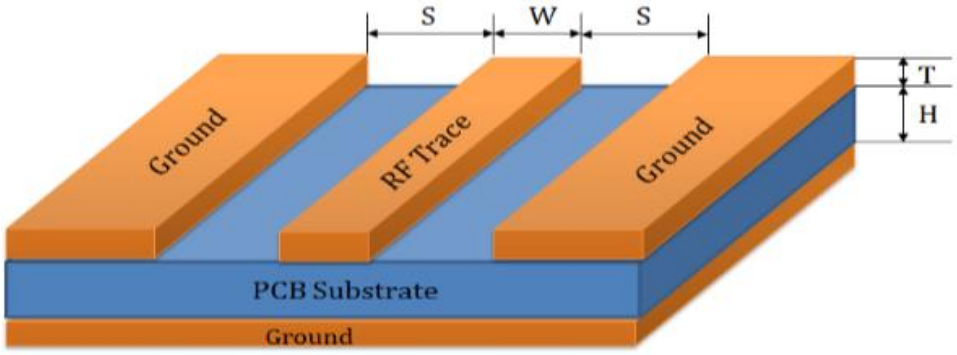
Checklist for PCB:

▪ MUST use a 50-Ohm RF trace (GCPW, that is Grounded Coplanar Waveguide) from RFOUT pad (pin33) of the Lyra 24P module (453-00148) to RF antenna connector (IPEX MHF4 Receptable (MPN: 20449-001E)) on host PCB.

▪ To ensure regulatory compliance, MUST follow exactly the following considerations for 50-Ohms RF trace design and test verification:



	Thickness		Dielectric	
	mil	mm	Constant Er	
Solder Mask	1.0	0.025	3.5	Stack up for 50 Ohms GCPW RF Track.
Layer1 Copper 1oz+plating	1.5	0.038		
Core	57.60	1.463	4.2	
Layer2 Copper 1oz+plating	1.5	0.038		
Solder Mask	1.0	0.025	3.5	
Total	62.6	1.59		

Figure 16: Lyra 24P development board PCB stack-up and 50-Ohms Grounded CPW RF trace design using GND on L1 and L2

Note 1: The plating (ENIG) above base 1ounce copper is not listed, but plating expected to be ENIG.

- The 50-Ohms RF trace design MUST be Grounded Coplanar Waveguide (GCPW) with
  - Layer1 RF track width (W) of 20 mil and
  - Layer1 gap (S) to GND of 5 mil and where the
  - Layer1 to Layer 2 dielectric thickness (H) MUST be 57.6 mil (dielectric constant Er 4.2).
  - Further the Layer1 base copper must be 1-ounce base copper (that is 1.5 mil) plus the plating and
  - Layer1 MUST be covered by solder mask of 1.0 mil thickness (dielectric constant Er 3.5).
- The 50-Ohms RF trace design MUST follow the PCB stack-up shown in Figure 16. (Layer1 to Layer2 thickness MUST be identical to the Lyra 24P development board).
- The 50-Ohms RF track should be a controlled-impedance trace e.g., ±10%.
- The 50-Ohms RF trace length MUST be identical (as seen in Figure 15) (43.3mil) to that on the Lyra 24P development board from Lyra 24P module RFOUT RF pad (pin33) to the RF connector IPEX MHF4 Receptable (MPN: 20449-001E).
- Place GND vias regularly spaced either side of 50-Ohms RF trace to form GCPW (Grounded coplanar waveguide) transmission line as shown in Figure 15 and use Lyra 24P module GND pin32, GND pin34.
- Use spectrum analyzer to confirm the radiated (and conducted) signal is within the certification limit.

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7.8 External Antenna Integration with the Lyra 24P Module, 20dBm, RF pad variant (453-00148)

Please refer to the Lyra 24P Regulatory Information Guide (coming soon) for details on using Lyra 24P module with external antennas in each regulatory region. This guide will be available at:

www.lairdconnect.com/lyra24-series

The Lyra 24P has been designed to operate with the below external antennas (with a maximum gain of 2.0dBi). The required antenna impedance is 50 ohms. See Table 23. External antennas improve radiation efficiency.

Table 23 : External antennas for the Lyra 24P

Manufacturer	Model	Laird Connectivity Part Number	Weight	Dimensions	Type	Connector	Peak Gain	
							2400-2500 MHz	2400-2480 MHz
Laird Connectivity	NanoBlue	EBL2400A1-10MH4L		44.45mm x 12.7mm x 0.81 mm	PCB Dipole	IPEX MHF4	2 dBi	-
Laird Connectivity	FlexPIFA	001-0022	1.13g	40.1mm x 11.0mm x 2.5mm	PIFA	IPEX MHF4	-	2 dBi
Mag Layers	EDA-8709-2G4C1-B27-CY	0600-00057	NA	NA	Dipole	IPEX MHF4	2 dBi	-
Laird Connectivity	mFlexPIFA	EFA2400A3S-10MH4L	1.8g	25.4 mm × 23.4 mm × 2.5 mm	PIFA	IPEX MHF4	-	2 dBi

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8 MECHANICAL SPECIFICATIONS

8.1 Dimensions (Lyra 24P series modules)

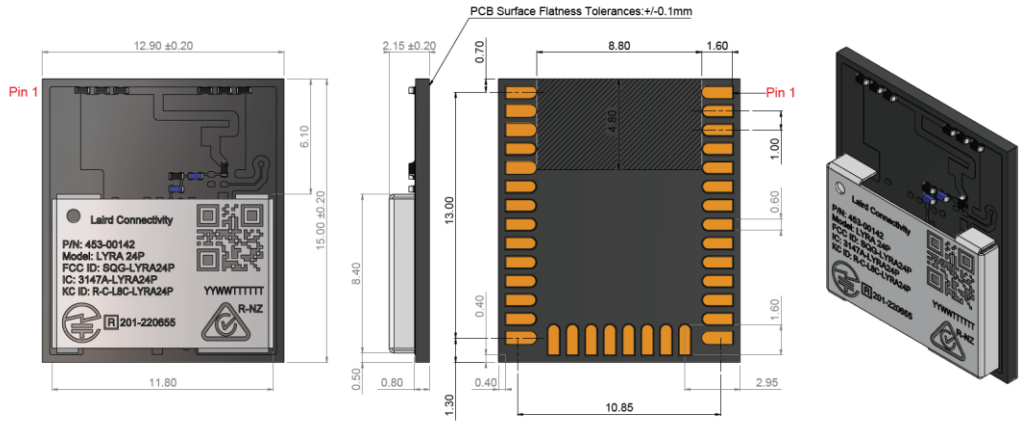

Figure 17: LYRA 24P +10 dBm Module dimensions (mm)

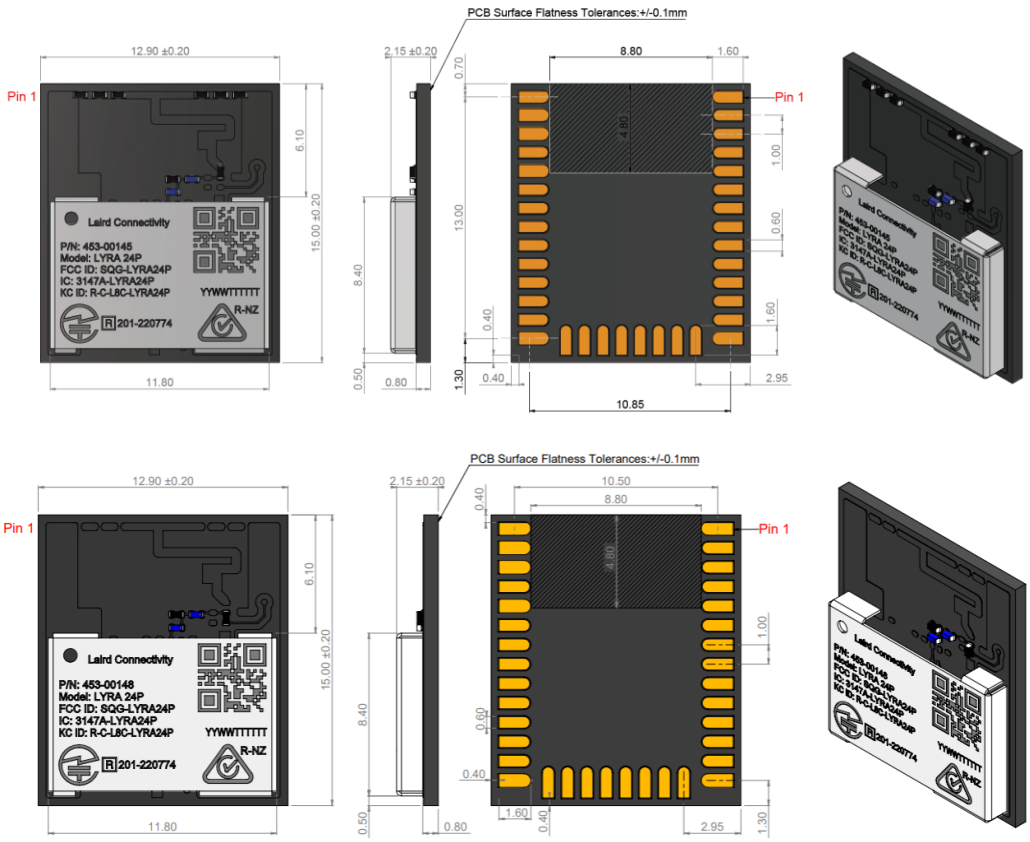

Figure 18: LYRA 24P +20 dBm Module, Integrated Antenna (453-00145) and LYRA 24P +20 dBm Module, RF Trace pad variant (453-00148) dimensions (mm)

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8.2 PCB Land Pattern (Lyra 24P series modules)

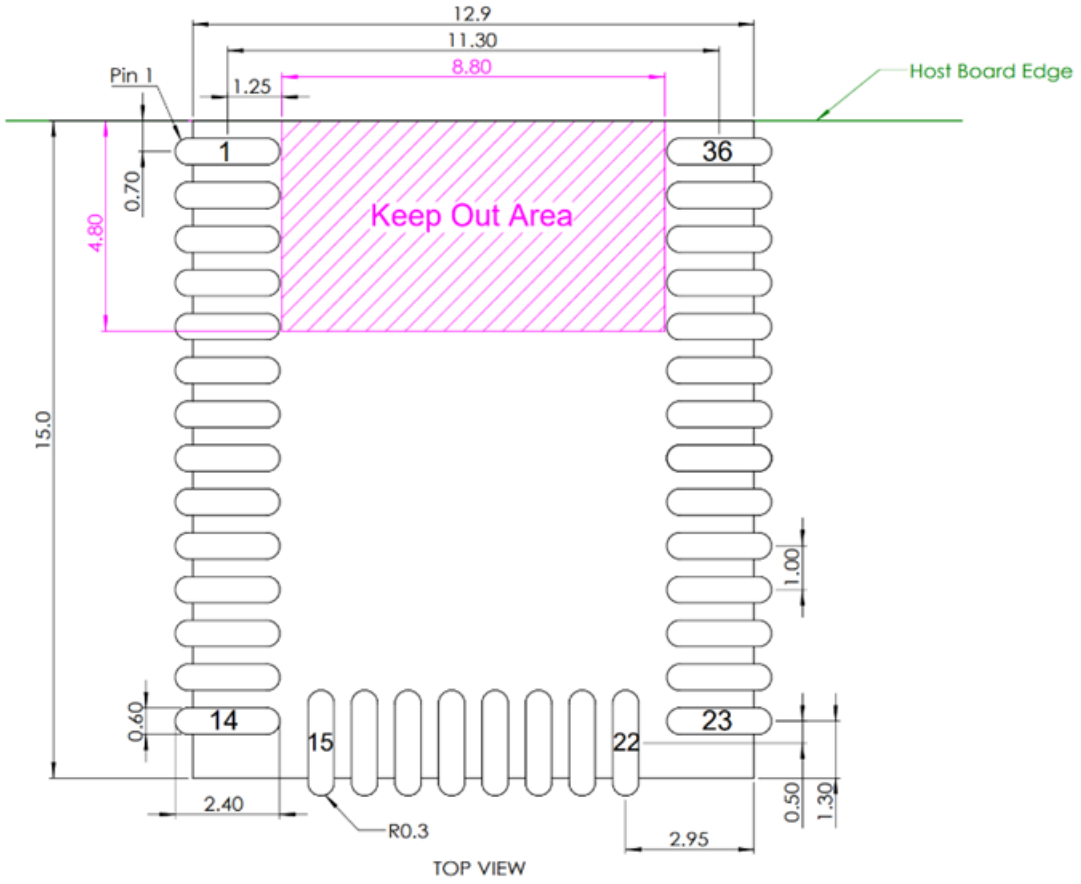

Figure 19: PCB land pattern

Note: For modules with RF pin, the antenna keep out zone in the PCB land pattern above should be omitted.

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8.3 Dimensions for 450-00184 Lyra 24P – Bluetooth v5.3 USB Adaptor (20dBm) with Integrated Antenna (Silicon Labs EFR32BG24)

The Lyra 24P USB dongle User Guide is available on the Lyra 24 Series product page:

https://www.lairdconnect.com/lyra24-series

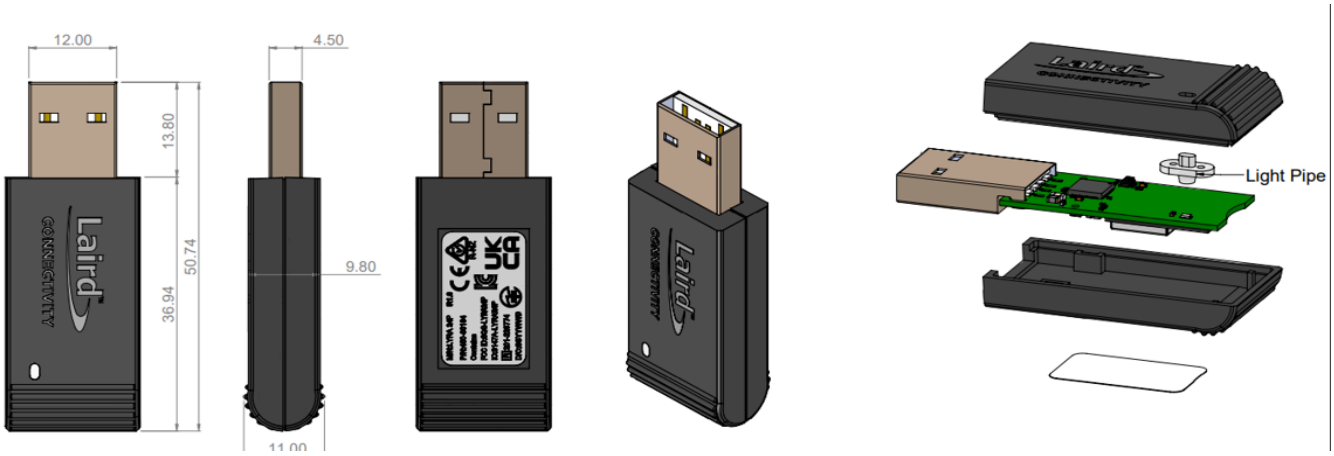

Figure 20: Lyra 24P USB Module - Dimensions

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8.4 Lyra 24P Series Module Label Marking

The figure below shows the module markings engraved on the RF shield.

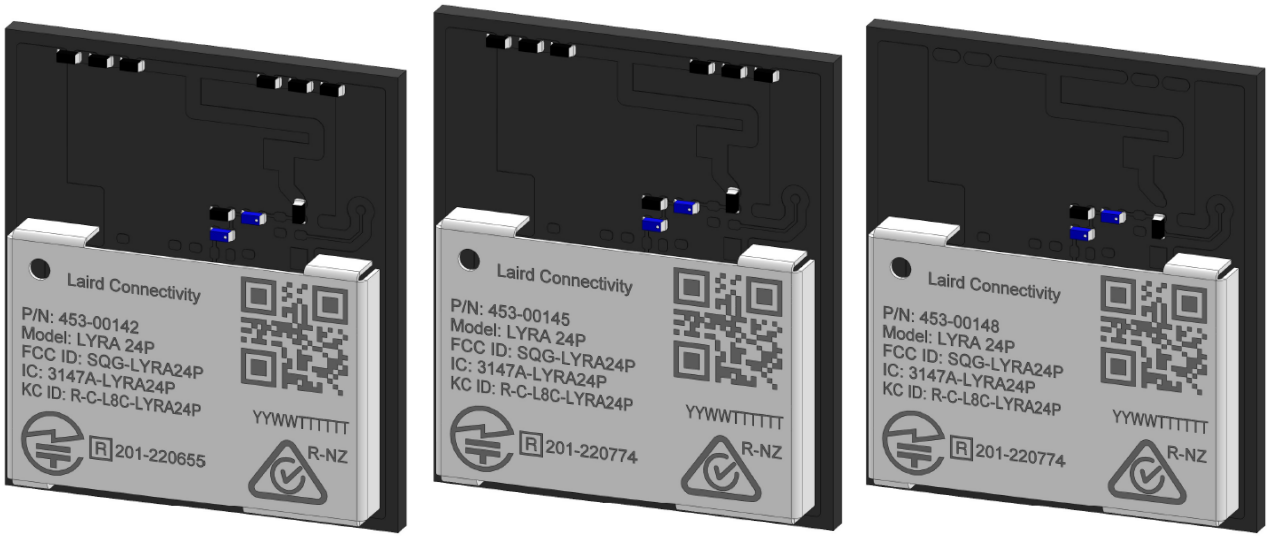

Figure 21: Lyra 24P Top Marking – +10dBm (Integrated antenna), +20 dBm (integrated antenna) and +20 dBm (RF pad) Modules Shown

Mark Description

The package marking consists of:

- P/N - Part number designation
- Model: Lyra 24P Model number designation
- QR Code: YYWWTTTTTT
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - TTTTTT – Manufacturing trace code. The first two letters are the ID of the manufacturer followed by 4 digits of trace code.
- Date code: YYWWTTTTTT
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - TTTTTT – Manufacturing trace code. The first two letters are the ID of the manufacturer followed by 4 digits of trace code.
- Certification marks such as the CE logo, FCC, and IC IDs, etc as per above image.

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8.5 Lyra 24P USB Adapter Label Marking

Figure 22: Lyra 24P USB Adapter Label Marking

Mark Description

The package marking consists of:

- P/N - Part number designation
- Model: Lyra 24P Model number designation
- Date Code: YYWWTTTTTT
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - TTTTTT – Manufacturing trace code. The first two letters are the ID of the manufacturer followed by 4 digits of trace code.
- Certification marks such as the CE logo, FCC, and IC IDs, etc as per above image.

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9 SOLDERING RECOMMENDATIONS

9.1 Reflow for lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier's recommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poor solderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

9.2 Recommended Reflow Profile for lead Free Solder Paste

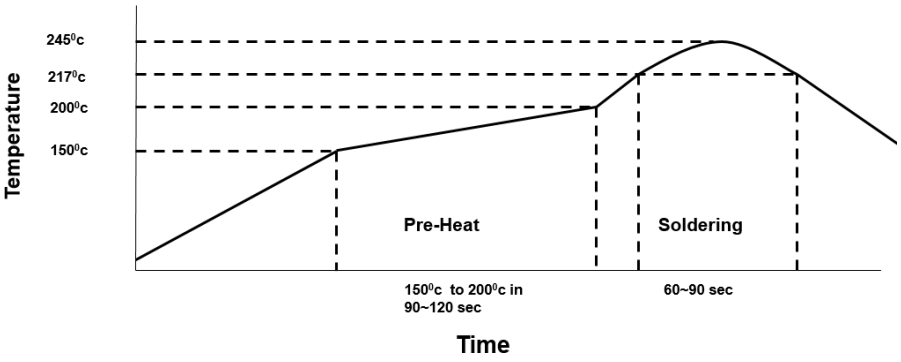

Figure 23: Recommended Reflow Profile

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10 MISCELLANEOUS

10.1 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

10.2Rework

The Lyra 24P module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, i.e. replacing individual components. Such actions terminate warranty coverage.

10.3Handling and Storage

10.3.1 Handling

The Lyra 24P module contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently.

10.3.2Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

10.3.3Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX. Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

10.3.4Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

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11 TAPE AND REEL

Lyra 24P modules are delivered to the customer in cut tape (250 pcs) or reel (1000 pcs) packaging with the dimensions below. All dimensions are given in mm unless otherwise indicated.

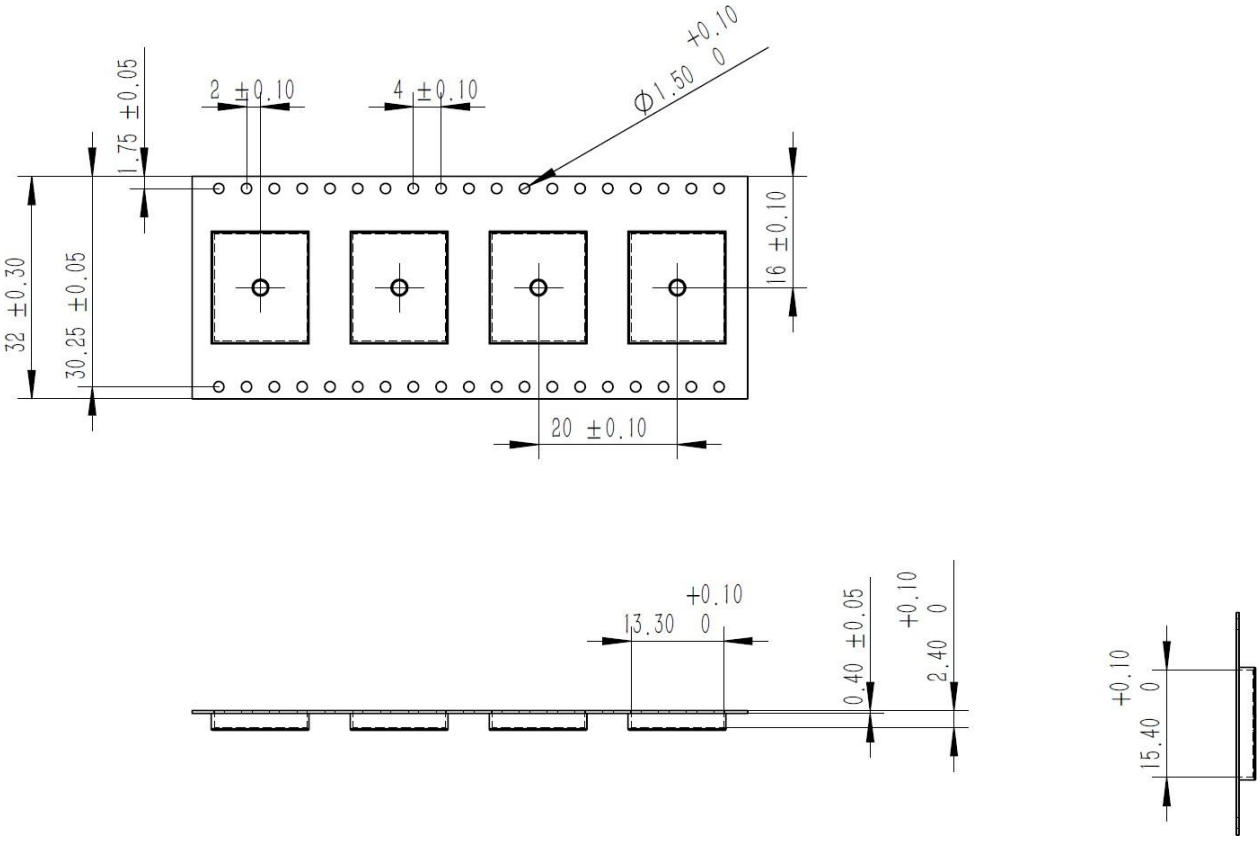

Figure 24: Carrier Tape Dimensions

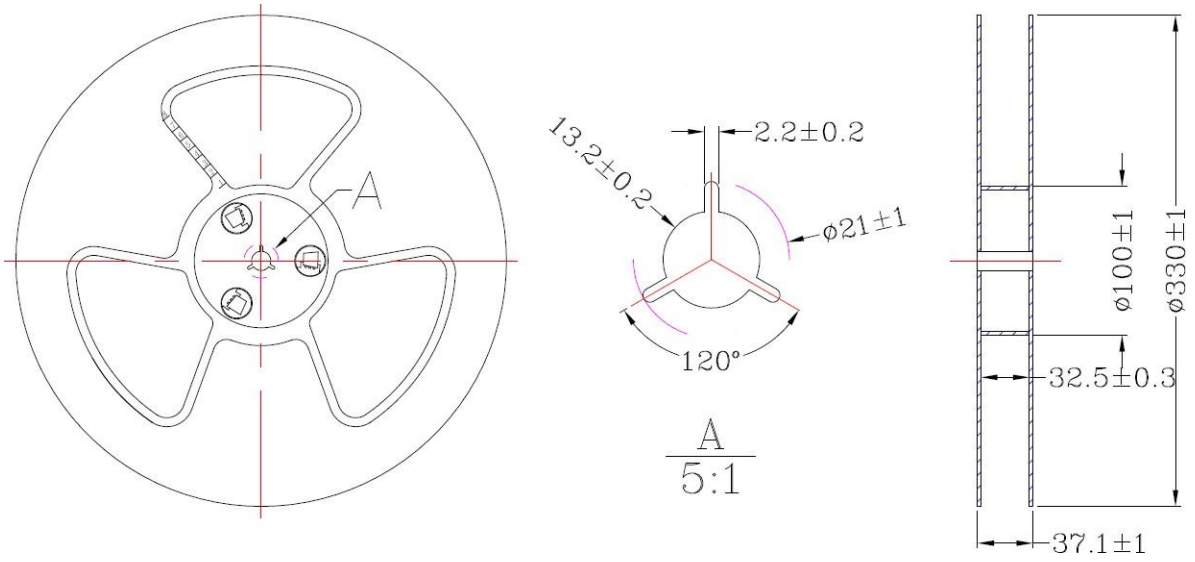

Figure 25: Reel Dimensions

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12 Reliability Test

12.1 Climatic And Dynamic

Table 24: Climatic and Dynamic Reliability Test Results

Standard	Test Item	Specification		Test Result
JESD22-A113	Step 1: Pre-conditioning	**Pre-check:**	1. Function check (Tools and SOP supplied by customers).	Pass
			2. Mechanical check.	
		Pre-conditioning:		
		1. Bake	125°C for 24 hours.	
		2. Moisture Soak	30°C/60% RH for 192 hours	
			Not shorter than 15 minutes and not longer than 4 hours after removal from the temperature/ humidity chamber, subject the sample to 3 cycles of the reflow.	
		Post-check:	1. Function check (Tools and SOP supplied by customers).	
			2. Mechanical check.	
			3. Perform inspections of short, open, delamination of DUTs by Optical Microscope (under 40X optical magnification).	
			4. X-RAY / CSAM (SAT) on any failed samples (Notify customers).	
			5. Cross-sections analysis based on X-RAY and CSAM results.	
JESD22-A104	Step 2: Temperature Cycling Non-operating	1. Temperature	-40°C for 15 minutes	Pass
		2. Shock Temperature	85°C within ramp rate 15°C /minute	
		3. Temperature	85°C for 15 minutes	
		4. Shock Temperature	-40°C within ramp rate 15°C/minute	
		5. Repeat steps 1-4	Stop to check functions at 500/ 700 cycles	
JEDEC 22-B110B.01 (2019)	Mechanical Shock Non-operating Unpackaged device	1. Pulse shape	Half-sine waveform	Pass
		2. Impact acceleration	1500 g	
		3. Pulse duration	0.5 ms	
		4. Number of shocks	30 shocks (5 shocks for each face)	
		5. Orientation	Bottom, top, left, right, front, and rear faces	

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12.2 Reliability MTBF Prediction

Table 25: MTBF Prediction

Laird Part Number	Environment	Test Result 40 ℃ (Hours)
453-00142R 453-00142C 453-00145R 453-00145C 453-00148R 453-00148C	Ground, Fixed, Uncontrolled	17,000,000
Laird Part Number	**Environment**	**Test Result 105 ℃ (Hours)**
453-00142R 453-00142C 453-00145R 453-00145C 453-00148R 453-00148C	Ground, Fixed, Uncontrolled	900,000

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13 REGULATORY

13.1 Regulatory information

Note: For complete regulatory information, refer to the Lyra 24P Regulatory Information document (coming soon) which will be available from the Lyra 24 Series Bluetooth 5.3 Solution Product page.

The Lyra 24P holds current certifications in the following countries:

Table 26: Lyra 24P Regulatory Information

Country/Region	Regulatory ID
USA (FCC)	SQG-LYRA24P
Canada (ISED)	3147A-LYRA24P
UK (UKCA)	N/A
EU	N/A
Japan (MIC)	201-220655 (+10 dBm) / 201-220774 (+20 dBm)
Korea (KC)	R-C-L8C-LYRA24P
Australia (AS)	N/A
New Zealand (NZS)	N/A

13.2 Maximum Regulatory Certified RF TX Power per Country (TBD)

AT firmware implements maximum RF TX power settings per country highlighted below.
Customers developing with **C Code –** Full software development with Silicon Labs SDK and Toolchain, MUST implement the maximum RF TX power settings per country and other parameters mentioned in this section.

To be defined.

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14 BLUETOOTH SIG QUALIFICATION

14.1 Overview

The Lyra 24P Series module is listed on the Bluetooth SIG website as a qualified End Product, using the combination of a RF-PHY, LL and Host Stack Components.

Table 27: Bluetooth SIG Qualification

Design Name	Owner	Declaration ID	Reference QDID	Link to listing on the SIG website
Lyra 24P	Laird Connectivity	TBD	TBD	TBD

14.1.1 Referenced Qualified Components

Table 28: Referenced Qualified Components

Design Name	Owner	Reference QDID	Link to listing on the SIG website
EFR32BG24 and EFR32MG42 RF-PHY	Silicon Laboratories	TBD	TBD
Wireless Gecko Link Layer	Silicon Laboratories	TBD	TBD
Wireless Gecko Host	Silicon Laboratories	TBD	TBD

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to registered as a member of the Bluetooth SIG – **https://www.bluetooth.com/**

The following link provides a link to the Bluetooth Registration page: **https://www.bluetooth.org/login/register/**

For each Bluetooth Design, it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/qualification-listing-fees/

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document:

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

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14.2 Qualification Steps When Referencing on End Product Listing

For this qualification, follow these steps:

1. To start a listing, go to: **https://www.bluetooth.org/tpg/QLI_SDoc.cfm**
2. Select Start the Bluetooth Qualification Process with **No Required Testing**.
3. Project Basics:
   - Enter the Project Name (this can be the product name or the Bluetooth Design name).
   - For Referenced Qualified Designs, enter QDID XXXX
4. Product Declaration:
   - Enter the Listing Date (this can any date ranging from the date of entry up to 90 days after submission) – Your design is qualified immediately but the listing does not go public until the specified date.
5. Add End Product(s) – Each end product that uses the Qualified Design (without modification) can be added in this section. The Bluetooth SIG requires that you add each individual model number separately.
6. Declaration ID:
   - Select a Declaration ID from the list.

   Important! To complete this step, you must have already paid your Bluetooth SIG Declaration ID fee. If you have not, refer to the Bluetooth SIG Qualification Overview section for instructions. You also have the option of clicking **Pay Declaration Fee** accessible from this step of the Bluetooth SIG Qualification process.
7. Review and Submit – With this, some automatic checks occur to ensure all sections are complete.
   - Review all entered information and make corrections, if needed.
   - Once you have reviewed your information, tick all of the check boxes and add your name to the signature page.
   - Click **Signature Confirmed – Complete Project & Submit Product(s) for Qualification**.
     (You will be asked to confirm to proceed with the final listing one more time)
8. Once the listing is confirmed please download the SDoC and place a copy in the compliance folder.

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

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15 Additional Information

Please contact your local sales representative or our support team for further assistance:

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Phone	Americas: +1-800-492-2320 Europe: +44-1628-858-940 Hong Kong: +852-2762-4823
Website	www.lairdconnect.com/
Technical Support	www.lairdconnect.com/resources/support
Sales Contact	www.lairdconnect.com/contact

Note: Information contained in this document is subject to change.

Laird Connectivity's products are subject to standard Terms & Conditions.

www.lairdconect.com

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