MP2491N

32V, 6A, High-Efficiency, Synchronous Step-Down Converter with External Soft Start

DESCRIPTION

The MP2491N is a fully integrated, high-voltage step-down converter. The MP2491N can achieve 6A of continuous output current (I_{OUT}), with excellent load and line regulation across a wide input supply range.

Constant-on-time (COT) control provides fast transient response, easy loop design, and tight output regulation.

Full protection features include over-current protection (OCP), current limiting with hiccup mode, output over-voltage protection (OVP), and thermal shutdown.

The MP2491N requires a minimal number of readily available, standard external components, and is available in a QFN-13 (2.5mmx3mm) package.

FEATURES

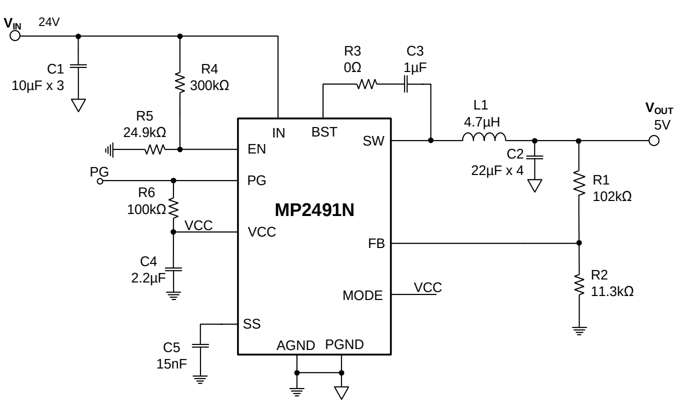
- Wide 4V to 32V Operating Input Voltage (V_{IN}) Range
- 0.5V to 30V Output Voltage (V_{OUT}) Range
- 6A Output Current (I_{OUT})
- Constant-On-Time (COT) Control
- Low-Dropout Mode
- 30mΩ/20mΩ Internal MOSFET Switches
- Fixed 540kHz Switching Frequency (f_{SW})
- EN Shutdown Discharge
- Output Over-Voltage Protection (OVP)
- Adjustable Automatic Pulse-Frequency Modulation (PFM)/Pulse-Width Modulation (PWM) Mode or Forced PWM Mode
- Power Good (PG) Indication
- Configurable Soft Start
- Available in a QFN-13 (2.5mmx3mm) Package

MPL Optimized Performance with MPS Inductor MPL-AY1050 Series

APPLICATIONS

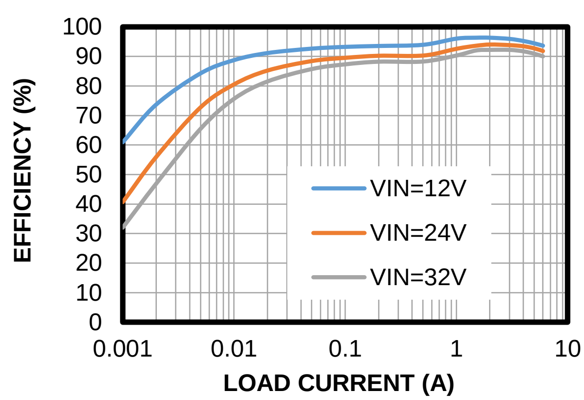
- TVs, Monitors
- MFP Power Supplies

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, DCR = 9.5mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2491NGQB	QFN-13 (2.5mmx3mm)	*See Below*	1

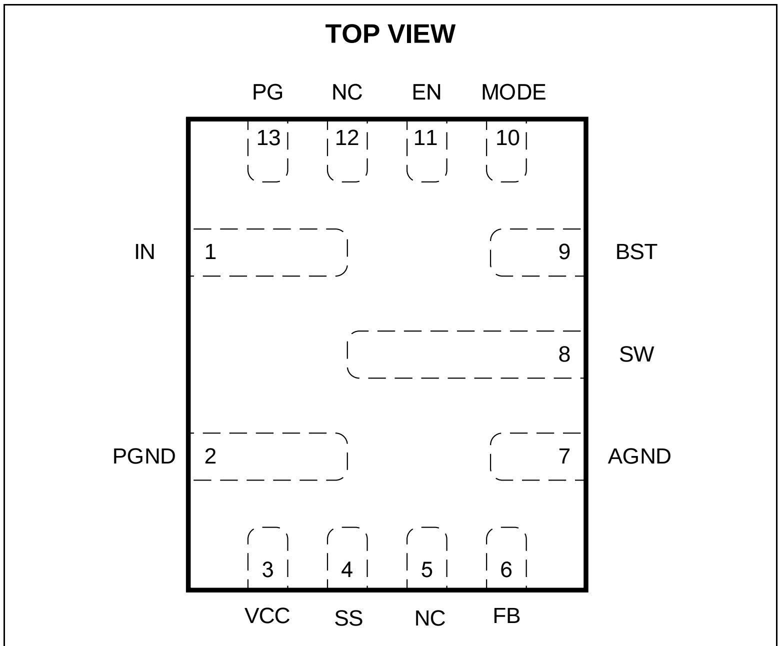
* For Tape & Reel, add suffix -Z (e.g. MP2491NGQB-Z).

TOP MARKING

BUP
YWW
LLL

BUP: Product code of MP2491NGQB
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-13 (2.5mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Supply voltage.** IN is the drain of the internal power device and power supply for the entire chip. The MP2491N operates from a 4V to 32V unregulated input. Place a capacitor (C_{IN}) as close to the IC as possible to prevent large voltage spikes from appearing at the input.
2	PGND	**Power ground.** Place the PGND node outside of the C_{IN} ground path to prevent switching current spikes from inducing voltage noise into the part.
3	VCC	**Internal 4.44V low-dropout (LDO) regulator output.** Decouple the VCC pin with a 2.2µF capacitor. The VCC LDO is active even if EN is pulled low.
4	SS	**Soft start.** Use an external capacitor to configure the switch-mode regulator's soft-start time. Do not float the SS pin.
5, 12	NC	**No connection.** Float the NC pin or connect it to AGND.
6	FB	**Feedback.** To set V_{OUT}, connect the FB pin to the tap of an external resistor divider from the output to AGND.
7	AGND	**Analog ground.** Connect the AGND pin to PGND.
8	SW	**Switch output.** The SW pin is the source of the high-side power device.
9	BST	**Bootstrap.** A BST capacitor is required to drive the power switch's gate above the supply voltage. Connect this capacitor between the SW and BST pins to form a floating supply across the power switch driver. An on-chip regulator charges up the external bootstrap capacitor.
10	MODE	**Buck operation mode set.** Connect the MODE pin to VCC or AGND to set automatic PFM/PWM or forced PWM mode. Do not float the MODE pin.
11	EN	**Enable control.** Drive EN high to enable the MP2491N. EN has a 2MΩ pull-down resistor connected to GND.
13	PG	**Power good output.** The PG pin is an open drain that indicates both output under-voltage (UV) and over-voltage (OV) conditions. PG does not respond when BST is low or experiencing a UV condition.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) 34V
V_{SW} .... -0.3V (-7V for <10ns) to V_{IN} + 0.3V
V_{BST} .... V_{SW} + 6V
V_{EN} .... 6V (<100µA when >6V)
All other pins ....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-13 (2.5mmx3mm) 3.57W (4)
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) .... ±2000V
Charged device model (CDM) .... ±750V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ....4V to 32V
Output voltage (V_{OUT}).......................0.5V to 30V
Output current 6A
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance

	θ_{JA}	θ_{JC}	
QFN-13 (2.5mmx3mm)			
EVL2491N-QB-00A (4)	35	4.5	°C/W
JESD51-7 (5)	66	63	°C/W

Notes:

1) The absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Measured on an EVL2491N-QB-00A evaluation board for the MP2491NGQB
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EVL2491N-QB-00A, 4-layer, 63.5mmx63.5mm PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 5V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted. The over-temperature limit is derived by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V, T_J = 25°C		37	50	μA
		V_{EN} = 0V, T_J = -40°C to +125°C			60	
Supply current (quiescent)	I_Q	No switching, T_J = 25°C		185	220	μA
		No switching, T_J = -40°C to +125°C			250	
EN rising threshold	V_{EN_RISING}		1.14	1.2	1.26	V
EN hysteresis	V_{EN_HYS}			280		mV
EN input current	I_{EN}	V_{EN} = 2V		1		μA
Reference voltage	V_{REF}	T_J = 25°C	0.495	0.5	0.505	V
		T_J = -40°C to +125°C	0.493	0.5	0.507	V
Thermal shutdown (7)	T_{STD}			165		°C
Thermal hysteresis (7)	T_{HYS}			25		°C
VCC regulator	V_{CC}		4.24	4.44	4.64	V
VCC load regulation	V_{CC_RG}	I_{CC} = 0mA - 10mA			3	%
V_{IN} under-voltage lockout (UVLO) threshold rising	$INUV_{VTH}$		3.5	3.7	3.9	V
V_{IN} UVLO threshold hysteresis	$INUV_{HYS}$			220		mV
High-side MOSFET (HS-FET) on resistance	R_{DSON_HS}			30		mΩ
Low-side MOSFET (LS-FET) on resistance	R_{DSON_LS}			20		mΩ
Output over-voltage protection (OVP) rising threshold	V_{OVP_R}		114	120	126	% of V_{REF}
OVP recovery threshold	V_{OVP_F}		102	108	114	% of V_{REF}
PG UV rising	$V_{PG\_UV\_R}$		83	89	95	% of V_{REF}
PG UV falling	$V_{PG\_UV\_F}$			81		% of V_{REF}
PG OV rising	$V_{PG\_OV\_R}$		109	115	121	% of V_{REF}
PG OV falling	$V_{PG\_OV\_F}$			109		% of V_{REF}
PG rising delay	$t_{PG\_R\_DLY}$			350		μs
PG falling delay	$t_{PG\_F\_DLY}$			70		μs
PG sink current capability	V_{PG_SINK}	Sink 1mA			0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted. The over-temperature limit is derived by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 32V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 32V, T_J = -40°C to +125°C			3	μA
MODE pin voltage threshold 1	V_{MODE_1}	Forced PWM mode			12	% of V_{CC}
MODE pin voltage threshold 2	V_{MODE_2}	Auto-PFM/PWM	90			% of V_{CC}
Zero-current detection (ZCD)	I_{ZCD}	Auto-PFM/PWM, V_{IN} = 24V, V_{OUT} = 5V		100		mA
Negative current limit (7)	I_{LIMITN}	Forced PWM mode, OVP or EN shutdown		-3		A
Output current limit	I_{LIMIT}	T_J = 25°C	6.3	7.9	9.4	A
Hiccup duty cycle (7)	D_{HICP}			10		%
Oscillator frequency	f_{SW}	MODE = 0V, T_J = 25°C	425	540	665	kHz
Maximum on time (7)	t_{ON_MAX}			15		μs
Minimum on time (7)	t_{ON_MIN}			60		ns
Minimum off time (7)	t_{OFF_MIN}			180		ns
Soft-start current	I_{SS}			9	13	μA

Notes:

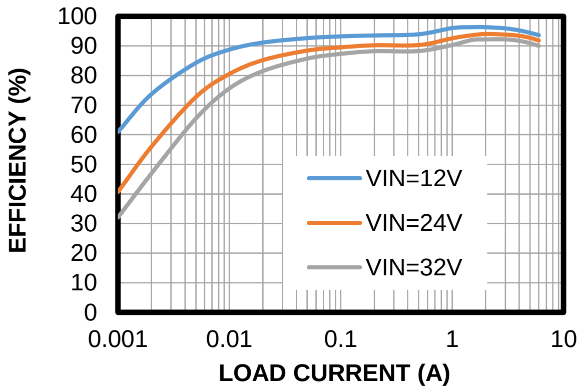
6) Not tested in production. Derived by over-temperature correlation.
7) Derived by sample characterization. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board (see the Design Example section on page 17). V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 540kHz, L = 4.7µH, PFM mode, T_A = 25°C, unless otherwise noted.

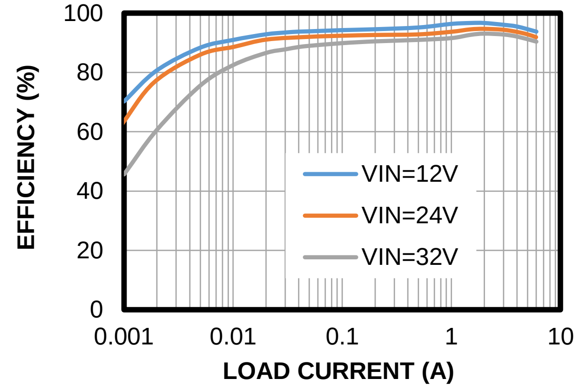
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, DCR = 9.5mΩ



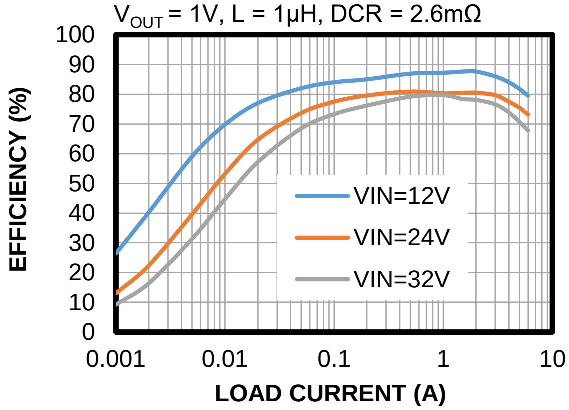
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, DCR = 9.5mΩ, VOUT connected to VCC with 1N5819



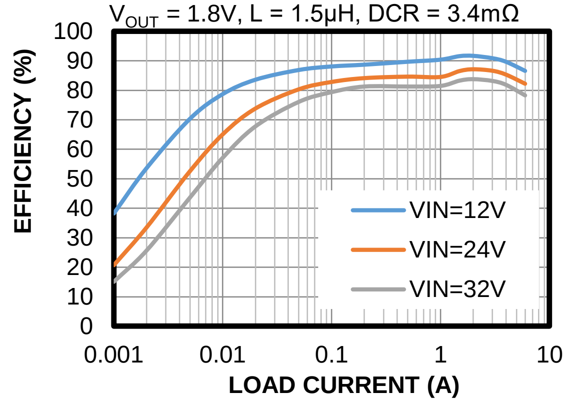
Efficiency vs. Load Current

V_{OUT} = 1V, L = 1µH, DCR = 2.6mΩ



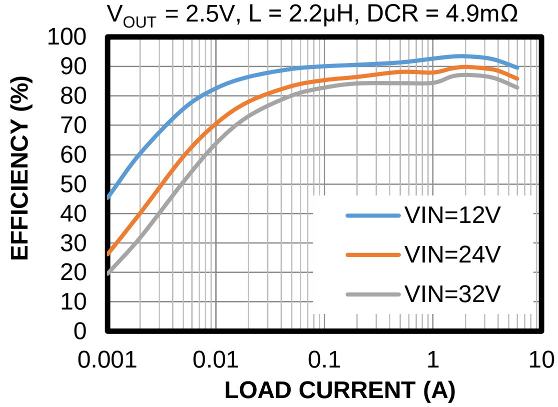
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 1.5µH, DCR = 3.4mΩ



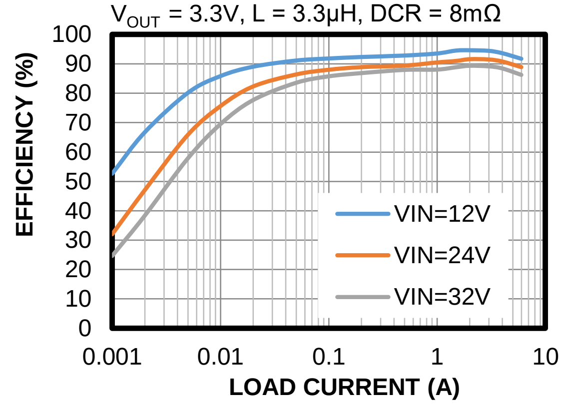
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 2.2µH, DCR = 4.9mΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 3.3µH, DCR = 8mΩ

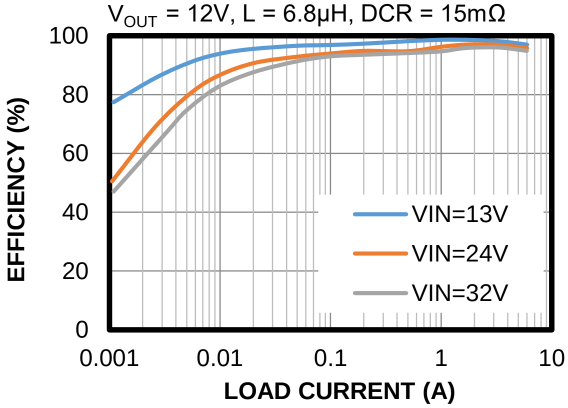


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board (see the Design Example section on page 17). V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 540kHz, L = 4.7µH, PFM mode, T_A = 25°C, unless otherwise noted.

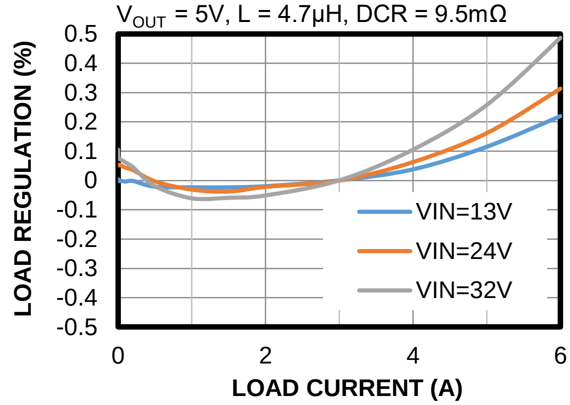
Efficiency vs. Load Current

V_{OUT} = 12V, L = 6.8µH, DCR = 15mΩ



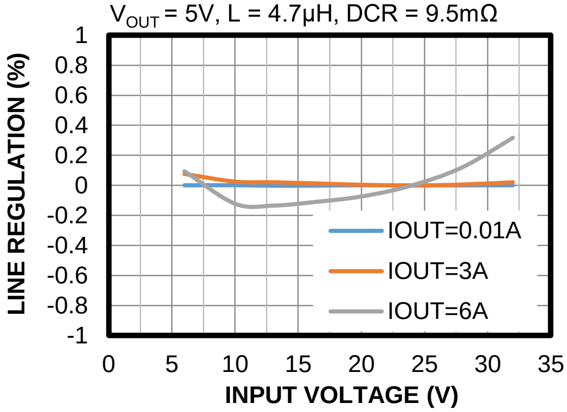
Load Regulation

V_{OUT} = 5V, L = 4.7µH, DCR = 9.5mΩ



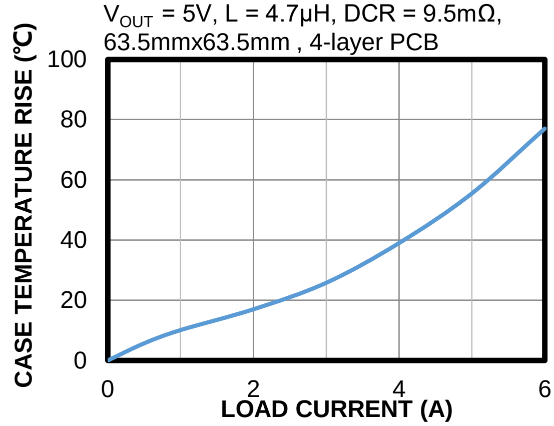
Line Regulation

V_{OUT} = 5V, L = 4.7µH, DCR = 9.5mΩ



Case Temperature Rise vs. Load Current

V_{OUT} = 5V, L = 4.7µH, DCR = 9.5mΩ, 63.5mmx63.5mm , 4-layer PCB

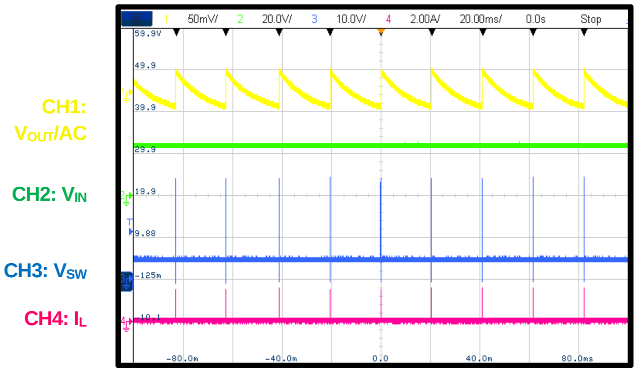


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board (see the Design Example section on page 17). V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 540kHz, L = 4.7µH, PFM mode, T_A = 25°C, unless otherwise noted.

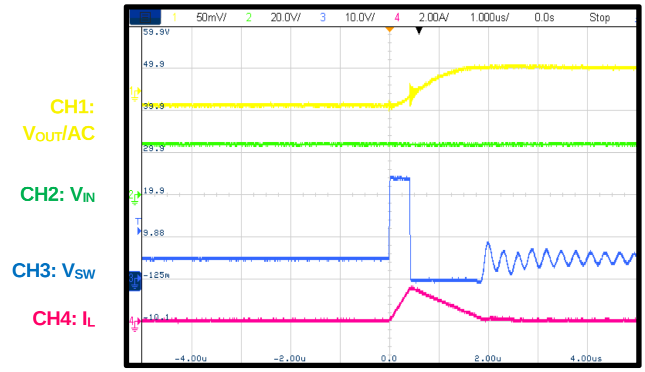
Output Voltage Ripple

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A



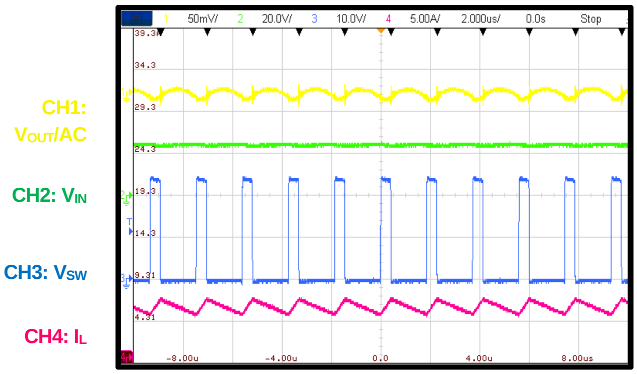
Output Voltage Ripple

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A



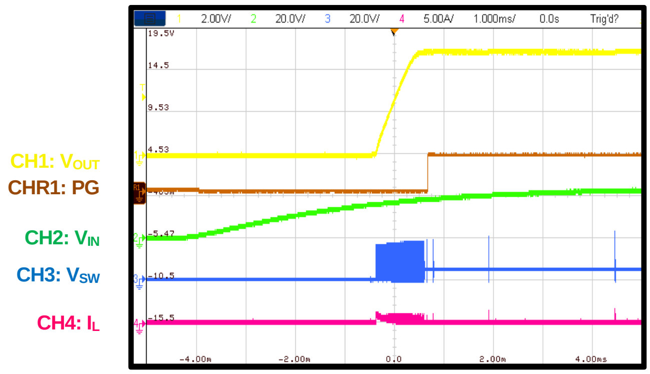
Output Voltage Ripple

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 6A



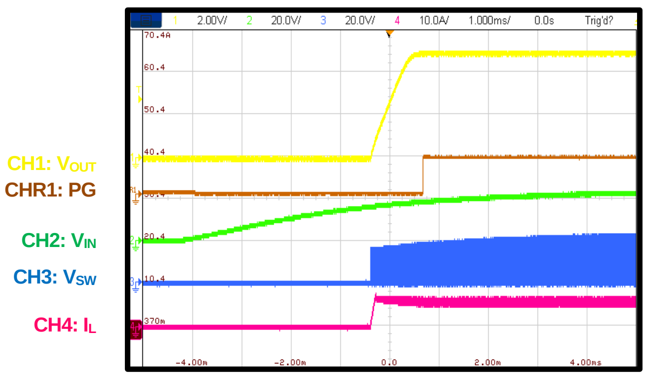
Start-Up through VIN

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A



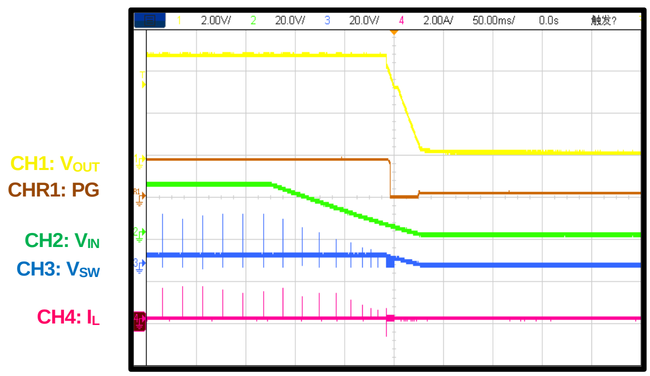
Start-Up through VIN

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 6A



Shutdown through VIN

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A

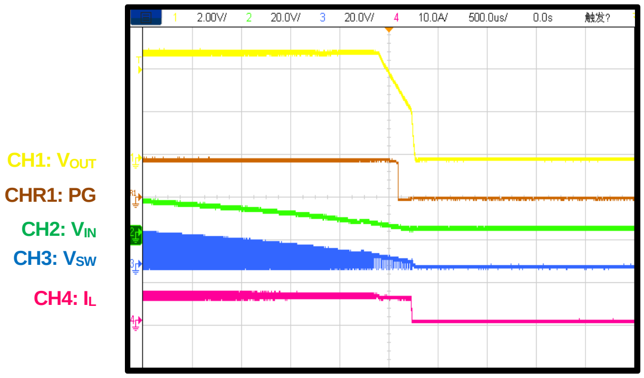


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board (see the Design Example section on page 17). V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 540kHz, L = 4.7µH, PFM mode, T_A = 25°C, unless otherwise noted.

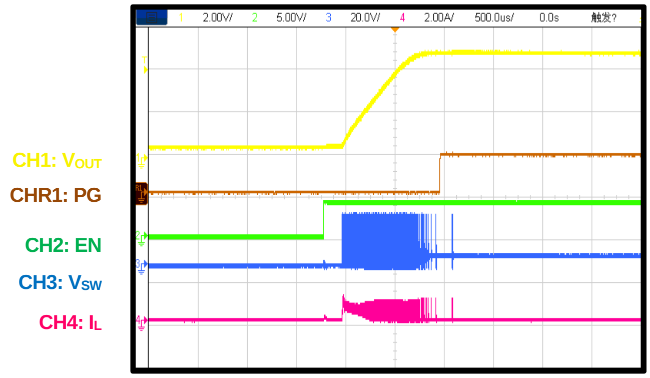
Shutdown through VIN

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 6A



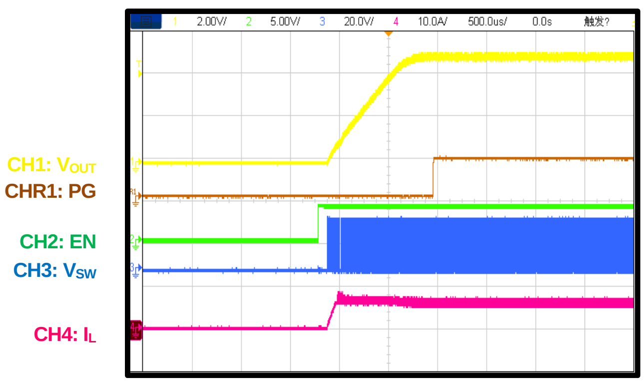
Start-Up through EN

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A



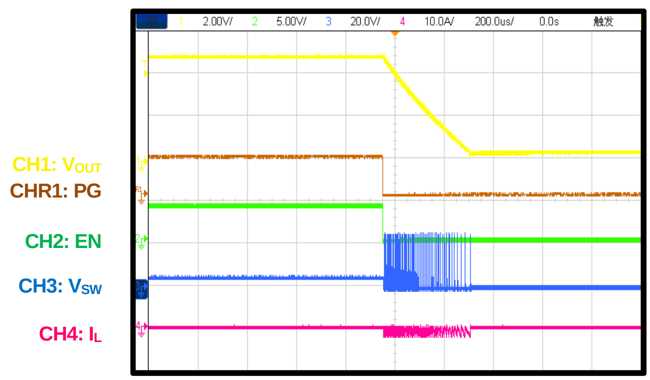
Start-Up through EN

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 6A



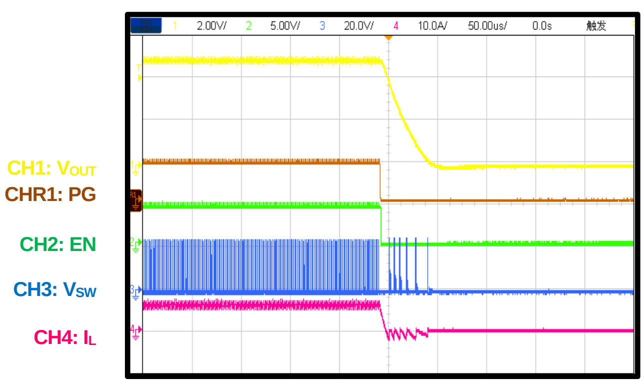
Shutdown through EN

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A



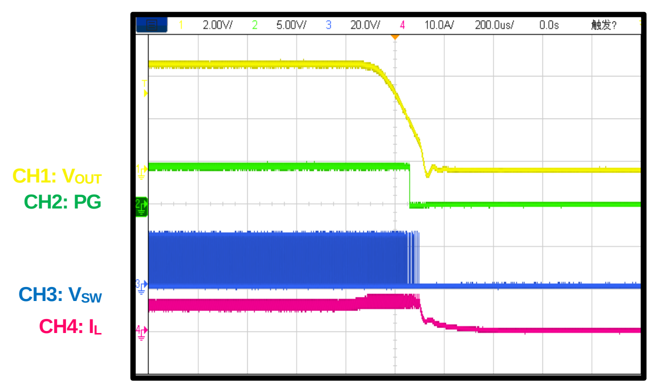
Shutdown through EN

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 6A



OCP

V_{IN} = 24V, V_{OUT} = 5V

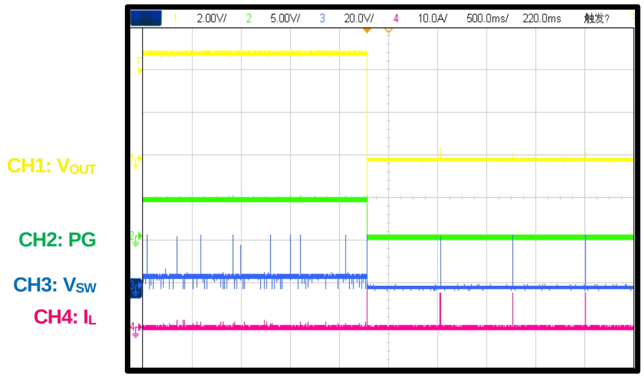


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board (see the Design Example section on page 17). V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 540kHz, L = 4.7µH, PFM mode, T_A = 25°C, unless otherwise noted.

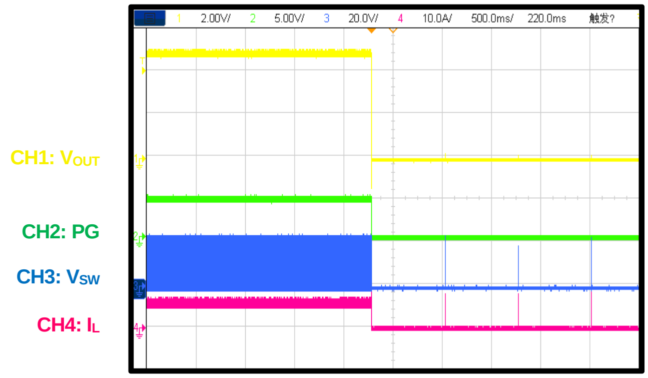
SCP Entry

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A



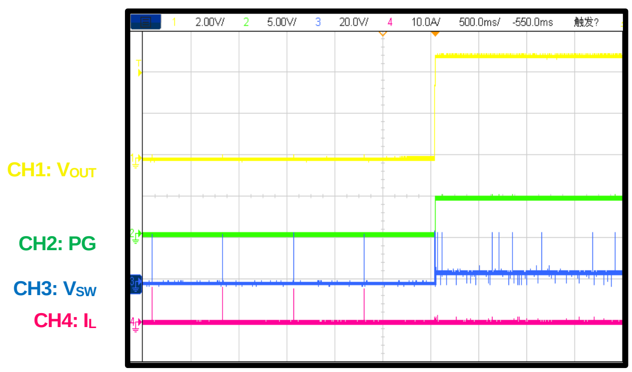
SCP Entry

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 6A



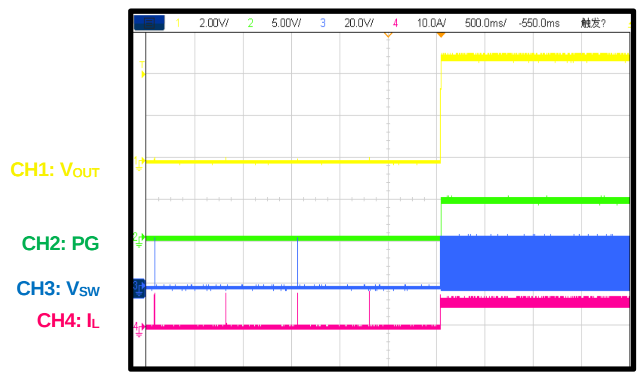
SCP Recovery

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A



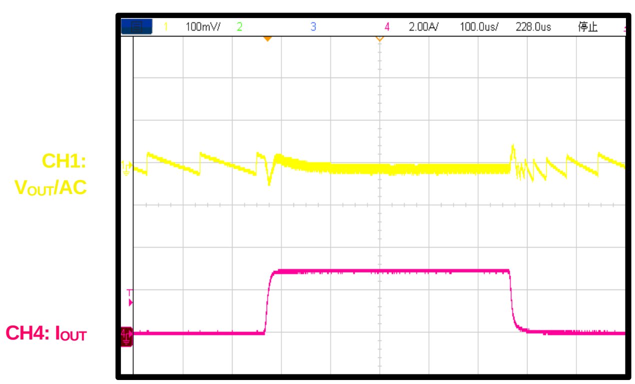
SCP Recovery

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 6A



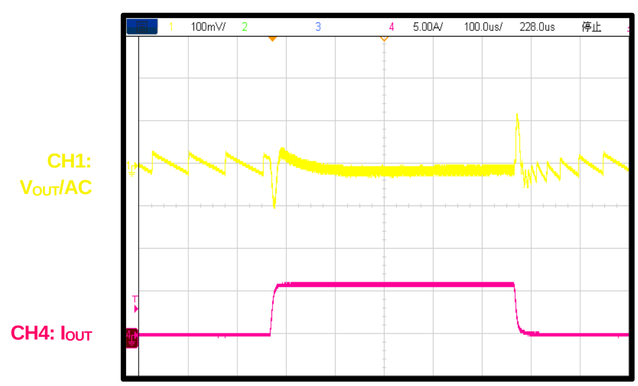
Load Transient Response

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A to 3A, 2.5A/µs with e-load



Load Transient Response

V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A to 6A, 2.5A/µs with e-load



FUNCTIONAL BLOCK DIAGRAM

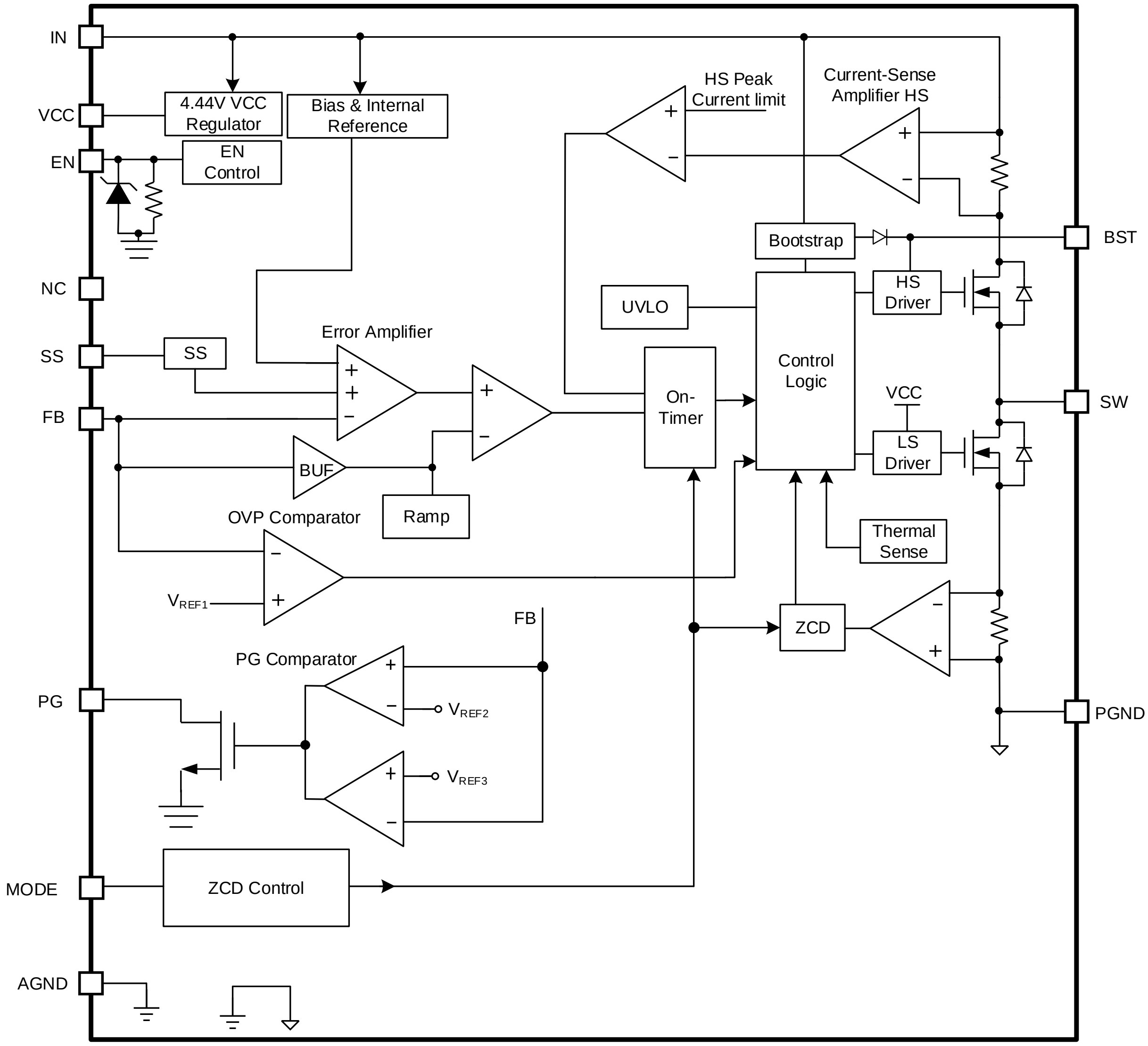


Figure 1: Functional Block Diagram

OPERATION

The MP2491N is a fully integrated, synchronous, rectified, step-down switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. Figure 2 shows the MP2491N's simplified ramp compensation block.

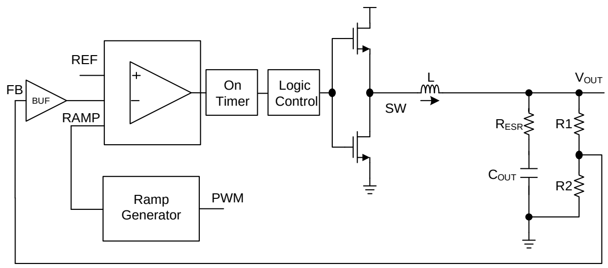


Figure 2: Simplified Ramp Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{RAMP}) is below the error amplifier output voltage (V_{EAO}), which indicates an insufficient output voltage (V_{OUT}). The on period is determined by both V_{OUT} and the input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the V_{IN} range.

After the on period elapses, the HS-FET turns off then turns on again when V_{RAMP} drops below V_{EAO}. By repeating this operation, the converter regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET turn on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period, and vice versa.

Internal compensation is applied for COT control to provide more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current (I_{OUT}) is high and the inductor current is always above 0A (see Figure 3). When V_{RAMP} is below V_{EAO}, the HS-FET turns on for a fixed interval determined by the one-shot on timer. When the HS-FET turns off, the LS-FET turns on until the next period.

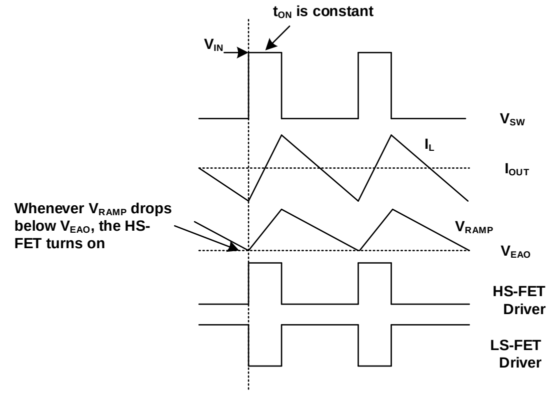


Figure 3: Heavy Load Operation

In CCM, f_{SW} is fairly constant. This is called pulse-width modulation (PWM) mode.

Light-Load Operation

When the MP2491N works in pulse-frequency modulation (PFM) mode during light-load operation, the MP2491N reduces f_{SW} automatically to maintain high efficiency, and the inductor current drops almost to zero. The HS-FET turns on when V_{RAMP} falls below V_{EAO}. The HS-FET turns off when the on timer elapses and the inductor current exceeds its given threshold.

When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 4). Then the output capacitors discharge slowly to GND through the LS-FET and the resistors (R1 and R2). This operation significantly improves device efficiency when I_{OUT} is low.

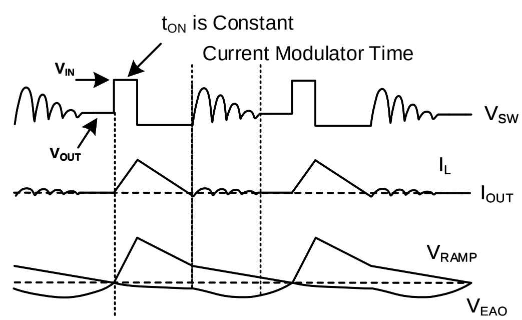


Figure 4: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does under heavy-load conditions.

The HS-FET turn-on frequency is a function of I_{OUT}.

As I_{OUT} increases, the current modulator regulation time period becomes shorter, and the HS-FET turns on more frequently. This increases f_{SW}. I_{OUT} reaches the critical level when the current modulator time is zero. I_{OUT} can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the I_{OUT} exceeds its critical level. Afterward, f_{SW} remains fairly constant across the I_{OUT} range.

Low-Dropout (LDO) Mode

The MP2491N supports low-dropout (LDO) mode. When V_{IN} is close to V_{OUT} and the minimum off time is triggered, the switching on timer is extended to avoid V_{OUT} reduction. f_{SW} decreases accordingly after the maximum on time is triggered (typically 15μs).

4.44V Internal VCC Regulator

The 4.44V internal regulator powers most of the internal logic circuitries. This regulator takes the V_{IN} input and operates across the full V_{IN} range. When V_{IN} exceeds 4.44V, the output of the regulator is in full regulation. When V_{IN} is below 4.44V, the output decreases with V_{IN}. The VCC regulator is active even if EN is pulled low. The VCC pin requires a 2.2μF ceramic decoupling.

Over-Current Protection (OCP)

The MP2491N senses the high-side and low-side currents and uses this information to protect the output from an over-current (OC) condition. If the high-side current exceeds the current-limit threshold, the HS-FET turns off to limit the increasing current. If the low-side current exceeds the valley current limit threshold, the HS-FET waits until the valley current limit is removed before turning on again. As the load resistance drops, V_{OUT} drops until the feedback voltage falls below the under voltage (UV) threshold (typically 40% below the reference voltage (V_{REF})).

Once a UV condition is triggered, the MP2491N enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This reduces the average short-circuit current greatly, alleviating thermal issues and protecting the regulator. The MP2491N exits hiccup mode once the OC condition is removed.

Mode Selection (MODE)

The MP2491N's MODE pin offers two different, configurable states to set the buck operation mode: forced PWM or auto PFM/PWM (see Figure 5).

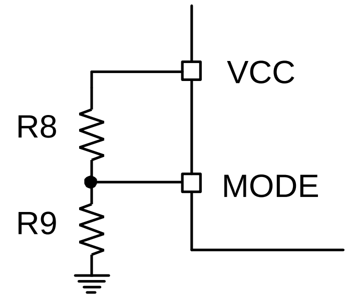


Figure 5: MODE Configuration

Table 1 lists detailed information according to different pin voltages.

Table 1: MODE Truth Table

Resistor Value	Pin Voltage	Buck Operation Mode
R8 = NS, R9 = 0Ω	0	Forced PWM
R8 = 0Ω, R9 = NS	V_{CC}	Auto PFM/PWM

MODE supports dynamic adjustment with a glitch time. Do not float MODE during normal operation.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2491N's UVLO comparator monitors V_{IN}.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN above 1.2V to turn the regulator on; drive EN below 0.92V to turn it off. EN has a 2MΩ pull-down resistor connected to GND.

EN is clamped internally using a 6V series Zener diode (see Figure 6).

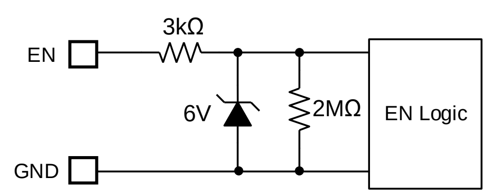


Figure 6: Zener Diode between EN and GND

Connecting the EN input to VIN via a pull-up resistor limits the EN input current below 100µA, which prevents damage to the Zener diode.

For example, when connecting 24V to VIN, then $R_{PULL\_UP} \geq (24V - 6V) / 100\mu A - 3k\Omega = 177k\Omega$.

Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the part starts, an internal current source (about 9µA) charges up the SS capacitor to generate a soft-start voltage (V_{SS}). When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}, the error amplifier uses V_{SS} as the reference, and V_{OUT} ramps up smoothly. Once V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. At this point, soft start finishes, and the part enters steady state operation.

The SS capacitor value (C_{SS}) can be calculated with Equation (2):

$$C_{SS}(nF) = \frac{t_{SS}(mS) \times I_{SS}(\mu A)}{V_{REF}} \quad (2)$$

Do not float the SS pin.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C3, L1, and C2 (see Figure 7). If V_{IN} - V_{SW} exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C3.

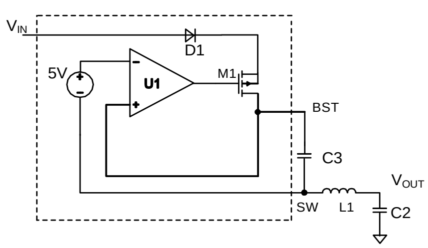


Figure 7: Internal Bootstrap Charging Circuit

Output Discharge

An active discharge path turns on when EN is low, or during output over-voltage protection (OVP). The LS-FET turns on until the negative inductor current reaches its current limit, then it turns off for a fixed period.

The LS-FET turns on again after a fixed delay, and the on/off cycles repeat. The discharge function turns off when V_{OUT} is fully discharged, or the 10ms maximum time has passed.

Output Over-Voltage Protection (OVP)

To protect the downstream device from an OV condition, the MP2491N provides an output OVP discharge function.

If the FB voltage (V_{FB}) exceeds 120% of V_{REF} for a 5µs deglitch time, the LS-FET repeats the turn-on process to discharge V_{OUT} until it drops to 108% of V_{REF}. Then the chip resumes normal operation.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 165°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 140°C), the chip is enabled again.

Power Good (PG)

The power good pin (PG) indicates whether V_{OUT} is in the normal range, when compared to the internal V_{REF}. PG is an open-drain structure and requires an external pull-up supply. During start-up, the power good output is driven low. This tells the system to remain off and keep the load on the output to a minimum. This helps reduce the inrush current during start-up.

When V_{OUT} exceeds the PG UV threshold and is below the PG OV threshold of the internal reference voltage (and soft start is finished), the PG signal is an open-drain output. When V_{OUT} is below the PG UV threshold or exceeds the PG OV threshold of the internal reference, PG switches low.

PG uses a deglitch time for both the rising and falling edge whenever V_{OUT} crosses the UV / OV rising and falling thresholds. The PG output is pulled low immediately when EN drops below its threshold or input UVLO is triggered.

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider sets V_{OUT}. First, choose a value for R2. Select a reasonable R2; a small R2 leads to considerable quiescent current loss, while are large R2 makes the FB pin noise-sensitive. Calculate R1 with Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (3)$$

Figure 8 shows the feedback circuit.

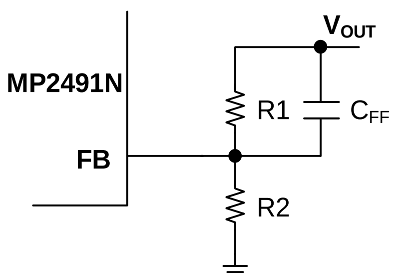


Figure 8: Feedback Network

Table 2 lists the recommended parameters for common V_{OUT} values.

Table 2: Parameter Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)	L (µH)
1	30	30	22	1
1.8	30	11.5	22	1.5
2.5	102	25.5	22	2.2
3.3	102	18.2	22	3.3
5	102	11.3	22	4.7
12	102	4.42	22	6.8

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AY1050 Series**

An inductor is required to supply constant current to the output load while being driven by the switched V_{IN}. A larger-value inductor results in less ripple current and a lower output voltage ripple. However, a larger-value inductor is physically larger, and has a higher series resistance and lower saturation current. Estimate the inductor value with Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (5):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 3 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 3: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AY	1µH to 6.8µH	MPS
MPL-AY1050-1R0	1µH	MPS
MPL-AY1050-1R5	1.5µH	MPS
MPL-AY1050-2R2	2.2µH	MPS
MPL-AY1050-3R3	3.3µH	MPS
MPL-AY1050-4R7	4.7µH	MPS
MPL-AY1050-6R8	6.8µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

Considering the inrush and discharge currents during a voltage change, the maximum output capacitance is recommended to be below 330µF. The MP2491N requires an output capacitor (C2) to maintain the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. Use low-ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (9)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulatory system. The MP2491N can be optimized for a wide range of capacitance and ESR values.

Design Example

Table 4 shows a design example when ceramic capacitors are applied.

Table 4: Design Example

V_{IN}	24V
V_{OUT}	5V
I_{OUT}	6A

Figure 10 on page 19 shows the detailed application schematics. The typical performance waveforms are shown in the Typical Performance Characteristics section on page 7. For more devices applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. Use a 4-layer PCB to improve thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input decoupling capacitor as close to the VIN and GND pins as possible.
3. Place the VCC decoupling capacitor as close to the VCC pin as possible.
4. To connect the inner and bottom ground planes, add multiple vias on the ground side of the VCC decoupling capacitor and the GND pins.
5. Place the external feedback resistors next to the FB pin.

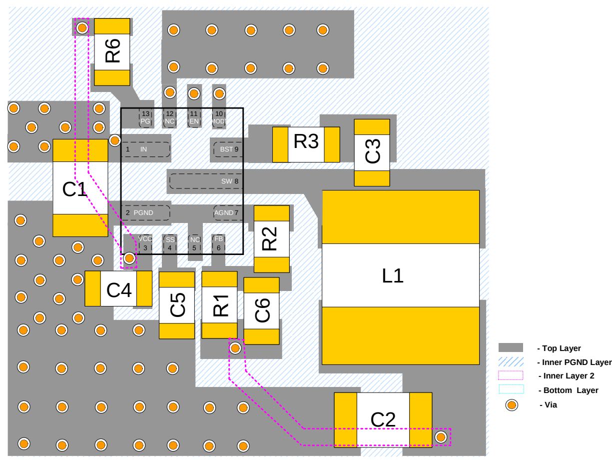


Figure 9: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

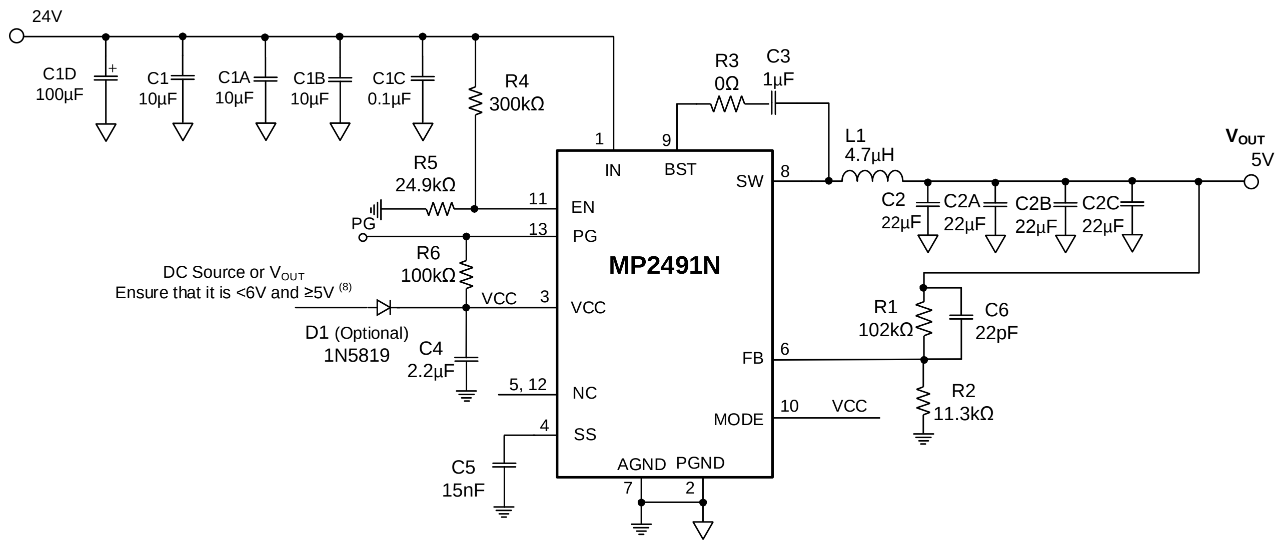


Figure 10: Typical Application (V_{IN} = 24V, V_{OUT} = 5V)

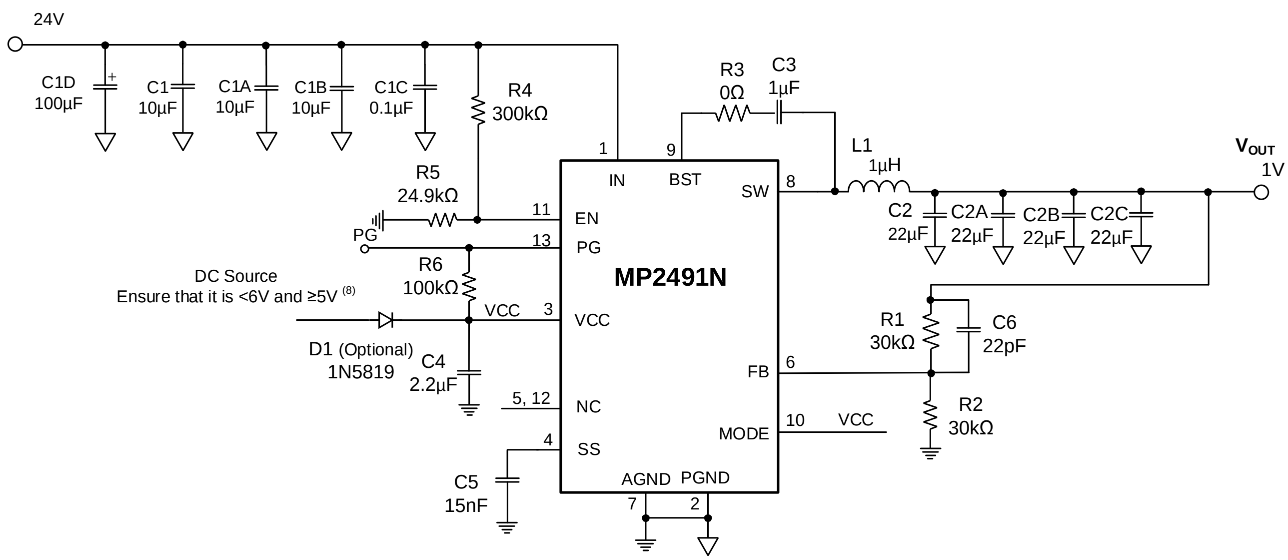


Figure 11: Typical Application (V_{IN} = 24V, V_{OUT} = 1V)

TYPICAL APPLICATION CIRCUITS *(continued)*

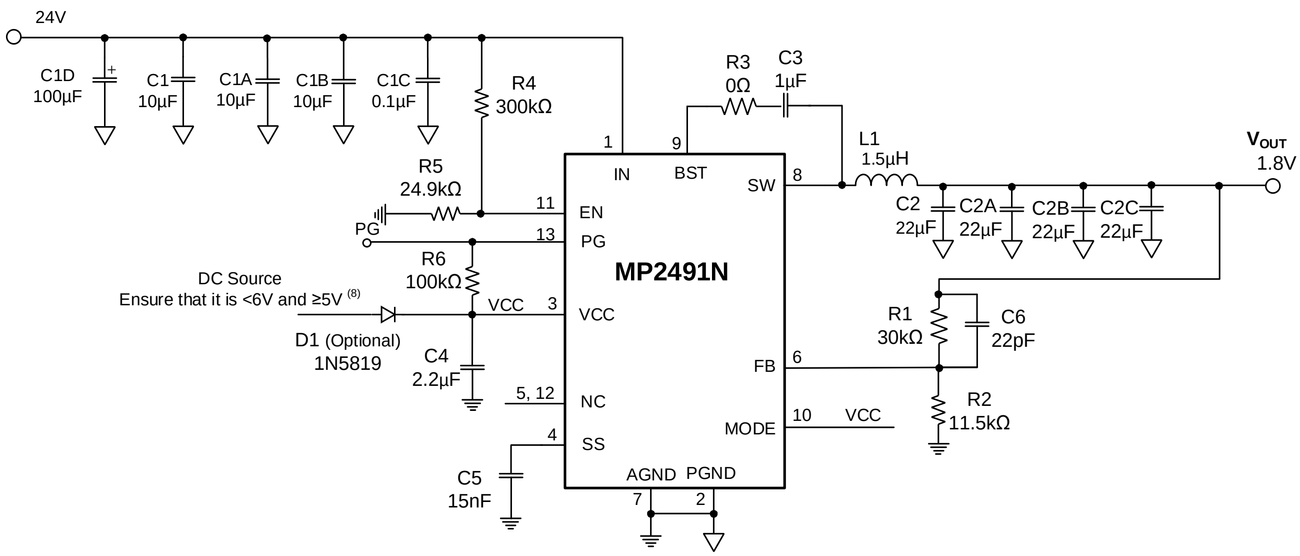


Figure 12: Typical Application (V_{IN} = 24V, V_{OUT} = 1.8V)

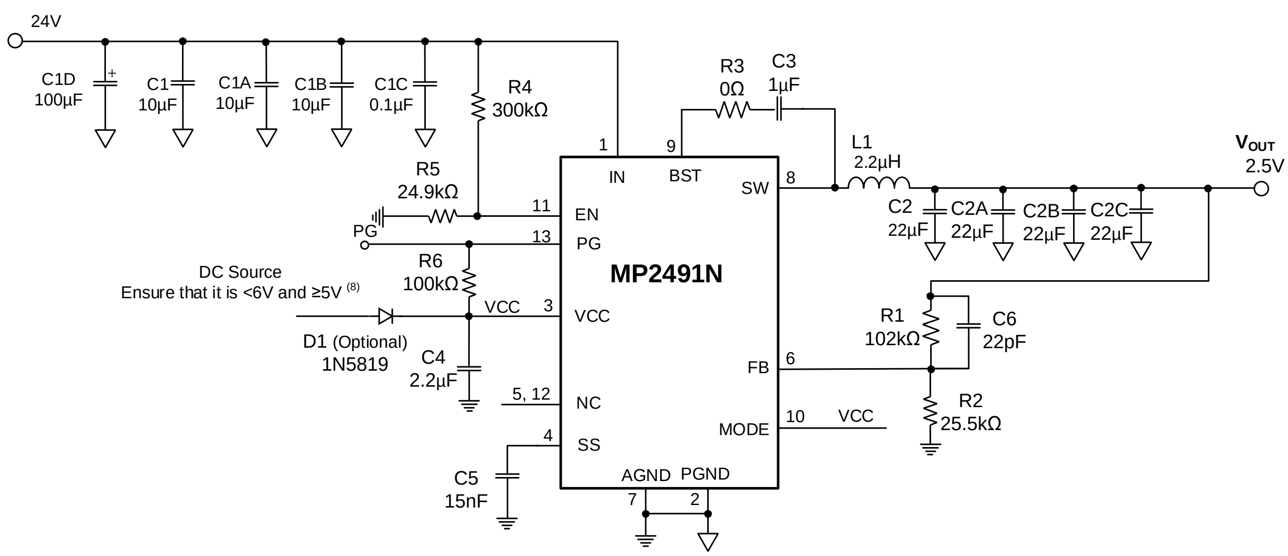


Figure 13: Typical Application (V_{IN} = 24V, V_{OUT} = 2.5V)

TYPICAL APPLICATION CIRCUITS *(continued)*

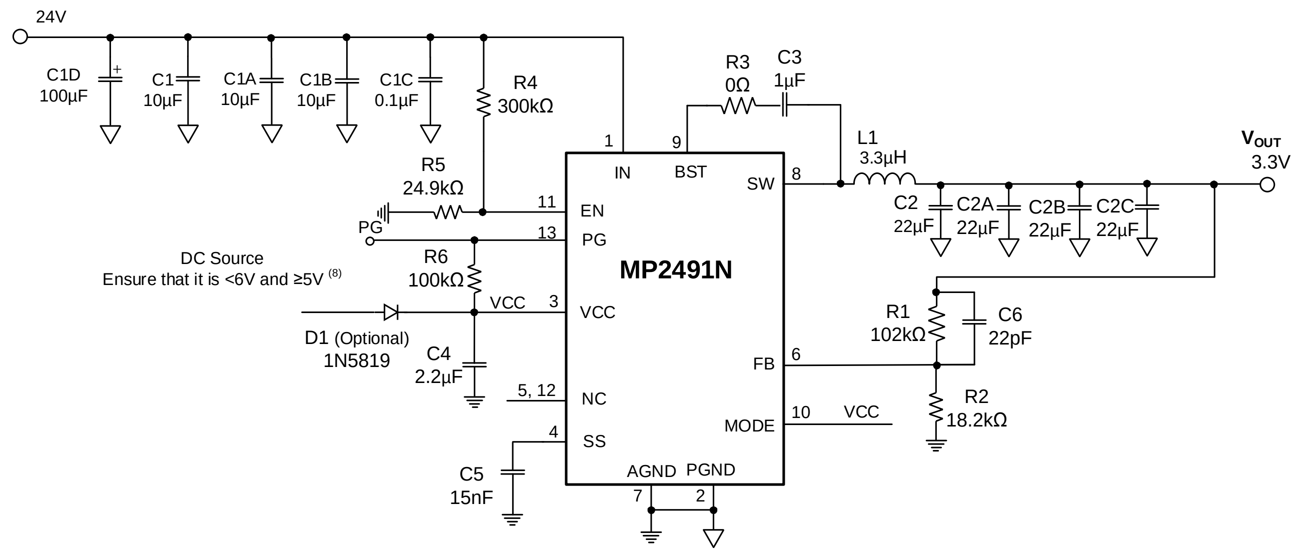


Figure 14: Typical Application (V_{IN} = 24V, V_{OUT} = 3.3V)

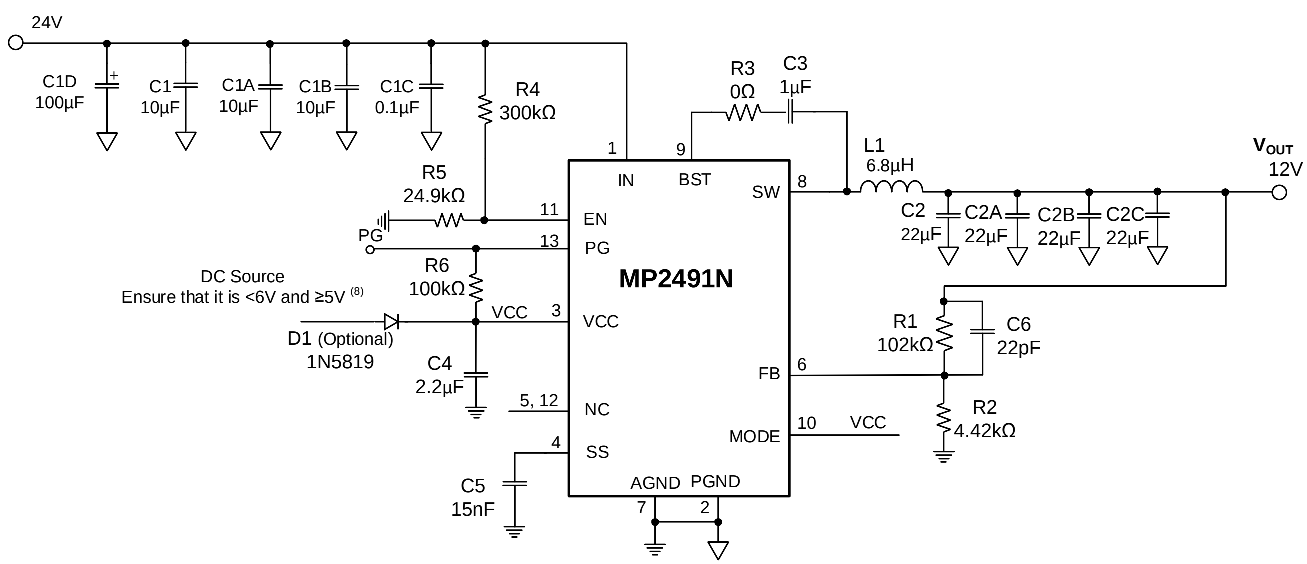


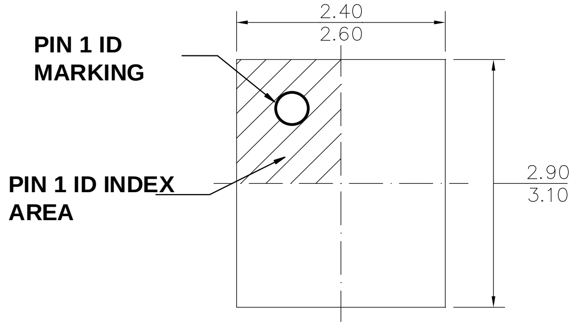
Figure 15: Typical Application (V_{IN} = 24V, V_{OUT} = 12V)

Note:

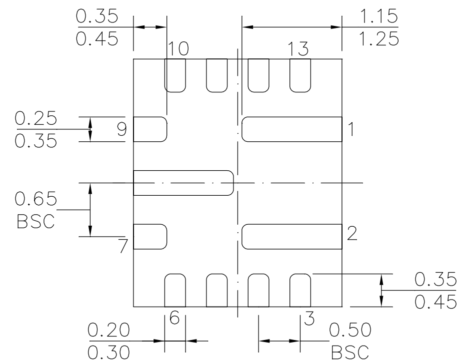
8) D1 is an optional diode that can be used to achieve high efficiency at light loads.

PACKAGE INFORMATION

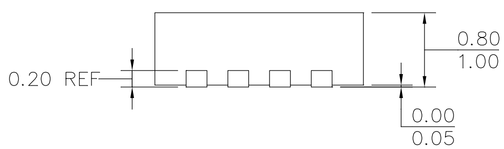
QFN-13 (2.5mmx3mm)



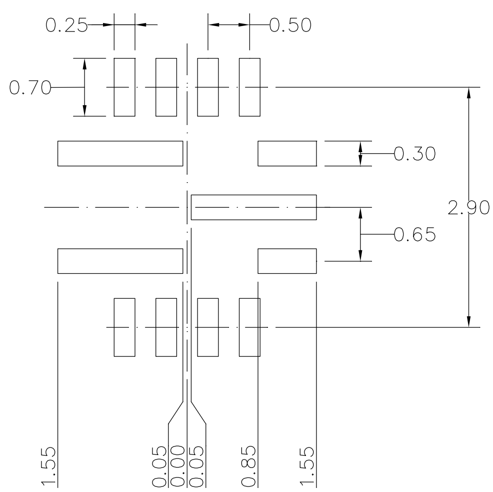
TOP VIEW



BOTTOM VIEW



SIDE VIEW

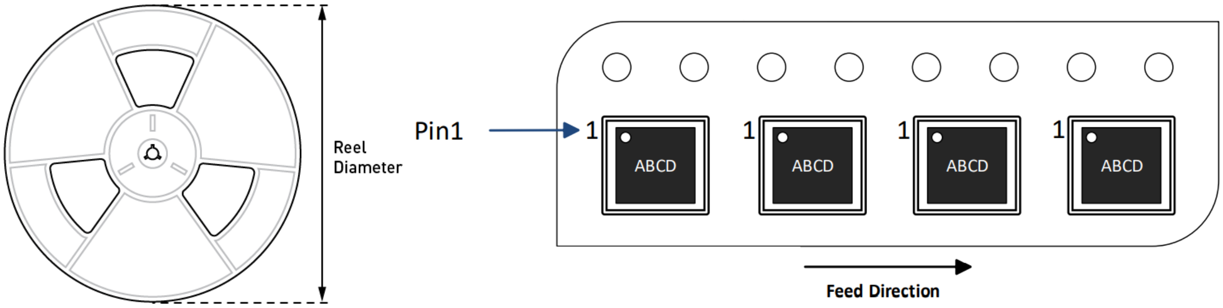


RECOMMENDED LAND PATTERN

NOTE:

1) THE LAND PATTERNS OF PIN 1, PIN 2, PIN 8 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2491NGQB-Z	QFN-13 (2.5mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/24/2022	Initial Release	-