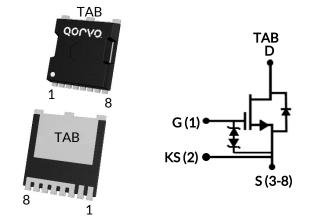


750V-5.4m Ω SiC FET

Rev. A, February 2023

DATASHEET

UJ4SC075005L8S



Part Number	Package	Marking
UJ4SC075005L8S	MO-229	UJ4SC075005



Description

The UJ4SC075005L8S is a 750V, $5.4m\Omega$ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving MO-229 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance R_{DS(on)}: 5.4mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 440nC
- Low body diode V_{ESD}: 1.03V
- Low gate charge: $Q_G = 164nC$
- + Threshold voltage $V_{G(th)}$: 4.7V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected, HBM class 2
- MO-229 package for faster switching, clean gate waveforms

Typical applications

- Solid state relays and circuit-breakers
- Line rectification and active-bridge rectification circuits in AC/DC front-ends
- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating





Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V _{DS}		750	V
Cata annualtara	V _{GS}	DC	-20 to +20	V
Gate-source voltage	V _{GS}	$\begin{tabular}{c} & DC \\ AC (f > 1Hz) \\ T_C < 144^{\circ}C \\ T_C = 25^{\circ}C \\ L = 15mH, I_{AS} = 6.5A \\ V_{DS} = 400V, \ T_{J(START)} = 175^{\circ}C \\ V_{DS} \le 500V \\ T_C = 25^{\circ}C \\ \end{tabular}$	-25 to +25	V
Continuous drain current ¹	I _D	T _C < 144°C	120	А
Pulsed drain current ²	I _{DM}	T _C = 25°C	588	А
Single pulsed avalanche energy ³	E _{AS}	L=15mH, I _{AS} = 6.5A	316	mJ
Short circuit withstand time ⁴	t _{sc}	V _{DS} = 400V, T _{J(START)} = 175°C	5	μs
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \le 500V$	100	V/ns
Power dissipation	P _{tot}	T _C = 25°C	1153	W
Maximum junction temperature	T _{J,max}		175	°C
Operating and storage temperature	T _J , T _{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 1	260	°C

1. Limited by bondwires

2. Pulse width t_{p} limited by $T_{J,\text{max}}$

3. Starting $T_J = 25^{\circ}C$

4. Short circuit current is independent of the gate voltage $V_{GS}{>}12V$

Thermal Characteristics

Parameter	Symbol Test Conditions -		Linite			
		Test Conditions	Min	Тур	Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.10	0.13	°C/W

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Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions		L lostes			
Parameter	Symbol	Test Conditions	Min	Тур	Max	- Units	
Drain-source breakdown voltage	BV _{DS}	V_{GS} =0V, I_{D} =1mA	750			V	
		V _{DS} =750V, V _{GS} =0V, T _J =25°C		6	130	μΑ	
Total drain leakage current	I _{DSS}	V _{DS} =750V, V _{GS} =0V, T _J =175°C		45			
Total gate leakage current	I _{GSS}	V _{DS} =0V, T _J =25°C, V _{GS} =-20V / +20V		6 20		μΑ	
		V _{GS} =12V, I _D =80A, T _J =25°C		5.4	7.2		
Drain-source on-resistance	R _{DS(on)}	V _{GS} =12V, I _D =80A, T _J =125°C		9.3		mΩ	
		V _{GS} =12V, I _D =80A, T _J =175°C		12.2			
Gate threshold voltage	V _{G(th)}	V_{DS} =5V, I_{D} =10mA	4	4.7	6	V	
Gate resistance	R _G	f=1MHz, open drain		0.8	1.5	Ω	

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions		Units			
Parameter	Symbol	Test Conditions	Min	Тур	Max	Units	
Diode continuous forward current ¹	ا _s	T _C < 144°C			120	А	
Diode pulse current ²	I _{S,pulse}	T _C =25°C			588	А	
	M	V _{GS} =0V, I _S =50A, T _J =25°C		1.03	1.16	Ň	
Forward voltage	V_{FSD}	V _{GS} =0V, I _S =50A, T _J =175°C		1.06		V	
Reverse recovery charge	Q _{rr}	V _{DS} =400V, I _S =80A, V _{GS} =0V, R _G =20Ω		440		nC	
Reverse recovery time	t _{rr}	di/dt=2800A/µs, T_=25°C		31		ns	
Reverse recovery charge	Q _{rr}	V_{DS} =400V, I _S =80A, V_{GS} =0V, R _G =20 Ω		525		nC	
Reverse recovery time	t _{rr}	di/dt=2800A/µs, T_j=150°C		37		ns	





Typical Performance - Dynamic

Devenetor	Symphol	Test Conditions		Linte		
Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Input capacitance	C _{iss}			8374		
Output capacitance	C _{oss}	- V _{DS} =400V, V _{GS} =0V - f=100kHz -		362		pF
Reverse transfer capacitance	C _{rss}			4		
Effective output capacitance, energy related	C _{oss(er)}	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		475		pF
Effective output capacitance, time related	C _{oss(tr)}	$V_{DS}=0V \text{ to } 400V,$ $V_{GS}=0V$		950		pF
C _{OSS} stored energy	E _{oss}	V _{DS} =400V, V _{GS} =0V		38		μJ
Total gate charge	Q _G	V _{DS} =400V, I _D =80A,		164		
Gate-drain charge	Q_{GD}	$V_{DS} = 0V \text{ to } 15V$		24		nC
Gate-source charge	Q _{GS}	VGS OV to ISV		46		
Turn-on delay time	t _{d(on)}			35		-
Rise time	t _r			39		ns
Turn-off delay time	t _{d(off)}			109		115
Fall time	t _f	Turn-on $R_{G,EXT}$ =1.5 Ω ,		13		
Turn-on energy including R _s energy	E _{ON}	Turn-off $R_{G,EXT}$ =5 Ω ,		766		
Turn-off energy including R_S energy	E _{OFF}	Turn-off $R_{G,EXT}=5\Omega$,inductive Load, FWD:same device with $V_{GS} = 0V$ and $R_G = 5\Omega$, RC snubber:		162		
Total switching energy	E _{TOTAL}			928		μJ
Snubber R _s energy during turn-on	E _{RS_ON}	-		17.6		•
Snubber R _s energy during turn-off	E _{RS_OFF}	T _J =25°C		7.2		
Turn-on delay time	t _{d(on)}			37		
Rise time	t _r	Notes 5 and 6, V _{DS} =400V, I _D =80A, Gate		41		-
Turn-off delay time	t _{d(off)}	Driver =0V to +15V,		114		ns
Fall time	t _f	Turn-on $R_{G,EXT}$ =1.5 Ω ,		13		
Turn-on energy including R_s energy	E _{ON}	Turn-off $R_{G,EXT}=5\Omega$, inductive Load, FWD: same		808		
Turn-off energy including R_s energy	E _{OFF}	device with V_{GS} = 0V and		187		
Total switching energy	E _{TOTAL}	$R_{\rm G} = 5\Omega$, RC snubber: - R _S =5Ω and C _S =680pF,		995		μJ
Snubber R_S energy during turn-on	E _{RS_ON}	T _J =150°C		18.3		
Snubber R_s energy during turn-off	E_{RS_OFF}			10.3		

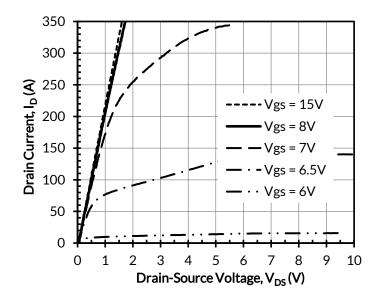
5. Measured with the switching test circuit in Figure 26.

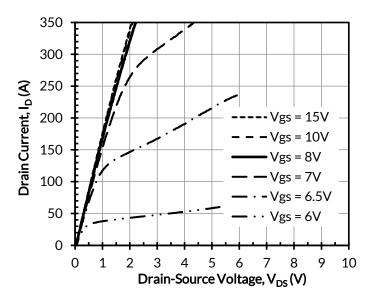
6. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

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Typical Performance Diagrams





< 250µs

Figure 1. Typical output characteristics at $T_1 = -55^{\circ}$ C, tp Figure 2. Typical output characteristics at $T_1 = 25^{\circ}$ C, tp < 250µs

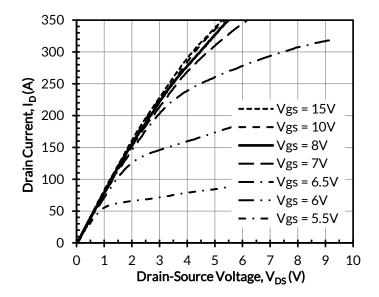


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

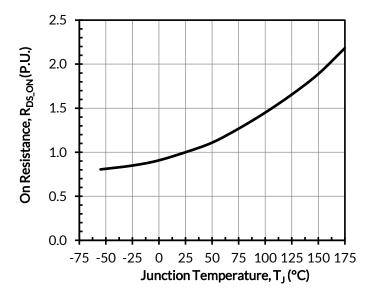


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 80A

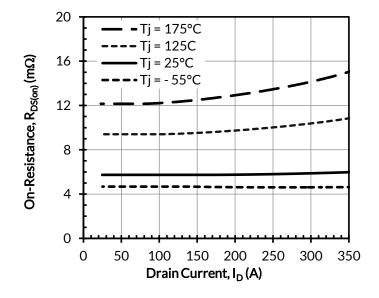


Figure 5. Typical drain-source on-resistances at V $_{\rm GS}$ = 12V

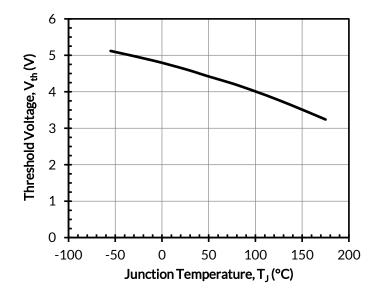
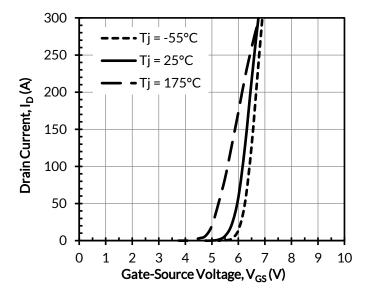


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 10mA



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Figure 6. Typical transfer characteristics at V_{DS} = 5V

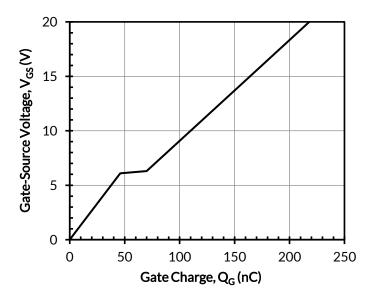


Figure 8. Typical gate charge at V_{DS} = 400V and I_{D} = 80A

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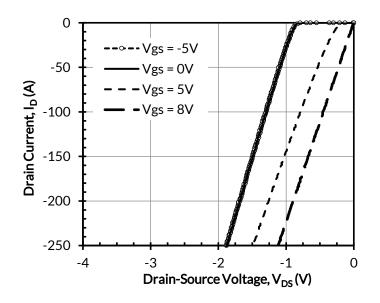


Figure 9. 3rd quadrant characteristics at $T_J = -55^{\circ}C$

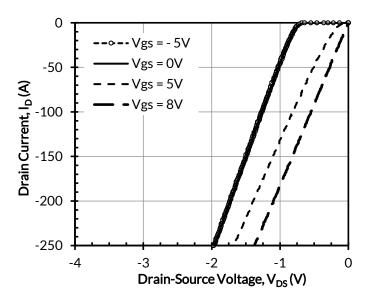


Figure 10. 3rd quadrant characteristics at $T_J = 25^{\circ}C$

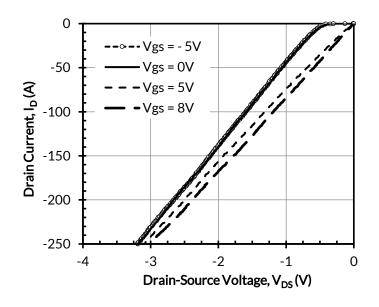


Figure 11. 3rd quadrant characteristics at T_J = 175°C

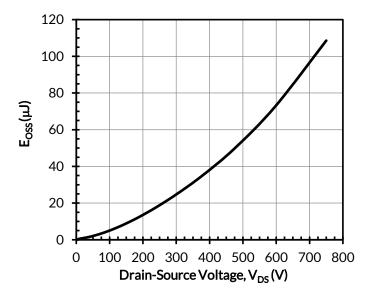


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

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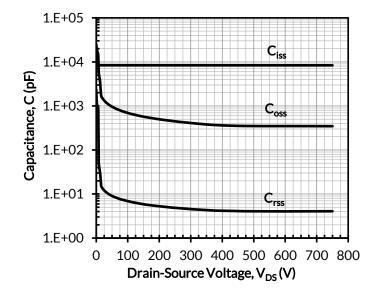
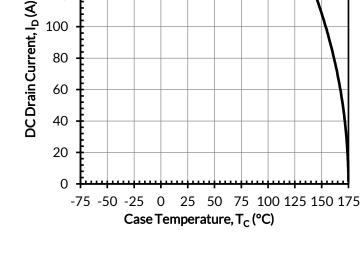


Figure 13. Typical capacitances at f = 100kHz and $V_{GS} = Figure 14$. DC drain current derating 0V



140

120

100

80

60

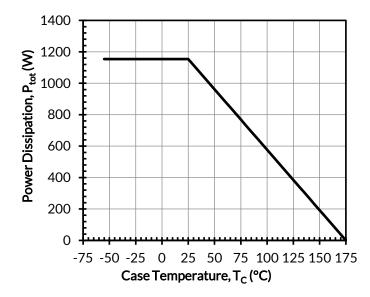


Figure 15. Total power dissipation

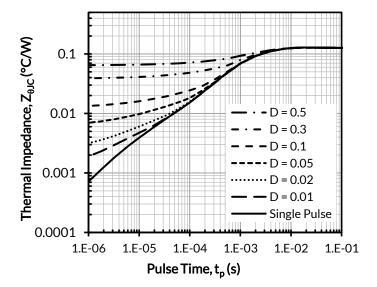


Figure 16. Maximum transient thermal impedance

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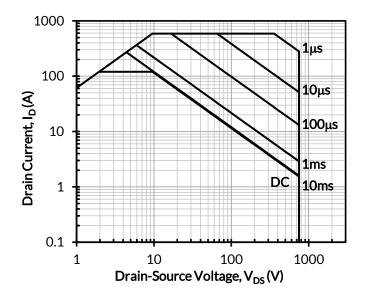
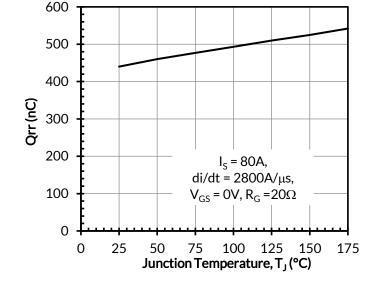


Figure 17. Safe operation area at $T_c = 25^{\circ}C$, D = 0, Parameter t_n



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Figure 18. Reverse recovery charge Qrr vs. junction temperature at V_{DS} = 400V

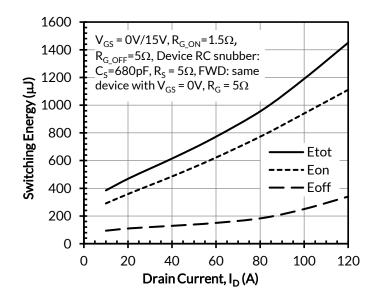
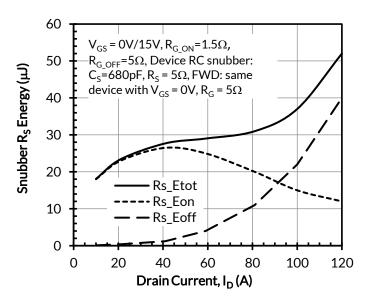


Figure 19. Clamped inductive switching energy vs. drain Figure 20. RC snubber energy loss vs. drain current at current at V_{DS} = 400V and T_J = 25°C



 V_{DS} = 400V and T_{J} = 25°C

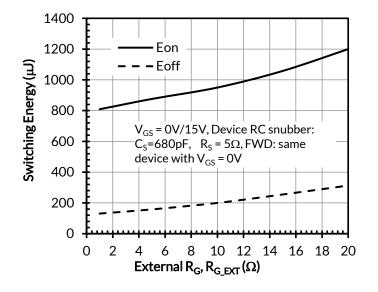
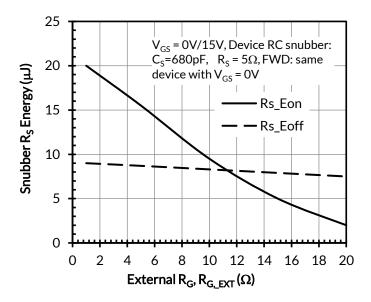


Figure 21. Clamped inductive switching energies vs. $R_{G,EXT}$ at V_{DS} = 400V, I_{D} = 80A, and T_{J} = 25°C



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Figure 22. RC snubber energy losses vs. $R_{G,EXT}$ at V_{DS} = 400V, I_D = 80A, and T_J = 25°C

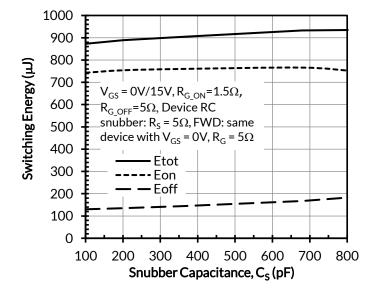


Figure 23. Clamped inductive switching energies vs. snubber capacitance C_s at V_{DS} = 400V, I_D = 80A, and T_J = capacitance C_s at V_{DS} = 400V, I_D = 80A, and T_J = 25°C 25°C

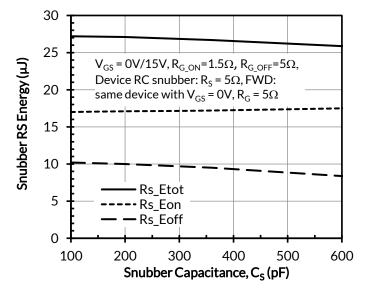


Figure 24. RC snubber energy losses vs. snubber

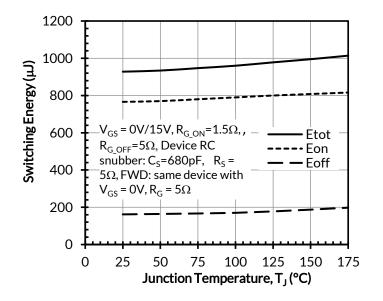
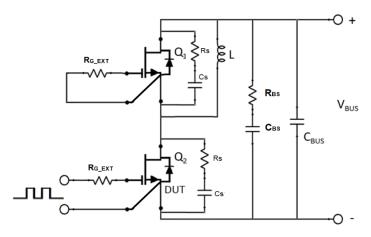


Figure 25. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_D = 80A



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Figure 26. Schematic of the half-bridge mode switching test circuit. Note, a device snubber (Rs =5 Ω , Cs = 680pF) and bus RC snubber (R_{BS} = 1 Ω , C_{BS}=100nF) is used to reduce the power loop high frequency oscillations.

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Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

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