MPQ3326A

16-Channel, 80mA/Ch, LED Driver with Separated PWM/Analog Dimming and I²C Interface, AEC-Q100 Qualified

DESCRIPTION

The MPQ3326A is a 16-channel LED driver that can operate from a wide 4.5V to 16V input voltage (V_{IN}) range. The MPQ3326A applies 16 internal current sources in each LED string terminal. The LED current (I_{LED}) of each channel is set by an external current-setting resistor. The maximum current for each channel is 80mA.

The MPQ3326A integrates an I²C interface with up to 10 configurable I²C addresses via an external resistor. This means the MPQ3326A can support up to 10 cascaded ICs to drive the LED array. Each channel can be enabled or disabled through the I²C.

The MPQ3326A employs both separated pulse-width modulation (PWM) dimming and analog dimming for each LED channel, as well as 12-bit PWM dimming and 6-bit analog dimming for each channel. The I_{LED} ramp rate and phase shift can be configured to reduce EMI.

The MPQ3326A can output a refresh signal from the RFSH/FLT pin, where the refresh signal frequency ($f_{REFRESH}$) can be set via the I²C.

Full protection features include LED open protection, LED short protection, and over-temperature protection (OTP). The device also features a fault indicator. If a protection is triggered, then the RFSH/FLT pin is pulled low, and the corresponding fault register is set.

The MPQ3326A is AEC-Q100 qualified, and is available in a QFN-24 (4mmx4mm) package.

FEATURES

- Wide 4.5V to 16V Input Voltage (V_{IN}) Range
- 16 Channels, Max 80mA/Ch
- LED Current (I_{LED}) Configured via External Resistor
- 6-Bit Analog Dimming for Each Channel
- 12-Bit Pulse-Width Modulation (PWM) Dimming for Each Channel
- Selectable 220Hz, 250Hz, 280Hz, or 330Hz PWM Dimming Frequency (f_{PWM})
- Refresh Signal Output
- I²C Interface
- 10 Addresses Configurable via External Resistor
- Configurable I_{LED} Slew Rate
- 40μs Phase Shift
- Fault Indicator
- LED Open Protection
- LED Short Protection with Configurable Threshold
- Under-Voltage Lockout (UVLO) Protection
- Over-Temperature Protection (OTP)
- Available in a QFN-24 (4mmx4mm) Package
- Available in Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Lights
- Automotive Displays
- Instruments Clusters
- General Industrial Displays

TYPICAL APPLICATION

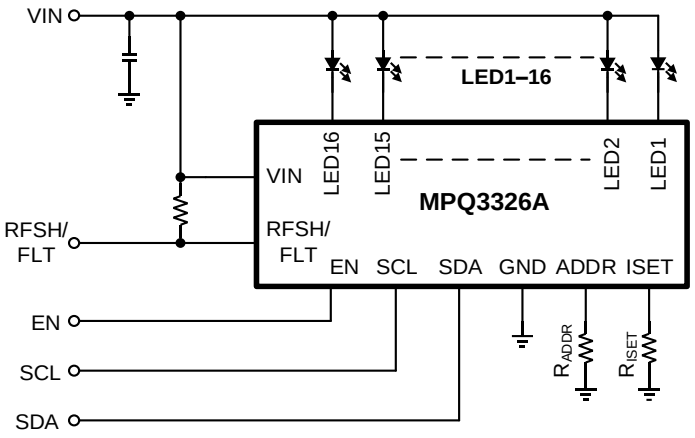


Figure 1: Typical Application Circuit

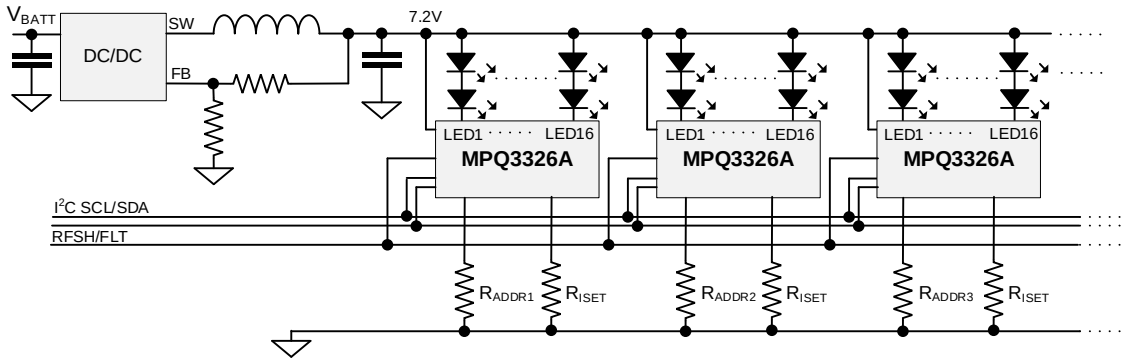


Figure 2: System Application Circuit with 2 LEDs in Series

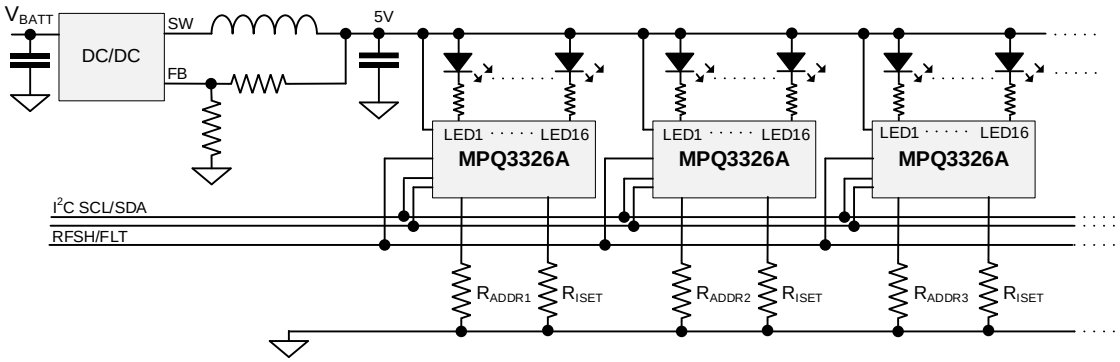


Figure 3: System Application Circuit with 1 LED and Resistor in Series

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Level**
MPQ3326AGRE-AEC1***	QFN-24 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ3326AGRE-AEC1-Z).

** Moisture Sensitivity Level Rating

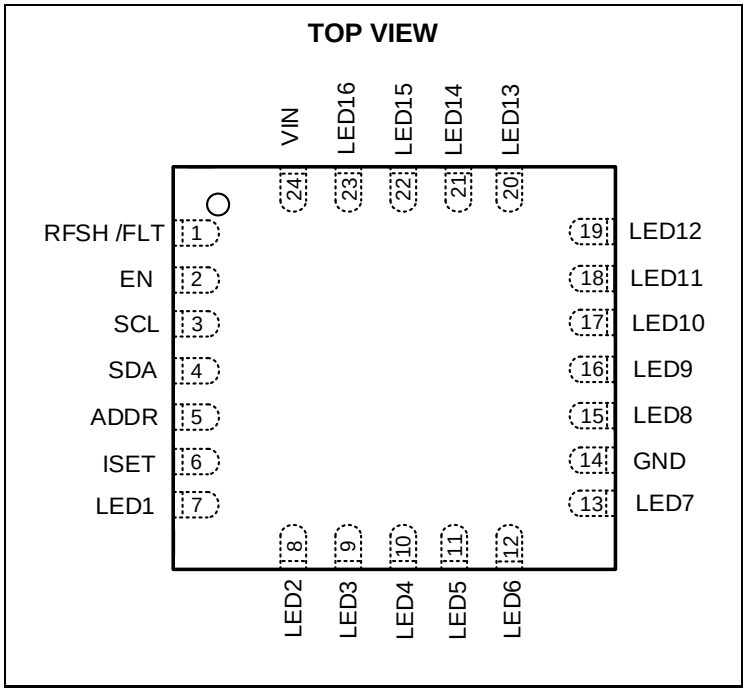
*** Wettable Flank

TOP MARKING

MPSYWW
M3326A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M3326A: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	RFSH/FLT	**Refresh signal output or fault flag.** If the FLTEN bit = 0, then the RFSH/FLT pin outputs a synchronized signal that is set by the FRFSH[9:0] register. If FLTEN = 1, RFSH/FLT indicates fault conditions and is pulled low if a fault occurs.
2	EN	**Enable control.** Pull the EN pin high to turn on the LED driver; pull EN low to turn off the LED driver.
3	SCL	**I²C interface clock input.**
4	SDA	**I²C interface data input.**
5	ADDR	**I²C address setting.** Configure the I²C addresses by connecting different resistors from ADDR to GND. ADDR can set the 4 least significant bits (LSB) of the I²C address. There are 10 configurable addresses.
6	ISET	**LED current setting.** Connect a current-setting resistor from ISET to GND to configure the current in each LED string.
7	LED1	**LED channel 1 current input.** Connect the LED channel 1 cathode to this pin.
8	LED2	**LED channel 2 current input.** Connect the LED channel 2 cathode to this pin.
9	LED3	**LED channel 3 current input.** Connect the LED channel 3 cathode to this pin.
10	LED4	**LED channel 4 current input.** Connect the LED channel 4 cathode to this pin.
11	LED5	**LED channel 5 current input.** Connect the LED channel 5 cathode to this pin.
12	LED6	**LED channel 6 current input.** Connect the LED channel 6 cathode to this pin.
13	LED7	**LED channel 7 current input.** Connect the LED channel 7 cathode to this pin.
14	GND	**Ground.**
15	LED8	**LED channel 8 current input.** Connect the LED channel 8 cathode to this pin.
16	LED9	**LED channel 9 current input.** Connect the LED channel 9 cathode to this pin.
17	LED10	**LED channel 10 current input.** Connect the LED channel 10 cathode to this pin.
18	LED11	**LED channel 11 current input.** Connect the LED channel 11 cathode to this pin.
19	LED12	**LED channel 12 current input.** Connect the LED channel 12 cathode to this pin.
20	LED13	**LED channel 13 current input.** Connect the LED channel 13 cathode to this pin.
21	LED14	**LED channel 14 current input.** Connect the LED channel 14 cathode to this pin.
22	LED15	**LED channel 15 current input.** Connect the LED channel 15 cathode to this pin.
23	LED16	**LED channel 16 current input.** Connect the LED channel 16 cathode to this pin.
24	VIN	**Power supply input.** The VIN pin supplies power to the IC. Connect a capacitor between VIN and GND.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +22V
V_{LED1} to V_{LED16} .....-0.5V to +22V
All other pins .....-0.3V to +5V
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm) 2.97W

ESD Ratings

Human body model (HBM).....Class 1C (3)
Charged device model (CDM).....Class C2b (4)

Recommended Operating Conditions

V_{IN} .....4.5V to 16V
Operating junction temp (T_J) (5).....
..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-24 (4mmx4mm)
JESD51-7 (6) ..... 42 ..... 9.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Operating devices at a junction temperature up to 150°C is possible. Please contact MPS for details.
6) Measured on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage (V_{IN}) range	V_{IN}		4.5		16	V
Quiescent supply current	I_Q				5	mA
Shutdown supply current	I_{ST}	V_{EN} = 0V, V_{IN} = 16V			2	µA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$	Rising edge	3.6	3.8	4.2	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	Falling edge	3.3	3.5	3.7	V
Enable						
EN rising threshold	V_{EN_RISING}	V_{EN} rising	2.1			V
EN falling threshold	$V_{EN\_FALLING}$	V_{EN} falling			0.8	V
EN pull-down resistance	R_{EN}			1		MΩ
RFSH/FLT						
Refresh signal frequency	$f_{REFRESH}$	FRFSH[9:0] = 0x1A9, FPWM[1:0] = 01	285	300	315	Hz
RFSH/FLT pull-down resistance	$R_{RFSH/FLT}$	FLTEN = 1, fault is triggered			100	Ω
LED Regulator						
ISET voltage	V_{ISET}	T_A = 25°C	1.176	1.2	1.224	V
LED current 1	I_{LED_1}	R_{ISET} = 24kΩ, ICHx[5:0] = 0x3F	-5%	50	+5%	mA
		R_{ISET} = 24kΩ, ICHx[5:0] = 0x3F, T_A = 25°C	-3%	50	+3%	mA
LED current 2	I_{LED_2}	R_{ISET} = 15kΩ, ICHx[5:0] = 0x3F	-5%	80	+5%	mA
		R_{ISET} = 15kΩ, ICHx[5:0] = 0x3F, T_A = 25°C	-3%	80	+3%	mA
Current sink headroom	V_{LEDx}	I_{LED} = 50mA		200	300	mV
		I_{LED} = 80mA		350	400	mV
Dimming						
Pulse-width modulation (PWM) frequency	f_{PWM}	FPWM[1:0] = 01	240	250	260	Hz
PWM duty step	t_{PWM}	12-bit resolution, f_{PWM} = 250Hz		1		µs
Phase shift	t_{DELAY}	PS_EN = 1		40		µs
LED current step		I_{LED} = 80mA, analog dimming step		1.25		mA
LED current slew rate in PWM dimming		SLEW[1:0] = 01, rising edge		5		µs
		SLEW[1:0] = 11, rising edge		20		µs
Protection						
LED short string protection threshold	V_{SLP}	STH[1:0] = 01	2.85	3	3.15	V
LED short string protection time	t_{SLP}	V_{LEDx} > STH[1:0]		4		ms
LED short string protection hiccup time	t_{SLP_HICCUP}			1		ms

ELECTRICAL CHARACTERISTICS *(continued)*

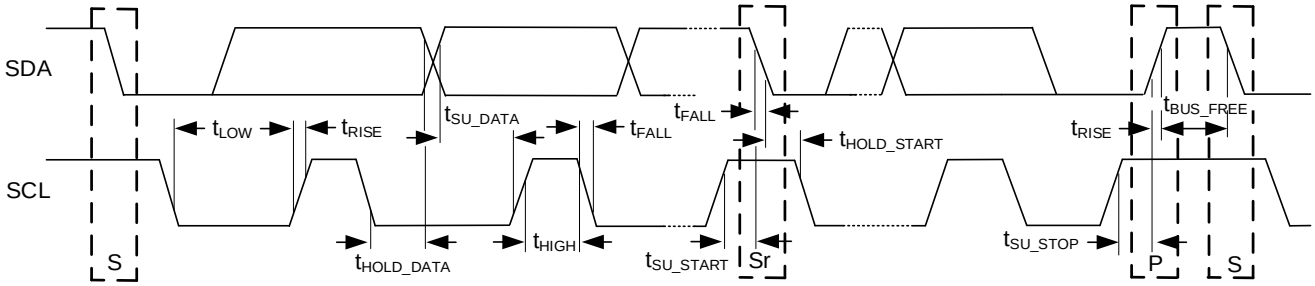
V_{IN} = 5V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED short string protection hiccup detection time	t_{SLP_DET}			32		µs
LED open string protection threshold	V_{OLP}			100	150	mV
LED open string protection time	t_{OLP}	V_{LEDx} < 100mV		4		ms
LED open string protection hiccup time	t_{OLP_HICCUP}			1		ms
LED open string protection hiccup detection time	t_{OLP_DET}			32		µs
Thermal shutdown threshold (7)	T_{SD}			170		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C
I^2C Interface						
Logic-low input voltage	V_{IN_LOW}		0		0.4	V
Logic-high input voltage	V_{IN_HIGH}		1.3			V
Logic-low output voltage (7)	V_{OUT_LOW}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (7)	f_{SCL}		10		1000	kHz
Bus free time (7)	t_{BUF_FREE}	Between stop and start condition	0.5			µs
Holding time after (repeated) start condition (7)	t_{HOLD_START}	After this period, the first clock is generated	0.26			µs
Repeated start condition set-up time (7)	t_{SU_START}		0.26			µs
Stop condition set-up time (7)	t_{SU_STOP}		0.26			µs
Data hold time (7)	t_{HOLD_DATA}		0			ns
Data set-up time (7)	t_{SU_DATA}		50			ns
Clock low timeout (7)	$t_{TIMEOUT}$		25		35	ms
Clock low time (7)	t_{LOW}		0.5			µs
Clock high time (7)	t_{HIGH}		0.26			µs
Clock/data falling time (7)	t_{FALL}				120	ns
Clock/data rising time (7)	t_{RISE}				120	ns

Note:

7) Guaranteed by characterization. Not tested in production.

I²C INTERFACE TIMING DIAGRAM



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

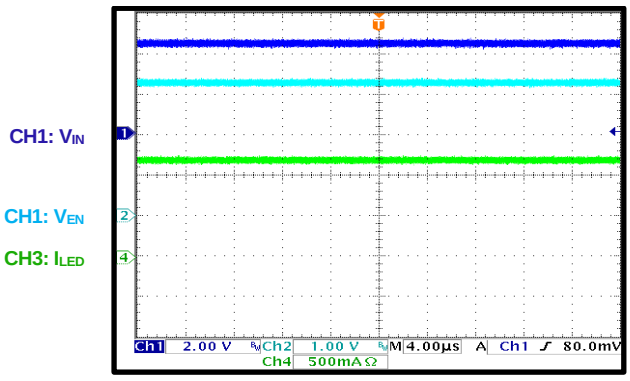
Figure 4: I²C Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

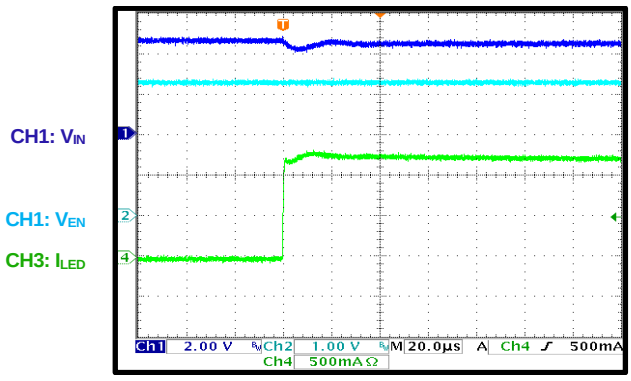
V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

Steady State

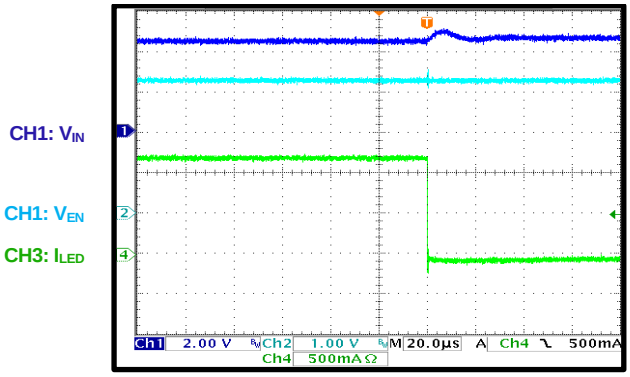
V_{IN} = 4.5V, 16P1S, 80mA/string



Start-Up via the EN Bit

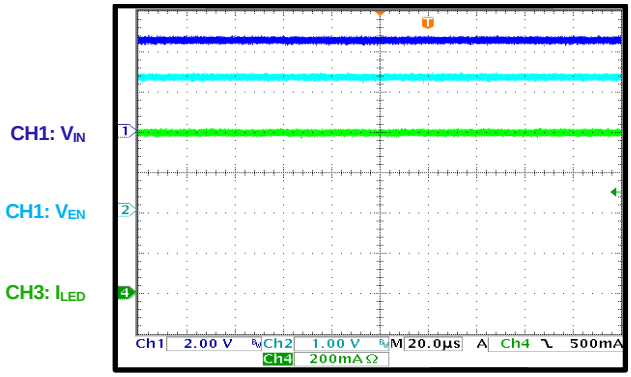


Shutdown via the EN Bit



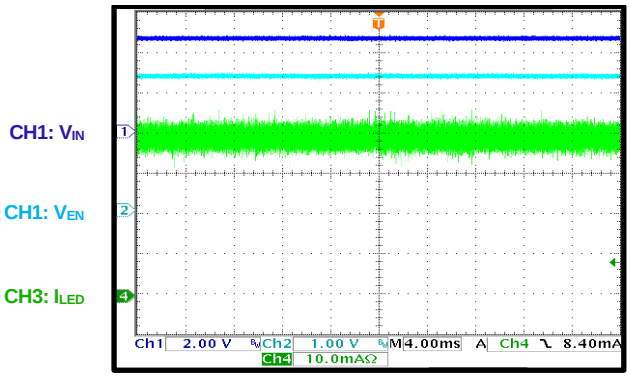
Analog Dimming

50mA/string



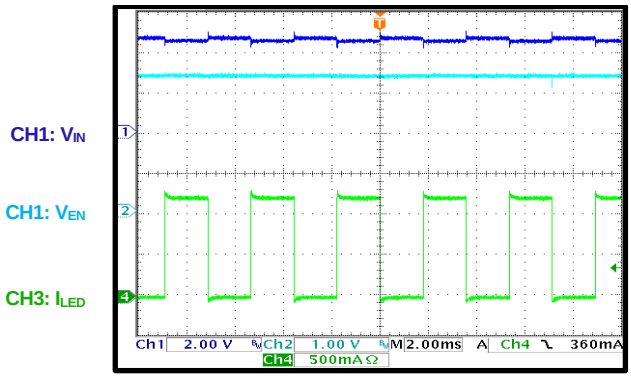
Analog Dimming

2.5mA/string



PWM Dimming

PWM duty = 50%

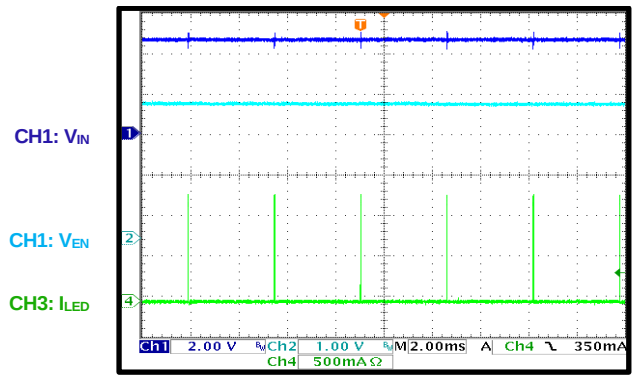


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

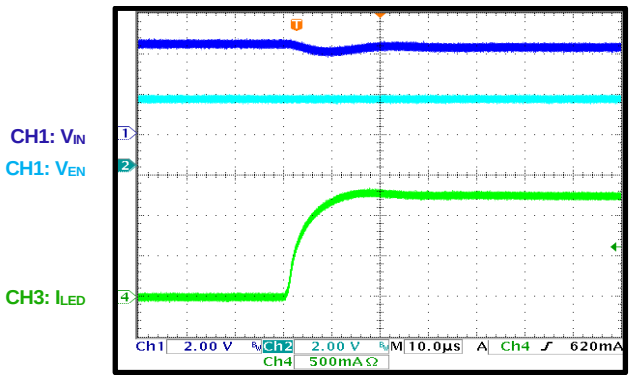
PWM Dimming

PWM duty = 0.5%



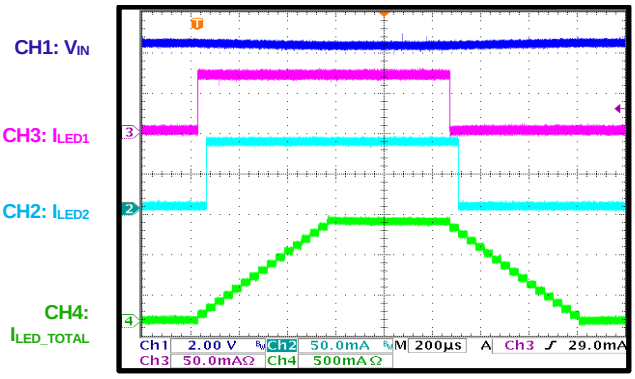
Slew Rate

PWM dimming slew rate = 5µs



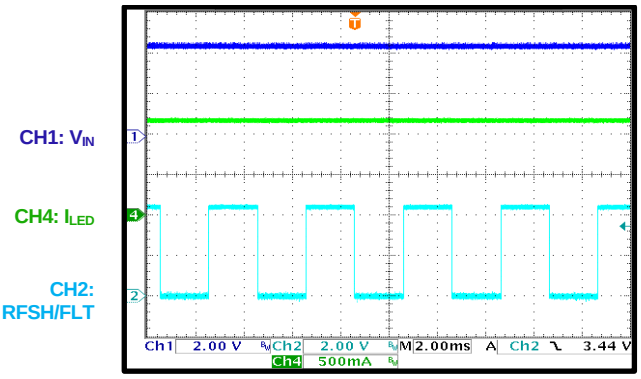
Phase Shift

PWM dimming duty = 20%



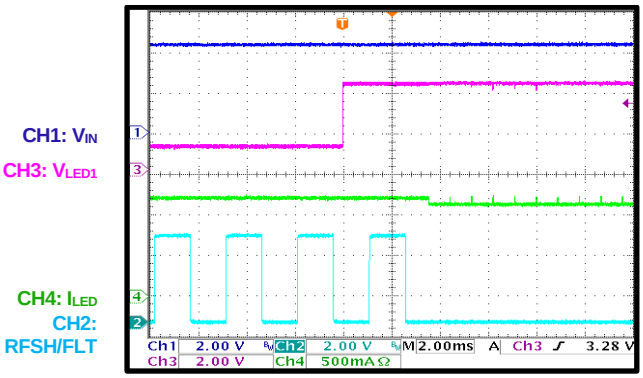
Refresh Function

f_{PWM} = 250Hz, RFRSH[9:0] = 0x1FF



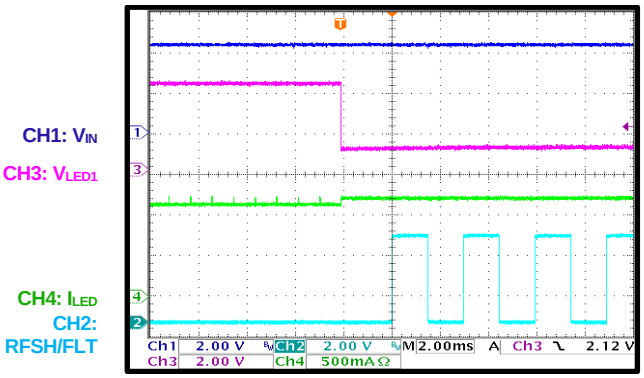
LEDx Short Entry

RFSH/FLT fault enabled, f_{PWM} = 330Hz, RFRSH[9:0] = 0x1FF



LEDx Short Recovery

RFSH/FLT fault enabled, f_{PWM} = 330Hz, RFRSH[9:0] = 0x1FF

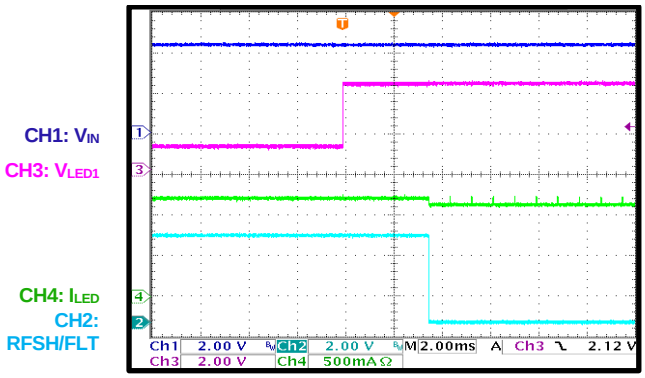


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4.5V, I_{LED} = 80mA per string, LED = 16P1S, T_A = 25°C, unless otherwise noted.

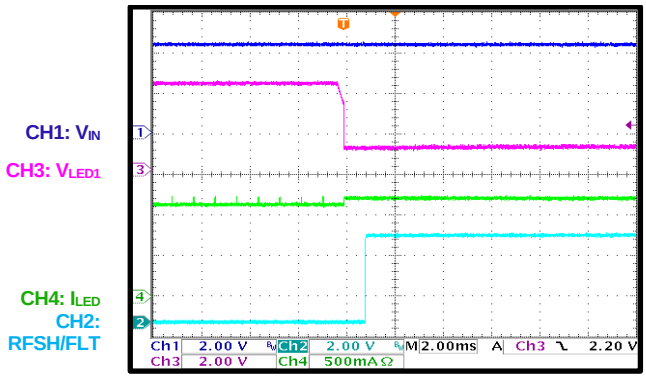
LEDx Short Entry

RFSH/FLT fault enabled, f_{PWM} = 250Hz,
RFRSH[9:0] = 0x000



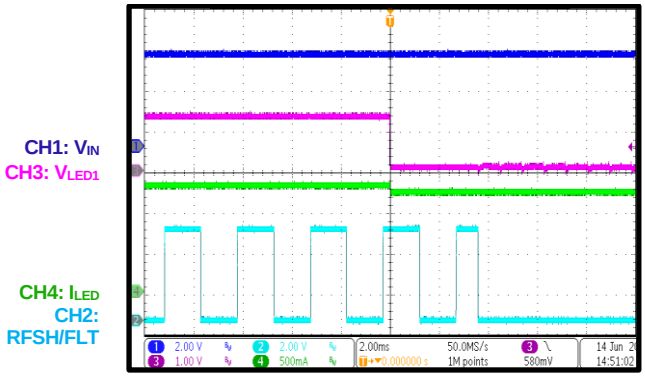
LEDx Short Recovery

RFSH/FLT fault enabled, f_{PWM} = 250Hz,
RFRSH[9:0] = 0x000



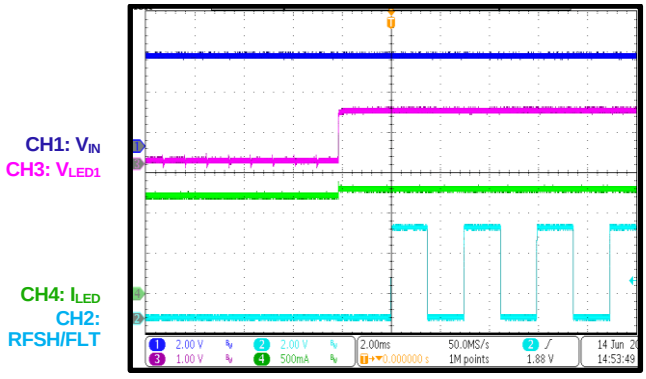
LEDx Open Entry

RFSH/FLT fault enabled, f_{PWM} = 330Hz,
RFRSH[9:0] = 0x1FF



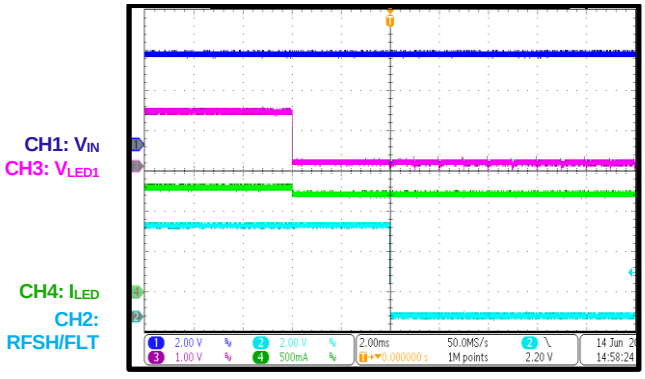
LEDx Open Recovery

RFSH/FLT fault enabled, f_{PWM} = 330Hz,
RFRSH[9:0] = 0x1FF



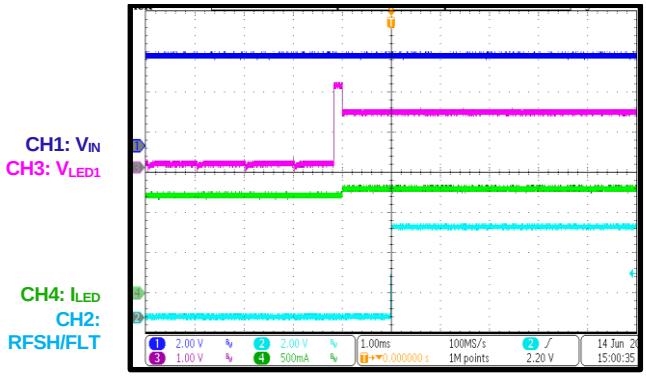
LEDx Open Entry

RFSH/FLT fault enabled, f_{PWM} = 250Hz,
RFRSH[9:0] = 0x000



LEDx Open Recovery

RFSH/FLT fault enabled, f_{PWM} = 250Hz,
RFRSH[9:0] = 0x000



FUNCTIONAL BLOCK DIAGRAM

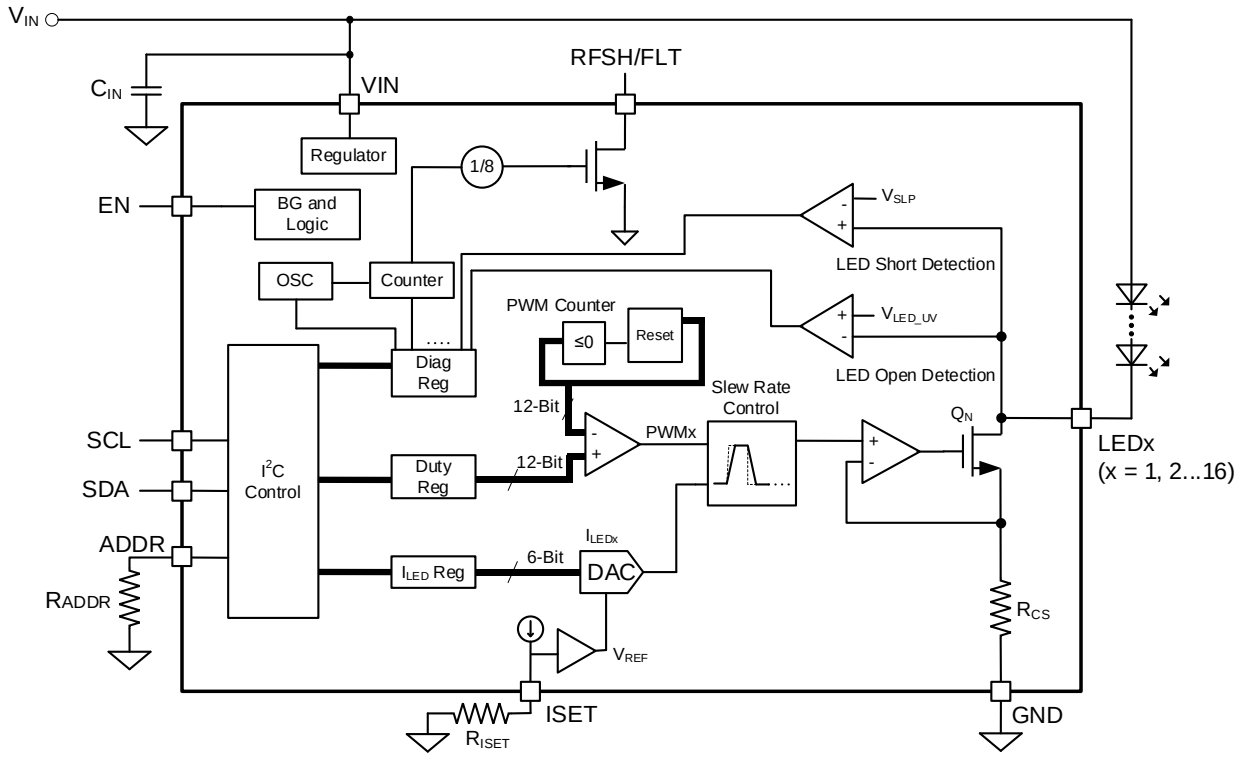


Figure 5: Functional Block Diagram

OPERATION

The MPQ3326A applies 16 internal current sources in each LED string terminal. The LED current (I_{LED}) of all the channels is set via an external current-setting resistor, with a maximum current up to 80mA.

Enable (EN) and Start-Up

Once the input voltage (V_{IN}) exceeds its under-voltage lockout (UVLO) rising threshold ($V_{IN\_UVLO\_RISING}$) and the EN pin's voltage (V_{EN}) exceeds its rising threshold (V_{EN_RISING}), the MPQ3326A enters standby mode and the I^2C interface is active. After setting the I^2C register, set the EN bit high to start up the system. The start-up sequence is as follows:

1. V_{IN}
2. V_{EN}
3. I^2C setting
4. Set the EN bit

Channel Selection

The channels can be disabled by pulling the corresponding CHxEN bit (where x = 1, 2…16) low.

Dimming

Each channel includes a separate 6-bit analog dimming register and 12-bit pulse-width modulation (PWM) dimming register. The MPQ3326A can support analog dimming and PWM dimming for each channel.

In analog dimming, the I_{LED} amplitude changes when the analog dimming register changes. Change the code in ICHx (x = 1, 2…16) to apply analog dimming for the corresponding channel. I_{LED} can be estimated with Equation (1):

$$I_{LED} = \frac{ICHx}{63} \times I_{SET} \quad (1)$$

Where ICHx is the analog dimming code for channel x (where x = 1, 2…16). If ICHx is set to 0, then the corresponding I_{LED} is 0A.

In PWM dimming, I_{LED} is a PWM waveform, the I_{LED} amplitude remains the same, and the I_{LED} duty varies with the PWM dimming register.

The PWM dimming duty (D_{PWM}) is set by the register PWMx (x = 1, 2…16), and it can be calculated with Equation (2):

$$D_{PWM} = \frac{PWMx}{4095} \quad (2)$$

Where PWMx is the D_{PWM} code for channel x (where x = 1, 2…16).

The duty changes only when the PWM duty register's 8 most significant bits (MSB) are written. If PWMx is set to 0, then the corresponding I_{LED} is 0A.

The PWM dimming frequency (f_{PWM}) can be selected via register FPWM[1:0]. Table 1 shows the FPWM[1:0] register setting for different PWM frequencies.

Table 1: PWM Frequency Setting

FPWM[1:0]	f_{PWM}
00	220Hz
01	250Hz (default)
10	280Hz
11	330Hz

To avoid glitches during normal operation, follow the steps below:

1. Change the FPWM[1:0] value only when the EN bit is set 0.
2. Write the FPWM register, then resume writing to the other registers after a 10µs delay.

Phase Shift

The channel-by-channel phase-shift function is enabled by setting the PS_EN bit high.

When the phase shift function is enabled, the rising edge of each channel occurs 40µs after the previous channel. This means that the rising edge of the channel x + 1 (where x = 1, 2…15) I_{LED} occurs 40µs after the rising edge of channel x's I_{LED}.

Synchronized Output for LCD Refresh Frequency

The fault indicator function can be enabled via the FLTEN bit.

If FLTEN = 0, the fault indicator function is disabled and the RFSH/FLT pin maintains the output refresh signal, even when a protection is triggered.

If FLTEN = 1, the fault indication is enabled and RFSH/FLT is pulled low when a fault occurs.

Table 2 shows the RFSH/FLT output status, which depends on the fault condition.

Table 2: RFSH/FLT Output Status

FLTEN	FRFSH[9:0] = 0x000		FRFSH[9:0] = 0x001 to 0x3FF	
	No Fault	Fault	No Fault	Fault
1	Pull high externally	Low	Rectangular signal	Low
0	Pull high externally		Rectangular signal	

The refresh signal frequency ($f_{REFRESH}$) is set by FRFSH[9:0]. If FRFSH[9:0] = 0x000, then RFSH/FLT outputs high. If FRFSH[9:0] = 0x001~0x3FF, then RFSH/FLT outputs a rectangular signal. $f_{REFRESH}$ can be calculated with Equation (3):

$$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} \text{ (Hz)} \quad (3)$$

Where FRFSH is the FRFSH[9:0] value (>0), and f_{PWM} is set by register FPWM[1:0]. f_{PWM} can be set to 220Hz, 250Hz, 280Hz, or 330Hz.

Note that all values in Equation (5) are decimal-based and $f_{REFRESH}$ does not change until the 8MSB are written.

The internal oscillator is divided by 8. As the clock refreshes the frequency generation, the FRFSH[9:0] register sets the counter number (see Figure 6).

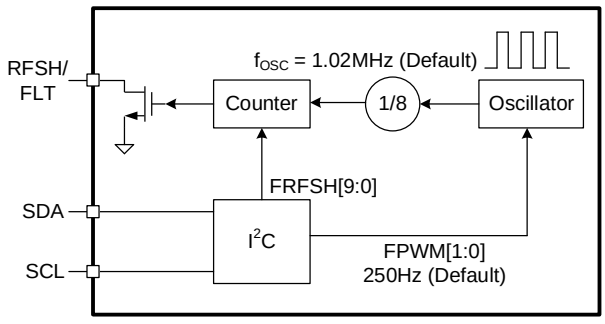


Figure 6: Refresh Frequency Generation

LED Current Slew Rate Control

To reduce EMI, change the I_{LED} rising and falling slew rate in PWM dimming. The I_{LED} rising and falling slew rate is controlled by the SLEW[1:0] register. Table 3 shows the SLEW[1:0] register settings for different slew rates.

Table 3: Slew Rate Setting

SLEW[1:0]	Slew Rate
00	No slew rate
01	5μs
10	10μs
11	20μs

Protections

The MPQ3326A employs V_{IN} UVLO protection, LED short protection, LED open protection, and thermal shutdown.

The RFSH/FLT pin is an active-low, open-drain output that is pulled high to an external voltage source. If a fault occurs, the corresponding fault bit is set and RFSH/FLT is pulled low.

For LED open and short protection, hiccup mode or latch-off mode can be selected via the LATCH bit in the I²C.

If LATCH = 1, the MPQ3326A enters latch-off mode once a fault occurs. The fault channel remains off until either VIN or EN turns off and resets. After the fault bit is read, FRSH/FLT is pulled high and the fault bit sets. If the fault bit is read again, then the fault bit resets.

If LATCH = 0, the MPQ3326A enters hiccup mode, during which the fault channel tries to conduct for 32μs every 1ms to detect whether the fault has been cleared. Once the fault condition is removed, FRSH/FLT is automatically pulled high and the fault bit resets when it is read.

V_{IN} Under-Voltage Lockout (UVLO) Protection

When V_{IN} reaches its UVLO threshold, the IC shuts down and all the I²C registers are reset.

LED Open Protection

The LEDx (x = 1, 2…16) voltage (V_{LEDx}) drops when an LED is open. If V_{LEDx} drops below the protection threshold (about 100mV) for 4ms, then LED open protection is triggered. In this scenario, the fault channel turns off, the corresponding open fault bit (CHxO, where x = 1, 2…16) is set, and RFSH/FLT is pulled low.

LED Short Protection

If there is an LED short condition, and V_{LEDx} (x = 1, 2…16) exceeds the voltage set by STH[1:0] for 4ms, then LED short protection is triggered. The short channel turns off, the corresponding

fault bit (CHxS, where x = 1, 2…16) is set, and RFSH/FLT is pulled low.

The LED short protection threshold (V_{SLP}) is configured via the STH[1:0] register. Table 4 shows the STH[1:0] register setting for different LED short protection thresholds.

Table 4: LED Short Protection Threshold Setting

STH[1:0]	V_{SLP}
00	2V
01	3V
10	4V
11	5V

Over-Temperature Protection (OTP)

If the IC temperature exceeds 170°C, then over-temperature protection (OTP) is triggered, all channels turn off, RFSH/FLT is pulled low, and FT_OTP is set. Once the temperature drops by about 150°C, all the channels turn on again and the IC resumes normal operation.

I²C INTERFACE

I²C Chip Address

The device address is 0x30~0x39, which can be configured via the ADDR resistor (R_{ADDR}). The internal current source flows to R_{ADDR}, and the ADDR voltage (V_{ADDR}) determines the I²C address. Ten different addresses can be configured via R_{ADDR}.

Table 5 shows the various resistor ratio (R_{ADDR} / R_{ISET}) configurations to set the I²C address.

Table 5: I²C Address Setting

R_{ADDR}, R_{ISET}	I²C Address (A3, A2, A1, A0)
<0.05	0000
>0.05, <0.15	0001
>0.15, <0.25	0010
>0.25, <0.35	0011
>0.35, <0.45	0100
>0.45, <0.55	0101
>0.55, <0.65	0110
>0.65, <0.75	0111
>0.75, <0.85	1000
>0.85, <0.95	1001

At start-up, the IC checks the I²C address first. This address remains the same during operation until the IC's power is reset.

After a start (S) condition, the I²C-compatible master sends a 7-bit address, followed by an eighth data direction bit (where 1 = read and 0 = write). The eighth bit indicates the register address to/from which the data is written/read (see Figure 7).

0	1	1	A3	A2	A1	A0	R/W

Figure 7: I²C-Compatible Device Address

To avoid glitches during normal operation, follow the steps below:

1. Change the FPWM[1:0] value only when the EN bit is set to 0.
2. Write the FPWM[1:0] register, then resume writing to the other registers after a 10μs delay.

I²C REGISTER MAP

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
00h	01	RESERVED						FPWM [1:0]	
01h	00	FLTEN	LATCH	STH[1:0]		SLEW[1:0]		PS_EN	EN
02h	01	RESERVED					FT_OTP	FRFSH[1:0]	
03h	6A	FRFSH[9:2]							
04h	FF	CH16EN	CH15EN	CH14EN	CH13EN	CH12EN	CH11EN	CH10EN	CH9EN
05h	FF	CH8EN	CH7EN	CH6EN	CH5EN	CH4EN	CH3EN	CH2EN	CH1EN
06h	00	CH16O	CH15O	CH14O	CH13O	CH12O	CH11O	CH10O	CH9O
07h	00	CH8O	CH7O	CH6O	CH5O	CH4O	CH3O	CH2O	CH1O
08h	00	CH16S	CH15S	CH14S	CH13S	CH12S	CH11S	CH10S	CH9S
09h	00	CH8S	CH7S	CH6S	CH5S	CH4S	CH3S	CH2S	CH1S
0Ah	3F	RESERVED		ICH1[5:0]					
0Bh	0F	RESERVED				PWM1[3:0]			
0Ch	FF	PWM1[11:4]							
0Dh	3F	RESERVED		ICH2[5:0]					
0Eh	0F	RESERVED				PWM2[3:0]			
0Fh	FF	PWM2[11:4]							
10h	3F	RESERVED		ICH3[5:0]					
11h	0F	RESERVED				PWM3[3:0]			
12h	FF	PWM3[11:4]							
13h	3F	RESERVED		ICH4[5:0]					
14h	0F	RESERVED				PWM4[3:0]			
15h	FF	PWM4[11:4]							
16h	3F	RESERVED		ICH5[5:0]					
17h	0F	RESERVED				PWM5[3:0]			
18h	FF	PWM5[11:4]							
19h	3F	RESERVED		ICH6[5:0]					
1Ah	0F	RESERVED					PWM6[3:0]		
1Bh	FF	PWM6[11:4]							
1Ch	3F	RESERVED		ICH7[5:0]					
1Dh	0F	RESERVED				PWM7[3:0]			
1Eh	FF	PWM7[11:4]							
1Fh	3F	RESERVED		ICH8[5:0]					
20h	0F	RESERVED				PWM8[3:0]			
21h	FF	PWM8[11:4]							
22h	3F	RESERVED		ICH9[5:0]					
23h	0F	RESERVED					PWM9[3:0]		
24h	FF	PWM9[11:4]							
25h	3F	RESERVED		ICH10[5:0]					
26h	0F	RESERVED					PWM10[3:0]		
27h	FF	PWM10[11:4]							
28h	3F	RESERVED		ICH11[5:0]					
29h	0F	RESERVED					PWM11[3:0]		

I²C REGISTER MAP *(continued)*

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
2Ah	FF	PWM11[11:4]							
2Bh	3F	RESERVED		ICH12[5:0]					
2Ch	0F	RESERVED					PWM12[3:0]		
2Dh	FF	PWM12[11:4]							
2Eh	3F	RESERVED		ICH13[5:0]					
2Fh	0F	RESERVED					PWM13[3:0]		
30h	FF	PWM13[11:4]							
31h	3F	RESERVED		ICH14[5:0]					
32h	0F	RESERVED					PWM14[3:0]		
33h	FF	PWM14[11:4]							
34h	3F	RESERVED		ICH15[5:0]					
35h	0F	RESERVED					PWM15[3:0]		
36h	FF	PWM15[11:4]							
37h	3F	RESERVED		ICH16[5:0]					
38h	0F	RESERVED					PWM16[3:0]		
39h	FF	PWM16[11:4]							

I²C REGISTER DESCRIPTION

REG00h: PWM Dimming Frequency Setting Register

Addr: 0x00				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:2	N/A	R	000000	Reserved.
1:0	FPWM[1:0]	RW	01	Sets the pulse-width modulation (PWM) dimming frequency. 00: 220Hz 01: 250Hz 10: 280Hz 11: 330Hz To avoid glitches during operation, follow the steps below: 1. Change the FPWM[1:0] value only when the EN bit is set to 0. 2. Write the FPWM[1:0] register, then resume writing to the other registers after a 10μs delay.

REG01h: Control Register

Addr: 0x01				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	FLTEN	RW	0	Enables the RFSH/FLT fault indicator. 0: Disabled. RFSH/FLT refreshes the signal output 1: Enabled. RFSH/FLT indicates if a fault has occurred
6	LATCH	RW	0	Enables latch-off mode. 0: Disabled. Hiccup mode used if a fault occurs 1: Enabled. Latch-off mode enabled if a fault occurs
5:4	STH[1:0]	RW	00	Sets the LED short protection threshold (V_{SLP}). 00: 2V 01: 3V 10: 4V 11: 5V
3:2	SLEW[1:0]	RW	00	Sets the LED current (I_{LED}) slew rate. 00: No slew rate 01: 5μs 10:10μs 11: 20μs
1	PS_EN	RW	0	Enables the phase shift. 0: Disabled 1: Enabled. The rising edge of channel x + 1 (where x = 1, 2…15) I_{LED} occurs 40μs after the rising edge of channel x's I_{LED}
0	EN	RW	0	Enables the IC. 0: Disabled 1: Enabled

REG02h: Refresh Frequency Setting and Over-Temperature (OT) Fault Register

Addr: 0x02				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:3	N/A	R	0	Reserved.
2	FT_OTP	R	0	Indicates whether an over-temperature (OT) fault has occurred. 0: No OT fault has occurred 1: An OT fault has occurred
1:0	FRFSH[1:0]	RW	01	Sets the 2 least significant bits (LSB) of the refresh frequency ($f_{REFRESH}$). FRFSH[9:0] = 0x000, outputs a high voltage FRFSH[9:0] > 0, $f_{REFRESH}$ can be calculated with the following equation: $f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250}$ (Hz) All of the values in the equation are decimal-based and $f_{REFRESH}$ does not change until the 8 most significant bits (MSB) are written. The default $f_{REFRESH}$ is 300Hz.

REG03h: Refresh Frequency Setting Register

Addr: 0x03				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	FRFSH[9:2]	RW	6A	Sets the 8 most significant bits (MSB) of $f_{REFRESH}$. FRFSH[9:0] = 0x000, outputs a high voltage FRFSH[9:0] > 0, $f_{REFRESH}$ can be calculated with the following equation: $f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250}$ (Hz) Where all values in the equation are decimal-based and $f_{REFRESH}$ does not change until the 8MSB are written. The default $f_{REFRESH}$ is 300Hz.

REG04h: Channel Enable Register (Channels 9–16)

Addr: 0x04				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH16EN	RW	1	Enables channel 16. 0: Disabled 1: Enabled
6	CH15EN	RW	1	Enables channel 15. 0: Disabled 1: Enabled
5	CH14EN	RW	1	Enables channel 14. 0: Disabled 1: Enabled
4	CH13EN	RW	1	Enables channel 13. 0: Disabled 1: Enabled
3	CH12EN	RW	1	Enables channel 12. 0: Disabled 1: Enabled
2	CH11EN	RW	1	Enables channel 11. 0: Disabled 1: Enabled
1	CH10EN	RW	1	Enables channel 10. 0: Disabled 1: Enabled
0	CH9EN	RW	1	Enables channel 9. 0: Disabled 1: Enabled

REG05h: Channel Enable Register (Channels 1–8)

Addr: 0x05				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH8EN	RW	1	Enables channel 8. 0: Disabled 1: Enabled
6	CH7EN	RW	1	Enables channel 7. 0: Disabled 1: Enabled
5	CH6EN	RW	1	Enables channel 6. 0: Disabled 1: Enabled
4	CH5EN	RW	1	Enables channel 5. 0: Disabled 1: Enabled
3	CH4EN	RW	1	Enables channel 4. 0: Disabled 1: Enabled
2	CH3EN	RW	1	Enables channel 3. 0: Disabled 1: Enabled
1	CH2EN	RW	1	Enables channel 2. 0: Disabled 1: Enabled
0	CH1EN	RW	1	Enables channel 1. 0: Disabled 1: Enabled

REG06h: Channel Open Fault Register (Channels 9–16)

Addr: 0x06				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH16O	R	0	Channel 16 open protection fault flag. 0: No fault 1: Fault
6	CH15O	R	0	Channel 15 open protection fault flag. 0: No fault 1: Fault
5	CH14O	R	0	Channel 14 open protection fault flag. 0: No fault 1: Fault
4	CH13O	R	0	Channel 13 open protection fault flag. 0: No fault 1: Fault
3	CH12O	R	0	Channel 12 open protection fault flag. 0: No fault 1: Fault
2	CH11O	R	0	Channel 11 open protection fault flag. 0: No fault 1: Fault
1	CH10O	R	0	Channel 10 open protection fault flag. 0: No fault 1: Fault
0	CH9O	R	0	Channel 9 open protection fault flag. 0: No fault 1: Fault

REG07h: Channel Open Fault Register (Channels 1–8)

Addr: 0x07				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH8O	R	0	Channel 8 open protection fault flag. 0: No fault 1: Fault
6	CH7O	R	0	Channel 7 open protection fault flag. 0: No fault 1: Fault
5	CH6O	R	0	Channel 6 open protection fault flag. 0: No fault 1: Fault
4	CH5O	R	0	Channel 5 open protection fault flag. 0: No fault 1: Fault
3	CH4O	R	0	Channel 4 open protection fault flag. 0: No fault 1: Fault
2	CH3O	R	0	Channel 3 open protection fault flag. 0: No fault 1: Fault
1	CH2O	R	0	Channel 2 open protection fault flag. 0: No fault 1: Fault
0	CH1O	R	0	Channel 1 open protection fault flag. 0: No fault 1: Fault

REG08h: Channel Short Fault Register (Channels 9–16)

Addr: 0x08				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH16S	R	0	Channel 16 short protection fault flag. 0: No fault 1: Fault
6	CH15S	R	0	Channel 15 short protection fault flag. 0: No fault 1: Fault
5	CH14S	R	0	Channel 14 short protection fault flag. 0: No fault 1: Fault
4	CH13S	R	0	Channel 13 short protection fault flag. 0: No fault 1: Fault
3	CH12S	R	0	Channel 12 short protection fault flag. 0: No fault 1: Fault
2	CH11S	R	0	Channel 11 short protection fault flag. 0: No fault 1: Fault
1	CH10S	R	0	Channel 10 short protection fault flag. 0: No fault 1: Fault
0	CH9S	R	0	Channel 9 short protection fault flag. 0: No fault 1: Fault

REG09h: Channel Short Fault Register (Channels 1–8)

Addr: 0x09				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	CH8S	R	0	Channel 8 short protection fault flag. 0: No fault 1: Fault
6	CH7S	R	0	Channel 7 short protection fault flag. 0: No fault 1: Fault
5	CH6S	R	0	Channel 6 short protection fault flag. 0: No fault 1: Fault
4	CH5S	R	0	Channel 5 short protection fault flag. 0: No fault 1: Fault
3	CH4S	R	0	Channel 4 short protection fault flag. 0: No fault 1: Fault
2	CH3S	R	0	Channel 3 short protection fault flag. 0: No fault 1: Fault
1	CH2S	R	0	Channel 2 short protection fault flag. 0: No fault 1: Fault
0	CH1S	R	0	Channel 1 short protection fault flag. 0: No fault 1: Fault

REG0Ah: Channel 1 LED Current Setting Register

Addr: 0x0A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH1[5:0]	RW	111111	Sets the channel 1 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG0Bh: Channel 1 PWM Dimming Duty Setting Register (LSB)

Addr: 0x0B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM1[3:0]	RW	1111	Sets the 4LSB for the channel 1 I_{LED} PWM dimming duty (D_{PWM}). D_{PWM} only changes when the 8MSB are written.

REG0Ch: Channel 1 PWM Dimming Duty Setting Register (MSB)

Addr: 0x0C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM1[11:4]	RW	11111111	Sets the 8MSB for the channel 1 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG0Dh: Channel 2 LED Current Setting Register

Addr: 0x0D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH2[5:0]	RW	111111	Sets the channel 2 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times I_{SET}$

REG0Eh: Channel 2 PWM Dimming Duty Setting Register (LSB)

Addr: 0x0E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM2[3:0]	RW	1111	Sets the 4LSB for the channel 2 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG0Fh: Channel 2 PWM Dimming Duty Setting Register (MSB)

Addr: 0x0F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM2[11:4]	RW	11111111	Sets the 8MSB for the channel 2 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG10h: Channel 3 LED Current Setting Register

Addr: 0x10				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH3[5:0]	RW	111111	Sets the channel 3 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times I_{SET}$

REG11h: Channel 3 PWM Dimming Duty Setting Register (LSB)

Addr: 0x11				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM3[3:0]	RW	1111	Sets the 4LSB for the channel 3 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG12h: Channel 3 PWM Dimming Duty Setting Register (MSB)

Addr: 0x12				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM3[11:4]	RW	11111111	Sets the 8MSB for the channel 3 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG13h: Channel 4 LED Current Setting Register

Addr: 0x13				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH4[5:0]	RW	111111	Sets the channel 4 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG14h: Channel 4 PWM Dimming Duty Setting Register (LSB)

Addr: 0x14				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM4[3:0]	RW	1111	Sets the 4LSB for the channel 4 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG15h: Channel 4 PWM Dimming Duty Setting Register (MSB)

Addr: 0x15				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM4[11:4]	RW	11111111	Sets the 8MSB for the channel 4 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG16h: Channel 5 LED Current Setting Register

Addr: 0x16				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH5[5:0]	RW	111111	Sets the channel 5 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG17h: Channel 5 PWM Dimming Duty Setting Register (LSB)

Addr: 0x17				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM5[3:0]	RW	1111	Sets the 4LSB for the channel 5 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG18h: Channel 5 PWM Dimming Duty Setting Register (MSB)

Addr: 0x18				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM5[11:4]	RW	11111111	Sets the 8MSB for the channel 5 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG19h: Channel 6 LED Current Setting Register

Addr: 0x19				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH6[5:0]	RW	111111	Sets the channel 6 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG1Ah: Channel 6 PWM Dimming Duty Setting Register (LSB)

Addr: 0x1A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM6[3:0]	RW	1111	Sets the 4LSB for the channel 6 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG1Bh: Channel 6 PWM Dimming Duty Setting Register (MSB)

Addr: 0x1B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM6[11:4]	RW	11111111	Sets the 8MSB for the channel 6 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG1Ch: Channel 7 LED Current Setting Register

Addr: 0x1C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH7[5:0]	RW	111111	Sets the channel 7 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG1Dh: Channel 7 PWM Dimming Duty Setting Register (LSB)

Addr: 0x1D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM7[3:0]	RW	1111	Sets the 4LSB for the channel 7 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG1Eh: Channel 7 PWM Dimming Duty Setting Register (MSB)

Addr: 0x1E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM7[11:4]	RW	11111111	Sets the 8MSB for the channel 7 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG1Fh: Channel 8 LED Current Setting Register

Addr: 0x1F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH8[5:0]	RW	111111	Sets the channel 8 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times I_{SET}$

REG20h: Channel 8 PWM Dimming Duty Setting Register (LSB)

Addr: 0x20				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM8[3:0]	RW	1111	Sets the 4LSB for the channel 8 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG21h: Channel 8 PWM Dimming Duty Setting Register (MSB)

Addr: 0x21				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM8[11:4]	RW	11111111	Sets the 8MSB for the channel 8 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG22h: Channel 9 LED Current Setting Register

Addr: 0x22				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH9[5:0]	RW	111111	Sets the channel 9 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times I_{SET}$

REG23h: Channel 9 PWM Dimming Duty Setting Register (LSB)

Addr: 0x22				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM9[3:0]	RW	1111	Sets the 4LSB for the channel 9 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG24h: Channel 9 PWM Dimming Duty Setting Register (MSB)

Addr: 0x24				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM9[11:4]	RW	11111111	Sets the 8MSB for the channel 9 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG25h: Channel 10 LED Current Setting Register

Addr: 0x25				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH10[5:0]	RW	111111	Sets the channel 10 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG26h: Channel 10 PWM Dimming Duty Setting Register (LSB)

Addr: 0x26				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM10[3:0]	RW	1111	Sets the 4LSB for the channel 10 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG27h: Channel 10 PWM Dimming Duty Setting Register (MSB)

Addr: 0x27				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM10[11:4]	RW	11111111	Sets the 8MSB for the channel 10 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG28h: Channel 11 LED Current Setting Register

Addr: 0x28				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH11[5:0]	RW	111111	Sets the channel 11 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG29h: Channel 11 PWM Dimming Duty Setting Register (LSB)

Addr: 0x29				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM11[3:0]	RW	1111	Sets the 4LSB for the channel 11 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG2Ah: Channel 11 PWM Dimming Duty Setting Register (MSB)

Addr: 0x2A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM11[11:4]	RW	11111111	Sets the 8MSB for the channel 11 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG2Bh: Channel 12 LED Current Setting Register

Addr: 0x2B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH12[5:0]	RW	111111	Sets the channel 12 I_{LED} for analog dimming, which can be calculated with the following equation: $$I_{LED} = \frac{Code}{63} \times I_{SET}$$

REG2Ch: Channel 12 PWM Dimming Duty Setting Register (LSB)

Addr: 0x2C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM12[3:0]	RW	1111	Sets the 4LSB for the channel 12 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG2Dh: Channel 12 PWM Dimming Duty Setting Register (MSB)

Addr: 0x2D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM12[11:4]	RW	11111111	Sets the 8MSB for the channel 12 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG2Eh: Channel 13 LED Current Setting Register

Addr: 0x2E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH13[5:0]	RW	111111	Sets the channel 13 I_{LED} for analog dimming, which can be calculated with the following equation: $$I_{LED} = \frac{Code}{63} \times I_{SET}$$

REG2Fh: Channel 13 PWM Dimming Duty Setting Register (LSB)

Addr: 0x2F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM13[3:0]	RW	1111	Sets the 4LSB for the channel 13 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG30h: Channel 13 PWM Dimming Duty Setting Register (MSB)

Addr: 0x30				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM13[11:4]	RW	11111111	Sets the 8MSB for the channel 13 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG31h: Channel 14 LED Current Setting Register

Addr: 0x31				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH14[5:0]	RW	111111	Sets the channel 14 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG32h: Channel 14 PWM Dimming Duty Setting Register (LSB)

Addr: 0x32				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM14[3:0]	RW	1111	Sets the 4LSB for the channel 14 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG33h: Channel 14 PWM Dimming Duty Setting Register (MSB)

Addr: 0x33				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM14[11:4]	RW	11111111	Sets the 8MSB for the channel 14 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG34h: Channel 15 LED Current Setting Register

Addr: 0x34				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH15[5:0]	RW	111111	Sets the channel 15 I_{LED} for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

REG35h: Channel 15 PWM Dimming Duty Setting Register (LSB)

Addr: 0x35				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM15[3:0]	RW	1111	Sets the 4LSB for the channel 15 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG36h: Channel 15 PWM Dimming Duty Setting Register (MSB)

Addr: 0x36				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM15[11:4]	RW	11111111	Sets the 8MSB for the channel 15 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG37h: Channel 16 LED Current Setting Register

Addr: 0x37				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	N/A	R	00	Reserved.
5:0	ICH16[5:0]	RW	111111	Sets the channel 16 I_{LED} for analog dimming, which can be calculated with the following equation: $$I_{LED}=\frac{Code}{63}\times I_{SET}$$

REG38h: Channel 16 PWM Dimming Duty Setting Register (LSB)

Addr: 0x38				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	N/A	R	0000	Reserved.
3:0	PWM16[3:0]	RW	1111	Sets the 4LSB for the channel 16 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

REG39h: Channel 16 PWM Dimming Duty Setting Register (MSB)

Addr: 0x39				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM16[11:4]	RW	11111111	Sets the 8MSB for the channel 16 I_{LED} D_{PWM}. D_{PWM} only changes when the 8MSB are written.

APPLICATION INFORMATION

LED Current Setting

Connect a resistor from the ISET pin to GND to set I_{LED} for all 16 channels. I_{LED} can be calculated with Equation (4):

$$I_{LED}(mA)=\frac{1200}{R_{ISET}(k\Omega)} \quad (4)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 8 and following the guidelines below:

1. Place the VIN capacitor close to the VIN pin.
2. Add some vias in the capacitor's GND.
3. Ensure that the traces from the LED anode to the LEDx pins are wide enough to support the set current (up to 80mA).

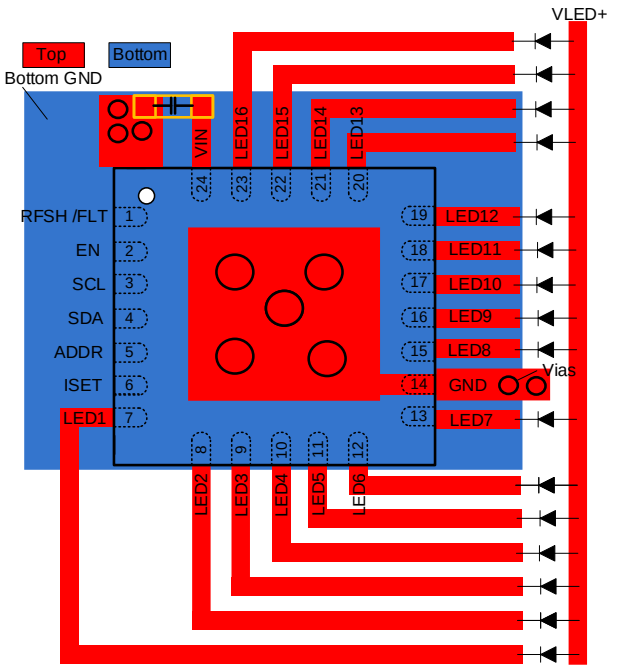


Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

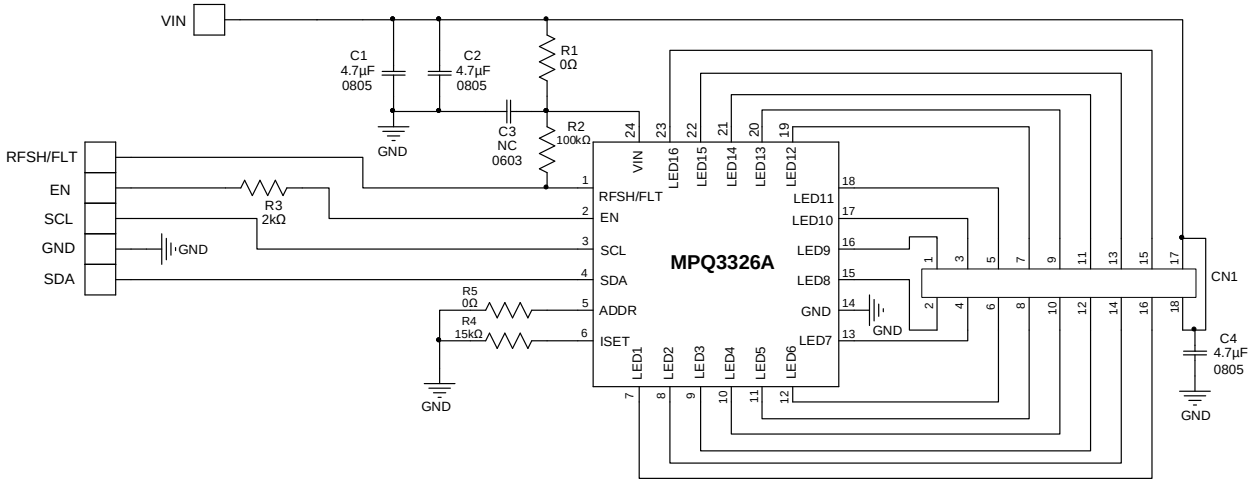


Figure 9: Typical Application Circuit (I_{LED} = 80mA/Channel)

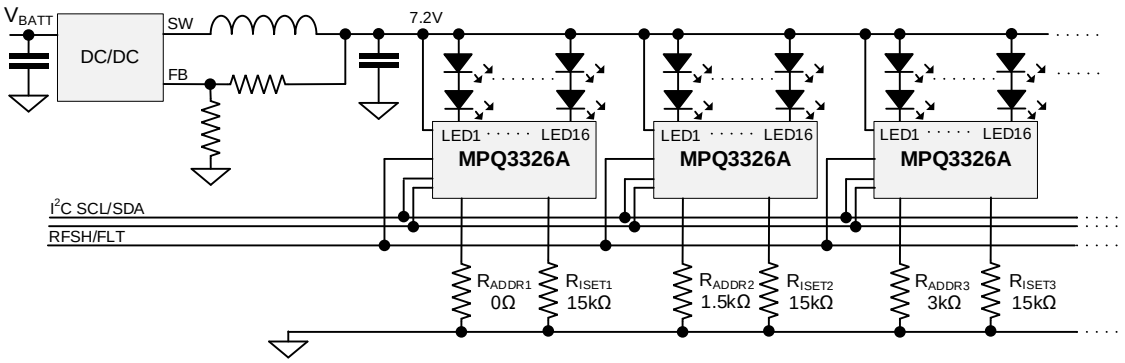
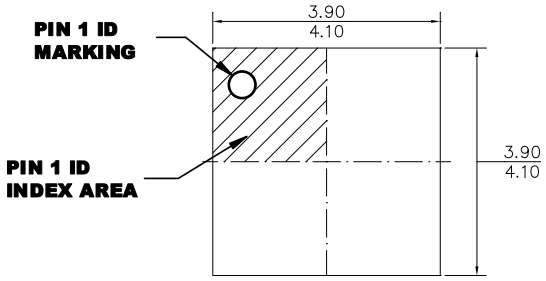


Figure 10: Typical System Application Circuit (2 LED in Series, I_{LED} = 80mA/Channel)

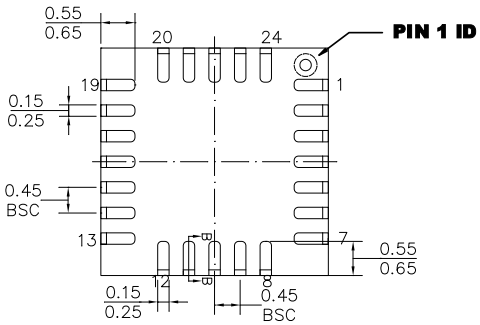
PACKAGE INFORMATION

QFN-24 (4mmx4mm)

Wettable Flank

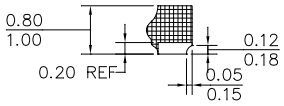


TOP VIEW

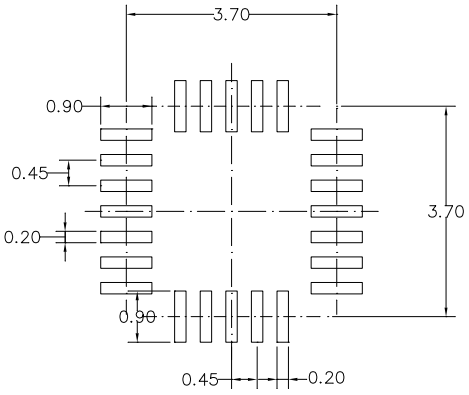


BOTTOM VIEW

SIDE VIEW



SECTION B-B

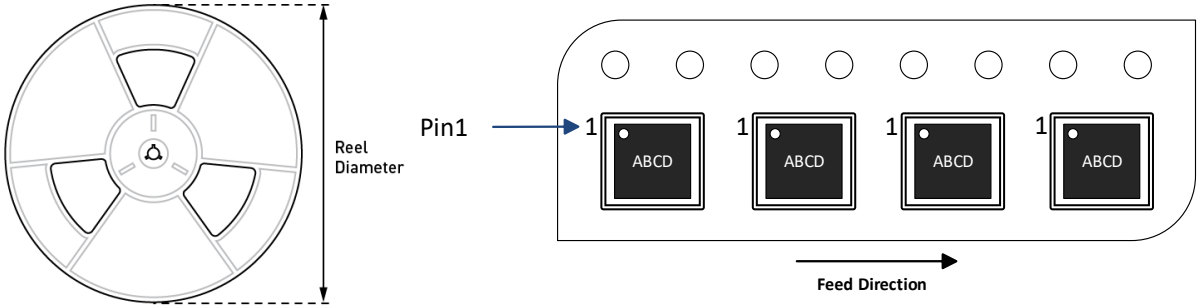


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3326AGRE-AEC1-Z	QFN-24 (4mmx4mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/7/2022	Initial Release	-