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TSC1641

Datasheet

60 V, 16-bit high-precision power monitor with I²C and MIPI I3C interface

DFN10 (3x3 mm)

Maturity status link
TSC1641

Features

- 16-bit resolution dual-channel sigma-delta ADC
- 2.7 V to 3.6 V power supply voltage
- From 128 µs to 32.7 ms total conversion time
- Bidirectional current, high-side, or low-side sensing
- Load voltage sensing from 0 V to 60 V
- Ultra-low input bias current: 20 pA typical at V_{CM} = 12 V
- Ultra-low shutdown current: 50 nA typical
- Shunt offset voltage: ±3 µV typical
- Shunt and load voltage gain error: 0.5% maximum
- Internal die temperature monitoring
- MIPI I3C up to 12.5 MHz
- I²C bus interface up to 1 MHz
- Default I²C address: 1000000(b) to 1000011(b)
- SMBus alert compatible
- Alert signals generated in case of over/undervoltage, over/undercurrent, overpower, or overtemperature
- Extended temperature range: -40 °C to 125 °C
- DFN10 3 x 3 mm² package

Applications

- Industrial battery packs
- Power inverters
- DC power supplies
- Data centers
- Telecom equipment
- Power tools

Description

The TSC1641 is a high-precision current, voltage power, and temperature monitoring analog front-end (AFE). It monitors current into a shunt resistor and load voltage up to 60 V in a synchronized way. The current measurement can be high-side, low-side, and bidirectional.

The device integrates high-precision 16-bit dual-channel ADC with a programmable conversion time from 128 µs to 32.7 ms.

Digital bus interface is flexible from I²C/SMbus 1 MHz data rate to MIPI I3C 12.5 MHz data rate. This allows connectivity to most of the recent STM32 products.

The TSC1641 allows the assertion of several alerts regarding the voltage, current, power and temperature. Thresholds can be set for each parameter in a specific register.

The TSC1641 comes in a plastic DFN10 package and can operate from -40 °C to 125 °C ambient temperature.

1 Block diagram and pin description

Figure 1. **Block diagram**

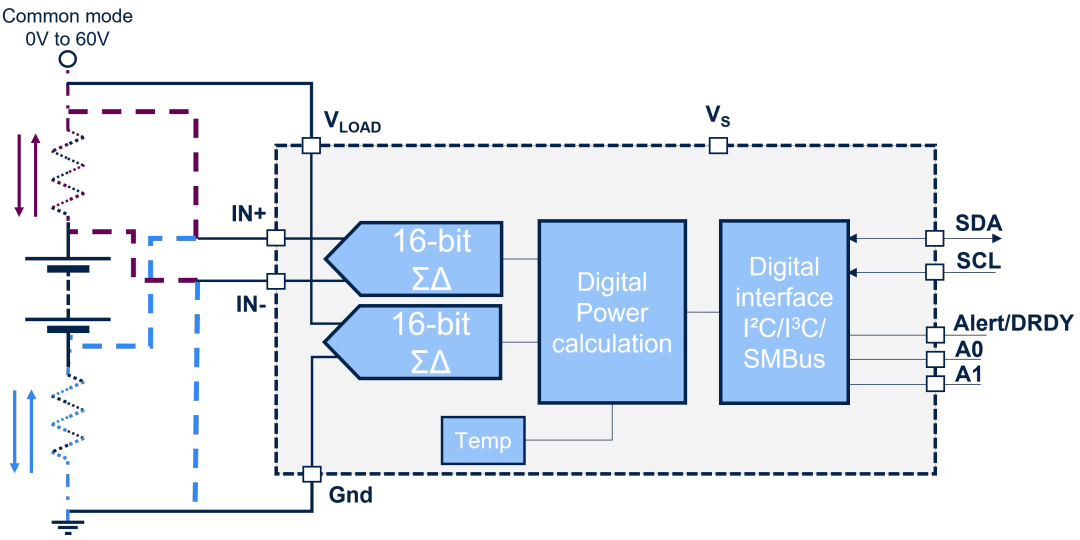


Figure 2. **Pin connections (top view – not to scale)**

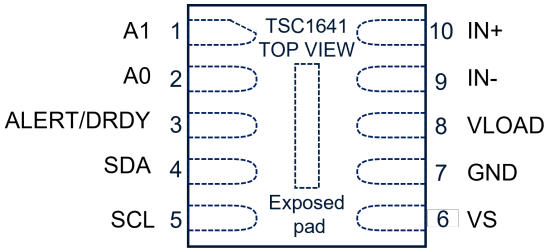


Table 1. **Pin description**

Pin	Pin name	Type	Description
1	A1	Digital input	I²C mode: A1 is a digital input to select the address of the target. See Table 6 for pin settings and the corresponding addresses. I3C mode: A1 is used to set static address (priority vs. virtual address).
2	A0	Digital input	I²C mode: A0 is a digital input to select the address of the target. See Table 6 for pin settings and the corresponding addresses. I3C mode: A0 is used to set static address (priority vs. virtual address).
3	ALERT/DRDY	Digital output	Multi-functional digital alert pin. Open-drain output in I²C. To be connected with a pull-up resistor. Not connected in I3C. Default state is active-low.
4	SDA	Digital input/output	Digital I/O, serial bus data line, open-drain input/output in I²C/ SMbus, open-drain or push-pull in MIPI I3C mode.
5	SCL	Digital input	Digital input, serial bus clock line.
6	V_S	Power supply	Power supply for the device, range is 2.7 V to 3.6 V.
7	GND	Ground	Ground reference point.
8	V_{LOAD}	Analog input	Analog input, the load voltage input from 0 V to 60 V.
9	IN-	Analog input	Analog input, lower side of the shunt resistor.
10	IN+	Analog input	Analog input, upper side of the shunt resistor.
-	Exposed pad	-	No electrical connection. Should be left floating.

2 Absolute maximum ratings and operation conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S (1)	Maximum supply voltage	-0.3 to 7	V
Vi	Maximum applied voltage on digital inputs	-0.3 to 7	V
V_{LOAD}	Load power supply maximum voltage	-0.3 to 65	V
VIN_D	Differential voltage between IN+ and IN-	-65 to 65	V
V_{IN+},V_{IN-}	Maximum analog input voltage on IN+, IN-	0 to 65	V
Tstg	Maximum storage temperature	-65 to 150	°C
Tj	Maximum junction temperature	+150	°C
Rthja	Junction to ambient thermal resistance (for DFN10) On a 2S2P JEDEC board, as per JESD51-9, area of 8.7 cm²	76	°C/W
Rthjc	Junction to case thermal resistance (for DFN10)	1	°C/W
Iout	Maximum open-drain digital output current	10	mA
Ii (2)	Maximum input current applied on any pin	±10	mA
ESD	Human body model (HBM)	2000	V
	Charged device model (CDM)	500	V

1. *All voltages are with respect to the network ground terminal.*
2. *When the input voltage of any pin exceeds the power supplies (that is VIN < GND or VIN > VS), the current on that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supply with an input current of 10 mA to two.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_S	Power supply voltage	2.7 to 3.6	V
V_{IN+},V_{IN-}	Analog input voltage on IN+, IN-	0 to 60	V
T	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

V_S = 3.3 V, V_{SENSE} = V_{IN+} - V_{IN-} = 0 V, V_{LOAD} = 48 V, $V_{CM} = \frac{V_{IN+} + V_{IN-}}{2} = 0V$, Ta = 25 °C.

Table 4. Electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Inputs						
V_{SENSE}	Shunt voltage input range		-81.9175		81.92	mV
V_{LOAD}	Load voltage input range		0		60	V
CMRR	Common mode rejection	0 V ≤ V_{CM} ≤ 48 V		115		dB
SRn_{Load}	Maximum measurable negative slew-rate on load voltage			80		V/s
VO_S	Shunt offset voltage			+/-3	+/-30	µV
	Shunt offset voltage drift vs. temperature	-40 °C ≤ T ≤ 125 °C		0.2		µV/°C
PSRR_S	Shunt offset voltage vs. power supply	2.7 V ≤ V_S ≤ 3.6 V		-15		LSB/V
IB	Input bias current (IN+, IN- pins)	V_{CM} = 12 V		20		pA
	Continuous conversion mode	V_{CM} = 48 V		70		pA
	V_{LOAD} input impedance			840		kΩ
DC accuracy						
	ADC native resolution			16		Bits
LSB_S	1 LSB step size for shunt			2.5		µV
LSB_L	1 LSB step size for load			2		mV
	Shunt voltage gain error	V_{IN-} = 0 V, V_{IN+} = 70 mV		±0.2	±0.5	%
	Shunt voltage gain error vs. temperature	-40 °C ≤ T ≤ 125 °C		±20		ppm/°C
	Load voltage gain error			±0.2	±0.5	%
	Load voltage gain error vs. temperature	-40 °C ≤ T ≤ 125 °C		±25		ppm/°C
DNL	Differential non-linearity	Conversion time = 128 µs		± 0.5		LSB
t_{CT}	ADC conversion time for current and voltage (1)	Config bits CT3-CT0=0000		128		µs
		Config bits CT3-CT0=0001		256		µs
		Config bits CT3-CT0=0010		512		µs
		Config bits CT3-CT0=0011		1024		µs
		Config bits CT3-CT0=0100		2048		µs
		Config bits CT3-CT0=0101		4096		µs
		Config bits CT3-CT0=0110		8192		µs
		Config bits CT3-CT0=0111		16384		µs
		Config bits CT3-CT0=1000		32768		µs
Clock source						
F_{OSC}	Internal oscillator frequency		3.8	4	4.2	MHz

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
SMBus						
Timeout	SMbus timeout	Resets the interface if SCL is low in this timing	25		35	ms
Temperature sensor characteristics						
	Accuracy			+/-1	+/-3	°C
	Accuracy vs. temperature	-40 °C ≤ T ≤ 125 °C		+/-2		°C
	LSB step size			0.5		°C
	ADC conversion time for temperature			8.192		ms
Digital characteristics						
	Input capacitance			3		pF
	Leakage input current	$0 V \le V_{SCL} \le V_S$		0.1	1	µA
		$0 V \le V_{SDA} \le V_S$				
		$0 V \le V_{Alert} \le V_S$				
		$0 V \le V_{A0} \le V_S$				
		$0 V \le V_{A1} \le V_S$				
V_{IH}	Input high voltage	I²C and I3C interface	$0.7xV_S$		V_S	V
V_{IL}	Input low voltage	I²C and I3C interface	GND		$0.3xV_S$	
V_{OL}	Low-level output voltage	I²C interface : I_{OL} = 8 mA	GND		0.27	V
	SDA, ALERT pins	MIPI I3C : I_{OL} = 3 mA			0.27	
V_{OH}	High-level output voltage	I²C interface : I_{OH} = - 8 mA	V_S-0.27		V_S	
	SDA, ALERT pins	MIPI I3C, push-pull only: I_{OH}= - 3 mA	V_S-0.27			
	Hysteresis			$0.1xV_S$		mV
Power supply characteristics						
V_S	Operating supply range		2.7	3.3	3.6	V
I_{DD}	Supply current	Shutdown mode (0h) in configuration register		50		nA
	Supply current	Idle mode (4h)		265		µA
	Supply current	Continuous mode (5h) or (6h)		650	800	mA
	Supply current	Continuous mode (7h)		1	1.2	mA
	Supply current	Continuous mode (7h) and temperature sensing		1.1	1.4	mA
V_{POR}	Power-on reset negative threshold		1.7	1.8	1.82	V
	Hysteresis		50	65	150	mV

1. *ADC conversion time is subject to internal clock accuracy.*

4 Typical characteristics

T_A = 25 °C V_S = 3.3 V, V_{LOAD} = 48 V, V_{IN+} = V_{IN-} = 0 V, unless otherwise stated.

Figure 3. Shunt input offset voltage production distribution (V_{CM} = 0 V)

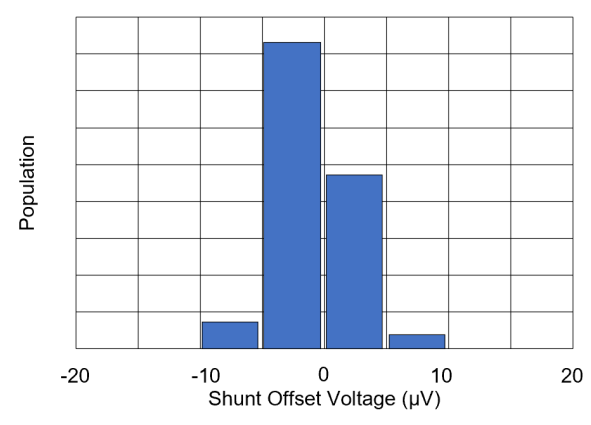


Figure 4. Shunt input offset voltage production distribution (V_{CM} = 48 V)

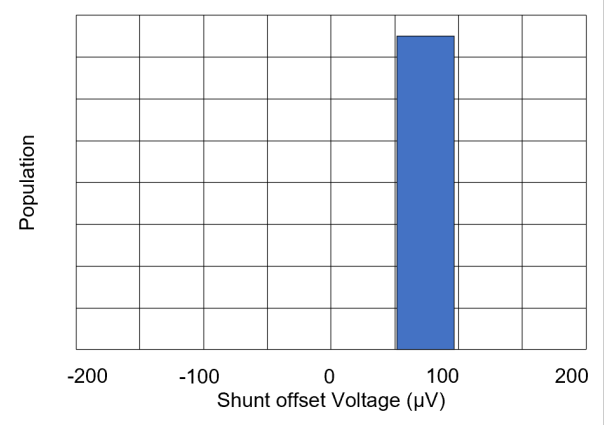


Figure 5. Shunt input offset voltage vs. temperature

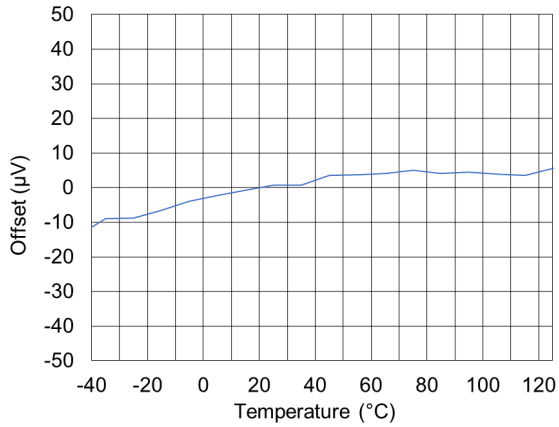


Figure 6. Common-mode rejection ratio production distribution

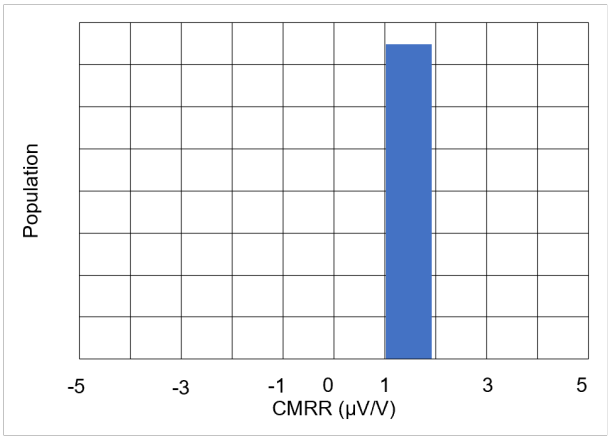


Figure 7. Shunt input common-mode rejection ratio vs. temperature

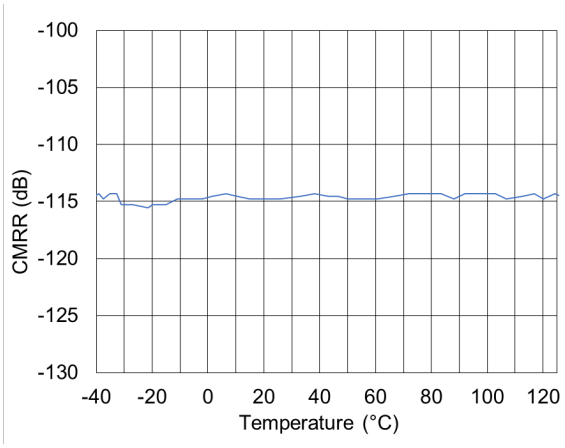


Figure 8. Shunt input gain error production distribution

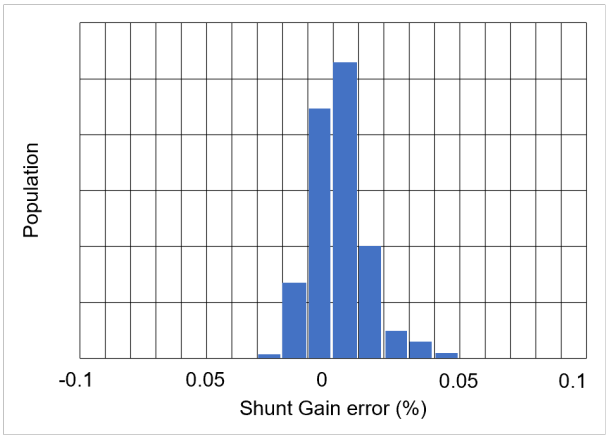


Figure 9. Shunt input gain error vs. temperature

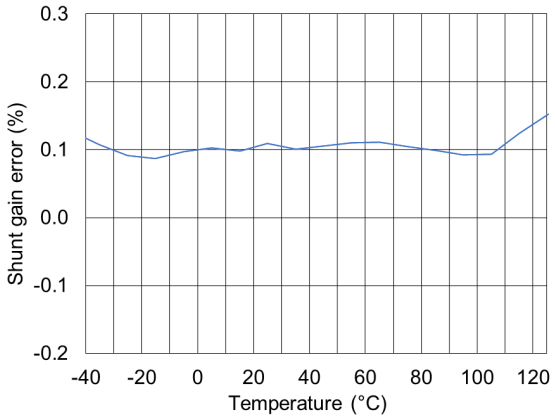


Figure 10. Shunt input gain error vs. V_{CM}

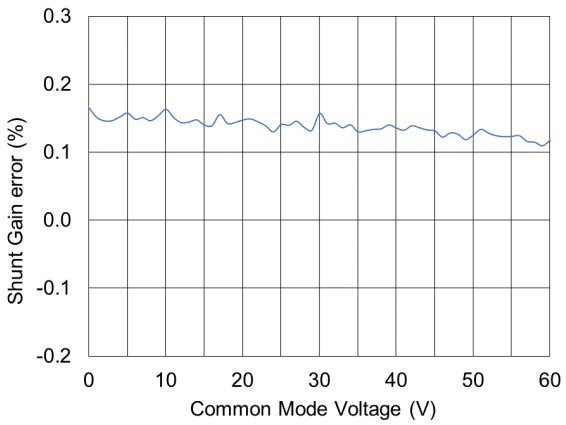


Figure 11. Load input gain error production distribution

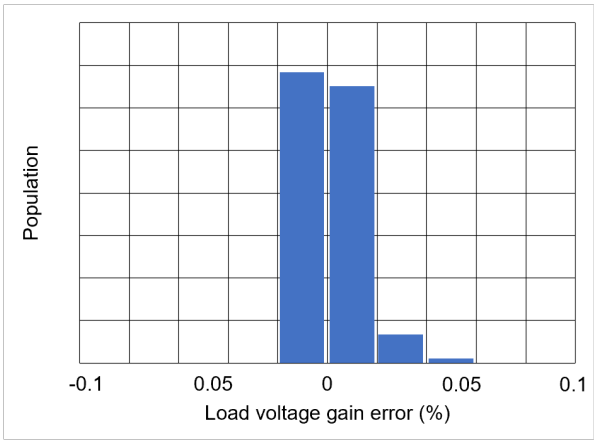


Figure 12. Load input gain error vs. temperature

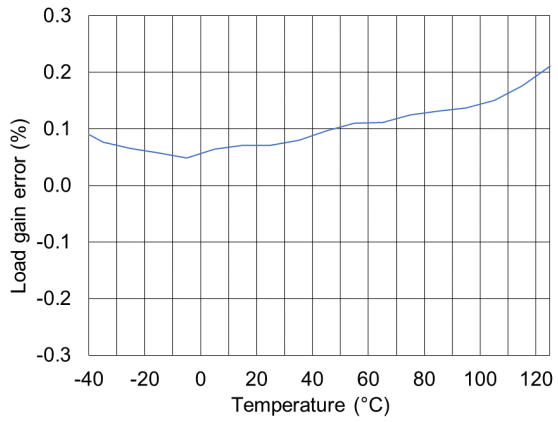


Figure 13. Current consumption (single ADC) vs. temperature

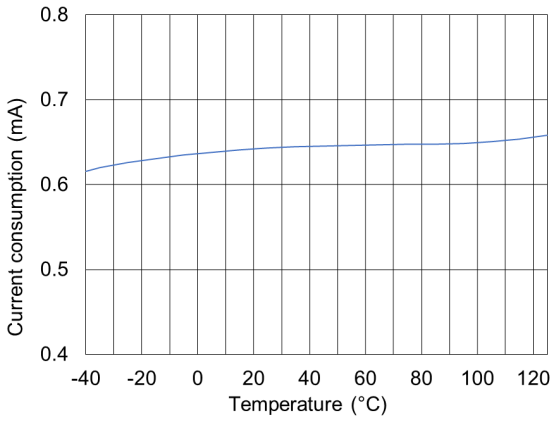


Figure 14. Current consumption (dual ADC) vs. temperature

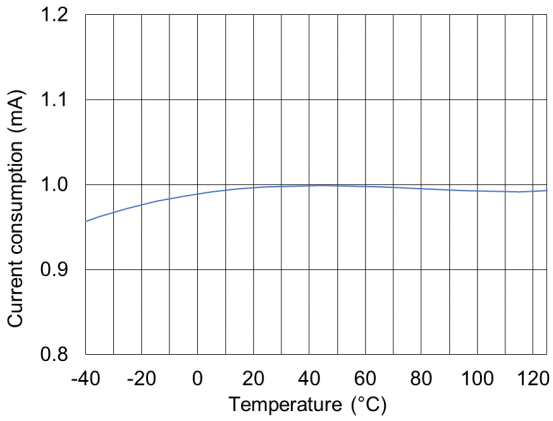


Figure 15. Shutdown current consumption vs. temperature

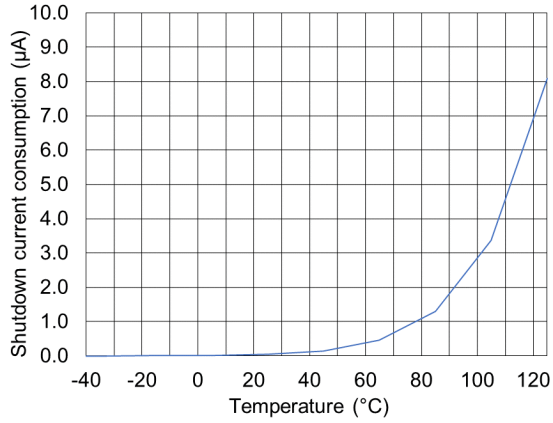


Figure 16. Current consumption (dual ADC) vs. power supply voltage

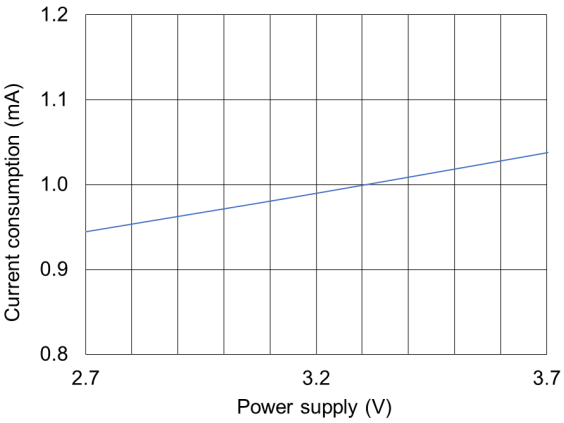


Figure 17. Current consumption (single ADC) vs. power supply voltage

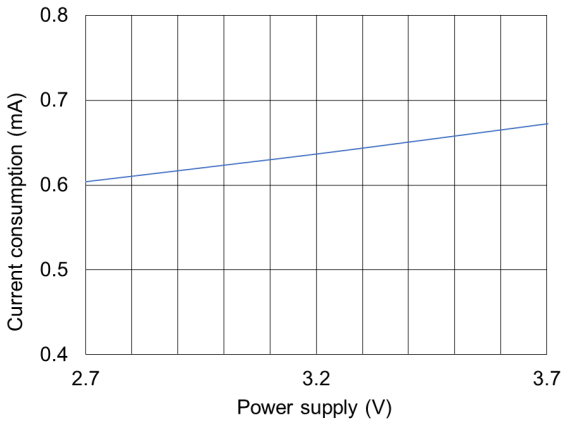


Figure 18. Shutdown current consumption vs. supply voltage

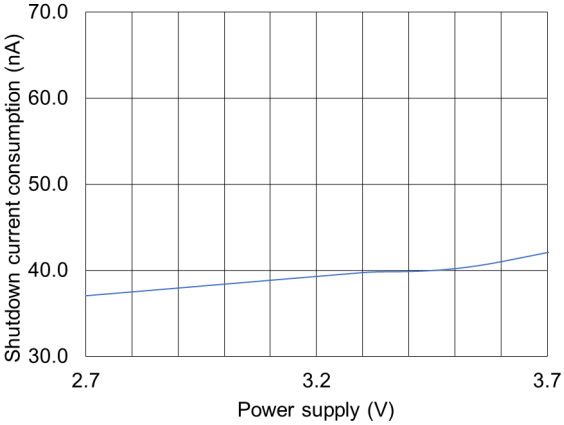


Figure 19. **Internal clock vs. power supply**

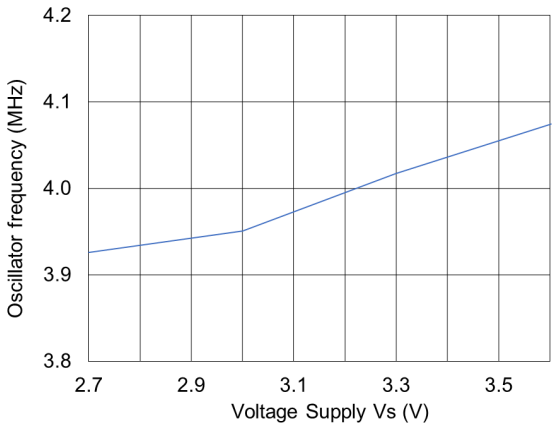
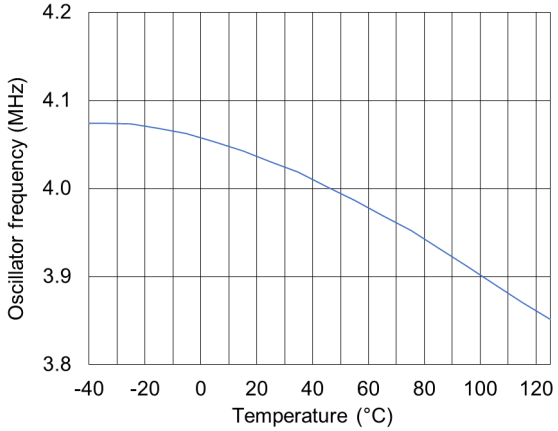


Figure 20. **Internal clock frequency vs. temperature**



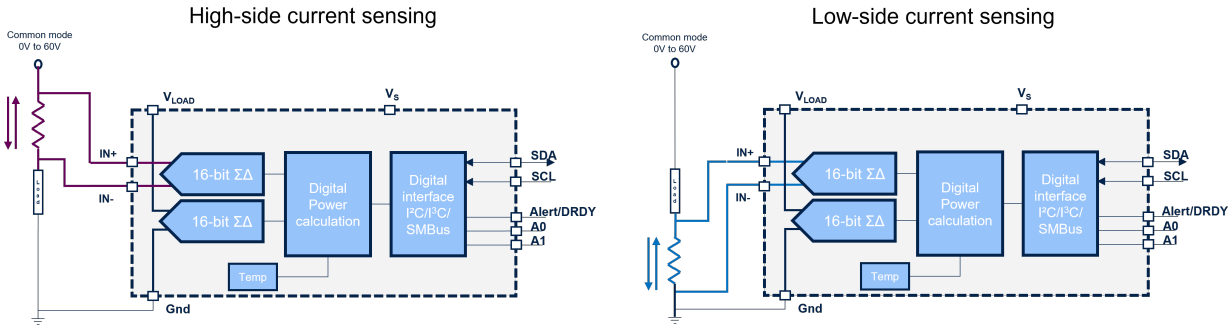
5 Application information

5.1 Overview of TSC1641

The TSC1641 is a digital power monitoring analog front end (AFE) meant to convert parameters such as current, voltage, and temperature and perform power calculation. A digital interface I²C, SMbus or MIPI I3C version 1.1.1 err02 SDR-only enables the communication to any system requiring an accurate monitoring of such variables.

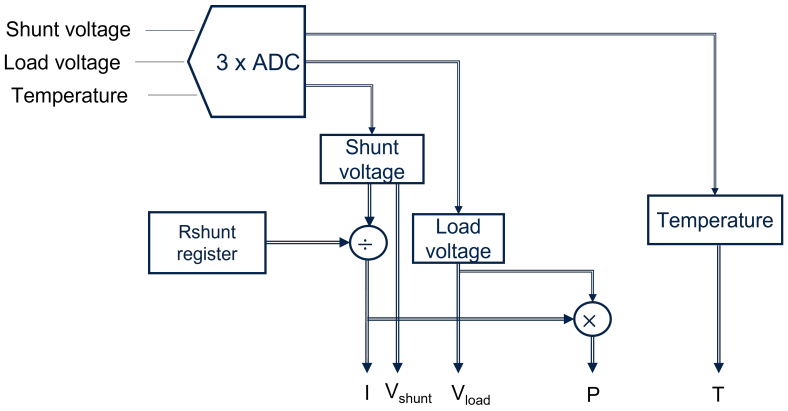
The TSC1641 can convert a shunt resistor voltage to determine the current in the load. The shunt resistor is placed outside the device and can be high-side or low-side, with bidirectional current measurements. The AFE can also monitor the load supply voltage up to 60 V. Current-sensing configurations are shown in Figure 21. There are three paths for each measurement: current, voltage, and temperature, which allows the most optimum computation of the DC power.

Figure 21. Current sensing configurations



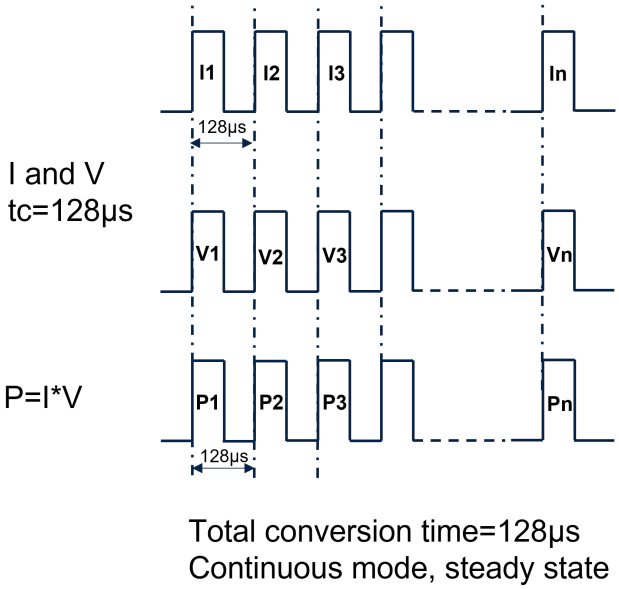
The different phases of the measurements are shown below in Figure 22. The user may choose to report through the configuration register, voltage only, current only, temperature only, a combination of these parameters, or all of them.

Figure 22. Voltage, current, power and temperature combinations



The TSC1641 enables a wide range of conversion times, suitable for many applications. The shunt channel and load voltage channel are sampled at the same rate from 128 µs to 32.768 ms. The conversion time is shown below in Figure 23.

Figure 23. **Conversion times for voltage, current, and power**



5.1.1 High-precision sigma-delta ADC

For very accurate measurement, the TSC1641 integrates two separated channels for the shunt voltage measurement and the load voltage measurement, thus simultaneous sampling is made possible for an optimum device power computation. The input range for the current channel is ± 81.92 mV and for the load voltage channel 0 V to 60 V. Each modulator has the same resolution, rated at 16 bits. The modulator is designed in such a way that only increasing the conversion time improves the noise performance of the device, thus simplifying the device configuration for the user.

The noise performances are summarized in Table 5, for each data rate. The effective resolution is given based on the peak-to-peak noise value measured for each setting, which ensures full coverage of the noise distribution.

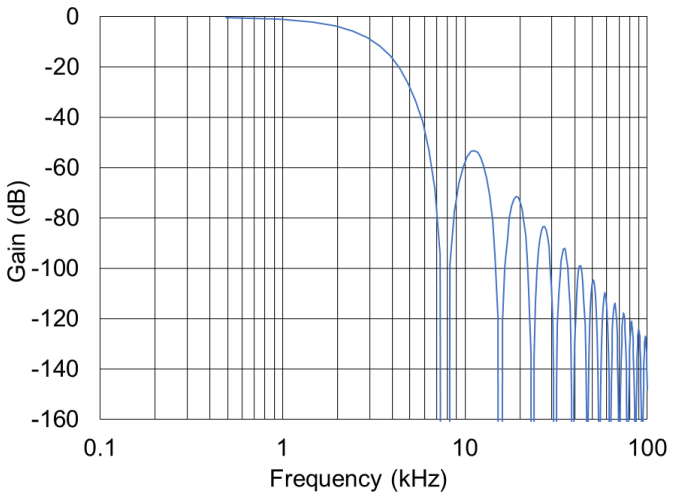
Table 5. **Noise performance table**

ADC conversion time	Output noise peak to peak (µV)	Noise-free resolution (+/-81.92 mV) p-to-p
128 µs	35	12.2
256 µs	26.7	12.6
512 µs	21.7	12.9
1.024 ms	16.7	13.3
2.048 ms	12.5	13.7
4.096 ms	9.2	14.1
8.192 ms	6.7	14.6
16.384 ms	3.3	15.7
32.768 ms	2.5	16

5.1.2 Digital filter

In each conversion channel, the TSC1641 implements a low-noise digital decimation filter to ensure the best noise performance. This digital filter self-adapts to the conversion rate, from 128 µs to 31.7 ms. In Figure 24, the response of the filter is shown for a 128 µs conversion rate.

Figure 24. **Digital filter response for 128 µs conversion time**



5.1.3 Negative slew-rate on V_{Load}

The TSC1641 monitors precisely the current and voltage on slow-moving signals. If the load voltage drops with a slew-rate above 80 V/s, the accuracy on the current measurement is transiently degraded above 3%, and performance recovers when the negative slew-rate is in the range supported by the TSC1641.

5.2 Digital interface

The TSC1641 can be addressed though I²C/SMbus or MIPI I3C interface. These protocols are compatible with each other.

SDA and SCL are shared for I²C/SMbus or MIPI I3C. They are open-drain connections to the bus in I²C mode and can be open-drain or push-pull connections in I3C mode. The change from open-drain mode to push-pull mode is done automatically by the TSC1641. The device that initiates communication on the bus is called a controller and generates the clock signal SCL, the START STOP conditions and controls the access to the bus. The devices under control are called targets. The TSC1641 is configured as a target device on the MIPI I3C bus.

The data sent on the digital I²C or MIPI I3C bus are driven MSB first.

5.2.1 Serial bus address

The TSC1641 can be addressed on the bus via an address byte that consists of 7 pre-defined bits and 1 bit to indicate if the device is going to be in read or write mode.

This so-called static address is used automatically on I²C bus and is used optionally on MIPI I3C. With MIPI I3C, despite the controller possibly allocating a virtual address to the devices on the bus (with the dynamic address assignment (DAA)), if a static address exists, it is primary to the virtual address assignment.

Two dedicated input pins, A1, A0 are used to set 4 different addresses. The first 5 MSBs are fixed and the 2 LSBs depend on the state of these pins. Table 6 lists the different states, the corresponding I²C static addresses, and the MIPI I3C PID content. The pins' A1, A0 states must be established before any activity on the bus.

Table 6. **Configuration of the address for I²C and PID for I3C**

A1	A0	Target address (binary)	Target address (h)	Provisional ID (PID) value (h)
GND	GND	1000000	40	0208020A0001
GND	VS	1000001	41	0208020A1001
VS	GND	1000010	42	0208020A2001
VS	VS	1000011	43	0208020A3001

5.2.2 I²C mode

Table 7. I²C target timing characteristics

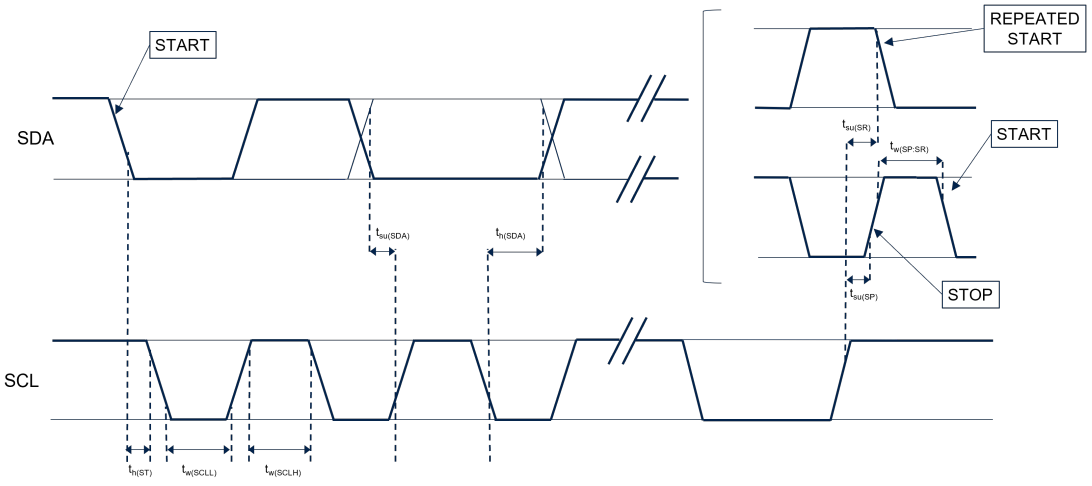
Symbol	Parameter (1)	I²C standard mode (1)		I²C fast mode (1)		I²C fast mode plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	10	100	10	400	10	1000	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		0.26		
$t_{su(SDA)}$	SDA setup time	250		100		50		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9		0.45	µs
$t_{h(ST)}$	START condition hold time	4		0.6		0.26		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		0.26		
$t_{su(SP)}$	STOP condition setup time	4.0		0.6		0.26		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		0.5		

1. *Data based on standard I²C protocol requirement, not tested in production.*

Table 8. Switching characteristics for I²C device on I3C bus

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{LFP}	Spike filter in I²C mode device for I3C mixed-bus compatibility (at 12.5 Mhz)			50	ns

Figure 25. I²C timing characteristics



5.2.3 MIPI I3C target interface

Both I²C and I3C are active on the TSC1641. I²C is initiated at startup. To enter the I3C mode, the controller must perform a dynamic address assignment with I²C fast mode plus timing. Once the TSC1641 is addressed, the I²C interface is disabled and the timing is compatible with MIPI I3C specifications.

The TSC1641 includes an MIPI I3C SDR only target interface with MIPI I3C SDR embedded features. Among them, the following features are supported by the TSC1641.

Common codes commands (CCC) are a standardized set of commands that can be transmitted either directly (direct communication) to a specific I3C target device, or to all I3C target devices simultaneously (broadcast communication). This specific address is reserved in I²C, meaning that no legacy I²C component can have this address.

The code for each CCC command is different based on whether they are used as direct or broadcast communication. Refer to Table 11 for the CCC supported by the TSC1641.

The TSC1641 can request hot-join on an I3C bus when it is powered off or physically disconnected from the application with an I3C bus already configured. Before starting a hot-join, the bus must be in an idle state.

The in-band interrupt (IBI) is supported by the TSC1641. If a start condition is done by the controller, the TSC1641 can emit its dynamic address into the arbitrated address header (0x7E) to notify of an interruption. If no start is forthcoming within the bus available condition (> 1 µs after stop), then the TSC1641 may issue a start request by pulling the SDA line low. The controller can accept or reject the IBI using the ACK bit.

The TSC1641 can communicate on multiple bus types. On a legacy I²C bus, the TSC1641 is seen as an I²C target device. On an I3C bus, it can communicate either on a mixed bus where both I3C and legacy I²C devices are present, or on a pure bus whose topology accepts only I3C devices.

Table 9. I3C open-drain timing requirements

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{LOW_OD}	Low period of SCL clock	200			ns
t_{HIGH}	High period of SCL clock			41	ns
t_{fDA_OD}	Fall time of SDA signal			12	ns
t_{rDA_OD}	Rise time of SDA signal			120	ns
t_{SU_OD}	SDA data setup time during open-drain mode	3			ns
t_{CAS}	Clock after start (S) condition	38.4		200	ns
t_{CBP}	Clock before stop (P) condition	19.2		200	ns
t_{AVAL}	Bus available condition	1			µs
t_{IDLE}	Bus idle condition	200			µs

Figure 26. I3C start and stop timings

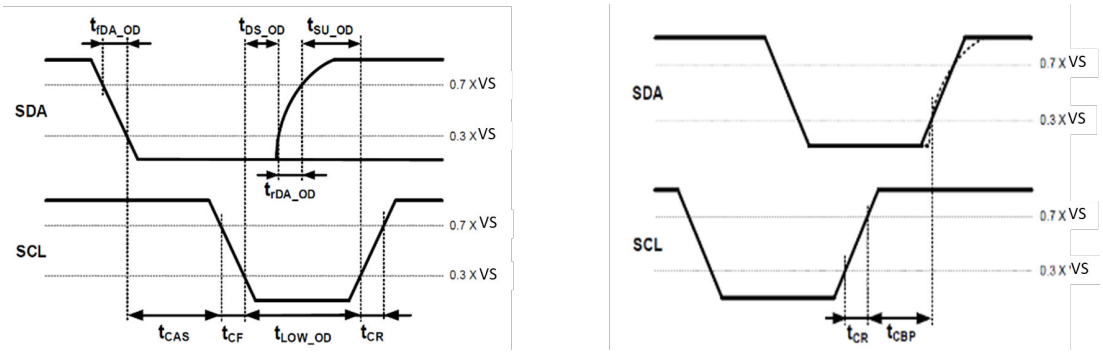


Table 10. I3C push-pull timing requirements for SDR

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency (1)	0.01	12.5	12.9	MHz
t_{LOW}	SCL clock low period	24			ns
t_{HIGH}	SCL clock high period for pure bus and/or mixed bus	24			ns
t_{SCO}	Clock in to data out for target			12	ns
t_{CR}	SCL clock rise time			$150x10^6*1/ f_{SCL}$ (Capped at 60)	ns
t_{CF}	SCL clock fall time			$150x10^6*1/ f_{SCL}$ (Capped at 60)	ns
t_{HD_PP}	SDA signal data hold in push-pull mode	0			
t_{SU_PP}	SDA signal data setup in push-pull mode	3			ns
t_{CASr}	Clock after repeated start condition (Sr)	19.2			ns
t_{CBSr}	Clock before repeated start (Sr) condition	19.2			ns
C_b	Capacitive load per bus line (SDA/SCL)			50	pF

1. $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$

Figure 27. I3C target device timing characteristics 1/2

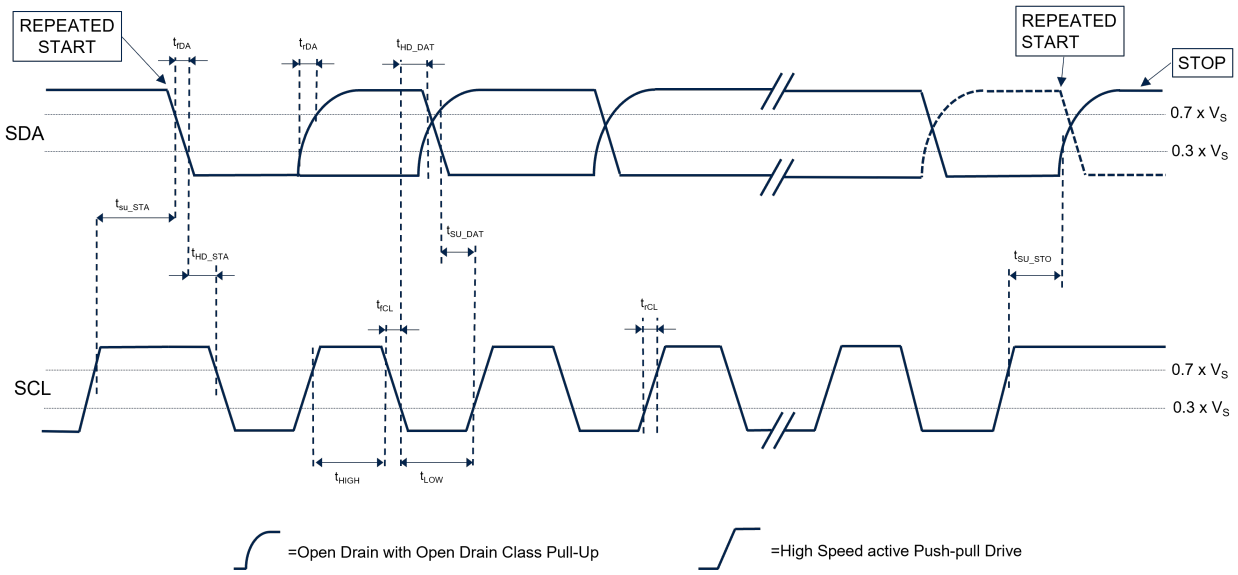


Figure 28. **I3C target device timing characteristics 2/2**

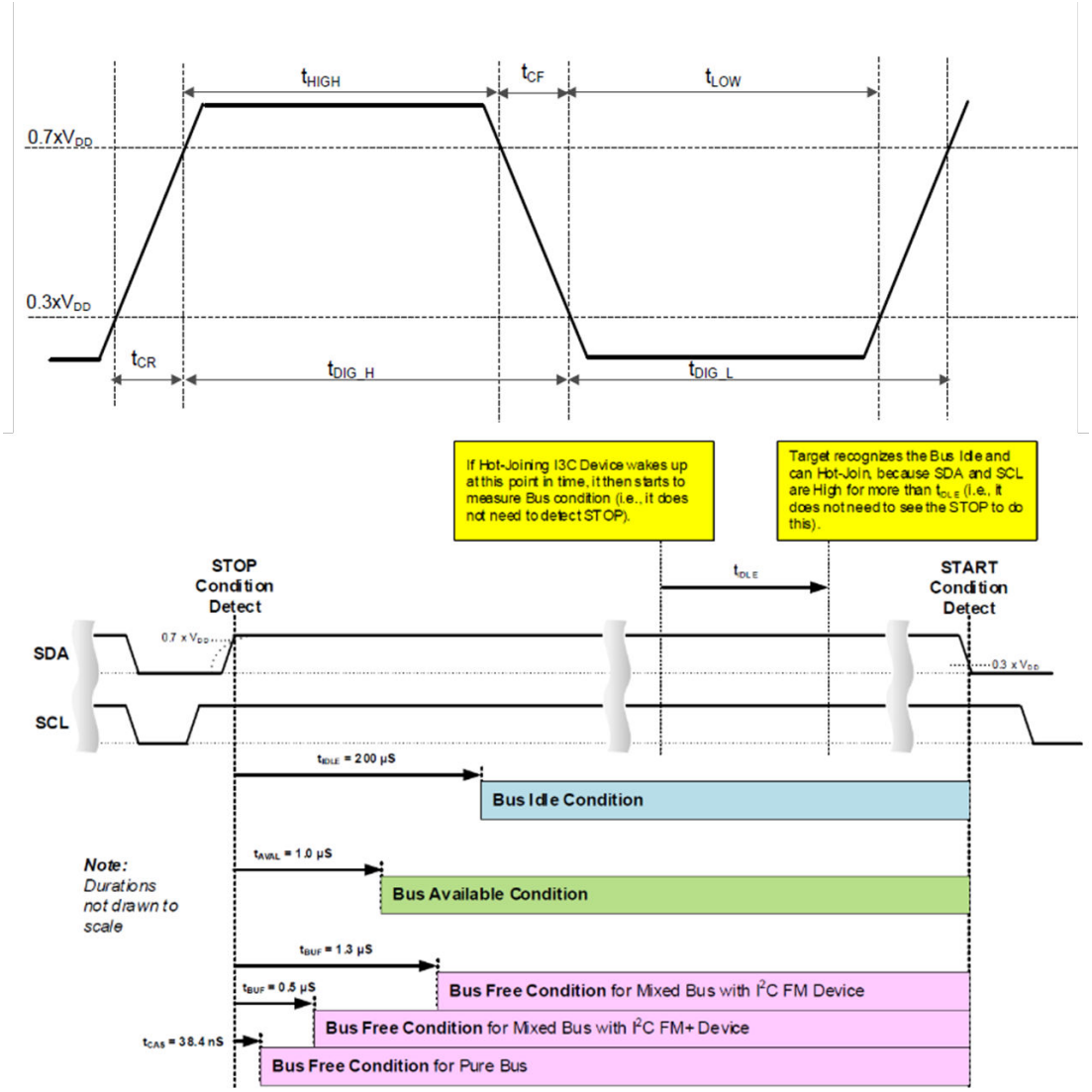


Table 11. **MIPI I3C supported commands**

Command name	Command code Broadcast / Direct	Default	Description
ENEC	0x00 / 0x80	On	Enable target event driven interrupts. At startup of the TSC1641, ENEC is enabled by default, which allows hot-join and IBI.
DISEC	0x01 / 0x81	Off	Disable target event driven interrupts.
RSTDAA	0x06 / N.A.		Forget current dynamic address and wait for new assignment.
ENTDAA	0x07 / N.A.		Enter controller initiation of target dynamic address assignment. Do not participate if the target already has an address assigned.
SETDASA	N.A. / 0x87		Controller assigns a dynamic address to a target with a known static address. Static address is 10000xx depending on A0/A1 in the case of TSC1641.
SETAASA	0x29 / N.A.		Controller tells every target with a static address to use it as the dynamic address

Command name	Command code Broadcast / Direct	Default	Description
SETNEWDA	N.A. / 0x88		Controller assigns a new dynamic address to any I3C target (only if ENTDAA is supported).
GETPID	N.A / 0x8D	0x02 0x08 0x02 0x0A 0x0 to 0x3 0x001	Get a target's provisional ID (ENTDAA supported).
GETBCR	N.A / 0x8E	0x02	Get a device's bus characteristics register.
GETDCR	N.A / 0x8F	0x00	Get a device's device characteristics register.
GETSTATUS	N.A / 0x90		Get a device's operating status.
RSTACT	0x2A / 09A		Configure and query target device reset action and timing. 0x00: no action on the target after the reset pattern. 0x01: I3C reset only. 0x02: equivalent to software reset (see Table 12).
SETGRPA	N.A. / 0x9B		Host assigns a group address to a device. The TSC1641 can be assigned to one group.
RSTGRPA	0x2C / 0x9C		Host removes a target device from an indicated group address by resetting the assigned group address.
GETCAPS	N.A. / 0x95		Host asks target device what optional capabilities it supports.

5.3 Register mapping

The registers to be addressed are shown in Table 12. Their addresses are defined by a pointer, an 8-bit register that contains the first register address to be read. During a continuous read, the pointer address is moved automatically to the next register address.

In normal operating mode, the content of the registers can be changed using standard I²C/SMBus or MIPI I3C commands.

Table 12. Register mapping table

Pointer address (hex)	Register name	Type	Default value	Reset after POR	Reset after shutdown mode	Reset after idle mode	Reset after software RST
00h	Configuration register	R/W	0037h	yes	no	no	yes
01h	Shunt voltage register	R	0000h	yes	no	no	yes
02h	Load voltage register	R	0000h	yes	no	no	yes
03h	DC power register	R	0000h	yes	no	no	yes
04h	Current register	R	0000h	yes	no	no	yes
05h	Temperature register	R	8000h	yes	no	no	yes
06h	Mask register	R/W	0000h	yes	no	no	yes
07h	Flag register	R	0000h	yes	no	no	yes
08h	Rshunt register	R/W	0000h	yes	no	no	no
09h	SOL alert limit register	R/W	0000h	yes	no	no	no
0Ah	SUL alert limit register	R/W	0000h	yes	no	no	no
0Bh	LOL alert limit register	R/W	0000h	yes	no	no	no
0Ch	LUL alert limit register	R/W	0000h	yes	no	no	no
0Dh	POL alert limit register	R/W	0000h	yes	no	no	no
0Eh	TOL alert limit register	R/W	0000h	yes	no	no	no
FEh	Manufacturing ID	R	0006h	yes	no	no	no
FFh	Die ID register	R	1000h	yes	no	no	no

5.3.1 Configuration register (00h) read/write

Table 13. Configuration register (00h) read/write

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST								CT3	CT2	CT1	CT0	TEMP	M2	M1	M0
POR value	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

RST: When this bit is set high, it generates a system reset. Some of the registers are reset as shown in the register mapping Table 12. Register mapping table. The RST bit is self-cleared.

CT3 to CT0: conversion time for both shunt and load voltage channels.

Table 14. CT3 to CT0: conversion time

CT3	CT2	CT1	CT0	Conversion time
0	0	0	0	128 µs
0	0	0	1	256 µs
0	0	1	0	512 µs

CT3	CT2	CT1	CT0	Conversion time
0	0	1	1	1024 µs (default)
0	1	0	0	2048 µs
0	1	0	1	4096 µs
0	1	1	0	8192 µs
0	1	1	1	16384 µs
1	0	0	0	32768 µs
1	x	x	x	Not to be used

TEMP: this bit turns on the temperature sensor when set to a high level and turns off the temperature sensor when set to a low level. Temperature sensing can only be done in the normal operating modes (thus excluding shutdown and idle mode). Temperature is sensed in a continuous way at a fixed conversion rate of 8.192 ms. When no temperature measurement is performed, the temperature register (05 h) returns the to code 8000 (h).

M2 to M0: all the different modes that are available.

Table 15. M2 to M0: operating modes of the TSC1641

M2	M1	M0	Mode	Content of read-only registers
0	0	0	0h: shutdown (low power mode). In this mode, no measurement can be made, and the device is in low current consumption. Communication interface is active to answer a signal on the bus. Table 12 summarizes the register's status. Timeout is not possible in this mode.	Registers 01h to 05h contain the latest data. Register 07h cannot be cleared.
0	0	1	1h: shunt voltage, triggered, single shot. In this mode, the shunt voltage delivers the current if the Rshunt register has been filled, otherwise the current register remains at 0. After the measurement, the CVRF (conversion ready flag) is set, and data can be read on the shunt voltage register. The ALERT/DRDY pin can also be asserted if the mask register has been assigned properly (CVNR=1). At this stage, the power is not updated.	Registers 01h, 04h, and 05h contain new data. Registers 02h and 03h contain ‘0’.
0	1	0	2h: load voltage, triggered, single shot. Once measurement is performed, the CVRF (conversion ready flag) is set, and data can be read on the load voltage register. The ALERT/DRDY pin can also be asserted if the mask register has been assigned properly (CVNR=1).	Registers 02h, 05h contain new data. Registers 01h, 03h to 04h contain ‘0’.
0	1	1	3h: shunt and load voltage, triggered, single shot. In this mode, shunt and load voltage measurements are made simultaneously, and power calculated if the Rshunt register has been filled. After the measurement the CVRF (conversion ready flag) is set, and data can be read on the shunt voltage register. The ALERT/DRDY pin can also be asserted if the mask register has been assigned properly (CVNR=1).	Registers 01h to 05h contain new data.
1	0	0	4h: idle mode. No measurement can be performed in this mode. Bus communication is active, and timeout can be detected. Device can be activated in a very short time. Table 12 summarizes the registers status.	Registers 01h to 05h contain last data. Register 07h is cleared after a read.
1	0	1	5h: continuous shunt voltage. Shunt voltage measurement is performed in a continuous way at the conversion time that is defined in the configuration register with the bits CT3-CT0. After the shunt voltage measurement is taken, and if the Rshunt register has been correctly filled, then the current (for current measurement) register can be computed. The conversion ready information is available similarly to the triggered mode.	Registers 01h, 04h, and 05h contain new data. Registers 02h and 03h contain ‘0’.
1	1	0	6h: continuous load voltage. Load voltage measurement is performed in a continuous way at the conversion time that is defined in the configuration register with the bits CT3-CT0. After the load voltage measurement is taken, and if the Rshunt register has been filled, then the power register can be computed. The conversion ready information is available similarly to the triggered mode.	Registers 02h and 05h contain new data. Registers 01h, 03h to 04h contain ‘0’.
1	1	1	7h: shunt and load voltage, continuous mode (default).	Registers 01h to 05h contain new data.

M2	M1	M0	Mode	Content of read-only registers
			In this mode, shunt and load voltages are measured simultaneously at the conversion time defined in the configuration register with the bits CT3-CT0. If the specific Rshunt register is correctly filled, then the power can be computed.	

Default power-up mode: when TSC1641 is switched on, applying a proper power supply on VS, the device automatically enters the default configuration, meaning that it starts I²C mode and converts continuously the current and load voltage at a 1024 µs conversion time. First valid data is available after 3 clock cycles of 128 µs and one cycle of 1024 µs. The CVNR bit from the MASK register is set to high to inform the user about the availability of the data.

5.3.2 Shunt voltage measurement register (01h) read-only

This read-only register stores the value measured on the shunt resistor. Positive value is binary: positive full-scale goes from 0000(h) to 7FFF (hex). Negative value is two's complement. Negative full-scale goes from 8000(h) (two's complement of decimal -32767 to 000(h)).

If the register returns either 7FFF or 8000, together with the bit SATF set to '1', the shunt voltage is out of the input range of the TSC1641.

If the shunt voltage is not measured (mode 2h or 6h), the value returned by the shunt voltage register is 0, as well as the ones of the current and power registers.

Bit 15: sign.

Bit 14-0: value referred to shunt-LSB: 2.5 µV.

5.3.3 Load voltage measurement register (02h) read-only

This read-only register contains the measurement of the load supply voltage. The LSB_load is 2 mV and full-scale 7FFF is 65.534V. Please refer to the operating conditions table to get the recommended voltage range supported on Vload.

If the register returns 0000(h) or 7FFF(h) with SATF set to '1', the load voltage is out of the input range of the TSC1641.

If the load voltage is not measured (mode 1h or 5h), the value returned by the load voltage register is 0 as well as the one of the computed power register.

5.3.4 Current register (03h) read-only

This register contains the value of the current flowing into the shunt. The value is given from an internal calculation using the Rshunt register. If no information has been set in the Rshunt register, then the current register returns to 0.

5.3.5 Power register (04h) read-only

This register contains the value of the computed DC power. Voltage and current are measured simultaneously to compute the power accurately. To have an adequate value, the Rshunt register must be filled in, otherwise, the power register returns to 0.

5.3.6 Temperature register (05h) read-only

An internal temperature sensor releases upon demand the temperature of the TSC1641. The bit TEMP in the configuration register is set to "1". The controller must read the register (16-bit wide) in two's complement format.

The temperature can be read within the range of -40 °C to 125 °C. Outside this window, the values are not representative of a physical quantity. A 0.5 °C/LSB resolution is implemented.

To get a simple value of the temperature, the user simply must take the decimal number of the register and divide it by a factor of two. For simplification, the register is symmetrical, and the code 0000 (h) represents 0 °C.

Examples:

Code: 0032(h) is 50 (dec), thus, after division by 2 is +25 °C

Code: 00AA(h) is 170 (dec) thus, after division by 2 is +85 °C

Code: FFD8(h) is -40 (dec) thus, after division by 2 is -20 °C

If the register returns 8000(h), the TEMP bit was not set.

5.3.7 Mask register (06h) read/write

The mask register selects the function that is enabled to control the alert pin and the functionality of the alert pin. There is one alert limit register per functionality. If multiple features are enabled, the alert pin is asserted based on priority of the bit with the highest significance (D15-D10).

Table 16. Mask register

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SOL	SUL	LOL	LUL	POL	TOL	CVNR								APOL	ALEN
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

These register bits select which parameter controls the alert pin (I²C) or the IBI (MIPI I3CSM). One 16-bit register threshold is associated to each mask bit.

SOL: shunt voltage over limit

Setting this bit high configures the ALERT pin to be asserted if the shunt voltage measurement following a conversion exceeds the value programmed in the SOL alert limit register.

SUL: shunt voltage under limit

Setting this bit high configures the ALERT pin to be asserted if the shunt voltage measurement following a conversion drops below the value programmed in the SUL alert limit register.

LOL: load voltage over limit

Setting this bit high configures the ALERT pin to be asserted if the load voltage measurement following a conversion exceeds the value programmed in the LOL alert limit register.

LUL: load voltage under limit

Setting this bit high configures the ALERT pin to be asserted if the load voltage measurement following a conversion drops below the value programmed in the LUL alert limit register.

POL: power over limit

Setting this bit high configures the ALERT pin to be asserted if the power calculation following a load voltage measurement exceeds the value programmed in the POL alert limit register.

TOL: temperature over limit

Setting this bit high configures the ALERT pin to be asserted if temperature measurement following a conversion exceeds the value programmed in the TOL alert limit register.

CVNR: conversion_ready

Setting this bit high configures the ALERT pin to be asserted when the conversion ready flag (CVNF) of the flag register is asserted, indicating that the device is ready for the next conversion.

APOL: alert polarity bit

Setting this bit high configures the polarity of the ALERT pin to be inverted and active high open-drain.

Setting this bit low configures the normal polarity of the ALERT pin, being active low open-drain.

ALEN: alert latch enable

When set to 0, transparent mode is enabled, the ALERT pin and corresponding fault bit in flag register is reset to default value once fault has been cleared. The ALEN bit does not apply to the CVNR bit.

When set to 1, latch mode is enabled, the ALERT pin and corresponding fault bit remain active following a fault until the flag register has been read.

5.3.8 Flag register (07h) read-only

The flag register is a read-only register that sets the flag bit high either automatically for OVF, SATF or when the selected function in the mask register has been set.

Table 17. Flag register

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		OVF	SATF							SOF	SUF	LOF	LUF	POF	TOF	CVNF
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OVF: math overflow flag

This bit is set high if an arithmetic operation resulted in an overflow error. It indicates that current or power data may be invalid. OVF is cleared when arithmetic operation leads to valid data.

SATF: saturation flag

This flag is internally set high when the signal under measurement is outside the input allowable range. It may be set high in the following conditions:

Vshunt < -81.9175 mV or +81.92 mV < Vshunt

7FFF(h) < Vload

The SATF does not trigger the alert pin in I²C or IBI in I3C.

The SATF bit is cleared if measurement is back to the allowable input range.

SOF: shunt overvoltage flag

This flag is internally set to high when the SOL bit of mask register is set to high and shunt voltage measurement following a conversion exceeds the SOL alert limit register. The SOF bit is cleared after reading the alert flag register.

SUF: shunt undervoltage flag

This flag is internally set to high when the SUL bit of mask register is set to high and shunt voltage measurement following a conversion drops below the SUL alert limit register. The SUF bit is cleared after reading the alert flag register.

LOF: load overvoltage flag

This flag is internally set to high when the LOL bit of mask register is set to high and load voltage measurement following a conversion exceeds the LOL alert limit register. The LOF bit is cleared after reading the alert flag register.

LUF: load undervoltage flag

This flag is internally set to high when the LUL bit of mask register is set to high and voltage measurement following a conversion drops below the LUL alert limit register. The LUF bit is cleared after reading the alert flag register.

POF: over power flag

This flag is internally set to high when the POL bit of mask register is set to high and power following a calculation exceeds the POL alert limit register. The POF bit is cleared after reading the alert flag register.

TOF: overtemperature flag

This flag is internally set to high when the TOL bit of mask register is set to high and temperature measurement following a conversion exceeds the TOL alert limit register. The TOF bit is cleared after reading the alert flag register.

CVNF: conversion ready flag

Although the device can be read at any time, and the data from the last conversion is available, the conversion ready flag can help to coordinate one-shot or triggered conversions. The CVNF bit is set each time a new data is entered into a register. The CVNF is cleared under the following conditions:

- Writing to the configuration register (except for the shutdown and idle mode selection)
- Reading the flag register

5.3.9 Rshunt register (08h) read/write

Table 18. Rshunt register

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

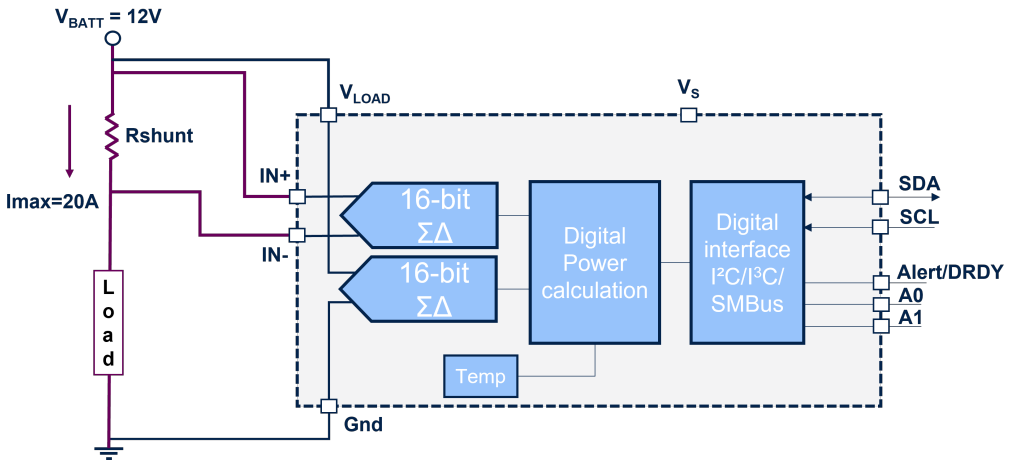
The Rshunt register (16-bit wide) stores the value of the Rshunt resistor placed in the application. The user enters the Rshunt value based on the current flowing into the application.

Rshunt_LSB is 10 µΩ, therefore the values could be entered from 0 Ω to 655.35 mΩ, but we recommend this range of values for Rshunt: 800 µΩ (Imax = 102 A) to 655.35 mΩ (Imax = 125 mA).

We remind the user that: Vshunt_LSB = 2.5 µV, Vload_LSB = 2 mV. And the DCpower_LSB is set to 25 mW. Maximum allowed DC power on TSC1641 is 1600 W.

Figure 29 shows an example of an application with Imax = 20 A, VBatt = 12 V, Iload = 8 A

Figure 29. **Typical applications with high-side current sensing**



- The first option for the user is to optimize the acquisition channel to full-scale +/-81.92 mV.

Rshunt is defined by 81.92 mV / 20 A = 4.096 mΩ.

Based on normalized values, the user may choose between Rshunt 4 mΩ to 4.1 mΩ.

Let us assume that the user chooses Rshunt = 4 mΩ, the digital value is Rshunt (dig) = 400 (dec) thus the Rshunt register value is: 0190(hex).

The LSB in current is then: I_LSB = Vshunt_LSB/Rshunt, thus, I_LSB = 625 µA.

The reading of the registers then gives:

- Shunt voltage: 3200 (hex) which is 12800 (dec), then 12800 (dec) * 2.5µV = 32 mV
- Load voltage: 1770 (hex) which is 6000 (dec), then 6000 (dec) * 2 mV= 12.0 V
- DC power: 0700 (hex), which is 3840 (dec), then 3840 (dec) * 25 mW = 96 W
- Current: 3200 (hex) which is 12800 (dec), then 12800 (dec) * 6 25 µA = 8 A
- The second option for the user is to get a simple distinctive current_LSB: say I_LSB = 1 mA, thus Rshunt = Vshunt_LSB/I_LSB = 2.5 mΩ

In this case the maximum full-scale is 20 A * 2.5 mΩ = 50 mV.

The registers reading should give:

- Shunt voltage: 1F80 (hex) which is 8000 (dec), then 8000 (dec) * 2.5 µV = 20 mV
- Load voltage: 1770 (hex) which is 6000 (dec), then 6000 (dec) * 2 mV = 12 V
- DC power: 0F00 (hex), which is 3840 (dec), then 3840 (dec) * 25 mW = 96 W
- Current: 1F80 (hex) which is 8000 (dec), then 8000 (dec) * 1 mA = 8 A

If no value is entered in the the Rshunt register, then the default value of Rshunt is 0, and the reading of the current register and the power register returns to 0.

5.3.10 Register SOL alert limit (09h) read-write

The user can write in the shunt over limit register the threshold voltage above which the alert is active. The SOL LSB is 2.5 µV.

Table 19. **Register SOL**

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3.11 Register SUL alert limit (0Ah) read-write

The user can write in the shunt under limit register the threshold voltage below which the alert is active. The SUL LSB is 2.5 µV.

Table 20. **Register SUL**

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3.12 Register LOL alert limit (0Bh) read-write

The user can write in the load over limit register the threshold voltage above which the alert is active. The LOL LSB is 2 mV.

Table 21. **Register LOL**

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3.13 Register LUL alert limit (0Ch) read-write

The user can write in the load over limit register the threshold voltage above which the alert is active. The LOL LSB is 2 mV.

Table 22. **Register LOL**

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3.14 Register POL alert limit (0Dh) read-write

The user can write in the power over limit register the threshold voltage above which the alert is active. The POL LSB is 25 mW.

Table 23. **Register POL**

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3.15 Register TOL alert limit (0Eh) read-write

The user can write in the temperature over limit register the threshold voltage above which the alert is active. The POL LSB is 0.5 °C.

Table 24. **Register POL**

Bit n°	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POR value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3.16 Manufacturer register (FEh) read-only

This register is accessible through standard read command and reports the STMICROELECTRONICS ID which is 0006h.

5.3.17 Die ID register (FFh) read-only

This register is accessible through a standard read command. Die ID is 1000(h).

5.4 Typical application circuit

Figure 30. Typical application for high-side sensing and MIPI I3C communication

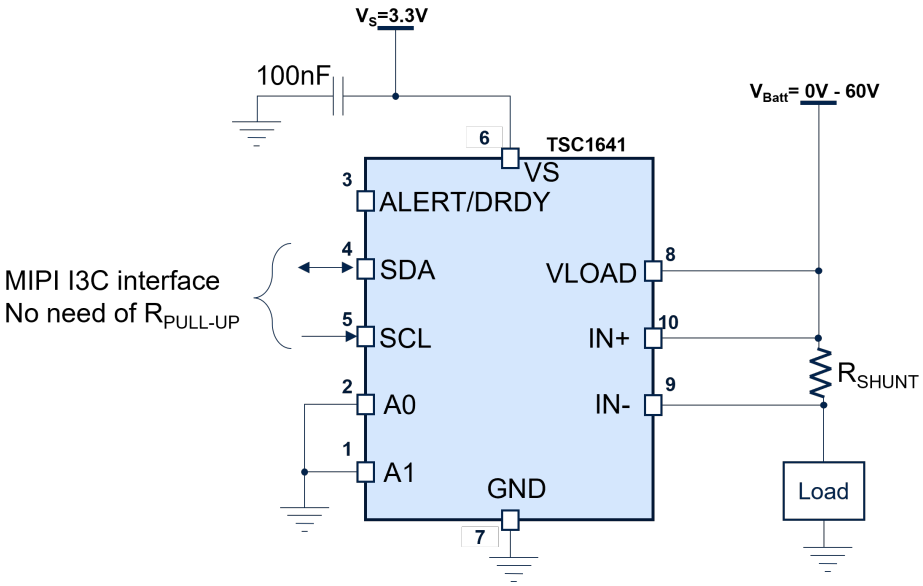


Figure 30 shows a typical configuration used when connecting the device to a controller with MIPI I3C interface. The pads A0/A1 are used in our case to set the provisional identification register (PID) accessed by the command 'GETPID' in Table 6. SDA and SCL are directly connected to the controller, no pull-up resistor is needed. The ALERT/DRDY pad is unused in I3C mode. Instead, , the IBI (in-band interrupt) plays the role of the interrupt. This configuration is a standard high-side current measurement with a load supplied by a voltage up to 60 V.

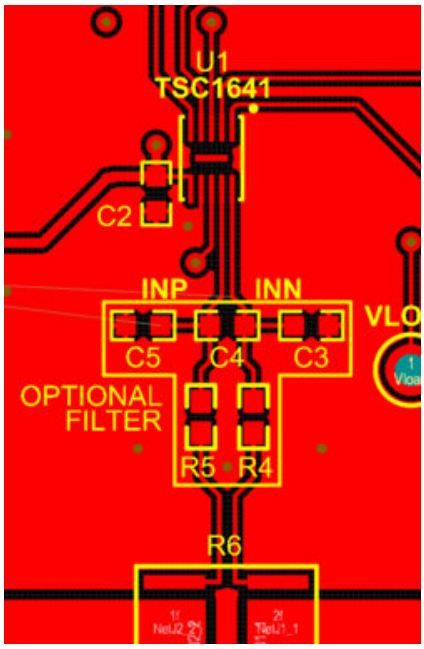
5.5 Layout recommendation

5.5.1 Shunt resistor layout

The shunt resistor layout must be designed carefully to guarantee the best performance. The kelvin connection must be used to ensure that only the shunt resistor impedance is sensed between the inputs.

Length of IN+ and IN- traces must be precisely balanced to keep the shunt offset voltage low.

Figure 31. Shunt resistor layout

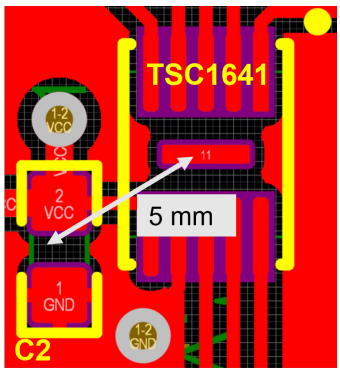


5.5.2 100 nF decoupling capacitor placement

To guarantee the best performance, the C2 decoupling capacitor must be placed very close to the circuit, at 5 mm from the circuit center, as shown in Figure 32. The layout recommendation must be followed precisely. We recommend using a 100 nF for C2 in 0603 format.

A ground plane must be present under the circuit.

Figure 32. TSC1641 layout



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 DFN10 (3x3 mm) package information

Figure 33. **DFN10 (3x3 mm) package outline**

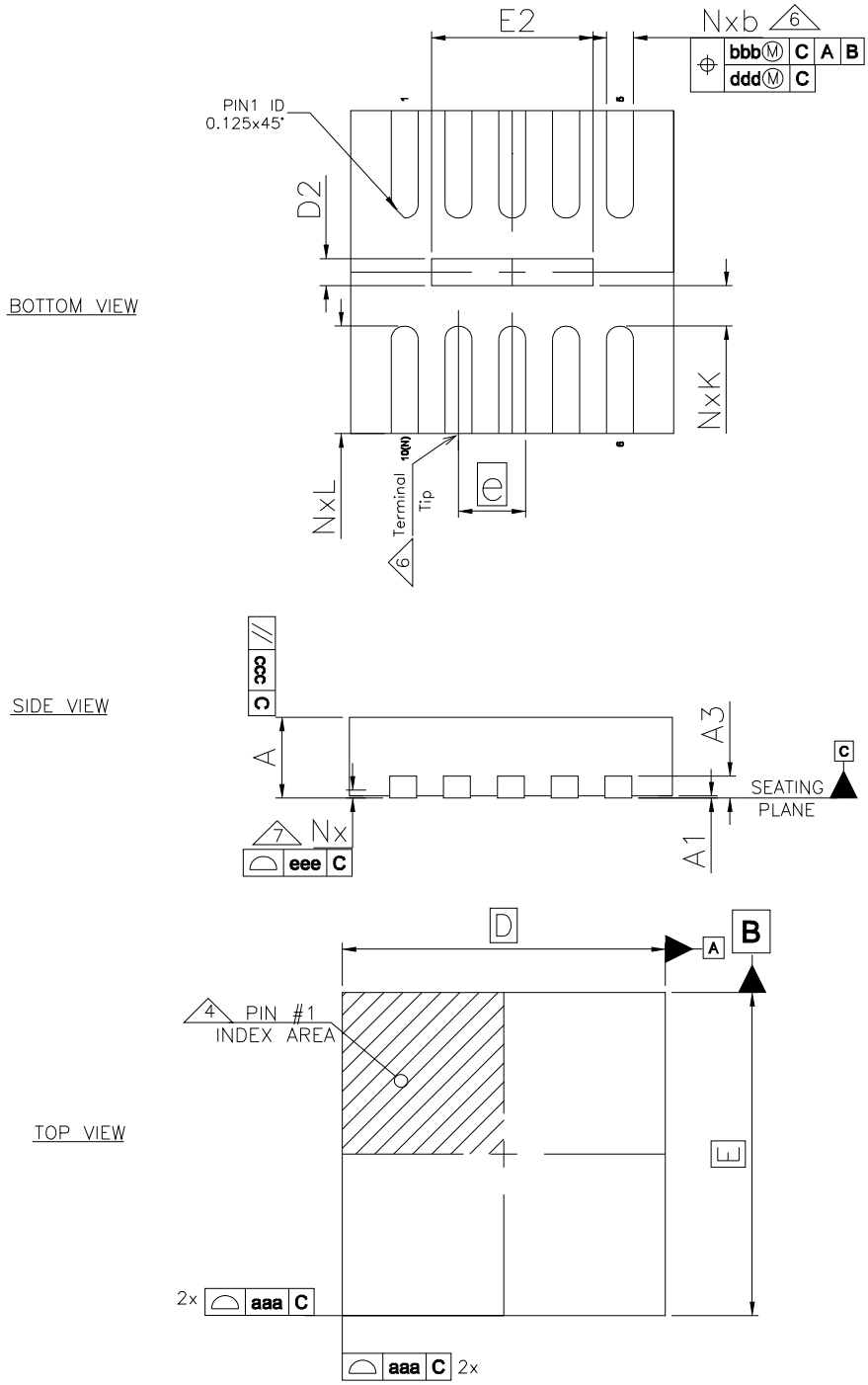
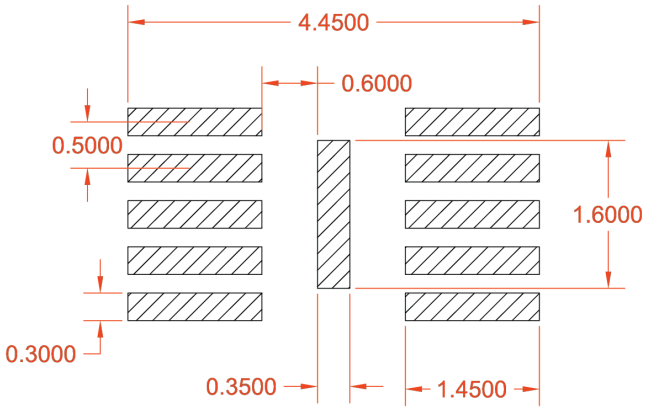


Table 25. **DFN10 (3x3 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	-	0.203 Ref.	-
b	0.20	0.25	0.30
D		3.00 BSC	
D2	0.15	0.25	0.30
E		3.00 BSC	
E2	1.40	1.50	1.60
e		0.50 BSC	
K	0.20	-	-
L	0.90	1.00	1.10
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 34. **DFN10 (3x3 mm) recommended footprint**



7 Ordering information

Table 26. **Order codes**

Order code	Package	Packaging	Marking
TSC1641IQT	DFN10	Tape & Reel	1641

Revision history

Table 27. **Document revision history**

Date	Revision	Changes
12-Sep-2023	1	Initial release.

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