



# PXM020-100QS

N-channel 100 V, 20 mOhm, standard level Trench MOSFET in MLPAK33

28 September 2023

Product data sheet

## 1. General description

General purpose MOSFET for standard applications, 31 A, standard level N-channel enhancement mode Power MOSFET in MLPAK33 package.

## 2. Features and benefits

- Standard level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

## 3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Home appliance
- Motor drive
- Load switching
- LED lighting

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	31	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	37	W
$T_j$	junction temperature		-55	-	150	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 9}$	-	17.4	20	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 5\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}; \text{Fig. 11}; \text{Fig. 12}$	-	3.5	-	nC
$Q_{G(tot)}$	total gate charge		-	13	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 15.6\text{ A}; V_{sup} \leq 100\text{ V}; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; \text{unclamped}$	[1]	-	24.3	mJ

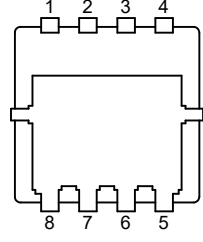
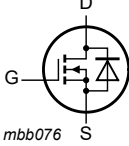
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Source-drain diode</b>							
$Q_r$	recovered charge	$I_S = 5 \text{ A}$ ; $di_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ; $V_{DS} = 50 \text{ V}$ ; $T_J = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 15</a>	[2]	-	24	-	nC

[1] Protected by 100% test

[2] includes capacitive recovery

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>MLPAK33 (SOT8002-1)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN020-100QS	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PXN020-100QS	7AQ

## 8. Limiting values

Table 5. Limiting values

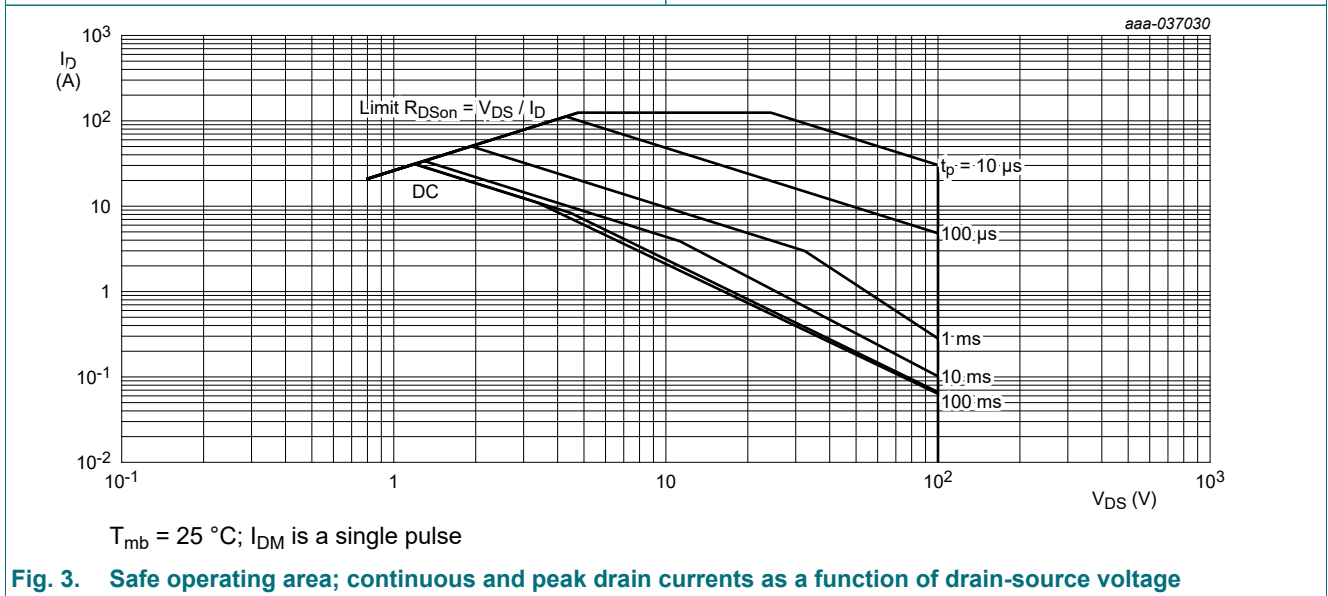
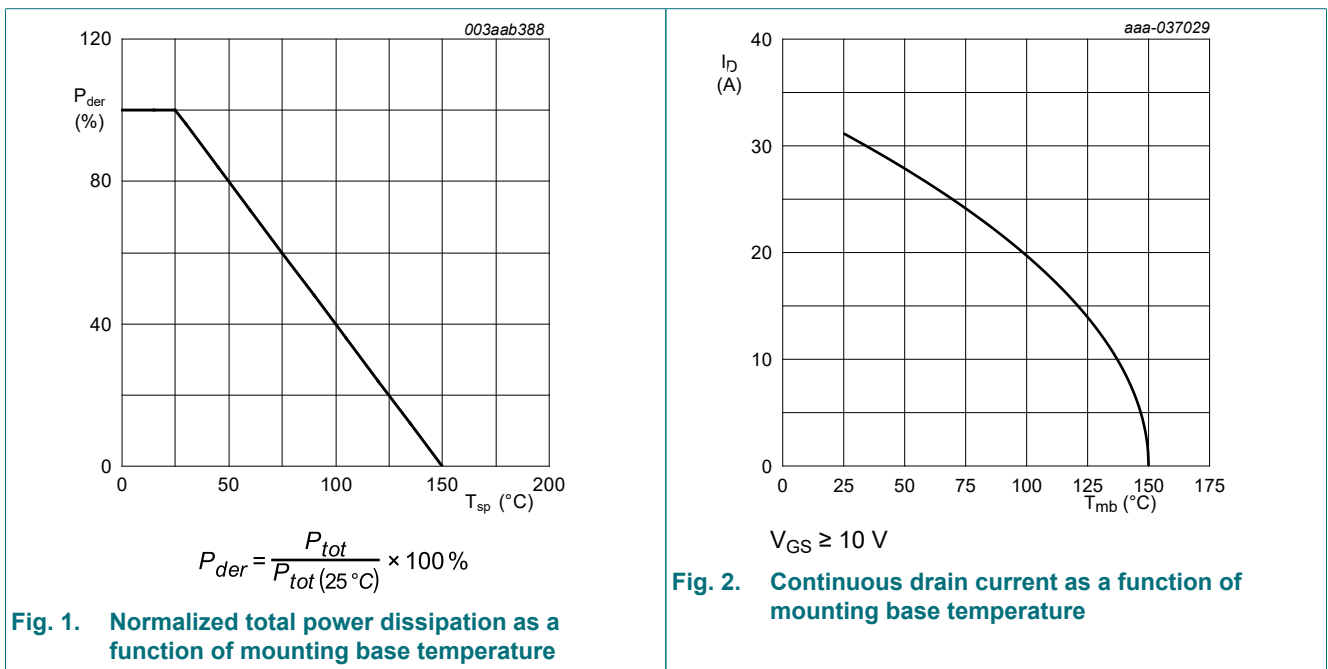
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_J = 25 \text{ }^\circ\text{C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_J \leq 150 \text{ }^\circ\text{C}$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	37	W
$I_D$	drain current	$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	31	A
		$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 100 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	20	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \mu\text{s}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 3</a>	-	125	A
$T_{stg}$	storage temperature		-55	150	$^\circ\text{C}$

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Symbol	Parameter	Conditions	Min	Max	Unit
$T_j$	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	31	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	125	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 15.6\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	[1]	-	24.3 mJ
$I_{AS}$	non-repetitive avalanche current	$T_{j(init)} = 25\text{ °C}$	[1]	-	15.6 A

[1] Protected by 100% test



## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	2.81	3.37	K/W

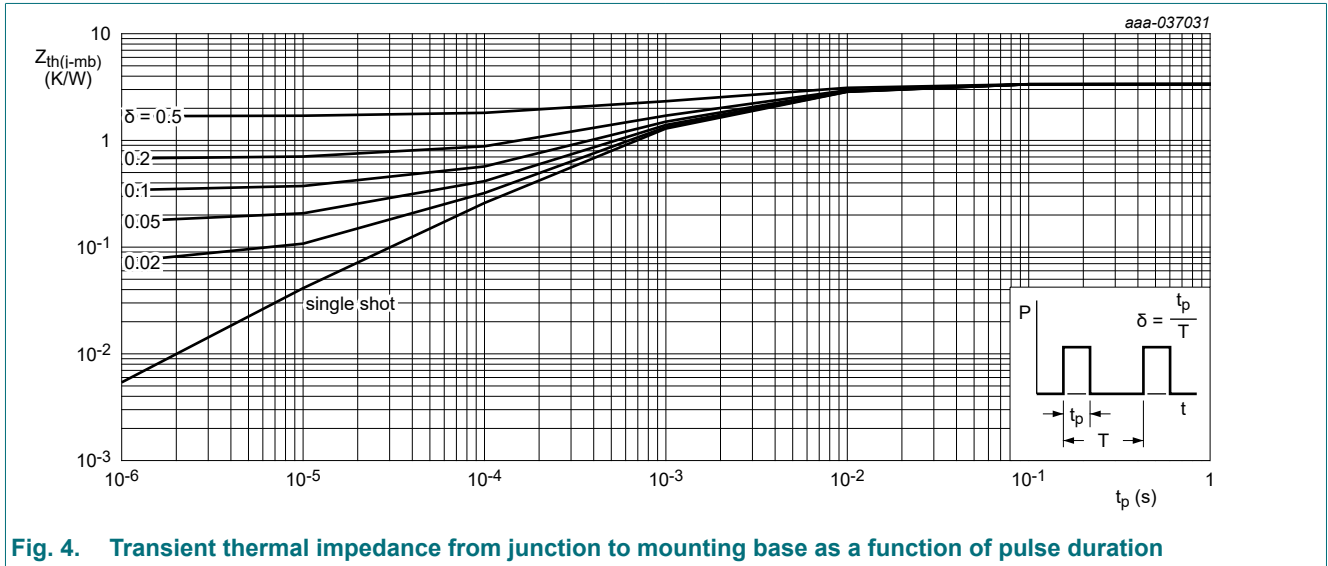


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

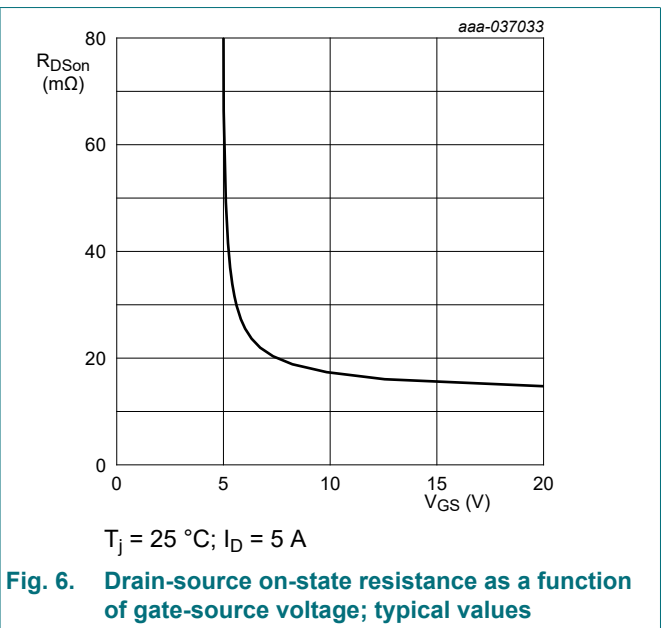
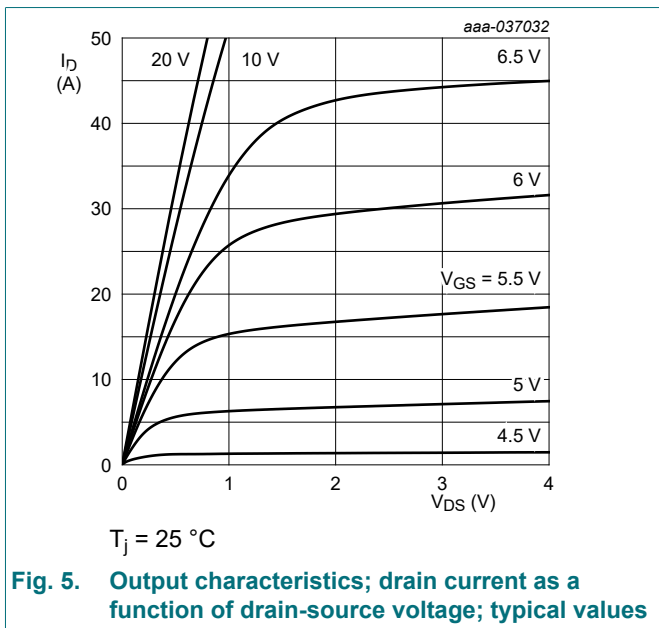
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	-	100	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 8	2	3	4	V
		$I_D = 0.25 \text{ mA}; V_{DS}=V_{GS}; T_j = 150 \text{ }^\circ C$	-	2.1	-	V
		$I_D = 0.25 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.9	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-9.3	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	$\mu A$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ C$	-	6	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 9	-	17.4	20	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 10	-	-	38	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	1	-	$\Omega$

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	13	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C	-	11	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	3.9	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	2.4	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	1.5	-	nC
Q <sub>GD</sub>	gate-drain charge		-	3.5	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	4.8	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a>	-	760	-	pF
C <sub>oss</sub>	output capacitance		-	238	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	10	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; R <sub>L</sub> = 10 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C	-	4.8	-	ns
t <sub>r</sub>	rise time		-	3.7	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	9.3	-	ns
t <sub>f</sub>	fall time		-	8.4	-	ns
Q <sub>oss</sub>	output charge	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz; T <sub>j</sub> = 25 °C	-	19	-	nC
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 5 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a>	-	0.82	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 5 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>	-	32	-	ns
Q <sub>r</sub>	recovered charge		[1]	24	-	nC

[1] includes capacitive recovery



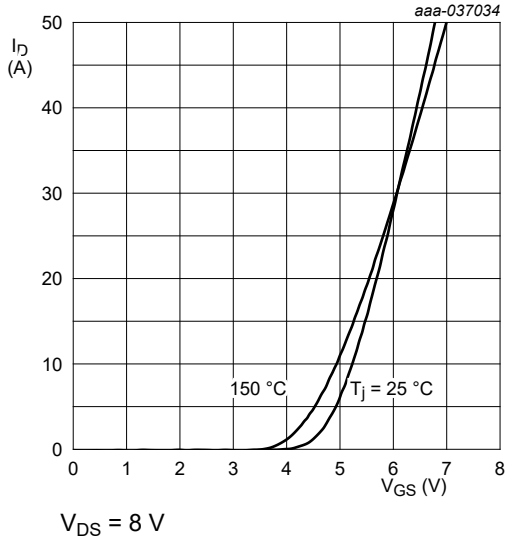


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

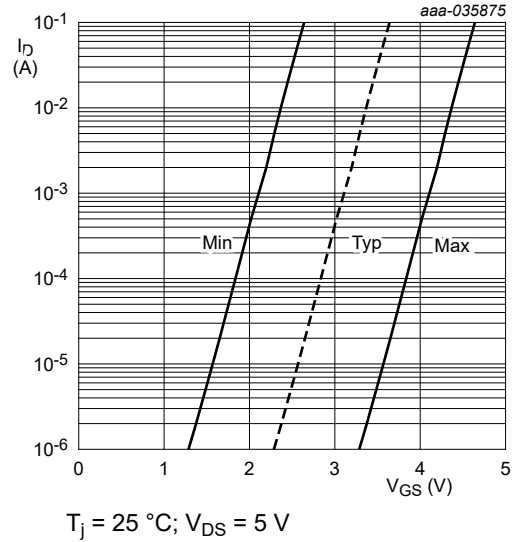


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

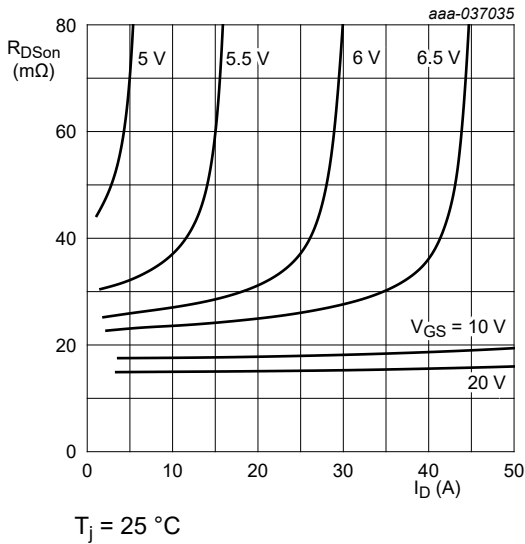


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

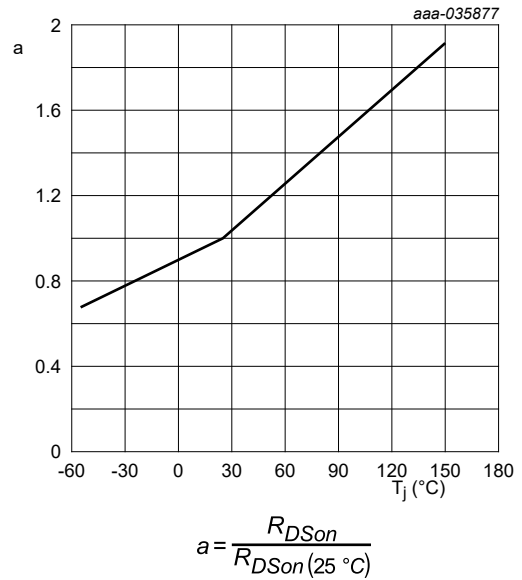
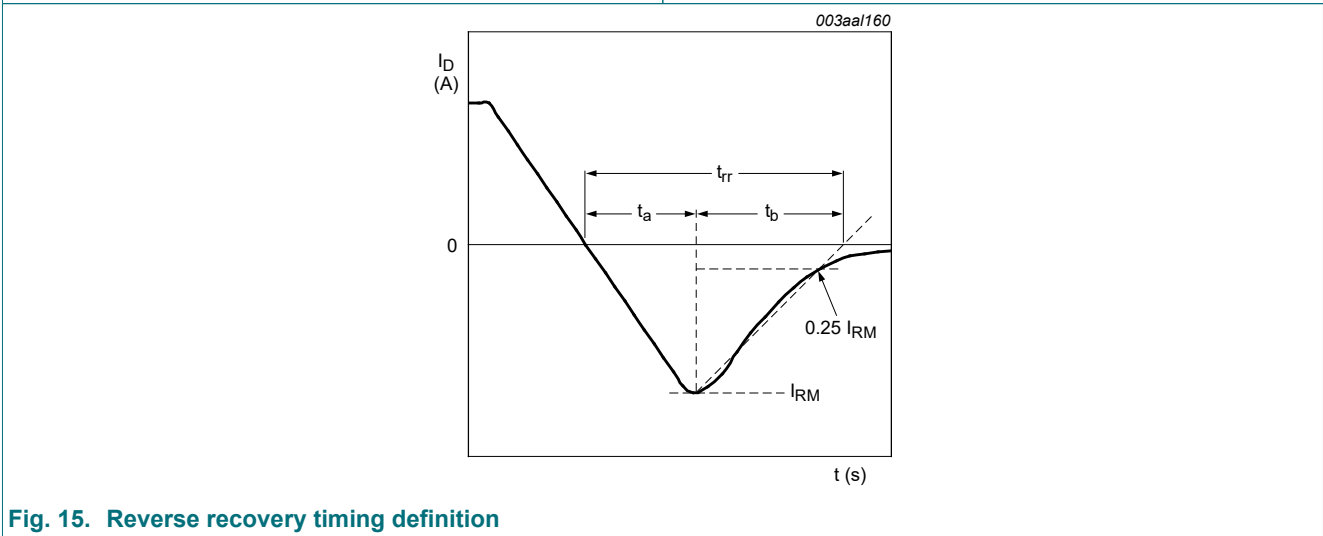
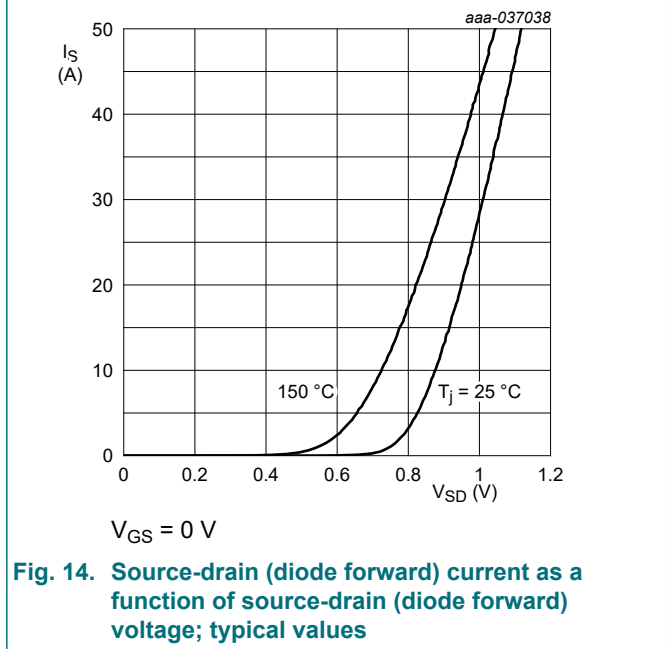
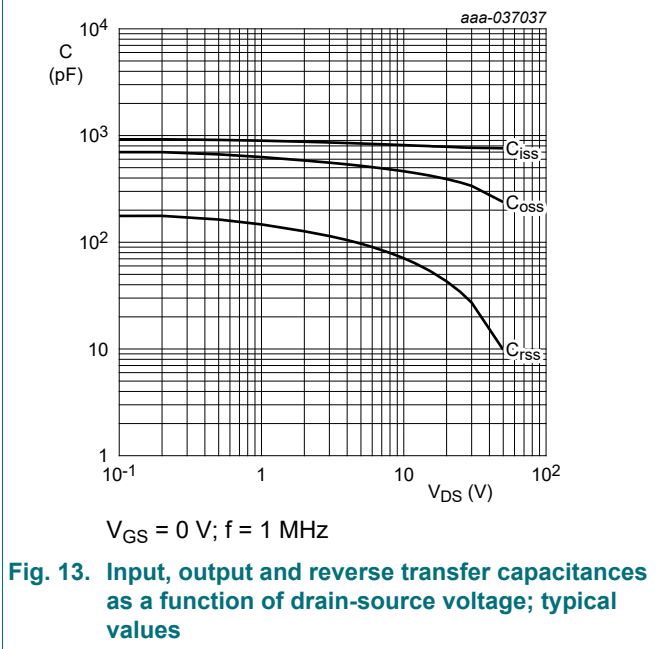
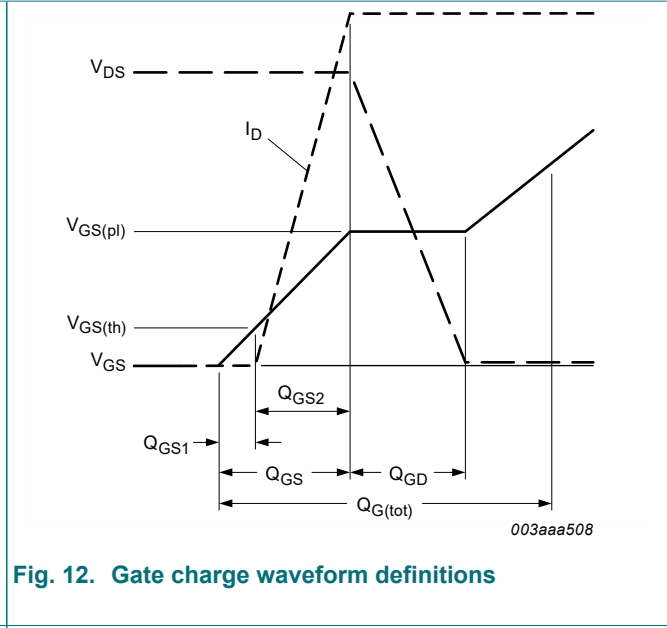
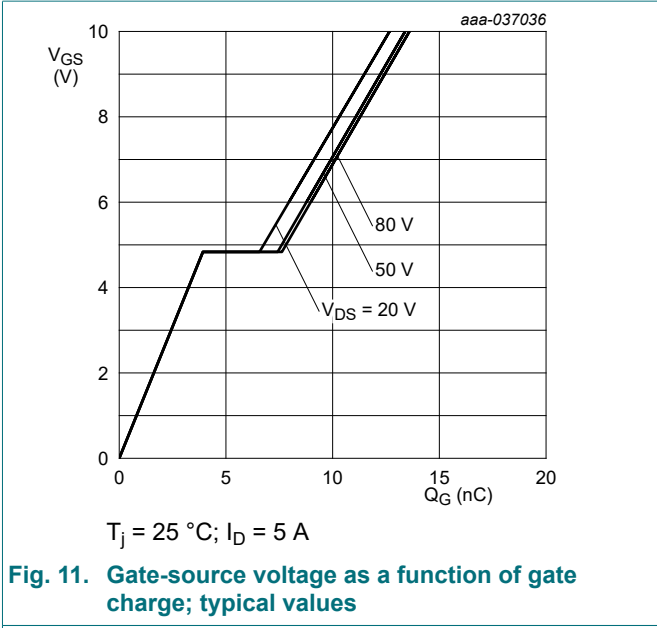


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

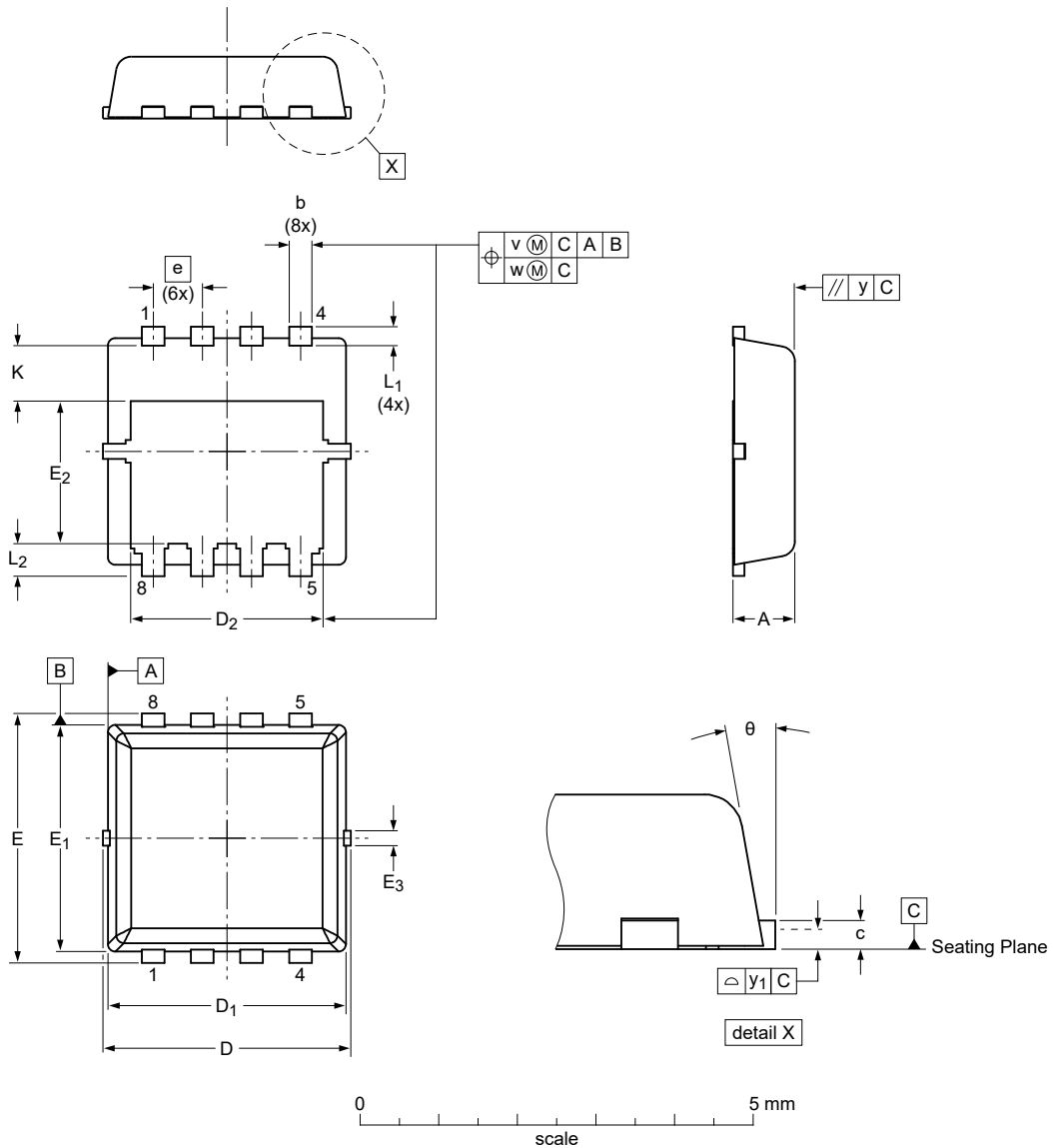
$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ °C})}$$



### 11. Package outline

MLPAK33: plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body

SOT8002-1



Dimensions (mm are the original dimensions)

Unit	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	e	E	E <sub>1</sub>	E <sub>2</sub>	E <sub>3</sub>	K	L <sub>1</sub>	L <sub>2</sub>	θ	y	y <sub>1</sub>	v	w
max	0.90	0.35	0.18	3.50	3.25	2.65		3.50	3.10	1.99	0.25		0.40	0.58	12°				
mm	nom	0.80	0.30	3.30	3.15	2.55	0.65	3.30	3.00	1.89	0.20	0.65 (ref)	0.25	0.43	10°	0.05	0.05	0.1	0.05
	min	0.70	0.25	3.10	3.05	2.45		3.10	2.90	1.79	0.15		0.10	0.28	8°				

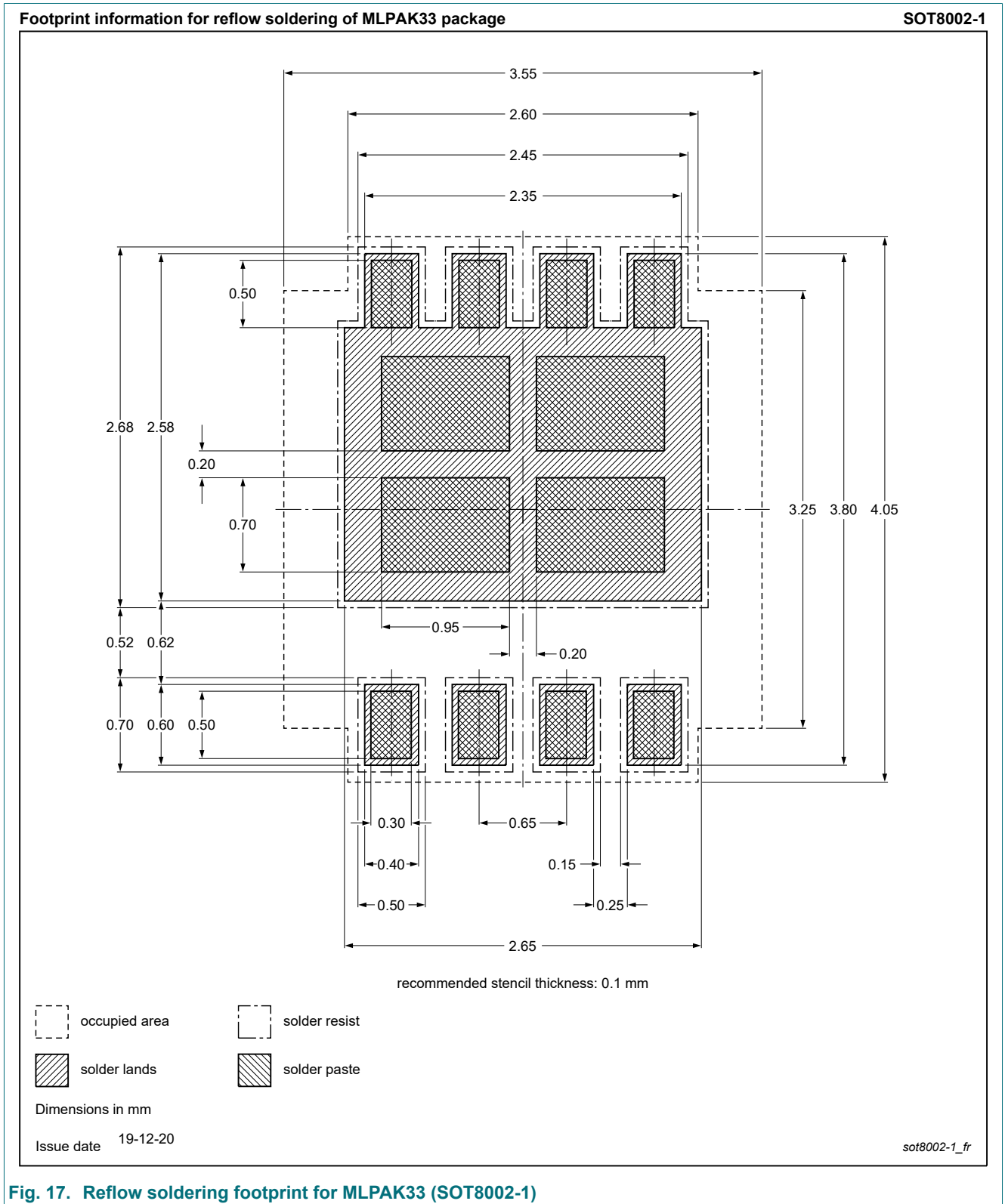
sot8002-1\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT8002-1						20-01-19 23-05-17

Fig. 16. Package outline MLPAK33 (SOT8002-1)



## 12. Soldering



**Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)**

## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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