



PSMN047-100NSE

N-channel 100 V, 53 mOhm standard level ASFET with enhanced SOA in DFN2020. Designed for high power PoE, inrush management, eFuse and relay replacement

12 December 2023

Product data sheet

1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90 W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of “soft-start”, thermal management and power density requirements. These ASFETs combine enhanced SOA in a compact 2 mm x 2 mm footprint making them ideally placed for a variety of applications including PoE, eFuse and relay replacement.

2. Features and benefits

- Enhanced safe operating area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- 2 mm x 2 mm space-saving DFN2020 package, 60% smaller than LFPAK33
- Very low I_{DSS} leakage

3. Applications

- High power PoE applications (60 W and higher)
- IEEE802.3at and proprietary PoE solutions
- Fault tolerant load switch - Inrush management and eFuse applications
- Battery management applications
- Relay replacement
- WIFI hotspots
- 5G picocells
- CCTV

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	18.4	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	42	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	-	42	53.4	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 100\text{ °C}; \text{Fig. 12}$	-	66	85	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	0.5	1.5	3.5	nC
$Q_{G(tot)}$	total gate charge		4.5	9	13.5	nC

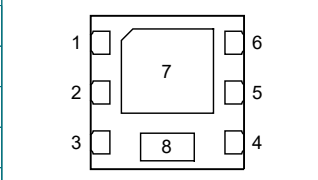
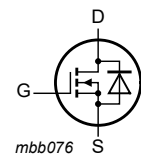
N-channel 100 V, 53 mOhm standard level ASFET with enhanced SOA in DFN2020. Designed for high power PoE, inrush management, eFuse and relay replacement

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 10.6 \text{ A}$; $V_{sup} \leq 100 \text{ V}$; $R_{GS} = 50 \text{ }\Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; $t_p = 20 \text{ }\mu\text{s}$; Fig. 4	[1]	-	-	13.8	mJ
Source-drain diode							
Q_r	recovered charge	$I_S = 5 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 50 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 17	-	22.3	-	nC	

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020M-6 (SOT1220-2)</p>	 <p>mbb076</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN047-100NSE	DFN2020M-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1220-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN047-100NSE	ZT

8. Limiting values

Table 5. Limiting values

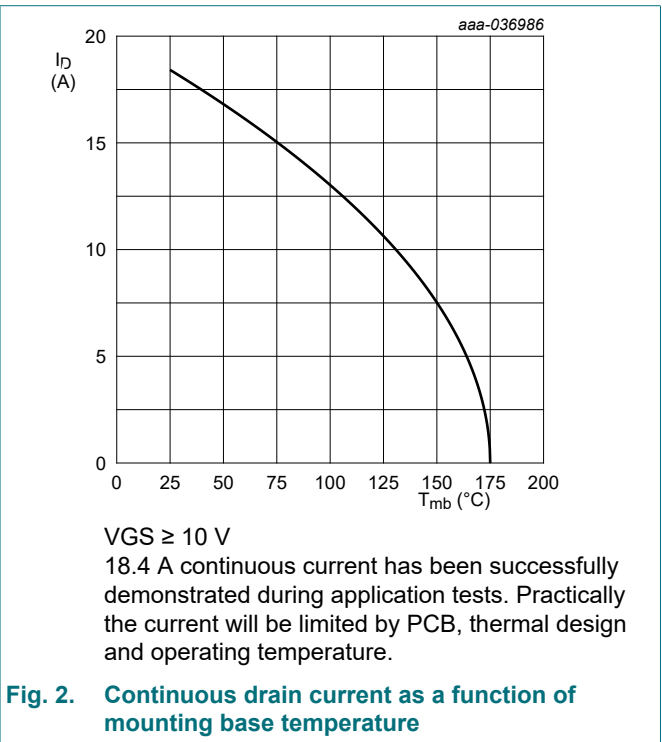
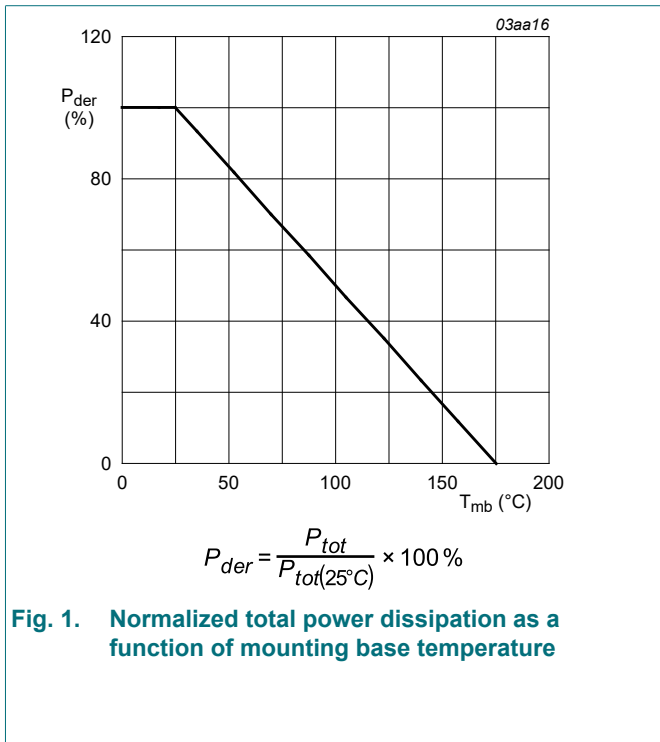
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25 \text{ }^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$	-	100	V
V_{DGR}	drain-gate voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$; $R_{GS} = 20 \text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 1	-	42	W

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Symbol	Parameter	Conditions	Min	Max	Unit
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	18.4	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	13	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	74	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	18.4	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	74	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 10.6 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 20 μs; Fig. 4	[1]	-	13.8 mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[1]	-	10.6 A

[1] Protected by 100% test



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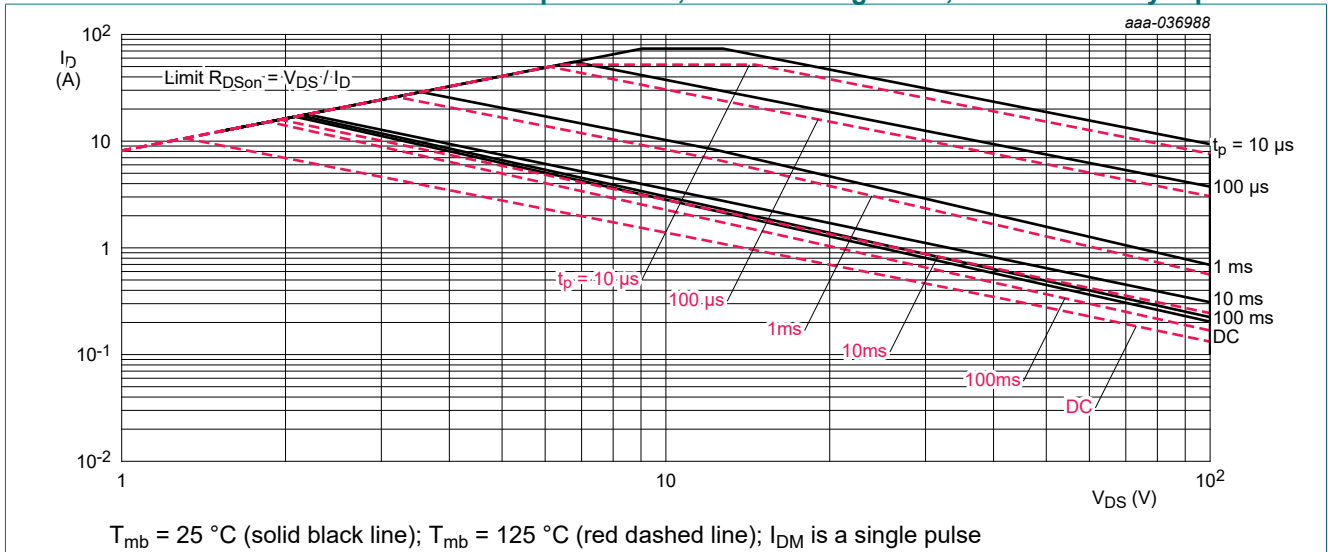


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

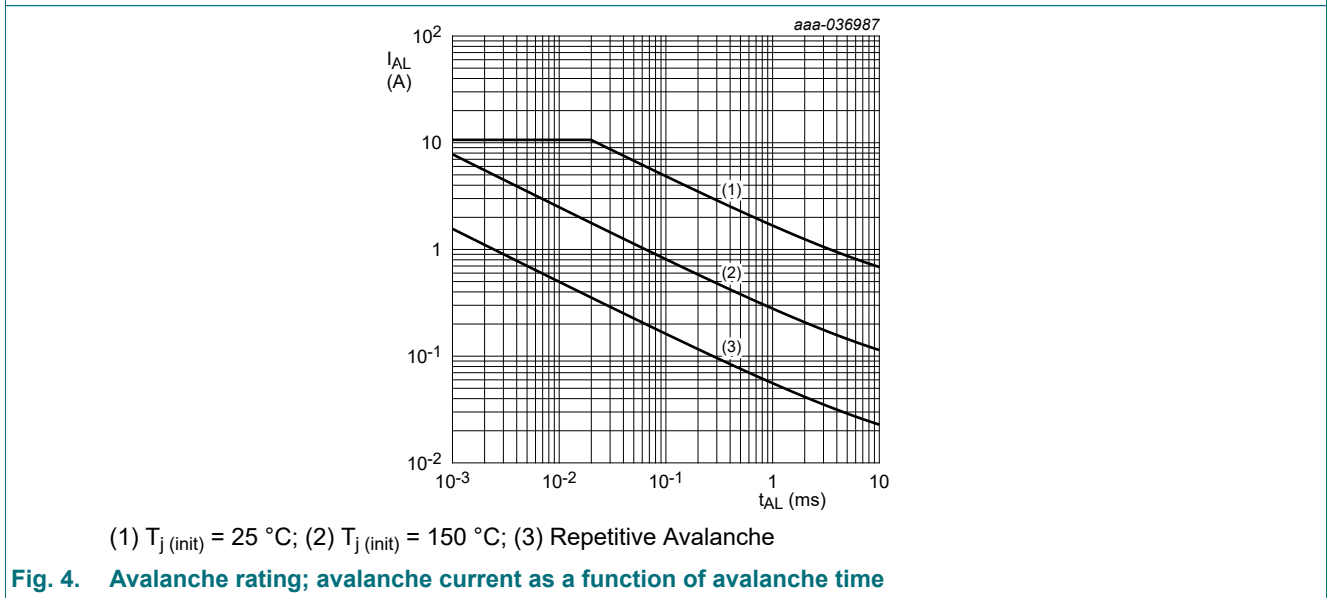


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	3.2	3.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	63	-	K/W
		Fig. 7	-	239	-	K/W

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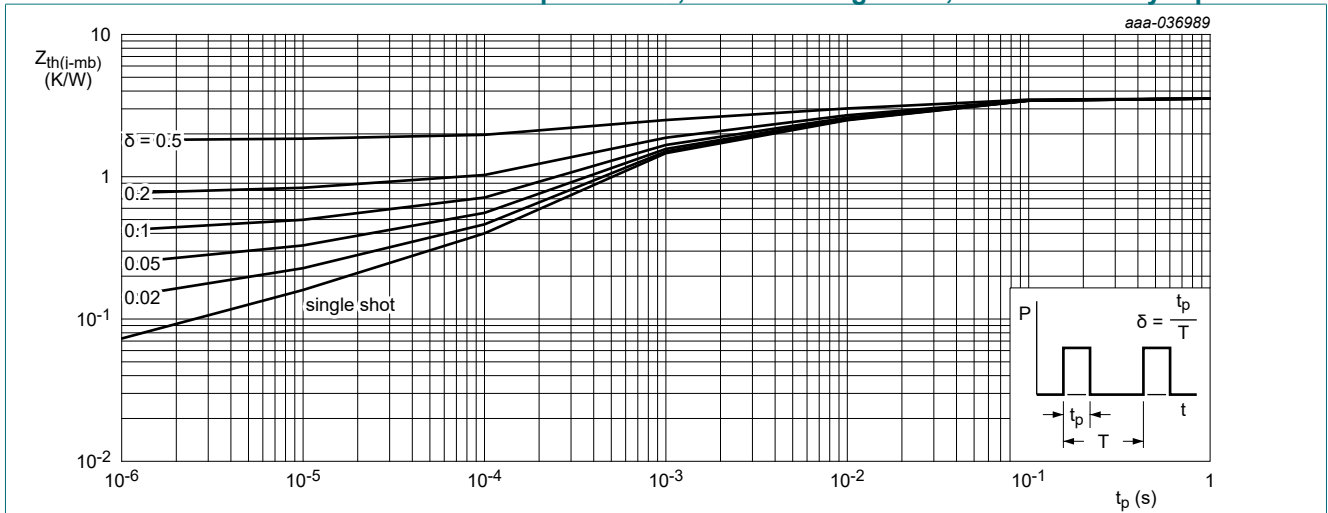


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-037076

Copper square 25.4 mm square; 70 μm thick on FR4 board

aaa-037077

70 μm thick copper on FR4 board

Fig. 6. PCB layout for thermal resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	2	2.8	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.9	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.1	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-5.2	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	1.3	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5 A; T _J = 25 °C; Fig. 11	-	42	53.4	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _J = 100 °C; Fig. 12	-	66	85	mΩ
		V _{GS} = 10 V; I _D = 5 A; T _J = 175 °C; Fig. 12	-	93	121	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C	0.5	1	2	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14	4.5	9	13.5	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C	-	8	-	nC
Q _{GS}	gate-source charge	I _D = 5 A; V _{DS} = 50 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14	2.4	4	5.6	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	2	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	2	-	nC
Q _{GD}	gate-drain charge		0.5	1.5	3.5	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 5 A; V _{DS} = 50 V; T _J = 25 °C; Fig. 13 ; Fig. 14	-	5.9	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 15	363	605	847	pF
C _{oss}	output capacitance		91.2	152	243	pF
C _{rss}	reverse transfer capacitance		0.6	5.7	15	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 10 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C	-	4.4	-	ns
t _r	rise time		-	3.3	-	ns
t _{d(off)}	turn-off delay time		-	6.2	-	ns
t _f	fall time		-	6.1	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 5 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 16	-	0.85	1	V
t _{rr}	reverse recovery time	I _S = 5 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _J = 25 °C; Fig. 17	-	28.5	-	ns
Q _r	recovered charge		-	22.3	-	nC

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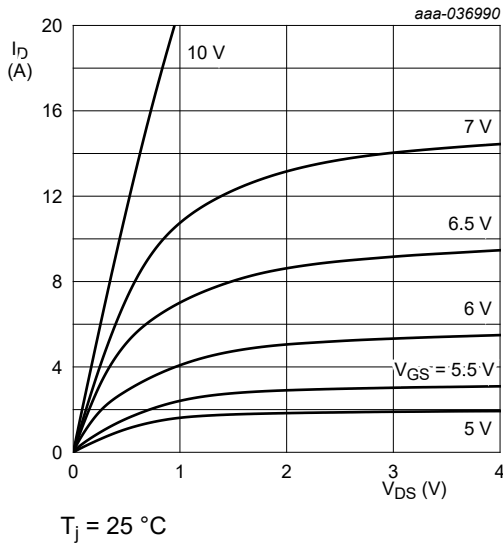


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

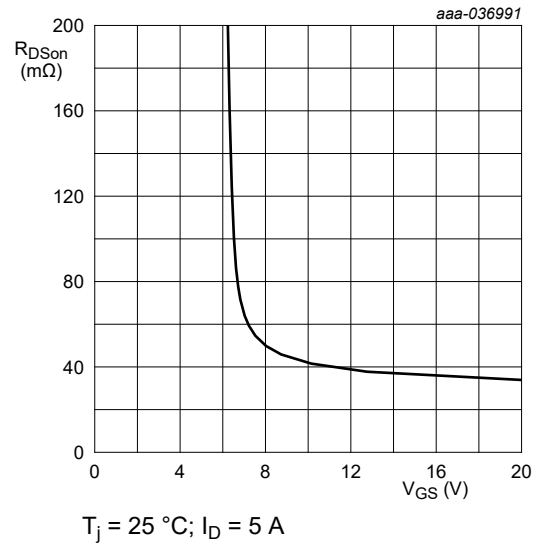


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

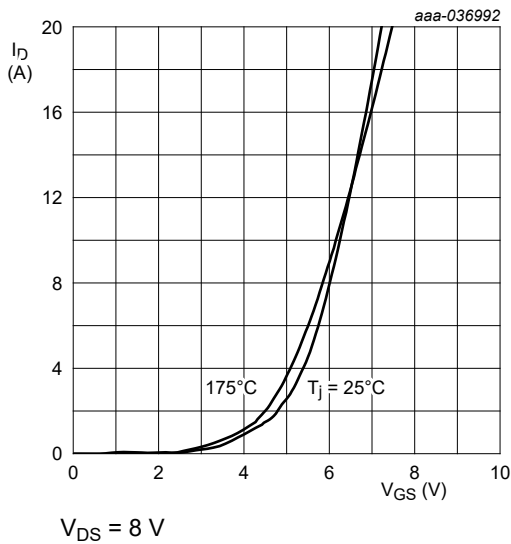


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

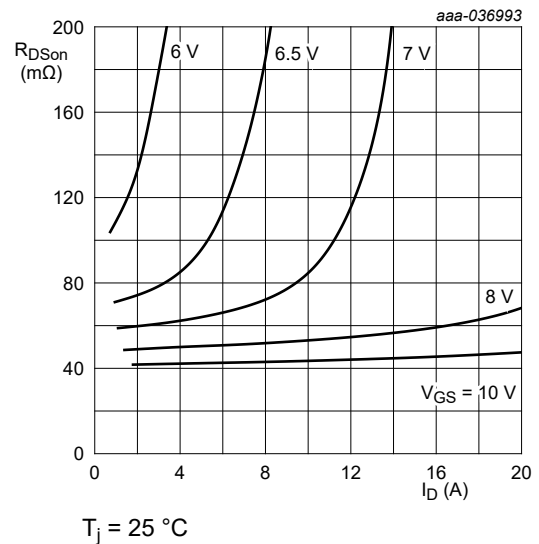
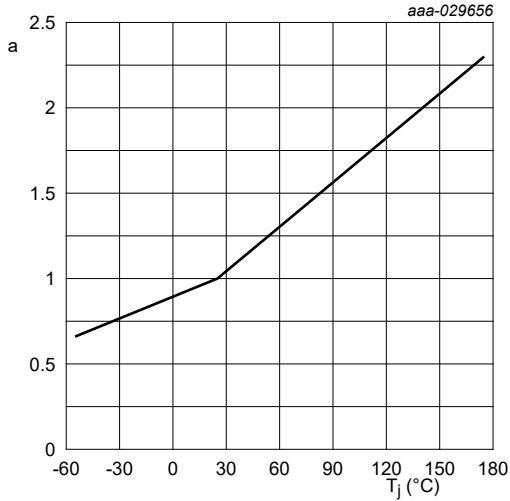


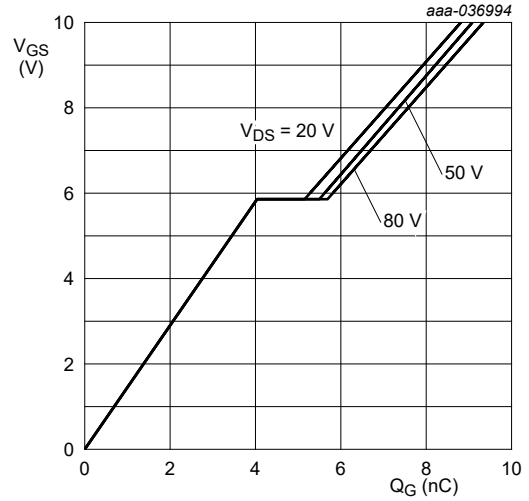
Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}; I_D = 5\text{ A}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

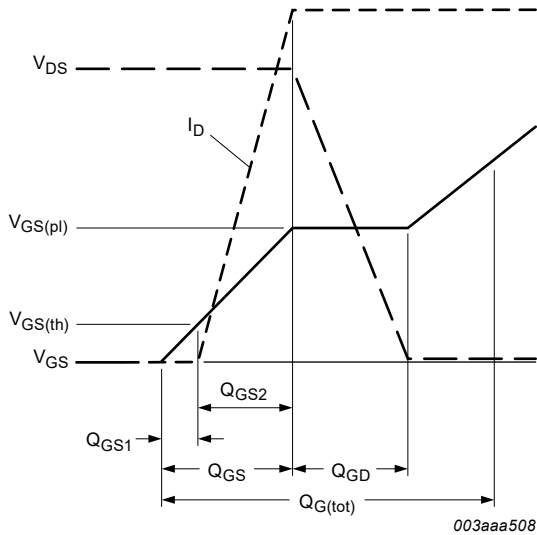
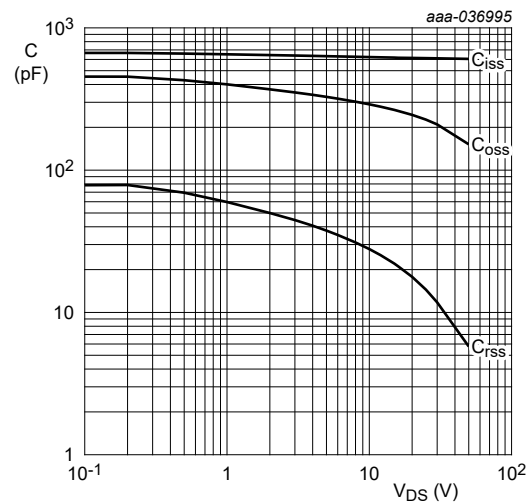


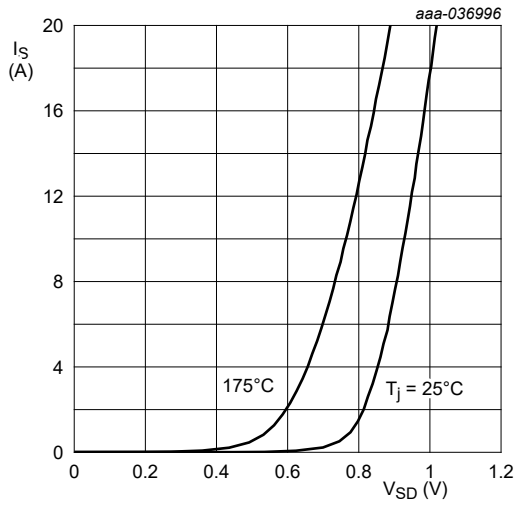
Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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$V_{GS} = 0\text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

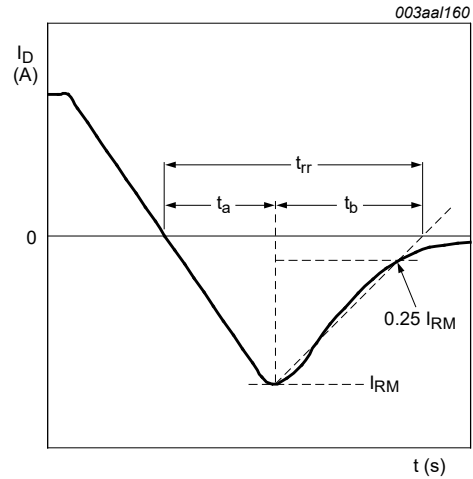


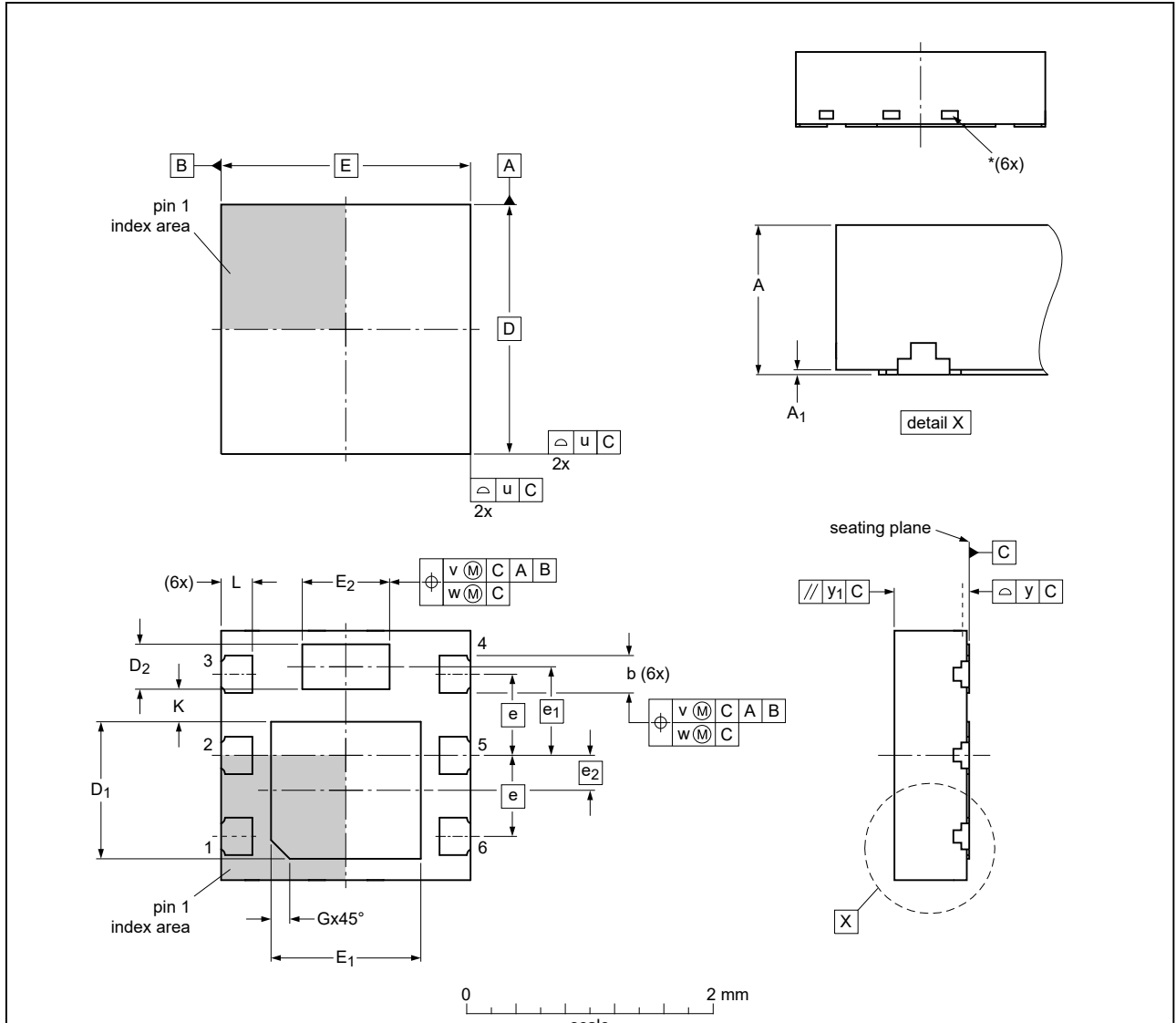
Fig. 17. Reverse recovery timing definition

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11. Package outline

DFN2020M-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm

SOT1220-2



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	D	D ₁	D ₂	E	E ₁	E ₂	e	e ₁	e ₂	G	K	L	u	v	w	y	y ₁
min	0.55	0	0.25	1.0	0.31	1.1	0.6													
mm	nom	0.60	0.02	0.30	2	1.1	0.36	2	1.2	0.7	0.65	0.71	0.28	0.15 (ref)	0.25	0.05	0.1	0.05	0.05	0.05
	max	0.65	0.04	0.35	1.2	0.41	1.3	0.8							0.30					

Note

1. Dimension A is including plating thickness.
2. * Visible depend upon used manufacturing technology.

sot1220-2_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1220-2		---			-20-03-31- 20-04-01

Fig. 18. Package outline DFN2020M-6 (SOT1220-2)

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12. Soldering

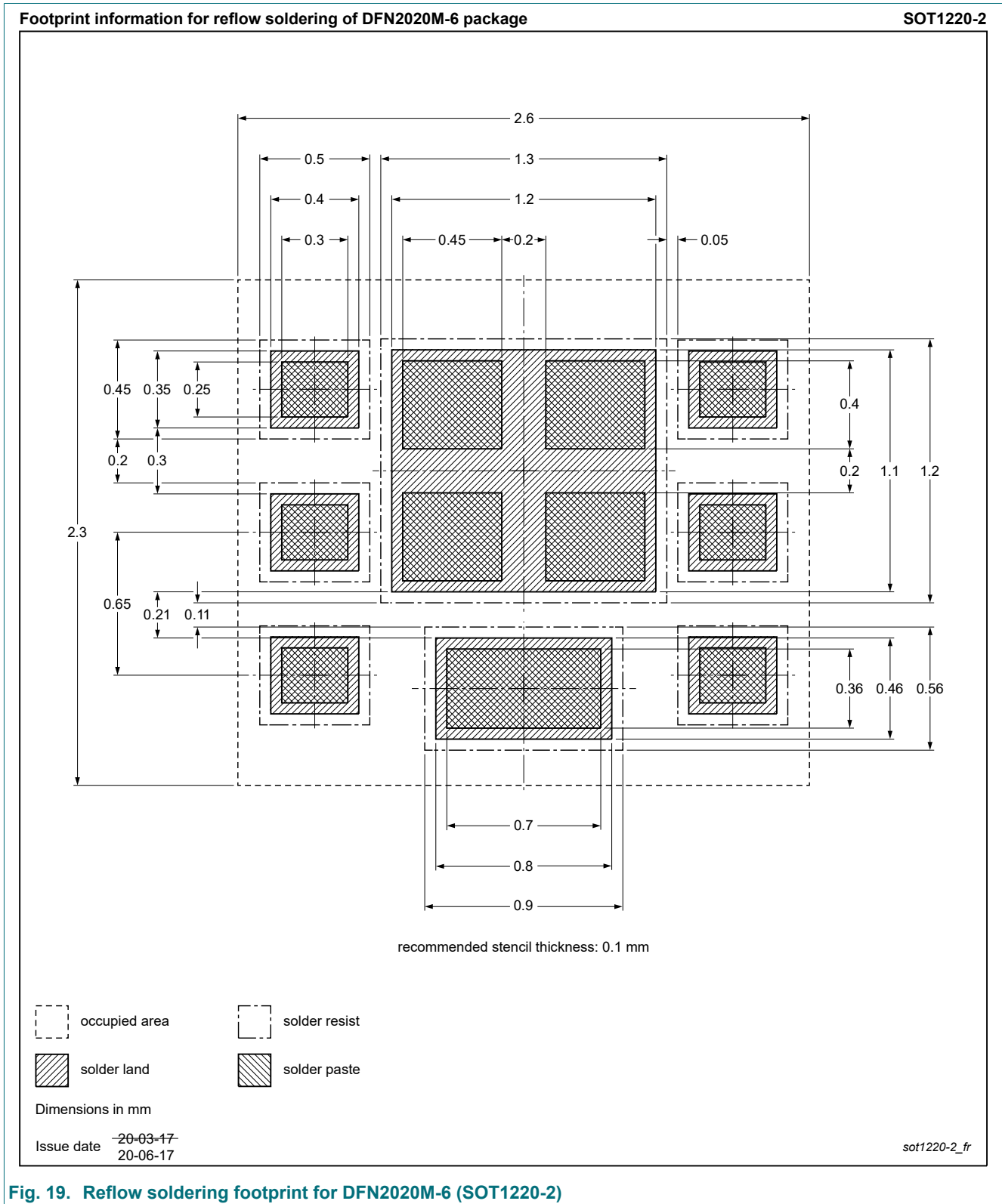


Fig. 19. Reflow soldering footprint for DFN2020M-6 (SOT1220-2)

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Product [short] data sheet	Production	This document contains the product specification.

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